A Self-Gating RF Energy Harvester for Wireless Power Transfer With High-PAPR Incident Waveform

Pengcheng Xu, *Graduate Student Member, IEEE*, Denis Flandre, *Senior Member, IEEE*, and David Bol, *Senior Member, IEEE*

***Abstract*— In this article, we propose a self-gating radio frequency (RF) energy harvester (RFEH) for reaching a high-power harvesting efficiency (PHE) at a low incident RF power level with a high peak-to-average power ratio (high-PAPR) waveform. It includes a power switch between a cross-coupled rectifier and its supplied load to cut off the reverse leakage current in between the short power bursts. The power switch is dynamically controlled based on an indication of the ability of the RFEH to effectively charge the load at the instantaneous incident power level. This is achieved by comparing the load voltage with the open-circuit voltage of a replica rectifier. A comparator with optional proteresis (reversed hysteresis) is proposed for compensating its logic delay at the start and at the end of the short RF power bursts. As a result, the power switch is accurately turned on only during the power bursts. The self-gating RFEH was prototyped for 2.45-GHz wireless power transfer (WPT). It includes a cross-coupled rectifier with the proposed self-gating circuit fabricated in a 65-nm process, a discrete balun, a parasitic-aware-sized π matching network, and an off-the-shelf power management unit (PMU) with maximum power point tracking (MPPT). Measurement results show sensitivity as low as −26.7 dBm with a peak PHE of 32.3% at −14.1-dBm incident power. Compared with the state-of-the-art works, the proposed design significantly improves the RFEH performance at the target low average incident power.**

***Index Terms*— High peak-to-average power ratio (high-PAPR), proteresis comparator, radio frequency (RF) energy harvester (RFEH), reverse leakage, self-gating, wireless power transfer (WPT).**

I. Introduction

IN FAR-FIELD or radiative wireless power transfer (WPT), power is transferred by beams of electromagnetic radiation with radio frequency (RF), such as license-free 2.45 GHz. Far-field WPT can transport electrical power over longer distances. It is, thus, a flexible way to supply Internet-of-Things (IoT) smart sensors for avoiding battery replacement, cable charging, or unpredictable ambient energy harvesting, as demonstrated in [1].

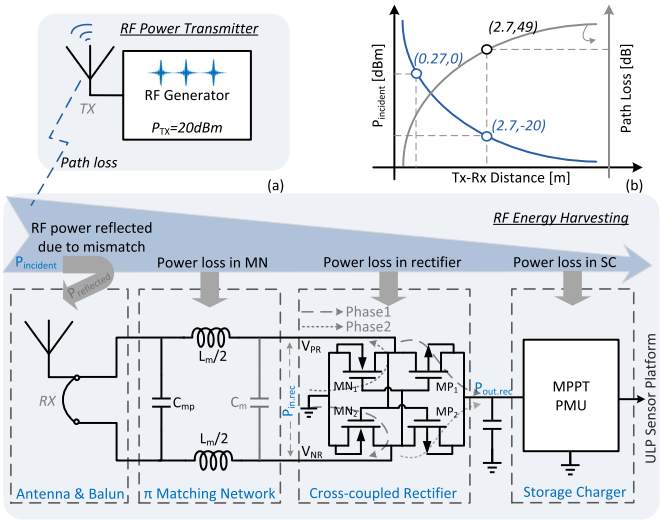

Fig. 1. RFEH for far-field WPT. (a) System architecture. (b) Link budget.

As illustrated in Fig. 1(a), the RF power transmitter is the power source, and it uses an RF generator and an antenna to transmit power to an RF energy harvester (RFEH) for supplying an ultra-low-power (ULP) sensor platform. The path loss over the wireless link significantly degrades the level of incident power P_{incident}. Each stage of RFEH also has a corresponding power loss. This reduces the harvested power $P_{\text{out.rec}}$ and further degrades the collected power to supply the IoT smart sensor. In this work, the storage charger is implemented by an off-the-shelf power management unit (PMU) with maximum power point tracking (MPPT). We, thus, express the power harvesting efficiency (PHE) without considering the PMU [2]

$$\text{PHE} = P_{\text{out.rec}}/P_{\text{incident}} = \text{PEE}_{\text{ant}} \times \text{PCE}_{\text{MN}} \times \text{PCE}_{\text{rec}} \quad (1)$$

where PEE_{ant}, PCE_{MN}, and PCE_{rec} are, respectively, the power extraction efficiency at the antenna $[=(P_{\text{incident}} - P_{\text{reflected}})/P_{\text{incident}}]$, the power conversion efficiency of the

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Pengcheng Xu is with the Electronic Circuits and Systems (ECS) Group, Department of Electrical Engineering, ICTEAM Institute, Universite catholiqué de Louvain (UCLouvain), 1348 Louvain-la-Neuve, Belgium, and also with the Department of Circuits and Systems, Fraunhofer Research Institution for Microsystems and Solid State Technologies EMFT, 80686 Munich, Germany (e-mail: pengcheng.xu@uclouvain.be).

Denis Flandre and David Bol are with the Electronic Circuits and Systems (ECS) Group, Department of Electrical Engineering, ICTEAM Institute, Universite catholiqué de Louvain (UCLouvain), 1348 Louvain-la-Neuve, Belgium (e-mail: denis.flandre@uclouvain.be; david.bol@uclouvain.be).

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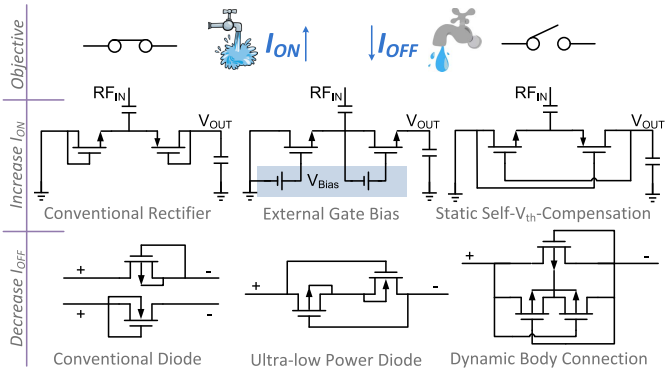

Fig. 2. RFEH state-of-the-art techniques for improving its PHE at low incident power.

matching network [$=P_{\text{in.rec}}/(P_{\text{incident}} - P_{\text{reflected}})$], and the power conversion efficiency of the rectifier ($=P_{\text{out.rec}}/P_{\text{in.rec}}$).

Instead of a single-tone power waveform, the RF generator can combine multiple tones to generate a waveform with a high peak-to-average power ratio (high-PAPR) for improving PHE at low incident power [3]. However, the RFEH suffers from serious reverse leakage with a high-PAPR waveform since the power is essentially intermittent. A self-gating RFEH design for WPT is proposed in this article for cutting off the reverse leakage with a power switch placed between the rectifier and PMU. The switch is dynamically controlled for delivering power or preventing reverse leakage according to the instantaneous level of the incident RF power. This article is organized as follows. The design challenge of far-field RFEH for IoT sensor applications is analyzed in Section II. Section III studies the generation of high-PAPR power waveform with a narrow bandwidth (BW) and its double-edged effect on RFEH. It drives the motivation for the self-gating RFEH design, as proposed in Section IV. Prototyping and measurement results are presented in Section V.

II. Far-Field RFEH Design Challenge

The supply range, i.e., the maximum distance between the power transmitter (TX) and the receiver (RX), depends on three factors: the power emitted by the RF transmitter, the PHE of the RFEH, and the power consumption of the WPT-supplied ULP sensor platform. The maximum power emitted by the RF transmitter is constrained by effective (or equivalent) isotropic radiated power (EIRP) regulations (e.g., 20 dBm at a 2.45-GHz band in accordance to the European law) for guaranteeing the protection of human health and the environment. As depicted in Fig. 1(b), P_{incident} depending on TX-to-RX distance is estimated for a TX output power P_{TX} of 11 dBm and antenna realized gain at the TX and RX sides G_{TX} and G_{RX} of 9 dBi. It is evaluated with $P_{\text{incident}} = P_{\text{TX}} + G_{\text{TX}} - L_{\text{FS}} + G_{\text{RX}}$, where L_{FS} is the free-space RF path loss.[1] The RFEH input P_{incident} is ranging from 0 to -20dBm for a TX-to-RX distance of about 0.27–2.7 m.

[1]The free-space RF path loss is $L_{\text{FS}}(\text{dB}) = 20\log_{10}(4\pi\,\text{distance}/\text{wavelength})$, where distance and wavelength are in the same units.

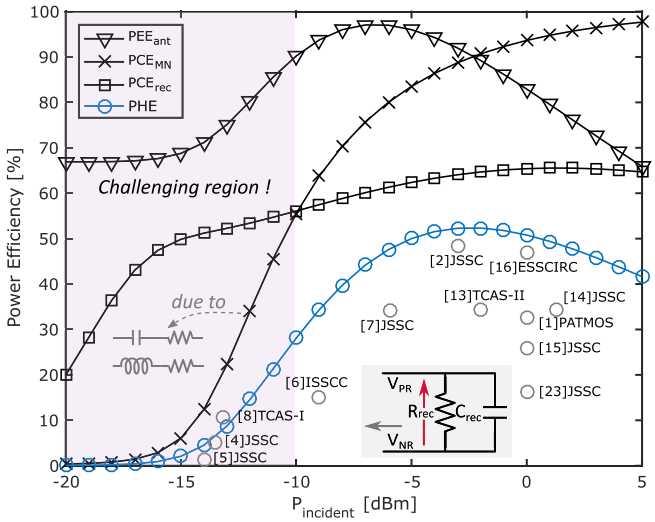

Fig. 3. Power efficiency simulation of each stage in RFEH and state-of-the-art PHE measurement results (with gray "o" marker) under single-tone incident power. The R_{rec} increases from 0.1 kΩ to 1 MΩ when P_{incident} changes from 5 to -20 dBm. C_{rec} is around 70 fF without significant variation.

For improving PHE at low incident power level, as depicted in Fig. 2, the state-of-the-art techniques at circuit level focuses on increasing rectifier forward current I_{ON} and/or decreasing its reverse leakage current I_{OFF} by adapting transistor threshold voltage V_{th}. Increasing I_{ON} can be done by discrete Schottky diode [4], additional gate-biasing with an external voltage source [5], and static self-gate-biasing using the rectifier output voltage [6], [7]. Schmickl *et al.* [8] use a zero-V_{th} NMOS rectifier for improving PHE at low incident power. However, it is subject to process, voltage, and temperature variations (PVTs), and therefore, the efficiency varies with these conditions. The ULP diode proposed in [9] and the dynamic body connection in [10] and [11] have been applied to limit rectifier I_{OFF}. The cross-coupled rectifier [12] shown in Fig. 1 features dynamic self-V_{th}-compensation which can not only improve I_{ON} but also reduce I_{OFF}. This provides a unique advantage in RFEH design and is used in this work.

A low-power path with low-V_{th} rectifier designs is optimized for low incident power level in [13]. Zeng *et al.* [14] show a way to reconfigure the number of rectifier stages in series at a low input power level. In [15] and [16], a capacitor bank is used for tuning the matching network. Similar to the photovoltaic (PV) energy harvesting system, MPPT is also introduced in [3] to regulate the rectifier output voltage for improving the PHE.

With a single-tone incident RF power, the RFEH of Fig. 1(a) as implemented in [2] has very low PHE at low P_{incident} level, as depicted in Fig. 3. We observe the same behavior for the state-of-the-art works even when specifically optimized for the low P_{incident} level. When P_{incident} is below 10 dBm, the significantly degraded PEE$_{\text{ant}}$, PCE$_{\text{MN}}$, and PCE$_{\text{rec}}$ result from the exponential increase in the rectifier equivalent input impedance. This effect combined with additional parasitic effect from PCB and package [17] makes it difficult to achieve good impedance conjugate matching and causes increased

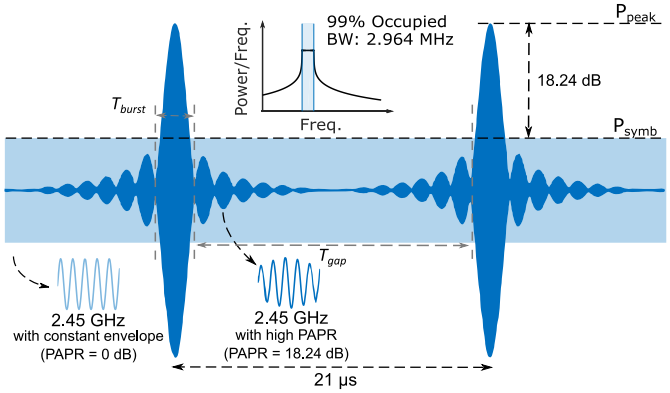

Fig. 4. OFDM high-PAPR WPT waveform (navy blue) with 18.24-dB PAPR and 21 μs between two power peaks compared to single-tone waveform (light blue). Power burst time $T_{\text{burst}} = 0.65$ μs, and power gap time $T_{\text{gap}} = 20.35$ μs. Both waveforms have the same average power.

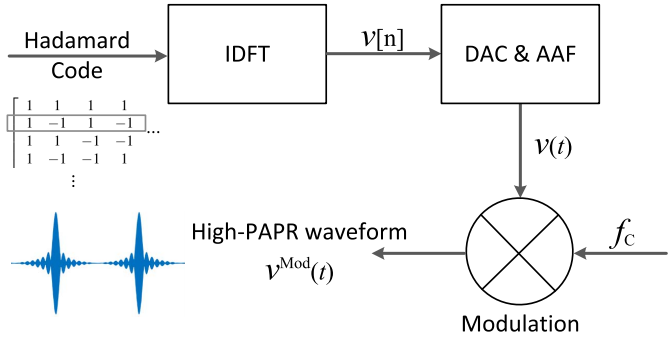

Fig. 5. Mathematical representation of high-PAPR waveform generation based on a 64-size Walsh–Hadamard code.

power loss in the matching network with a limited quality factor, especially at 2.45-GHz WPT frequency. Thus, optimizing PHE at a low incident power level is a challenge in practical design. Instead of using a single-tone continuous power waveform, this motivates the exploration of custom WPT power waveform with non-constant envelope in order to achieve short high-power WPT bursts while keeping the average TX output power below the EIRP regulation, i.e., high-PAPR WPT waveform, as explained in Section III.

III. High-PAPR WPT Waveform

A. Waveform Generation

The high-PAPR waveform can be generated through the superposition of different tones where the peak power level can be controlled by introducing a phase offset between the tones. Due to their symmetry properties [18], Walsh–Hadamard codes allow a simple way to easily adapt PAPR. The signal generation can then be obtained through a simple inverse fast Fourier transform (IFFT) operation, thus making it compatible with the popular orthogonal frequency-division multiplexing (OFDM)-based wireless systems. OFDM-like modulation also allows us to confine and adapt the total BW of the power signal to avoid generating out-of-band emissions that represent harmful inter-channel interference with data transmission in

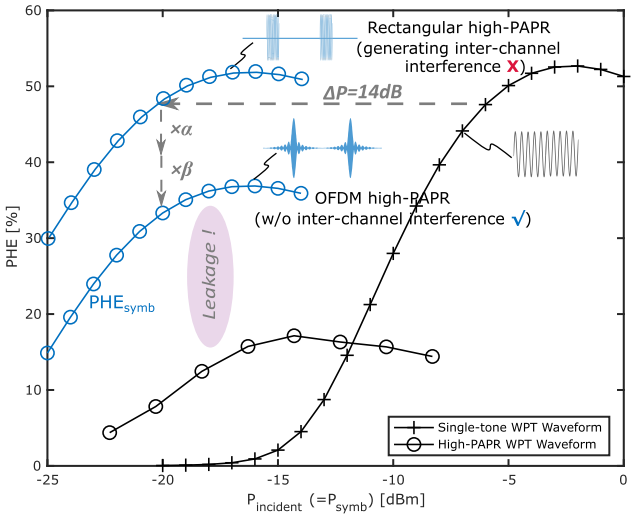

Fig. 6. Theoretical estimation (line in blue) and practical simulation (line in black) of the PHE improvement due to the high-PAPR WPT waveform.

the same frequency band, for simultaneous wireless information and power transfer (SWIPT).

In this work, we consider an SWIPT scheme collocating WPT with Bluetooth Low Energy (BLE) data transmission as in [3]. BLE has 40 2-MHz channels with a total 80-MHz BW from 2.40 to 2.48 GHz. We generate the high-PAPR WPT waveform in Fig. 4 by using 64 binary phase shift keying (BPSK) modulated tones for a total 3-MHz occupied BW fit in two 2-MHz adjacent BLE channels that we allocate to WPT.

We, thus, propose to generate the high-PAPR waveform from a 64-size Walsh–Hadamard code with a 64-point IFFT, as illustrated in Fig. 5. The OFDM symbol period is

$$T_{\text{symb}} = N/BW = 64/(3 \times 10^6) \approx 21.33\ \mu\text{s} \tag{2}$$

which corresponds to the burst-to-burst period. Assuming that the Walsh–Hadamard code is $w_0, \ldots, w_{N-1} \in \{-1, 1\}$ in a certain column, after inverse discrete Fourier transform (IDFT), digital-to-analog conversion (DAC), anti-aliasing filtering (AAF), and modulation with the 2.45-GHz carrier frequency f_c, we have

$$v^{\text{Mod}}(t) = \frac{1}{N}\sum_{k=0}^{N-1} w_k \cdot e^{j2\pi(k/T_{\text{symb}}+f_c)t}$$
$$= \frac{1}{N}\sum_{k=0}^{N-1} w_k \cdot \left[\cos\left(2\pi\left(\frac{k}{T_{\text{symb}}}+f_c\right)t\right) + j\sin\left(2\pi\left(\frac{k}{T_{\text{symb}}}+f_c\right)t\right)\right]. \tag{3}$$

In baseband, the PAPR is expressed as

$$\text{PAPR} = 10\log_{10}\frac{P_{\text{peak}}}{P_{\text{symb}}} = 20\log_{10}\frac{V_{\text{peak}}/\sqrt{2}}{V_{\text{symb.rms}}} \tag{4}$$

where P_{symb} is the average power over T_{symb}. There are 32 different high-PAPR waveforms corresponding to the symmetric 64 columns of the Walsh–Hadamard matrix. It reaches a maximum achievable PAPR of 18.24 dB with the first or

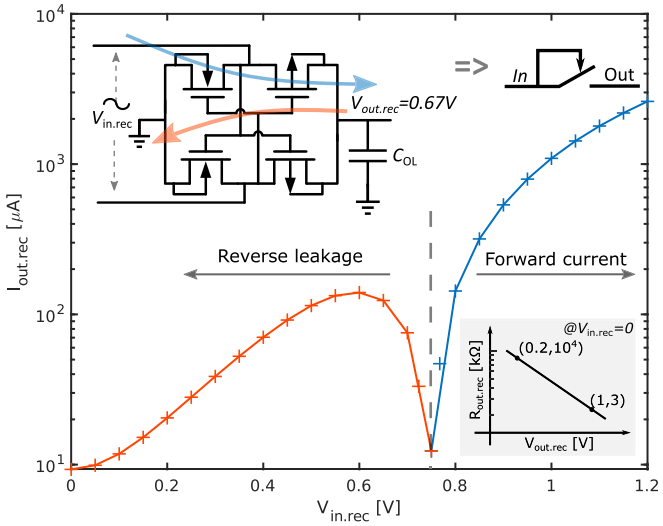

Fig. 7. Rectifier forward current and reverse leakage (in absolute value).

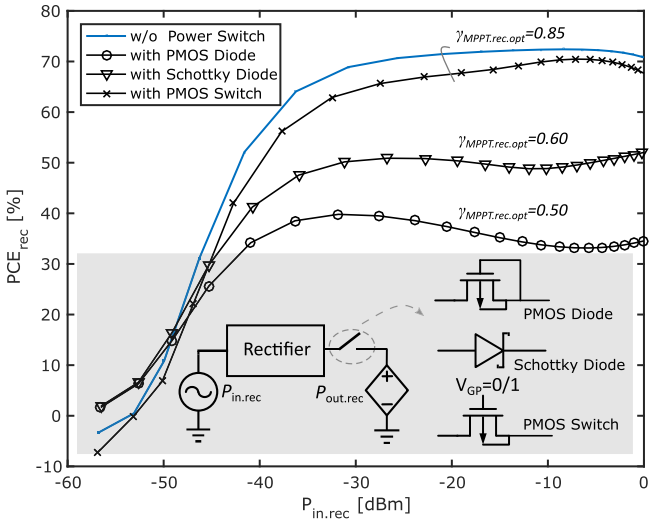

Fig. 8. Rectifier power conversion efficiency depending on its input power level. PMOS diode and PMOS switch widths are about 100× and 1× the rectifier correspondingly. The Schottky diode is HSMS-286 from Avago Technologies.

second column is chosen in this work for optimizing PHE at low incident RF power level. Universal software radio peripheral (USRP) has been used in this work to practically generate the proposed high-PAPR waveform by using the aforementioned processing.

B. Interest and Limitation

With the aforementioned high-PAPR WPT waveform, the average PHE over T_{symb}, i.e., PHE_{symb}, significantly benefits from the power burst P_{burst} with high average power level, which leads to a high average PHE over T_{burst} and noted $\text{PHE}_{\text{burst}}$. In the case of an ideal rectangular WPT waveform with constant-envelope power bursts and zero incident power in T_{gap}, this can be interpreted as an ideal shift of the PHE curve to lower P_{incident}. This shift in dB unit can be expressed as

$$\Delta P = P_{\text{burst}}[\text{dBm}] - P_{\text{symb}}[\text{dBm}] = 20\log_{10}\frac{V_{\text{burst.rms}}}{V_{\text{symb.rms}}}. \quad (5)$$

However, for the practical ODFM waveform, some energy is spent at very low power level during T_{gap}, which will results in a lower effective PHE_{symb} expressed as

$$\text{PHE}_{\text{symb}} = \alpha\text{PHE}_{\text{burst}} = \frac{V^2_{\text{burst.rms}}T_{\text{burst}}}{V^2_{\text{symb.rms}}T_{\text{symb}}}\text{PHE}_{\text{burst}}. \quad (6)$$

Moreover, because of OFDM modulation, the waveform envelope is not constant over T_{burst}. This results in a reduction of $\text{PHE}_{\text{burst}}$ by a factor β compared to the PHE that would be obtained with a constant envelop during T_{burst}. Let us mention here that the rising and falling transitions of the power burst are also at a very low power level and, therefore, difficult to be harvested by the RFEH. As shown in Fig. 6, the PHE_{symb} resulting from these two effects in reduced by 0.71× ($=\alpha \times \beta$) compared to the ideal $\text{PHE}_{\text{burst}}$ is shifted by ΔP. However, there is a significant PHE drop between the theoretical estimations and the simulation results of the RFEH from Fig. 1 with the high-PAPR WPT waveform. It is

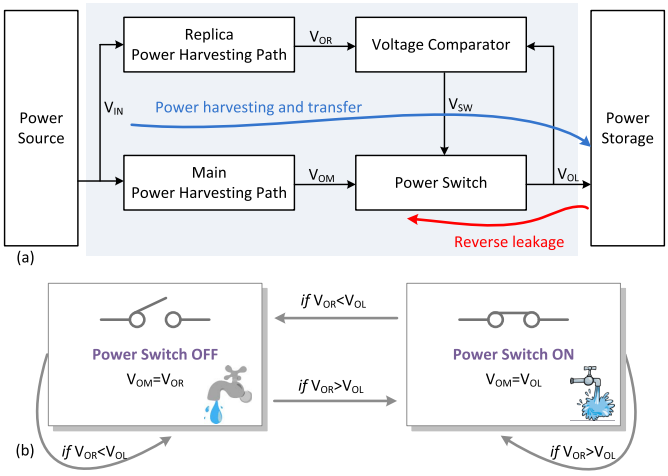

Fig. 9. Proposed smart self-gating energy-harvesting principle: (a) circuit diagram and (b) states logic.

due to the reverse leakage current of the rectifier. Indeed, the cross-coupled rectifier has quite a low equivalent output resistance $R_{\text{out.rec}}$ due to its drain-connected CMOS transistors, e.g., $R_{\text{out.rec}} = 73\ \text{k}\Omega @ V_{\text{out.rec}} = 0.67$ V. When the rectifier input voltage becomes low during T_{gap}, the energy stored on capacitor C_{OL} during T_{burst} with high $V_{\text{out.rec}}$ leaks back toward the ground, as shown in Fig. 7.

This reverse leakage is even more severe at $V_{\text{in.rec}}$ of 0.9× $V_{\text{out.rec}}$ than $V_{\text{in.rec}}$ of 0 V since $V_{\text{in.rec}}$ serves as gating voltage due to the cross-coupled connection. In fact, the cross-coupled rectifier can be modeled as an input voltage-controlled switch, as depicted in Fig. 7. The leakage increases from 0 to 0.6 V because a larger $V_{\text{in.rec}}$ has which turns the switch more on. After 0.6 V, the difference between $V_{\text{out.rec}}$ and $V_{\text{in.rec}}$ drops significantly, which becomes the dominant factor influencing the leakage. Thus, the reverse leakage drops after that. In fact,

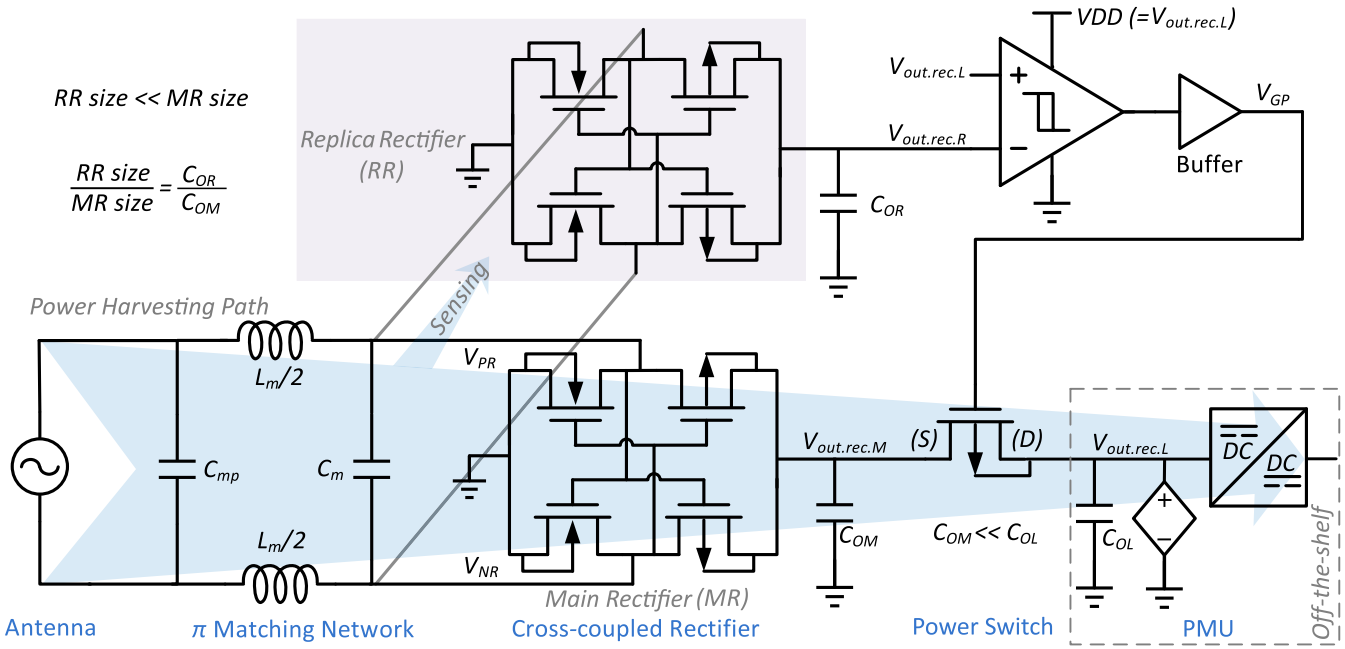

Fig. 10. Proposed smart self-gating RFEH schematic. $V_{\text{out.rec.M}}$, $V_{\text{out.rec.R}}$, and $V_{\text{out.rec.L}}$ are corresponding to V_{OM}, V_{OR}, and V_{OL} in Fig. 9, respectively.

fluctuation of incident power level could happen not only for high-PAPR WPT waveform but also for arbitrary RF path environment. On the one hand, we need a high-PAPR incident waveform for improving PHE at low incident RF power, but, on the other hand, it induces high reverse leakage power loss due to its intermittent power shape in the time domain. Thus, the high-PAPR incident waveform has a double-edged effect on the performance of RFEH.

A simple method for solving the reverse leakage problem is adding a diode at the rectifier output node [19]. However, this diode degrades the PHE during the power burst because of its non-negligible forward resistance, which limits the rectifier ON current. Fig. 8 shows that PCE_{rec} drops by 30% with a PMOS diode, even with a width 100× larger than the rectifier itself. Using a discrete Schottky diode (HSMS-286 from Avago Technologies) gives better results. However, this solution has a huge impact on both the size and cost of the RFEH design. The alternative is to use a smart controlled PMOS power switch, turned on during the power bursts T_{burst} and kept off during the power gaps T_{gap}. This solution gives the best results, with less than 5% PCE_{rec} drop compared to the intrinsic PCE_{rec}, obtained with a PMOS width equivalent to the rectifier width. It also has the highest optimal rectifier MPPT regulation ratio $\gamma_{\text{MPPT.rec}}$ (defined as $V_{\text{out.rec}}$ over its value $V_{\text{out.rec.OC}}$ at open circuit), which is good for improving the PCE of the PMU. Let us see in Section IV how to dynamically control this switch to exploit the PHE improvement of high-PAPR incident waveform without prohibitive leakage.

IV. Proposed Self-Gating RFEH

A. Gating Method

For improving the global PHE of the RFEH under intermittent input power, the harvester needs a smart control scheme to close the power switch for power delivery when the rectifier input power is high enough to charge the storage capacitor and to prevent storage reverse leakage by opening the switch when the input power is too low to be harvested. The proposed smart self-gating energy harvesting concept is depicted in Fig. 9(a). Besides the main power harvesting path for power conversion and delivery, it includes a replica power harvesting path for sensing the instantaneous input power level. A single power switch is placed between the output of the main rectifier and the input of the energy storage. As illustrated in Fig. 9(b), the output voltage of the replica power harvesting path V_{OR} represents the output voltage of the main power harvesting path V_{OM} when the power switch is OFF. V_{OM} equals to the voltage across the power storage V_{OL} when power switch is ON. The output voltage of the replica power harvesting path V_{OR} represents the output of the main power harvesting path in open-load condition and can be the indication of input power level. The voltage comparator compares V_{OR} and the voltage across the power storage V_{OL} for smart gating of the power switch. As illustrated in Fig. 9(b), the power switch is only closed if $V_{\text{OR}} > V_{\text{OL}}$, which indicates that the input power is high enough to charge the load. Otherwise, it is kept open for preventing reverse leakage.

B. Gating Implementation

As depicted in Fig. 10, the proposed self-gating RFEH implementation is based on the cross-coupled rectifier for taking advantage of its dynamic self-V_{th}-compensation. Its drawback of low output resistance leading to serious reverse leakage can be solved by the proposed smart self-gating method. The power switch is a PMOS transistor whose size is two times larger than the PMOS transistors in the main rectifier for decreasing its forward ON-resistance. The PMOS power switch is good for cold-start since it is closed by default with a low voltage level on its gate. The size of the replica rectifier

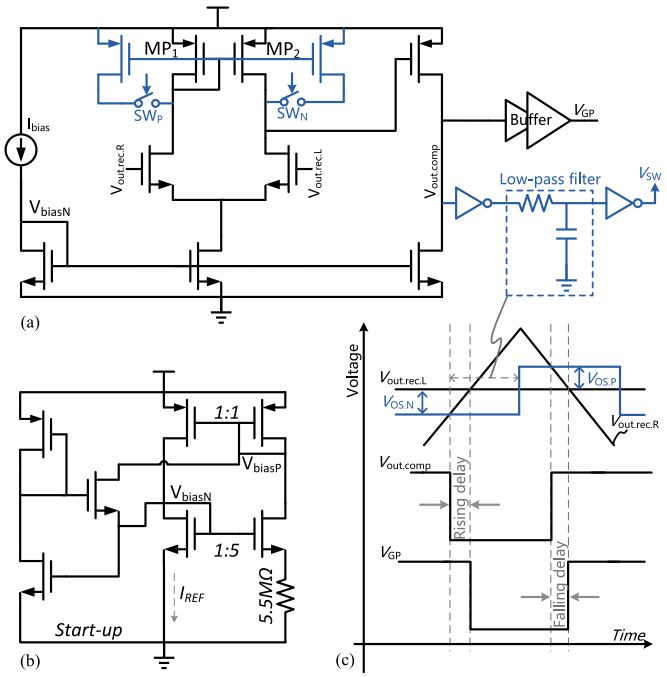

Fig. 11. Comparator sub-block schematics. (a) Proposed continuous-time proteretic comparator with intentional dynamic offset in a reverse hysteresis fashion. The baseline comparator alternative uses the same architecture but without the circuits in blue. (b) BMR for comparator biasing. (c) Proteretic comparator operating principle.

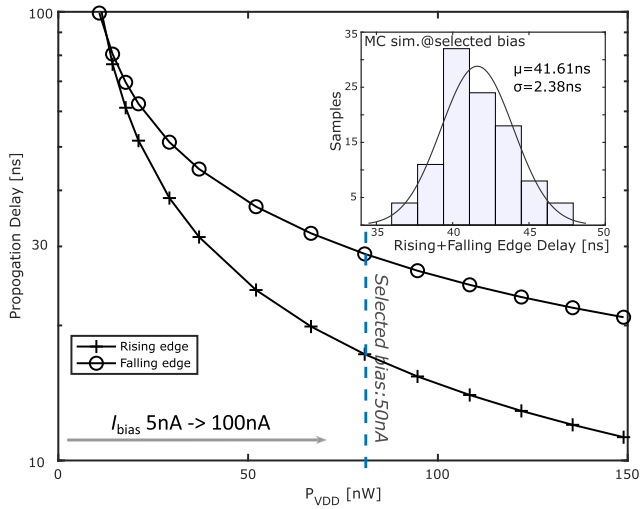

Fig. 12. Continuous-time baseline comparator propagation delay depending on power consumption by sweeping its bias current.

has an effect on the power consumed for sensing, which is wasted because it is not harvested by the main rectifier. The smaller the dimension of the replica, the less the power spent on sensing. The minimum replica-rectifier size usually depends on the minimum RF transistor width allowed by the CMOS fabrication process. In our design, the main rectifier uses transistors dimensions of 24 μm/60 nm and 48 μm/60 nm, respectively, for NMOS and PMOS, which is around 60× larger than for the replica rectifier. It results in a 60× higher input resistance (R_{rec}). The replica-rectifier output is open,

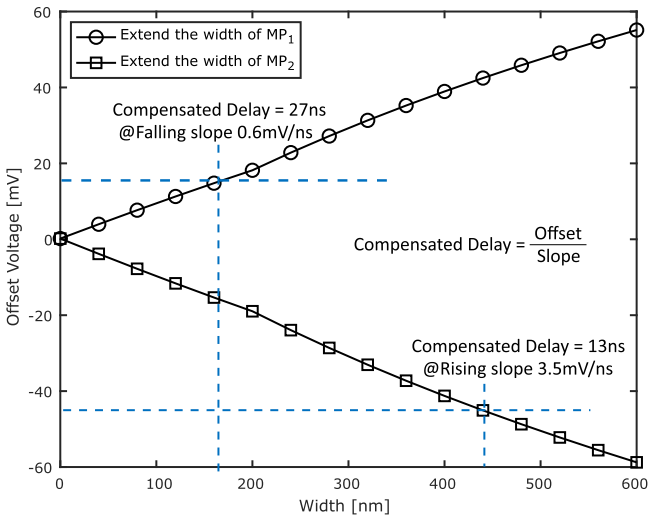

Fig. 13. Offset voltage depending on extended width in continuous-time proteretic comparator PMOS current mirror.

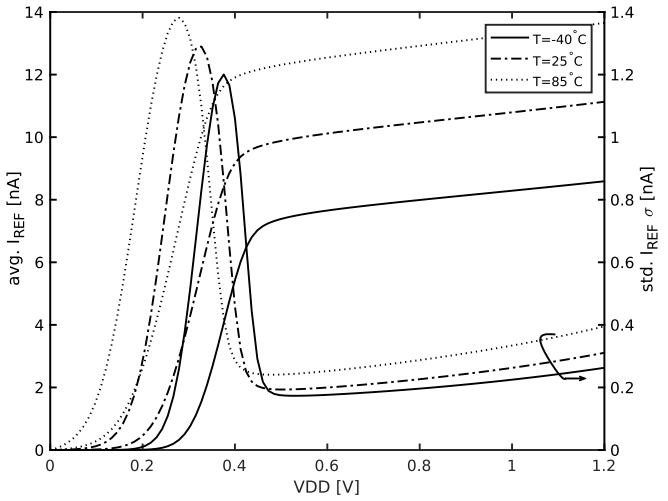

Fig. 14. BMR current average value and standard deviation over PVT by the Monte Carlo (MC) simulation.

which further increases its R_{rec}. Thus, the replica rectifier adds a negligible load to the power source. The capacitors C_{OR} and C_{OM} are used to filter out the ripple of the rectifier output voltage. The ratio between C_{OR} and C_{OM} should be the same as the ratio between the transistor sizes of the replica rectifier and those of the main rectifier for the replica to accurately track over time the open-circuit voltage of the main rectifier.

The comparator compares the voltage $V_{\text{out.rec.L}}$ on the energy storage capacitor C_{OL} and the replica-rectifier output voltage $V_{\text{out.rec.R}}$. The output of the comparator dynamically controls the power switch through a buffer for improving driving ability. If $V_{\text{out.rec.R}} > V_{\text{out.rec.L}}$, it means that the input power is high enough to charge the load, and the power switch turns on. On the contrary, if $V_{\text{out.rec.R}} < V_{\text{out.rec.L}}$, it stands for the low input power, and the power switch turns off for avoiding the stored energy reverse leakage. As depicted in Fig. 11(a), we use a two-stage voltage comparator with n-type differential pairs because its inputs have a high common-mode voltage level. The comparator is implemented with

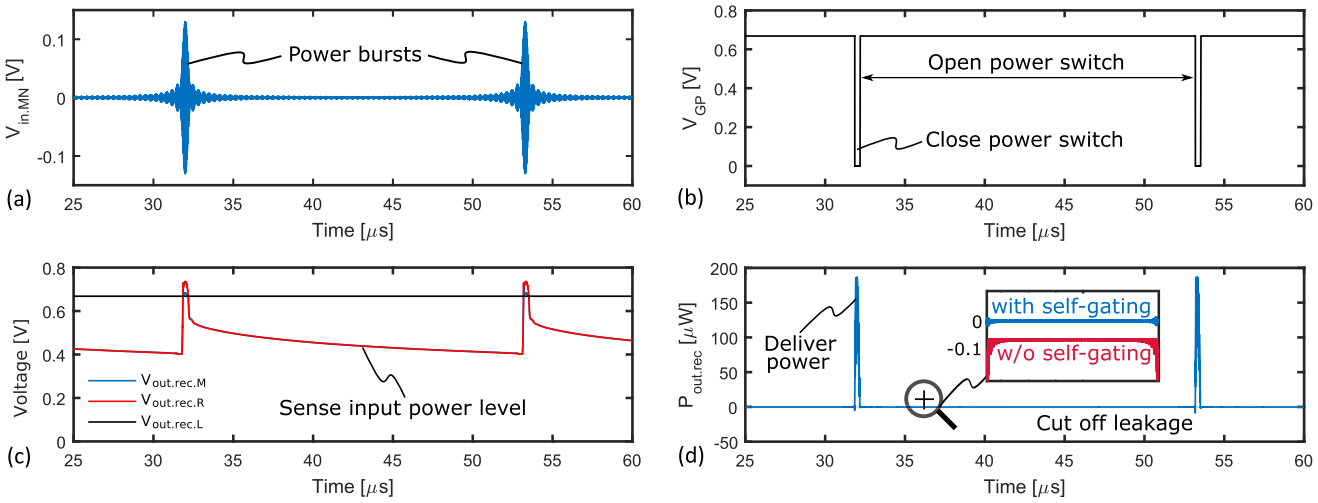

Fig. 15. Self-gating RFEH transient behavior of (a) MN input voltage, (b) power switch gating voltage, (c) rectifier output voltage, and (d) harvested power under the high-PAPR incident power waveform.

LVT transistors and a medium gate length of 0.2 μm for preserving low capacitive load while improving comparator analog performance compared to minimum gate length. The buffer transistor width is the geometric mean (square root of the product) of the comparator second stage transistor width and the power switch width.

The comparator rising- and falling-edge delays have a critical impact on the performance of the proposed smart self-gating system. Provided that the power gate cannot operate in time, the available power cannot be delivered to the storage side or previously stored energy reversely leaks to the ground. Fig. 12 shows the propagation delay of a continuous-time baseline comparator (i.e., the comparator depicted in Fig. 11(a) without circuits in blue) depending on its power consumption by sweeping the bias current. The propagation delay and power consumption here include the contributions of the buffer and power switch. The falling edge has a longer delay than the rising edge since the reverse leakage current on $V_{\text{out.rec.R}}$ (causing a falling edge) is less sharp than its forward current (causing a rising edge). The propagation delay decreases as the power consumption P_{VDD} increases by stepping up the comparator bias current. We choose a bias current of 50 nA, which typically leads to 80 nW of power consumption as a tradeoff.

To avoid wasting input power at the start of the power burst and leaking at the end of the burst, we propose to compensate for the comparator delay by using a protoretic comparator. Such a comparator features an intentional input offset working as reversed hysteresis. In Fig. 11(a), we propose an implementation of a proteretic comparator based on a disbalance of the PMOS current mirror as a function of the comparator output. As illustrated in Fig. 11(c), the high level of V_{SW} opens switch SW_P and closes switch SW_N for extending the width of MP_2. It causes a negative offset $V_{\text{OS.N}}$ for compensating the rising-edge delay. Conversely, it causes a positive offset $V_{\text{OS.P}}$ for compensating the falling-edge delay by extending the width of MP_1. As a result, the power switch is more precisely turned on when $V_{\text{out.rec.R}}$ is above $V_{\text{out.rec.L}}$. With negative hysteresis, protoretic comparators can be unstable. To avoid instability, we add a small RC filter to delay the change in the comparator offset. As depicted in Fig. 13, we achieve a negative offset of 45.5 mV by extending the width of MP_2 by 225% with the parallel switchable transistor, which compensates for a 13-ns rising-edge delay with a 3.5-mV/ns input signal slope. A lower positive offset of 16.2 mV is achieved by an extension of 75% of MP_1 width to compensate a 27-ns falling-edge delay due to the lower falling slope of 0.6 mV/ns.

The comparator bias current is generated by a beta-multiplier reference (BMR) [20], as shown in Fig. 11(b). It includes a startup circuit for avoiding the unwanted operating point where zero current flows in this self-biased circuit. As depicted in Fig. 14, the startup voltage can be as low as 0.4 V with around 300-mV bias voltage V_{biasN} at typical room temperature. The power supply VDD for the self-gating circuits comes from the output of the rectifier $V_{\text{out.rec.L}}$ for easy cold-start instead of the output of the external PMU. The MPPT is performed by the off-the-shelf PMU. To this end, it includes a switch for periodic disconnection of the power trace to sense rectifier open-circuit voltage and then regulates the rectifier output voltage to a given ratio $\gamma_{\text{MPPT.RFEH}}$ of its open-circuit voltage. At 2.45 GHz, we need to size the matching network in a parasitic-aware manner [2]. We have here $C_{\text{mp}} = 2$ pF, $L_{\text{m}} = 7$ nH, and $C_{\text{OM}} = 0.45$ pF, which is formed by package and PCB parasitic capacitor.

The RFEH transient behavior is illustrated in Fig. 15. Replica-rectifier output $V_{\text{out.rec.R}}$ represents the input power level. During T_{burst}, the gate voltage V_{GP} is at low level for closing the PMOS power switch, and then, the delivered power $P_{\text{out.rec}}$ shows a pulse. During T_{gap}, the gate voltage V_{GP} is at high level for opening the PMOS power switch. It avoids the reverse leakage, which happens without the proposed self-gating mechanism. The voltage comparator response edge delay is clearly shown in Fig. 16. At the start of the power burst, the sharp rising edge on $P_{\text{out.rec}}$ means that it turns on

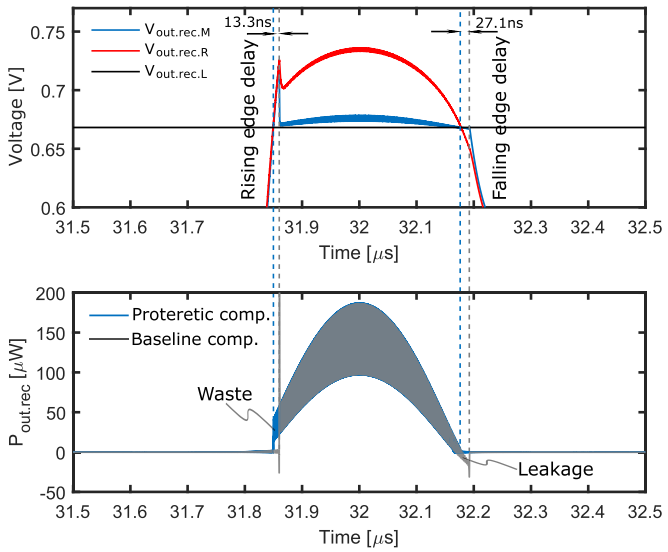

Fig. 16. Zoomed-in view of the transient behavior of Fig. 15(c) and (d).

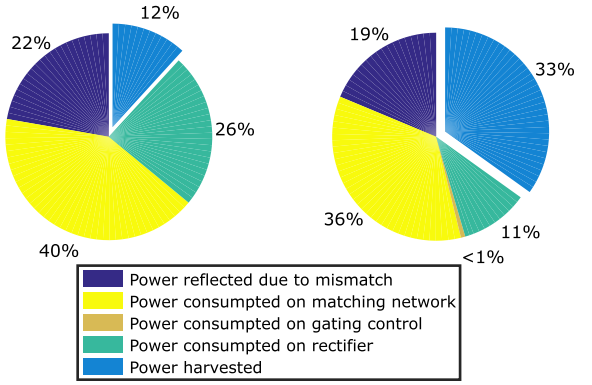

Fig. 17. Power budget comparison at $P_{\text{incident}} = -16$ dBm. Left pie: without gating control. Right pie: with gating control.

when the instantaneous incident power is already significant, which leads to some power loss. At the end of the power burst, $P_{\text{out.rec}}$ goes to negative, meaning that the storage power leaks to the ground due to the power switch opening delay. The power waste and reverse leakage are reduced by the proposed proteretic comparator with the dynamic offset. As depicted in Fig. 17, the power budget clearly illustrates that the proposed self-gating RFEH harvests more power than the one without gating control. The power consumed on the rectifier significantly drops due to the self-gating preventing serious power leakage.

V. Prototyping and Measurement

As depicted in Fig. 18, the proposed high-PAPR power waveform is generated by a USRP-2944 from National Instruments (NI) as an RF generator implementing the mathematical process, as shown in Fig. 5. The RFEH prototype is interfaced with an off-chip 50-Ω Balun for converting the single-end RF input to differential inputs for the cross-coupled rectifier. The PHE here includes the Balun insertion loss (around 1 dB). The Balun, which degrades the power efficiency, can be avoided if the rectifier output voltage is referring to

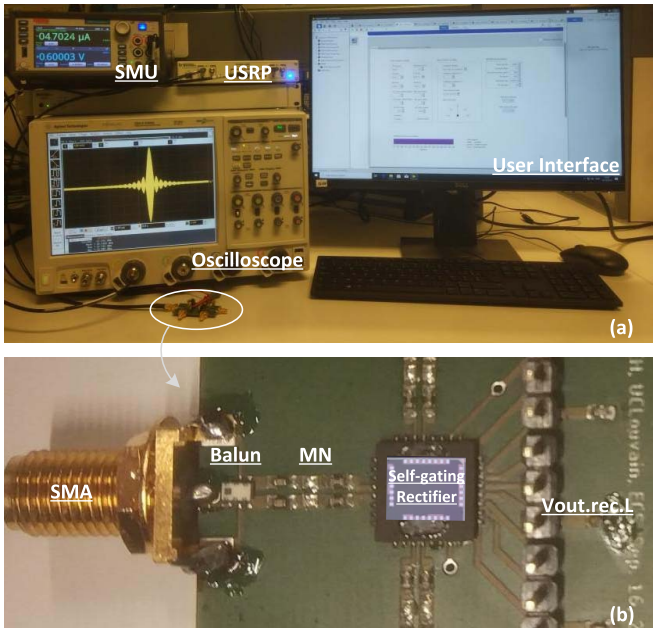

Fig. 18. Self-gating RFEH prototype test setup. (a) High-PAPR WPT power waveform generation. (b) Self-gating RFEH test PCB board.

a floating (virtual) ground [21]. The matching network is composed of discrete components, which have a better quality factor ($Q_{\text{ind.}} = 35$ and $Q_{\text{cap.}} = 200$) compared to on-chip inductor and capacitors. The cross-coupled rectifier with a smart self-gating control circuit is designed and fabricated in 65-nm LP CMOS technology from TSMC. The rectifiers use low-V_{th} (LVT) RF transistors for targeting low input P_{incident}. The threshold voltages are about 350 mV for NMOS and 400 mV for PMOS at their minimum gate length, i.e., 60 nm. The rectifier output is regulated by the AEM30940 PMU from e-peas semiconductors for MPPT and storage charging [22]. It performs MPPT by disconnecting its internal converters from its input at every 0.33 s. The open-circuit sensing time window is about 5 ms, which is far longer than the incident high-PAPR power waveform symbol period of 21.33 μs. It allows configuring the γ_{MPPT} ratio at 50%, 65%, or 80%. Its regulation ratio is selected to optimize the PHE. This PMU can cold-start from a 380-mV input voltage. We, thus, define here the RFEH sensitivity as the minimum P_{incident} for reaching around 400-mV rectifier output voltage at the open circuit. As depicted in Fig. 14, the beta-multiplier current reference also starts to work when VDD reaches 400 mV.

The measured power consumption overhead of the self-gating control is shown in Fig. 19. It is supplied from $V_{\text{out.rec.L}}$ for easy cold-start. The power consumption is around 120 nW at incident power -15 dBm with 0.6-V VDD, which meets our design target, as depicted in Fig. 12. Around 74% of the power is consumed by the comparator. The power loss proportion is less than 1.5% if $P_{\text{incident}} > -22$ dBm. The self-gating control with the proteretic comparator consumes an additional power of 13 nW since the *RC* low-pass filter incurs more short-circuit power loss, as depicted in Fig. 11. As depicted in Fig. 20, the PHE of the RFEH depends on its output voltage $V_{\text{out.rec.L}}$ since $V_{\text{out.rec.L}}$ has an effect on PCE_{rec} and Z_{rec}. The optimal $V_{\text{out.rec.L}}$

TABLE I
TECHNIQUE AND PERFORMANCE COMPARISON

	This work	[2] 2019 JSSC	[8] 2020 TCAS-I	[13] 2017 TCAS-II	[14] 2019 JSSC	[15] 2017 JSSC	[16] 2017 ESSCIRC	[23] 2013 JSSC
Process	65nm	65nm	0.18µm	65nm	0.18µm	0.18µm	40nm	130nm
Frequency	2.45GHz	2.45GHz	868MHz	900MHz	915MHz	915MHz	900MHz	2.4GHz
Rectifier Topology	Cross-coupled	Cross-coupled	Greinacher doubler	Cross-coupled	Greinacher doubler	Greinacher doubler	Cross-coupled	Cross-coupled
Techniques	High-PAPR, self-gating	Parasitic-aware	ULP diode, V_{th} compensation	Dual-path	Reconfigure rectifier	Reconfigure MN and rect.	Reconfigure MN	Co-design
Config. Switch	No	No	No	Yes	Yes	Yes	Yes	No
Rectifier Stages	1	1	5	5	2-12	2-8	1	4
Rectifier Load	MPPT PMU	MPPT PMU	Resistor 330kΩ	Resistor 147kΩ	PMU	PMU	MPPT PMU	PMU
Sensitivity @$V_{out.rec.OC}$	-26.7dBm @400mV	-17.1dBm @400mV	-15.8dBm* @400mV	-17.7dBm @1V	-17.8dBm @1V	-14.8dBm @1V	-15dBm @N.A.	-12.6dBm @500mV
Peak PHE @$P_{incident}$	32.3% @-14.1dBm	48.3% @-3dBm	10.7% @-13.3dBm	34.5% @-2dBm	34.4% @1.3dBm	26% @0dBm	47% @0dBm	15.9% @0dBm

* Estimated from figure of measurement results.

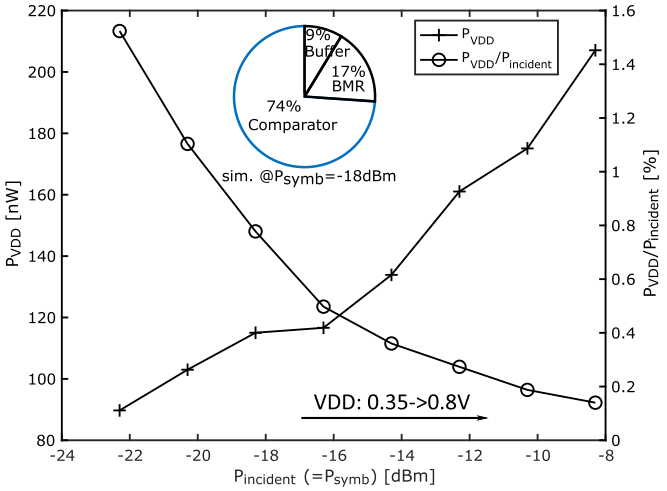

Fig. 19. Power consumption measurement of the self-gating control circuit with the baseline comparator. The proteretic comparator marginally increases the power consumption of the self-gating control circuit by 10%, which remains negligible compared to the incident power.

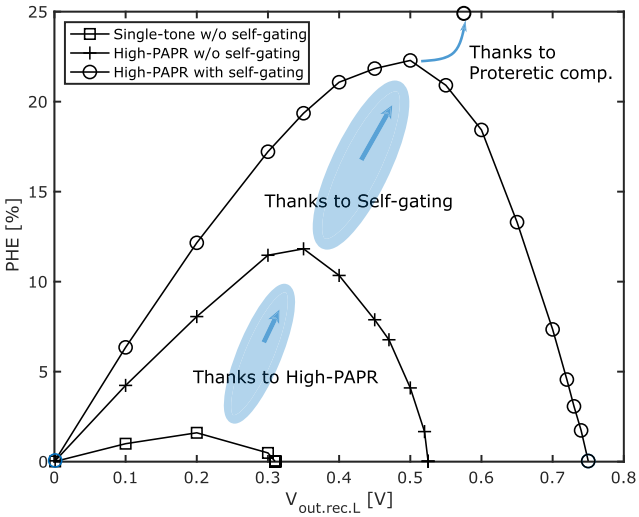

Fig. 20. PHE measurement of different RFEH systems depending on rectifier output voltage with $P_{\text{incident}} = -18$ dBm.

is about 65% of its open-circuit voltage, i.e., the optimal $\gamma_{\text{MPPT.RFEH}} = 0.65$. The proposed self-gating RFEH improves the PHE with a larger rectifier open-circuit output voltage (=0.75 V) at a low incident RF power level of −18 dBm. Both Figs. 21 and 22 show the progressive RFEH performance improvement at low input P_{incident} due to high-PAPR incident waveform, the proposed self-gating RFEH, and the proteretic comparator. Without the proposed self-gating circuit, the PHE does not increase as expected with high-PAPR incident power due to the reverse leakage, as analyzed in Section III. When P_{incident} is above −8 dBm, the RFEH with single-tone incident RF power has the best result. Since the RFEH is optimized at $P_{\text{incident}} = -5$ dBm, the higher the average power P_{symb}, the higher the burst power P_{burst} with low PHE if $P_{\text{burst}} > -5$ dBm and, finally, the less benefits coming from the use of high-PAPR incident waveform, as expressed in (5) and (6).

In Figs. 21 and 22, the degraded performance of self-gating control with the proteretic comparator compared to the baseline comparator is due to an over-compensation of the delay at high level P_{symb}. The delay is actually decreased at high input P_{symb} because of the higher supply voltage of the buffer after the comparator. When the compensation by proteretic comparator exceeds the practical delay, it causes power leakage before $V_{\text{out.rec.R}}$ reaches up to $V_{\text{out.rec.R}}$ and power waste before $V_{\text{out.rec.R}}$ drops down to $V_{\text{out.rec.R}}$. Measurement results are compared with the state-of-the-art works in Table I. Our design has the peak PHE at the lowest incident RF power level. The proposed smart self-gating RFEH has the lowest sensitivity at −26.7 dBm with 0.4-V open-circuit voltage. Let us mention here that the proposed system uses only one rectifier stage. The rectifier output voltage can be easily boosted by increasing the number of stages.

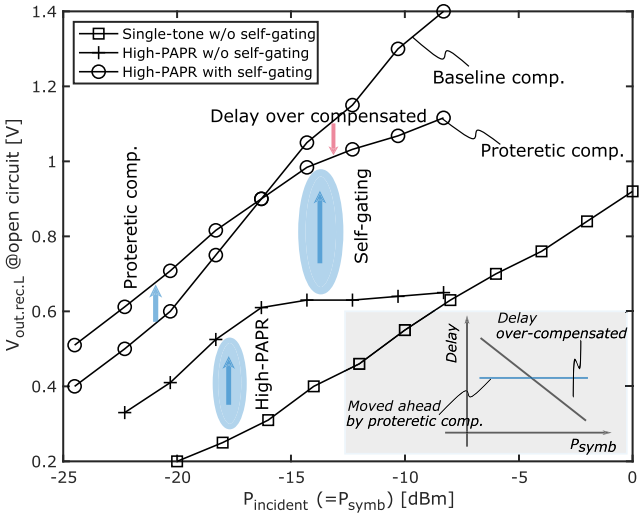

Fig. 21. Open-circuit voltage measurement of different RFEH systems depending on input RF incident power level.

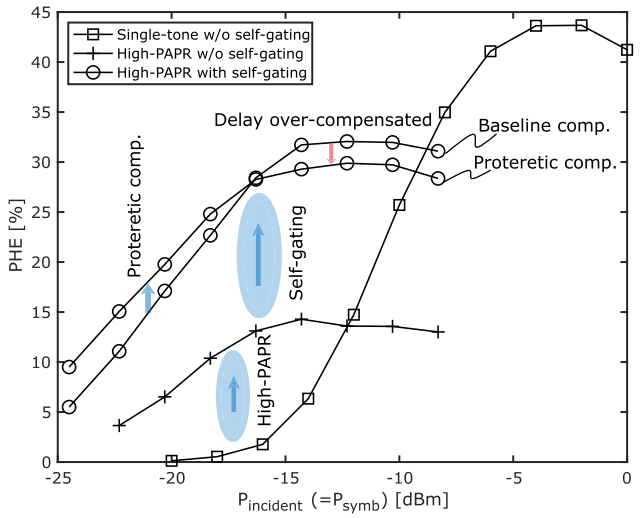

Fig. 22. PHE measurement of different RFEH systems depending on input RF power level.

VI. Conclusion

Both cross-coupled rectifier and high-PAPR WPT waveform are suited for improving the PHE of RFEHs at low incident RF power levels, which is the target for far-field WPT in IoT applications. However, if we directly combine the two techniques together, the PHE is seriously degraded by the reverse leakage current in between the power bursts due to the low cross-coupled rectifier output resistance.

The proposed self-gating RFEH is useful to exploit the potential of the cross-coupled rectifier with the high-PAPR WPT waveform and to improve the PHE at low incident RF power level. A power switch is added between the output of the rectifier and its load (energy storage capacitor or PMU). A continuous-time sensing circuit is designed to provide an indication of the level of input power. As a function of this power level, the switch is controlled to dynamically connect or gate the power path for delivering the harvesting power or preventing the reverse current leakage, respectively. The critical gating-control delay is compensated by a proposed proteretic comparator. Both PHE and sensitivity are greatly improved at low RF incident power levels under EIRP regulation.

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Pengcheng Xu (Graduate Student Member, IEEE) received the bachelor's degree (Hons.) in physics from Shanghai Normal University, Shanghai, China, in 2013, the master's degree (Hons.) in integrated circuit engineering from Tongji University, Shanghai, in 2016, and the Ph.D. degree in electrical engineering from the Université catholique de Louvain (UCLouvain), Louvain-la-Neuve, Belgium, in 2021.

In 2015, he was an Exchange Student with the University of Erlangen-Nuremberg, Erlangen, Germany. From February 2017 to November 2020, he was a Research Assistant in electrical engineering with UCLouvain. Since November 2020, he has been a Research Associate with the Department of Circuits and Systems, Fraunhofer Research Institution for Microsystems and Solid State Technologies EMFT, Munich, Germany. He was the Holder of the Chinese National Scholarship three times. He has authored or coauthored nine technical articles, including JSSC, IEEE International Solid-State Circuits Conference (ISSCC), and IEEE Asian Solid-State Circuits Conference (ASSCC). He holds one delivered European patent. His research area includes analog and mixed-signal integrated circuit design.

Mr. Xu is also a Student Member of IEEE Solid-State Circuits Society (SSCS). He was a recipient of the Shanghai Outstanding Graduates Student Award and the Meritorious Winner in the 2013 Mathematical Contest in Modeling of America (MCM). He also serves as a Reviewer for various journals and conferences, such as the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I/II, IEEE WIRELESS COMMUNICATIONS LETTERS, and IEEE ACCESS.

Denis Flandre (Senior Member, IEEE) received the M.S. degree in electrical engineering, the Ph.D. degree, and the Research Habilitation degree from the Université catholique de Louvain (UCLouvain), Louvain-la-Neuve, Belgium, in 1986, 1990, and 1999, respectively. His Ph.D. research was on the modeling of silicon-on-insulator (SOI) MOS devices for characterization and circuit simulation. His Ph.D. thesis was on a systematic and automated synthesis methodology for MOS analog circuits.

Since 2001, he has been a Full-Time Professor with UCLouvain. He is a Co-Founder of CISSOID, Mont-Saint-Guibert, Belgium, a spin-off company, focusing on SOI and high-reliability integrated circuit design and products, and a Scientific Advisor of other UCLouvain start-ups: INCIZE (semiconductor characterization and modeling), e-peas (energy harvesting and processing solutions for the IoT), and VOCSens (gas sensing microsystems). He has authored or coauthored more than 1000 technical articles or conference contributions. He has co-invented 14 patents. He has organized or lectured many short courses on SOI technology, devices, and circuits in universities, industrial companies, and conferences. He has participated in or coordinated numerous research projects funded by regional and European institutions. He is involved in the research and development of SOI MOS devices, digital and analog circuits, and sensors, MEMS, and solar cells, for special applications, more specifically ultralow-voltage low-power, microwave, biomedical, radiation-hardened and high-temperature electronics, and microsystems.

Dr. Flandre has been a member of several EU Networks of Excellence on High-Temperature Electronics, SOI Technology, and Nanoelectronics and Micro-Nanotechnology and is an Active Member of the SOI Industry Consortium and the EUROSOI Network. He was a recipient of several scientific prizes and best paper awards.

David Bol (Senior Member, IEEE) received the M.Sc. degree in electromechanical engineering and the Ph.D. degree in engineering science from the Université catholique de Louvain (UCLouvain), Louvain-la-Neuve, Belgium, in 2004 and 2008, respectively.

In 2005, he was a Visiting Ph.D. Student with the CNM National Center for Microelectronics, Seville, Spain, in advanced logic design. In 2009, he was a Post-Doctoral Researcher with intoPIX, Louvain-la-Neuve, where he was involved in low-power design for JPEG2000 image processing. In 2010, he was a Visiting Post-Doctoral Researcher with the Laboratory for Manufacturing and Sustainability, University of California at Berkeley (UC Berkeley), Berkeley, CA, USA, where he was involved in life-cycle assessment of the semiconductor environmental impact. He is currently an Assistant Professor with UCLouvain. In 2015, he participated in the creation of e-peas semiconductors, Louvain-la-Neuve. He leads the Electronic Circuits and Systems (ECS) Research Group, UCLouvain, focused on the ultra-low-power design of smart-sensor integrated circuits for the IoT and biomedical applications with a specific focus on environmental sustainability. He has authored or coauthored more than 120 technical articles and conference contributions. He holds three delivered patents. His personal IC interests include circuit design for computing, power management, sensing, and wireless communications. He is actively engaged in the social-ecological transition in information and communications technology (ICT) innovation.

Dr. Bol also serves as a TPC Member of IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S) and a Reviewer for various journals and conferences, such as IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, and IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I/II. He (co-)received three Best Paper/Poster/Design Awards in IEEE conferences (such as IEEE International Conference on Computer Design (ICCD) 2008, SOI Conference 2008, and IEEE Faible Tension Faible Consommation (FTFC) 2014). Since 2008, he has presented several invited papers and keynote tutorials in international conferences, including a forum presentation at IEEE International Solid-State Circuits Conference (ISSCC) 2018.