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**Design and Characterization of Monolithic
Microwave Integrated Circuits in CMOS SOI
Technology for High Temperature
Applications**

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Scientific Publications

Articles in periodicals

- [1] **M. El Kaamouchi**, M. Si Moussa, G. Wybo, A. Bens, J.-P. Raskin and D. Vanhoenacker-Janvier, “A 2.4-GHz Fully Integrated ESD-Protected Low-Noise Amplifier in 130-nm PD SOI CMOS Technology,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 55, pp. 2822 – 2831, Dec. 2007.
- [2] D. Vanhoenacker-Janvier, **M. El Kaamouchi**, M. Si Moussa, “Silicon-on-Insulator for high-temperature applications,” *IET circuits, Devices and Systems*, vol. 2, pp. 151 – 157, Feb. 2008.
- [3] **M. El Kaamouchi**, P. Delatte, M. Si Moussa, J.-P. Raskin and D. Vanhoenacker-Janvier, “Temperature Behavior of Spiral Inductors on High Resistivity Substrate in SOI CMOS Technology,” *Journal of Solid-State Electronics*, (Accepted).

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- [1] **M. El Kaamouchi**, M. Si Moussa, J.-P. Raskin and D. Vanhoenacker-Janvier, “DTMOS Low Noise Amplifier Design in Partially Depleted SOI CMOS Technology,” *IEEE International SOI Conference*, Niagara Falls, USA, pp. 127 – 128, October 2-5, 2006.
- [2] **M. El Kaamouchi**, M. Si Moussa, P. Delatte, G. Wybo, A. Bens, J.-P. Raskin, and D. Vanhoenacker-Janvier, “A 2.4-GHz Fully Integrated ESD-Protected Low-Noise Amplifier in 130-nm PD SOI CMOS Technology,” *IEEE MTT-S International Microwave Symposium IMS 2007*, 3-8 June 2007, pp. 2091 – 2094.
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- [5] A. El Oualkadi, **M. El Kaamouchi**, J.-M. Paillot, D. Vanhoenacker-Janvier and D. Flandre, “Fully Integrated High-Q Switched Capacitor Bandpass Filter with

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- [8] **M. El Kaamouchi**, M. Si Moussa, J.-P. Raskin and D. Vanhoenacker-Janvier, “A 2-mW Power Consumption Low Noise Amplifier in PD SOI CMOS Technology for 2.4 GHz Applications,” *IEEE MTT Wireless, 7th Silicon Monolithic Integrated Circuits in RF Systems*, Long-Beach, USA, pp. 253 – 256, 10-12 January 2007.
- [9] M. Emam, **M. El Kaamouchi**, M. Si Moussa, J.-P. Raskin and D. Vanhoenacker-Janvier, “High Temperature Antenna Switches in 130 nm SOI Technology,” *IEEE International SOI Conference 2007*, Indian Wells, USA, pp. 121 – 122, October, 2007.
- [10] **M. El Kaamouchi**, G. Dambrine, M. Si Moussa, D. Vanhoenacker-Janvier and J.-P. Raskin, “Body-Biasing Control on Zero-Temperature-Coefficient in Partially Depleted SOI MOSFET,” *IEEE MTT Wireless, 8th Silicon Monolithic Integrated Circuits in RF Systems*, Orlando, FL, USA, pp. 114 – 117, 23-25 Jan. 2008.

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- [2] M. Emam, **M. El Kaamouchi**, M. Si Moussa, J.-P. Raskin, and D. Vanhoenacker-Janvier, “RF Antenna Switches Based on 130 nm Floating and Body-Tied SOI CMOS Technology,” *Third Workshop of the Thematic Network on SOI Technology, Devices and Circuits*, Leuven, Belgium, pp. 78 – 79, 24-26 January 2007.
- [3] **M. El Kaamouchi**, M. Si Moussa, J.-P. Raskin and D. Vanhoenacker-Janvier, “Temperature Behavior of Spiral Inductors on High Resistivity Substrate in SOI CMOS Technology,” *Fourth Workshop of the Thematic Network on SOI Technology, Devices and Circuits*, Tyndall National Institute, Cork, Ireland, pp. 72 – 73. Jan 23-25, 2008.

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- [5] **M. El Kaamouchi**, M. Emam, C. Roda Neve, J.-P. Raskin and D. Vanhoenacker-Janvier, “CMOS technologies for RF applications in harsh environment,” *MTT workshop CMOS technologies for RF applications, MTT 2008*, esa 2008 (Accepted).

Glossary

BC	Body-Contacted
BOX	Buried Oxide
BT	Body-Tied
CMOS	Complementary Metal-Oxide Semiconductor
CPW	CoPlanar Waveguide
DC	Direct Current
DTMOS	Dynamic Threshold MOSFET
DUT	Device Under Test
ELO	Epitaxial Lateral Overgrowth
ESD	ElectroStatic Discharge
FB	Floating-Body
FBE	Floating-Body Effect
FD	Fully Depleted
FET	Field-Effect Transistor
GIFBE	Gate Induced Floating-Body Effect
HBM	Human Body Model
HR	High Resistivity
HT	High Temperature
IC	Integrated Circuits
IF	Intermediate Frequency
LNA	Low-Noise-Amplifier
MAG	Maximum Available Gain
MEMS	Micro-Electro-Mechanical Systems
MESFET	MEtal-Semiconductor Field Effect Transistor
MIM	Metal-Insulator-Metal
MIS	Metal-Insulator-Semiconductor
MMIC	Monolithic Microwave Integrated Circuit
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MS	MicroStrip Line
MSG	Maximum Stable Gain
NF	Noise Figure
PD	Partially Depleted
PMD	Primary Metal Dielectric
RF	Radio Frequency
SCE	Short Channel Effects
SIMOX	Separation by IMplanted OXYgen

SoC	System-on-Chip
SOI	Silicon-on-Insulator
SOS	Silicon-on-Sapphire
STD	Standard Resistivity
STI	Shallow Trench Isolation
TFMS	Thin Film MicroStrip
TLP	Transmission Line Pulse
TRL	Thru-Reflect-Line
ULG	UniLateral Gain
VCO	Voltage Control Oscillator
VNA	Vector Network Analyzer
ZMR	Zone Melting Recrystallization
ZTC	Zero-Temperature-Coefficient

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CHAPTER 1

INTRODUCTION

Wireless communication has thrived in the last decade, owing to exploding user demand for information and the commensurate need for connectivity. Substantial research effort has focused on many application areas, such as cellular phones, cordless phones, GPS (global positioning system), and WLANs (wireless local area networks).

The radio frequency integrated circuits (RFIC) have been the primary domain of III-V (GaAs, GaN) and silicon germanium (SiGe), bipolar silicon (BiCMOS) technologies since those technologies provide relatively high cut-off frequencies and superior noise performances.

Because the baseband analog and digital chips can be implemented on the same CMOS chips, CMOS can provide an extremely low-cost technology to implement the future circuit blocks, along with the added benefit of potential large-scale integration. For this reason, most successful commercializations of RF bulk CMOS products have been implemented with systems-on-chip (SoCs), in which a high level of integration could be achieved: radio transceivers for WLAN, Bluetooth and ZigBee standards, GPS receivers, transceivers for DECT (Digital European Cordless Telephony) cordless and GSM cellular phones.

Moreover, as device dimensions have continued to scale down, CMOS technologies are now able to seriously compete with compound semiconductors. For instance, 45 nm gate length nMOS devices were recently reported with a transit frequency of 485 GHz. The rapid improvement of the RF capability of silicon is now widely considered as a viable option to replace GaAs in many applications.

Passive components which usually include resistors, capacitors, inductors, varactors and transmission lines, are frequently used for impedance matching, resonant circuits, filters, and bias circuits in radio frequency integrated circuits (RFICs), such as Low-Noise-Amplifiers (LNAs), Voltage-Control-Oscillators (VCOs), mixers, and Power-Amplifiers (PAs). The performance of RF CMOS transistors is usually good enough for most of the RF applications. Therefore, the RF performance of passive devices always plays a key role in determining the overall characteristics of the entire circuit. For instance, integrating VCOs into RF transceivers with standard CMOS technologies is usually one of the most challenging design tasks, because there are many critical parameters that must be considered. Examples of such critical parameters are large frequency tuning range, low power consumption, and low phase noise. All these parameters are primarily determined by the passives used in VCO circuits.

In this context, SOI technology constitutes a good candidate for mixed signal

RF CMOS applications. Due to its low junction capacitance and reduced leakage current, SOI provides reduced static and dynamic power consumption of the digital logic combined with increased cut off frequencies. Moreover, in terms of passive device integration the major benefit of SOI when compared to the conventional bulk is the possibility to use a high resistivity substrate which allows a drastic reduction of substrate losses allowing a high quality factor of the passive devices.

Another issue is the harsh environment applications. Harsh environments are characterized by temperature ranges up to 200°C – 300°C for the majority of applications. Electronics capable of operation at high temperatures find application in a number of industries, including the automobile industry, the aerospace industry, the electrical and nuclear power industries, and the well-logging industry.

High temperature is a large value market that has been difficult to serve up to now. In automotive electronics, on-engine and on-transmission applications are projected to require maximum temperatures of up to 200°C with the wheel-mounted applications going even higher. These applications include engine control, transmission control, antilock brake system (ABS), active suspension and wheel speed sensors. Further high temperature application areas include aerospace and environmental monitoring, such as mining and well logging. A system in which both the sensor and control electronics are fabricated in SOI technology would allow the complete assembly to reside in a thermally harsh environment. This would allow cost and weight reduction by eliminating requirements for cabling for remotely located electronics.

The capability of SOI circuits to expand the operating temperature range of integrated circuits up to 300°C has been demonstrated. SOI devices and circuits present advantages in this field over bulk counterparts such as the absence of thermally-activated latch up and reduced leakage current. Indeed, SOI technology is emerging as the most mature solution for harsh environment applications.

1.1 Receiver architectures for low-power applications

The capability of radio-waves to provide almost instantaneous distant communications without interconnection wires has been a major factor in the explosive growth of communications during the twentieth century.

In addition, the rapid multiplication of standard applications using wireless communication has dramatically increased the demand for universal wireless connectivity. In order for the companies that support the standards to stay competitive, low-cost, small form-factor portable wireless communication devices are critical components. Cost is a very important concern to attract a large group of users. The desire for a low-cost wireless device with reasonable performances has exploded as well [1] [2] [3].

The current implementations, while they are becoming denser, are still extremely complex and do not conduct to significant reductions in cost and size. A radical change in thinking regarding the implementation of the transceiver is necessary [4] [5] [6]. To that end, the amount of investigation into the feasibility of using adequate technologies for the implementation of the circuitry used in these devices has dramatically increased as well.

Two main transmitter-receiver architectures are possible: the super-heterodyne and homodyne architectures. The architecture choice is usually dependent of two parameters: cost and power consumption. In fact, “the cost/performances” compromise is the most important parameter in the integration of RF architectures. The size and power consumption of communication systems are mainly imposed by the RF-block situated between antenna and signal processing. Many improvements are actually made on different RF functions in order to minimize these two parameters [7].

1.1.1 *Super-heterodyne architectures*

The super-heterodyne (or heterodyne) receiver is the most widely used reception architecture. This technique finds numerous applications from personal communication devices to radio and TV tuners... Many varieties exist, but they essentially rely on the same concept: the RF signal is first amplified by a Low-Noise Amplifier stage, then translated to a lower intermediate frequency (IF), with significant amplification and additional filtering, and finally down-converted to baseband. The super-heterodyne architecture is illustrated in Fig. 1.1. The super-heterodyne receivers have several trade-offs. Image signal is the major inconvenient in this architecture. The image signal is due to the mixing operation between the local oscillator frequency and IF frequency. Because of the non-linearity of the mixers (often a simple analog multiplier), the result of the up-conversion operation generates signals at $f_{LO} - f_{IF}$ and at $f_{LO} + f_{IF}$ frequencies [1]. If the received band of interest is centered around $f_{LO} - f_{IF}$, then the image is around $f_{LO} + f_{IF}$ and vice versa [8] [9].

In some cases, when the integration parameter is not very important, the critical filtering functions are realized by passives and are not implemented on silicon; the power consumption of these receivers can be kept low. In this case the passive filters are placed on an external substrate in combination with flip-chip bonding. The insertion loss in high frequency high Q filters must be compensated by a corresponding increase in gain to keep the SNR constant. This increases the power consumption of the super-heterodyne transceiver. Integrating these high-Q filters on silicon (using active filters) is not feasible because the power consumption of an active filter is proportional to the square of its quality factor. Additionally, the specificity of the IF filter to the signal bandwidth and hence the standard used, makes super-heterodyne

receivers unsuitable for multi-standard operation. Nonetheless, super-heterodyne is praised for its high selectivity and sensitivity.

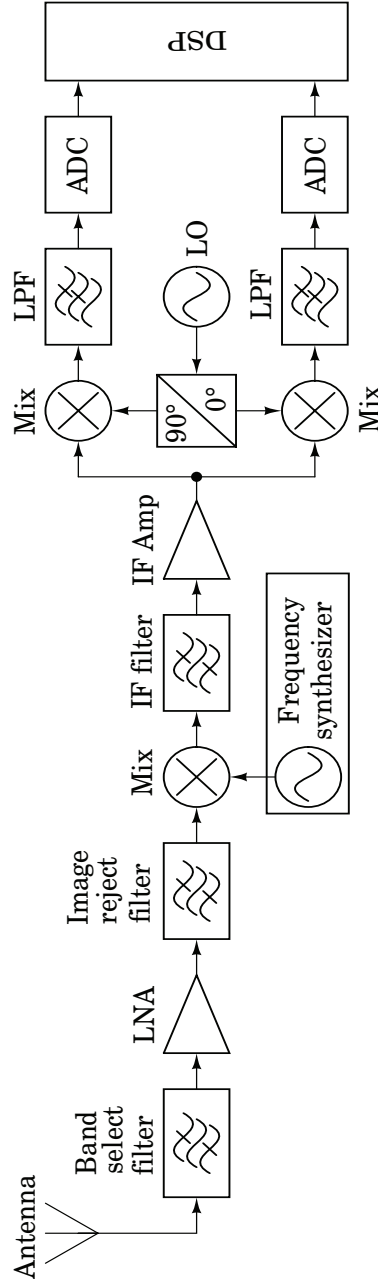


Figure 1.1: Architecture of super-heterodyne receiver.

1.1.2 Homodyne architectures

Zero-IF receiver architecture, also referred to as homodyne or direct-conversion and illustrated in Fig. 1.2, is the most natural solution to receive information vehiculed by a carrier [10] [11]. In the Zero-IF architecture the signal is converted directly to DC.

It has several qualities, which make it very suitable for integration as well as multi-band, multi-standard operation, but severe inherent obstacles that had for long kept it in the shadow of the super-heterodyne. First, the image problem is no longer present, since the IF is zero and the image to the desired channel, for all but single sideband signals, is the channel itself. Then, only one local oscillator (LO) is needed, which means only one phase noise contribution. Obviously, direct-conversion receivers require no expensive and bulky external filters for analog channel selectivity [12] [13]. Filtering now only occurs at low frequencies (baseband) with some amplification. This means less current consumption than at higher frequencies, fewer components, lower cost, etc. Practically, however, strong out of band interferers or blockers may need to be removed prior to down-convert in order to avoid desensitizing the receiver by saturating subsequent stages, as well as producing harmonics and intermodulation terms, which then appear in baseband. Such a filter may be placed after the LNA, for example. Zero-IF architectures, however, have serious inconvenient. In direct conversion, as the signal of interest is converted to baseband very early in the receive chain without any filtering other than RF band-selection, various phenomena contribute to the creation of DC signals, which are directly appearing as interfering signals in the band of interest [14] [15]. The LO may be conducted or radiated through an unintended path to the mixers RF input port, thus effectively mixing with itself, producing an unwanted DC component at the mixer output.

The Low-IF receiver architecture illustrated in Fig. 1.3 is one solution to protect the receiver from the direct current related obstacles that pertain to Zero-IF conversion, while retaining the homodyne benefit of the elimination of high-Q IF filters [16] [17]. As its name indicates, instead of directly converting the signal to baseband, the LO frequency is slightly offset from the RF carrier, typically one to two channels. The low-IF means that the fractional bandwidth of the IF bandpass filtering is large, making it possible to implement it with low-Q filters.

1.2 The IEEE 802.15.4 standard

The IEEE 802.15.4 standard (or ZigBee) is specially designed to satisfy the market need for a low cost and flexible wireless network technology, which supports low power consumption, reliability, low-cost and security for control and monitoring ap-

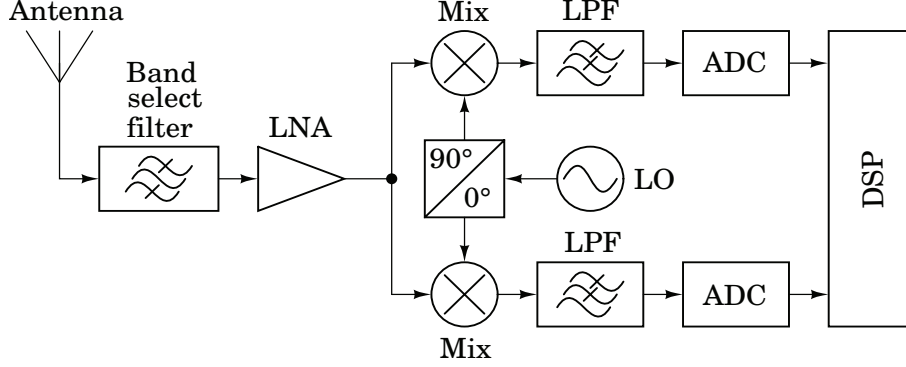


Figure 1.2: Zero-IF architecture receiver.

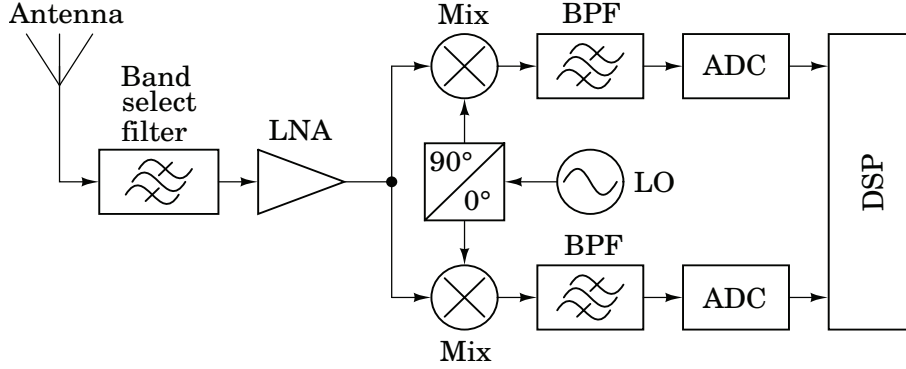


Figure 1.3: Low-IF architecture receiver.

plications with low to moderate data rates. The complexity and cost of the IEEE 802.15.4 compliant devices are intended to be low and scalable in order to enable broad commercial adaptation within cost sensitive applications.

Moreover, the demand of the ZigBee solution for harsh environments has increased these last years. Most of the applications are related to temperature sensor which is a fully featured radio sensor designed for harsh environments such as cold chain monitoring in transport and storage. These wireless temperature sensors have many applications. An example of an existing ZigBee device is the *TemperatureSensorOne* (TS1) provided by *IntelliSensingTM*, which is a ZigBee temperature sensor used for wireless industrial temperature measurement (-100°C to 200°C) operating at 2.4 GHz ISM frequency band.

Traditional heterodyne receivers with one or more intermediate frequency stages offer good channel selectivity and robustness, but they require expensive and bulky

off-chip filters resulting in low degree of integration and increased power consumption. The heterodyne receiver architectures are not optimal solutions for achieving the low-cost, low-power targets of IEEE 802.15.4 applications. With the homodyne architectures, there is no need for external high-Q filters, and these architectures offer a high degree of integration. The homodyne architectures (direct conversion and low-IF) are excellent candidates for completely integrated receivers with good performance at low power and small silicon area.

1.3 This work

This work has been funded by the “Région Wallonne” (Convention n° 03/1/5623), Belgium, in connection with the “Witness MEDEA+” project, in order to study and develop RF circuits for the IEEE 802.15.4 standard, intended for low-power and high temperature applications. The following chapters provide extensive and detailed information about the high temperature performances of devices and circuits implemented on SOI substrates.

The second chapter of this work introduces the SOI technology. Various SOI technologies and different existing processes of fabrication are presented. The electrical proprieties of the MOSFETs are discussed and the comparison between partially depleted, fully depleted and bulk transistors are presented.

The third chapter presents the analysis and characterization of transmission lines and integrated spiral inductors on SOI substrate. The impact of temperature on various types of transmission lines and on integrated spiral inductors implemented on high and standard resistivity substrate is investigated.

The temperature behavior of the SOI transistors is presented in the fourth chapter. The main figures-of-merit of the floating body, body contacted and dynamic threshold transistors are compared and the extraction of the extrinsic and intrinsic parameters of the small signal equivalent circuit is performed. It has been shown that the major high temperature effects in MOSFET devices are decreased threshold voltage, decreased mobility, and increased leakage current.

An example of RF circuit applications of the SOI technology, based on a fully integrated Low-Noise Amplifier for low-power and narrow-band applications, is investigated and characterized at high temperature in the fifth chapter. The main factors-of-merit of the designed circuit are extracted and discussed.

Finally, the importance of the ESD protection in RF devices and circuits is briefly introduced and an example of a LNA with an on chip ESD protection using an on-chip plug-and-play diodes protection strategy is proposed. The degradations of the LNA performances due to the ESD protection circuit are discussed.

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CHAPTER 2

SOI TECHNOLOGIES FOR RF ANALOG APPLICATION

2.1 Introduction

Silicon-on-Insulator (SOI) CMOS technology was considered as an exotic technology during several years and used for very specific applications. The explosion of low-voltage and low-power applications in a market widely dominated by portable and wireless communication systems, opened the door for SOI.

With advancement in state-of-the-art electronic systems and a huge demand for low-cost high-speed mixed-signal integrated systems, a considerable effort has recently been made to migrate several high-frequency elementary circuit blocks from GaAs to CMOS Silicon process. Since CMOS SOI devices present a very good high frequency behavior and a low-power consumption, it is of great interest to use them in RF circuit design [1]. Table 2.1 illustrates the factor-of-merit for the main Si technologies.

In the last decade, the MOS transistor channel length scaled down to deep sub-micron and improved device performance in terms of cut-off frequency. Recently, a 45 nm partially depleted (PD) SOI CMOS technology with a transition frequency f_T of 485 GHz, has been reported [2]. Such transition frequencies well above 100 GHz offer a comfortable frequency margin for designers. Recently, many designs of different RF blocs have demonstrated the interest of this technology for low-voltage and low-power applications [3]. Fig. 2.1 shows the evolution of transition frequency and maximum frequency of oscillation in the CMOS technologies.

Moreover, the CMOS SOI technology has many advantages compared to the conventional CMOS Bulk technology: lower substrate parasitic capacitances and therefore better RF performances, smaller devices without latch-up phenomena, reduction of short-channel effects, improved subthreshold slope and possibility to use high resistivity substrate to improve the quality factor of passive elements. All these advantages make the CMOS SOI a competitive technology for RF applications due mainly to low-power, low-cost, higher level of integrability and high performance mixed-mode circuits [4] [5].

Another superiority of the CMOS SOI on bulk technology concerns particular applications like harsh environment. In fact, the capability of SOI circuits to expand the operating temperature range of integrated circuits up to 300°C has been demonstrated. SOI devices and circuits present advantages in this field over bulk

counterparts, such as the absence of thermally-activated latch up and reduced leakage current. The SOI CMOS technology can be a viable alternative because the almost perfect isolation of nMOS and pMOS is afforded by the elimination of the CMOS well junctions which results in a latch-up-free operation [1] [6].

In this chapter, we will briefly present some properties of the SOI technology and SOI MOSFETs. In the following sections, the main advantages of SOI compared to the conventional bulk MOSFET transistors are presented. Then, some general properties of the SOI material are shown to introduce the different MOSFETs available in this technology and the main differences between the partially and fully depleted devices (PD and FD).

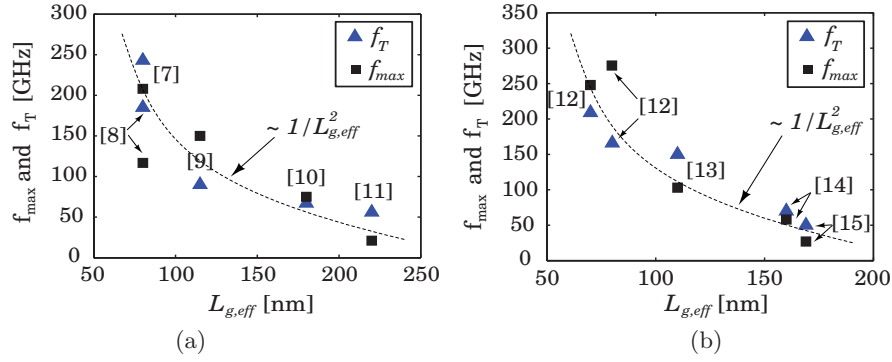


Figure 2.1: Evolution of transition frequency (f_T) and maximum frequency of oscillation f_{MAX} of nMOSFET versus the effective channel length ($L_{g,eff}$), for CMOS (a) SOI and (b) Bulk technology.

Technology	CMOS	Bipolar	HBT SiGe
Cost	++	+	+
Consumption	++	-	--
f_T and f_{MAX}	-	+	++
Noise	-	+	++
Integration	++	--	--
Linearity	++	+	+

Table 2.1: Factor-of-merit comparison in silicon technologies.

2.2 The CMOS SOI material

Silicon on insulator (SOI) is a layered structure consisting of a thin layer of silicon, from 50 nm to some μm , which is created on an insulating substrate. This insula-

tor material is usually sapphire (Silicon-on-Sapphire, SOS), air (Silicon-on-Nothing, SON) or silicon dioxide (Silicon-on-Insulator, SOI).

Various processes have been developed in industry to achieve a thin layer of silicon on insulator. The oldest one is the Silicon-On-Sapphire (SOS) commercialized for the first time in 1971 [1]. Fig. 2.2 shows the cross section of Silicon-on-Insulator and Silicon on Sapphire. Since 1980s, other process techniques have been developed and became, industrial standards. The two main processes are SIMOX (Separation-by-Implanted-Oxygen) and BSOI (Bonded SOI). The SOI wafers fabricated with these last processes (SIMOX and BSOI) currently represent 90% of the total of the SOI wafer market production. This paragraph presents the main commercial process fabrications of SOI wafers as well as the advantages and inconvenients each of them.

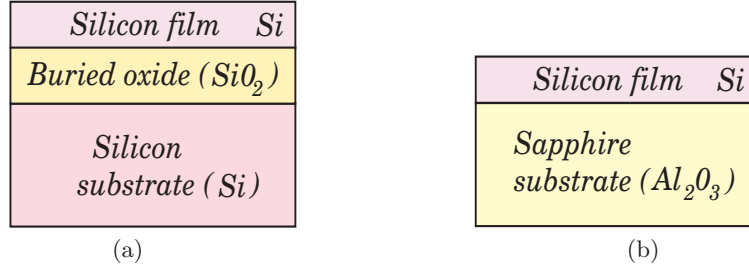


Figure 2.2: Cross section of Silicon-on-Insulator (a) and Silicon-on-Sapphire (b) substrate.

2.2.1 Silicon-on-Sapphire

The Silicon-on-Sapphire or SOS has been developed since 1964 [7] [8]. At the beginning this technology was mainly intended for space digital applications owing to radiate hardness of the technology [9]. Since the 1980s, the SOS technology has taken new interest in analog applications in order to find an alternative of conventional CMOS bulk [10]. Silicon-on-Sapphire substrates are obtained by growing a silicon film on top of a sapphire substrate (Al_2O_3). The main drawbacks of this technology are the high fabrication cost and the presence of defects between the silicon film and sapphire substrate. These defects induce a decrease in the mobility, which then degrades the performances of this technology [11]. However, a new step has been introduced in the process fabrication of SOS wafers: it consists in recrystallization in solid phase of the wafer (step n°3), after the epitaxy (step n°1) and the implant of silicon ions, Si^+ (step n°2). This operation has been added in order to minimize the defects in the substrate. It is called SPER (Solid Phase Epitaxial Regrowth). Fig. 2.3 shows the main steps in SOS process fabrication.

Thanks to the interesting properties of sapphire substrate, the SOS technology has many advantages. In fact, with a very high resistivity, the sapphire substrates allow high quality factors for passive elements, very low dielectric losses and no crosstalk perturbations. The drawbacks of SOS technology are the high fabrication cost and presence of defects at the interface between the silicon film and sapphire substrate.

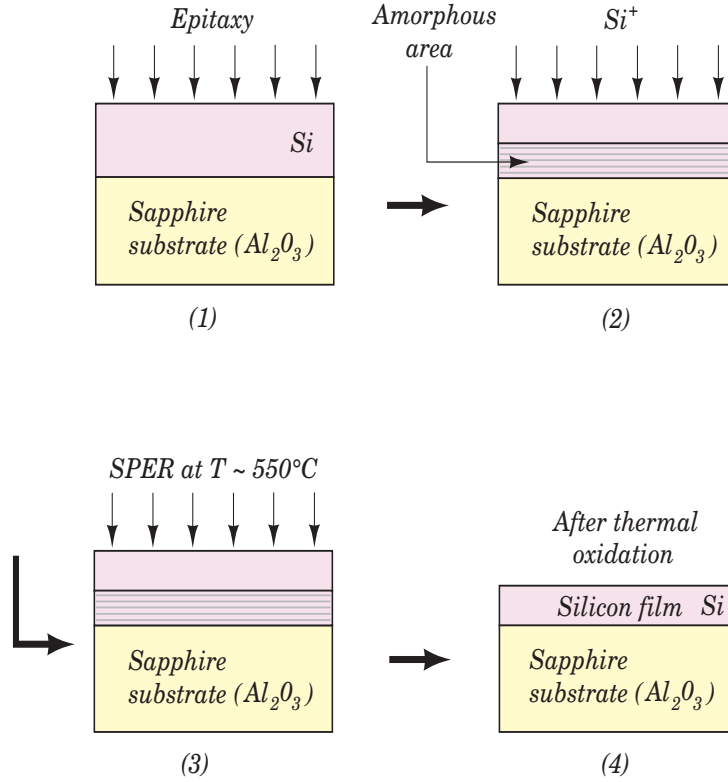


Figure 2.3: The different steps in fabrication process of SOS wafers.

2.2.2 SIMOX fabrication process

The Separation by IMplantation of OXygen or SIMOX process, has been developed in 1970s by professor Izumi [12]. Since 1980, this technique has been improved and adapted for the fabrication of SOI wafers. Fig. 2.4 shows the different steps for the fabrication of the buried oxide layer in SOI technology. This process technique uses an implant of oxygen ions at $650^\circ C$. In this last operation, a high dose of oxygen ions are necessary to allow the isolation of a thin silicon layer in a bulk silicon wafer (see step n°2). Then, a thermal annealing at high temperature ($T \approx 1320^\circ C$) allows

the creation of a SiO_2 (buried oxide layer) at the desired depth (see step n°3). The thermal annealing also allows to reduce the defects introduced in the oxygen ions implantation step. The SIMOX technology has been highly used between 1985 and 1995 for SOI fabrication process and is still used nowadays by some foundries like IBM.

MICROX or Microwave SIMOX, developed since 1990s, is another SOI fabrication process based on the SIMOX principle. The MICROX process, is only used in the case of silicon high resistivity substrates. The passive devices fabricated on high resistivity substrates have a better performances compared to the devices fabricated on standard resistivity. In the analog domain, these performances are comparable with those achieved with GaAs technology [13].

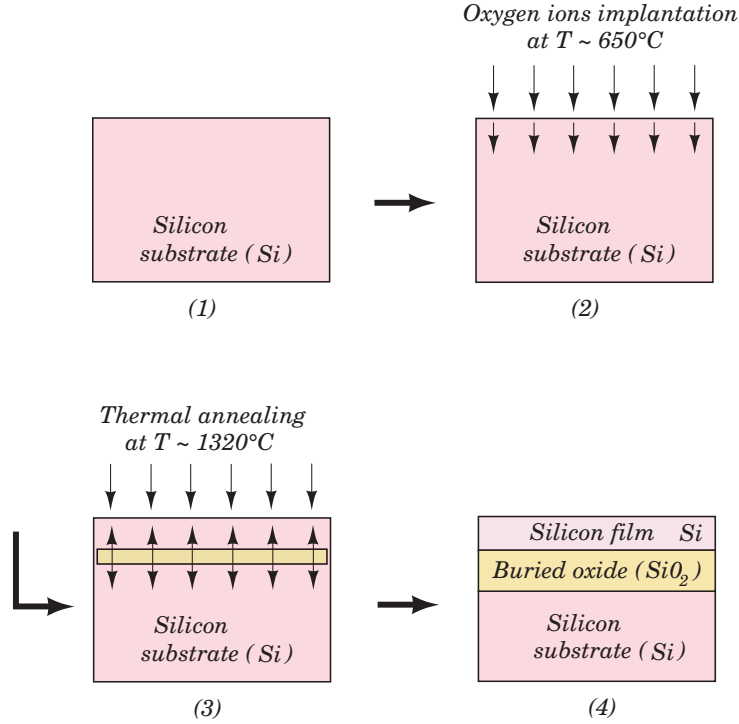


Figure 2.4: Different steps in SIMOX fabrication process of SOI wafers.

2.2.3 Bonded SOI fabrication process

SOI wafer bonded materials are built by bonding two wafers together. A variety of bonding approaches have been developed, such as the Bonded Etched-back (BESOI)

and the Smart-Cut process. The Smart-Cut method has been developed in 1991 by M. Bruel [14] and is widely used nowadays by SOITEC under the name of Unibond material. Fig. 2.5 illustrates the different steps of the fabrication of Unibond SOI wafers using the Smart-Cut process: a first bulk silicon wafer (wafer A) receives a thermal oxidation (step n°1). Then, this wafer receives a implant of hydrogen ions (step n°2). The wafer A is then bonded with a second silicon bulk wafer (wafer B), by hydrophilic bonding (step n°3). After a thermal annealing, the wafer is split into two parts at Etch-stop depth (step n°4). Then the SOI wafer obtained receives a new thermal annealing at $T \approx 1100^{\circ}C$ and chemo-mechanical polishing in order to achieve the desired surface roughness and layer thickness of the Silicon film (step n°5). The remainder wafer A can still be used to make other silicon films. The advantages of the Smart-Cut technique are [1] [15]: a good quality of silicon film and buried oxide with a better uniformity of the silicon surface than in the SIMOX process case. This is very interesting for the integration of MEMS devices. The Smart-Cut technique is widely used in industrial fabrication and can be used for large volume production. Note that the Smart-Cut technique can be also applied for other substrates as GaAs, InP, SiC etc [16].

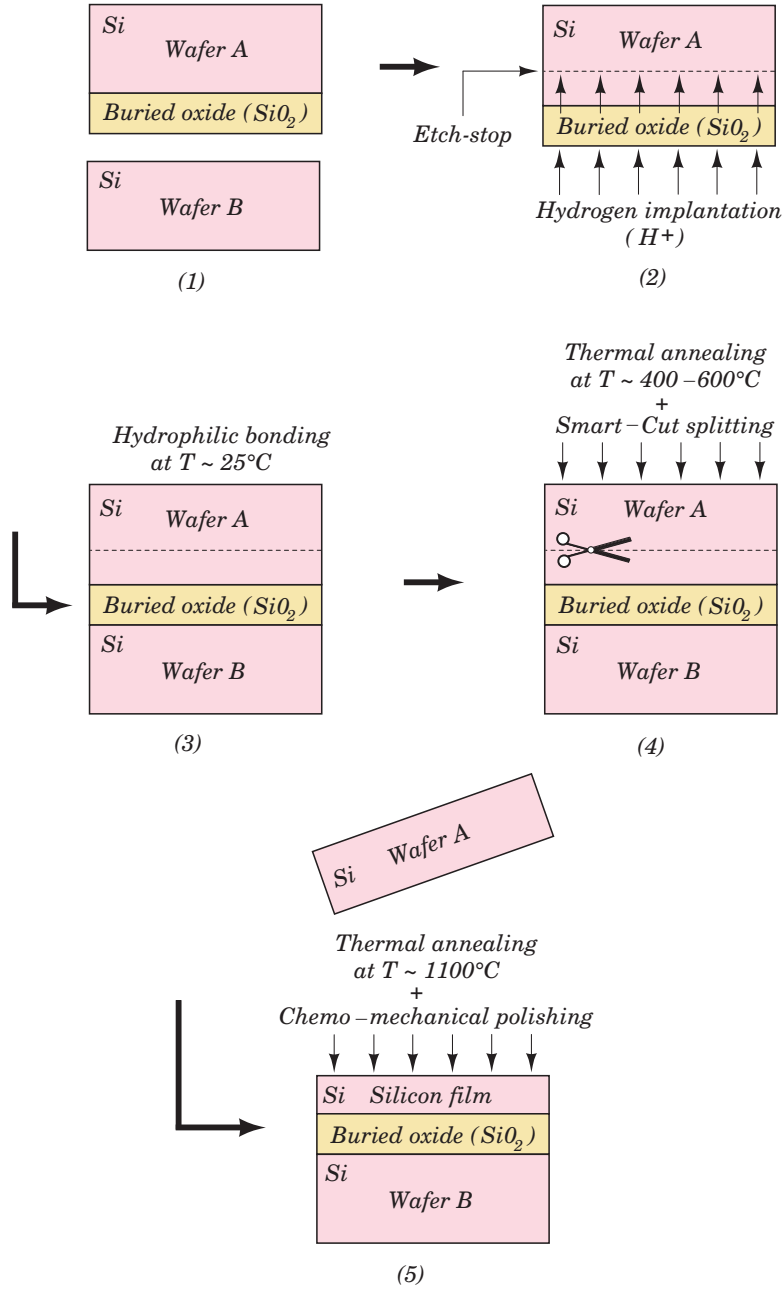


Figure 2.5: Different steps of the fabrication of Unibond fabrication wafers in CMOS SOI technology using the Smart-Cut process.

2.2.4 Other SOI fabrication methods

Other techniques are used for fabrication of SOI wafers as ELO (Epitaxial Lateral Overgrowth), ZMR (Zone Melting Recrystallization) and FIPOS (Full Isolation by Porous Oxidized Silicon). The ELO and ZMR methods are mainly used in the fabrication process of 3D integrated circuits. The ELO technique consists in growing the silicon from opening in the silicon oxide. The ZMR method consists in recrystallization of a silicon introduced at the surface of the silicon oxide layer by using a thermal source (laser beam, halogen lamps etc.). Fig. 2.6 illustrates the ELO and ZMR technologies. These two technologies give a bad quality SOI material [17]. The FIPOS method is mainly intended for photonic applications.

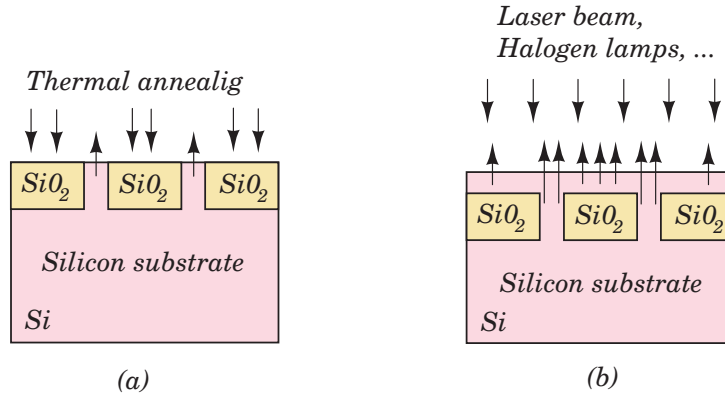


Figure 2.6: Fabrication of wafers in CMOS SOI technology using (a) ELO and (b) ZMR process.

2.3 Comparison between SOI and bulk technologies

The success of the SOI technology is due to its superiority when compared to the conventional bulk silicon. The advantages of the SOI make this technology one of most promising candidates in the future [18] [15]. In SOI structures (see Fig. 2.7), the top active silicon region is separated from the underlying substrate by a thick insulator layer (Buried oxide layer) whereas a Bulk MOSFETs is built atop the surface of a monocrystalline silicon wafer (see Fig. 2.8). Thanks to the BOX layer, the SOI devices are insulated from the substrate [19]. So there is no need to further isolate the devices from one another as in the case of bulk silicon. This minimizes the area occupied by the MOSFETs and offers a higher integration density. Moreover, the source/substrate and drain/substrate junctions capacitances and leakage currents

2.3 COMPARISON BETWEEN SOI AND BULK TECHNOLOGIES

are radically reduced. The reduction of the parasitic capacitances of the MOSFET increases the cut-off frequency of the transistor, allowing very high speed devices when compared to the bulk silicon devices. Another way of comparing the devices is that, for the same speed of SOI and bulk CMOS technologies, the CMOS SOI devices have a lower power-consumption. The insulation from the substrate also provides immunity against the unwanted thyristor triggering (also called latchup parasitic effect [4] [20]). In the SOI MOSFETs, the space charge in the thin film of silicon is well controlled by the gate. As a consequence, the well known Short Channel Effects (SCE) are reduced when compared to classical bulk MOSFET. As reported by [1], in the SOI MOSFETs, the inverse subthreshold slope is lower than in a bulk MOSFET, allowing better performances in particular at low power supply. And finally, the SOI technology provides a good insulation from substrate injection noise (crosstalk) due to the oxide insulation between devices and specially between the analog and digital devices [21] [22]. As seen earlier, the buried oxide layer offers a isolation between the active device region and the bulk substrate. This provides an additional degree of freedom when selecting the resistivity of the substrate. Using a near intrinsic substrate to reduce the capacitive coupling and the losses is impossible in bulk technology due to latchup.

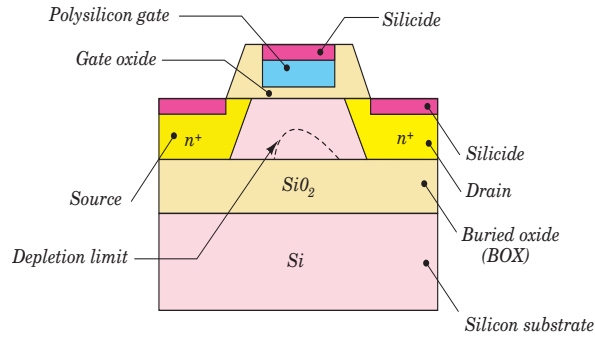


Figure 2.7: Illustration of a cross section in a CMOS SOI MOSFET.

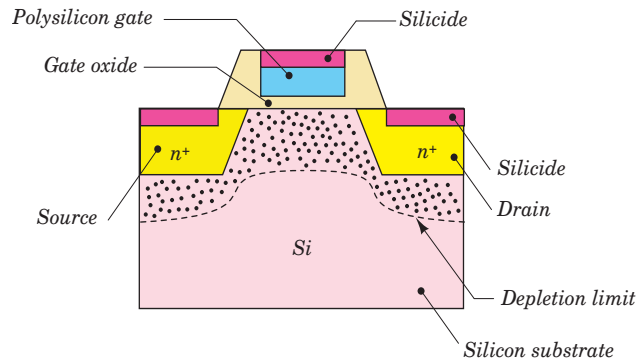


Figure 2.8: Illustration of a cross section in a CMOS bulk MOSFET.

2.4 CMOS SOI technology

2.4.1 PD and FD SOI technologies

In SOI technology, there are two distinct families of devices: the Fully-Depleted (FD) and the Partially-Depleted (PD). The difference between these families is the thickness of the maximum depletion zone. The polysilicon-gate, the gate-oxide and the undepleted region above the buried oxide (called the body) form a Metal-Insulator-Semiconductor (MIS). Another MIS is formed by the silicon substrate, buried-oxide and the body. The consequence is the formation of two space charge zones near the front and the back interfaces of the *Si* film as shown in Fig. 2.9. The first one is governed by the gate voltage while the second is controlled by the substrate voltage (the substrate is often called back-gate). Each gate of the SOI structure imposes a potential on its *Si/SiO₂* interface and as a consequence, induces specific working modes (accumulation, depletion or inversion). When the MIS structure is working in inversion mode, the thickness of the depleted zone is maximum.

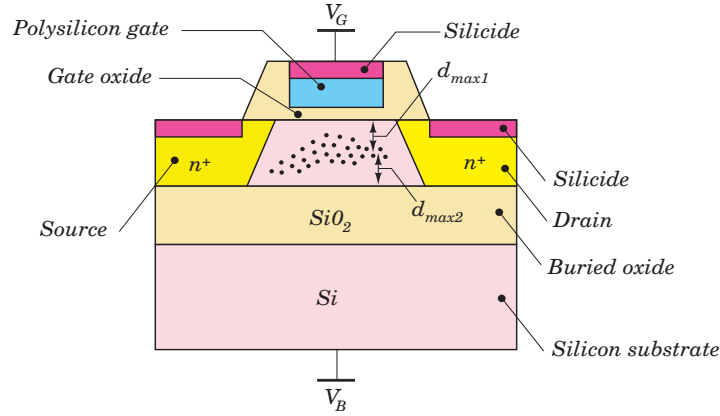


Figure 2.9: Illustration of a depleted zone in Partially depleted CMOS SOI MOSFET.

The maximum thickness of each depleted zone is approximatively given by the following equation:

$$d_{max1,2} = \sqrt{\frac{4\epsilon_{si}\phi_F}{qN_a}} \quad (2.1)$$

where ϕ_F and ϵ_{si} are respectively the Fermi potential and the permittivity of the silicon. N_a and q are the density of acceptors atoms and the charge of the electron.

The MOSFET is fully depleted when the space charge zone extends over the entire thickness of the active film of silicon. When a small zone of this silicon film is not

depleted, the device is referred to as partially depleted. The small zone where the silicon film is not fully depleted is called the floating body [23]. In the fully depleted SOI MOSFET, the depletion zone is controlled by the front-gate and back-gate (substrate) potentials via the the gate-oxide (C_{ox1}) and buried oxide capacitances (C_{ox2}), respectively. In case of the partially depleted SOI MOSFET, the front-gate capacitance is connected to the depletion capacitance of the silicon film (C_{dep}). Fig. 2.10 illustrates the total capacitances in PD and FD SOI structures. V_G and V_{GB} are, front-gate and back-gate potentials, respectively. C_{si} and C_{sub} are, the capacitance of silicon film and the substrate capacitance, respectively.

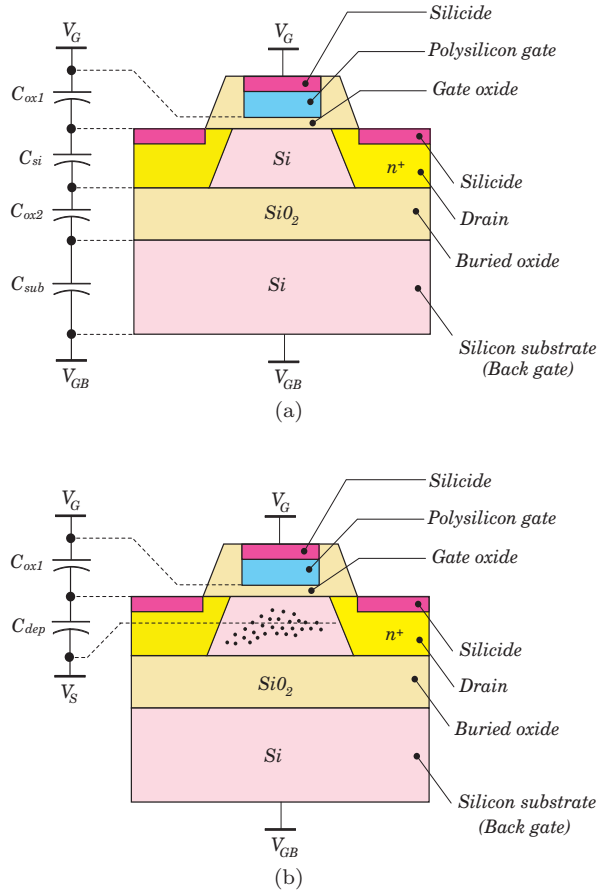


Figure 2.10: Illustration of a simplified capacitive network seen from the gate of a fully depleted (a) and a partially depleted (b) SOI MOSFET.

2.4.2 Threshold voltage

In PD SOI MOSFET, the threshold voltage (V_{TH}) is defined in the same way as for the conventional bulk MOSFET. The threshold voltage can be considered as the limit for which the channel is in depletion mode. In case the body is floating, the potential of the substrate can be neglected and the expression of V_{TH} for a n-channel transistor is given by:

$$V_{TH} = V_{FB} + 2\phi_F + \frac{qN_a d_{max}}{C_{ox1}} \quad (2.2)$$

where V_{FB} is the flat band voltage, ϕ_F is the Fermi potential, q is the charge of the electron, N_a is the density of acceptor atoms and C_{ox1} is the gate oxide capacitance. Replacing the parameter d_{max} by the expression (2.1) and introducing a new coefficient γ , usually called the body-effect parameter [$V^{1/2}$], the threshold voltage of the PD SOI n-channel MOSFET can be expressed as:

$$V_{TH} = V_{FB} + 2\phi_F + \frac{\sqrt{4\epsilon_{si}qN_a\phi_F}}{C_{ox1}} = V_{FB} + 2\phi_F + \gamma\sqrt{2\phi_F} \quad (2.3)$$

$$\gamma = \frac{\sqrt{2\epsilon_{si}qN_a}}{C_{ox1}} \quad (2.4)$$

The influence of the body bias (V_B) on the threshold voltage in a thin-film SOI n-channel MOSFET is given by:

$$V_{TH} = V_{FB} + 2\phi_F + \frac{\sqrt{4\epsilon_{si}qN_a\phi_F}}{C_{ox1}} = V_{FB} + 2\phi_F + \gamma\sqrt{2\phi_F - V_B} \quad (2.5)$$

Only the last term depicts the dependence of threshold voltage on body bias. When a negative bias is applied to the body, the threshold voltage increases as a square-root function of the body bias.

2.4.3 Subthreshold slope

When the SOI MOSFET works in weak-inversion mode, the drain-source (I_{DS}) current is mainly due to the minority carriers diffusion and it only depends exponentially on the front-gate voltage V_{GS} . The expression of I_{DS} versus V_{GS} can be approximated by:

$$I_{DS} \approx \frac{W}{L_g} \mu C_{ox1} \phi_T^2 e^{\frac{V_{GS} - V_{TH}}{n\phi_T}} \left(1 - e^{-\frac{V_{DS}}{n\phi_T}} \right) \quad (2.6)$$

where the parameter W and L_g are the width and the length of the MOSFET, μ is the mobility. The coefficient n and the parameter ϕ_T are equivalent (according to [1]) to

$$n = 1 + \frac{\gamma}{2\sqrt{2\phi_F - V_B}} \approx 1 + \frac{C_{dep}}{C_{ox1}} \quad (2.7)$$

$$\phi_T = \frac{k_B T}{q} \quad (2.8)$$

where k_B is the Boltzmann constant, T is the temperature and q is the charge of the electron. In these conditions, the $\log(I_{GS}) - V_{GS}$ characteristic has a linear behavior. The inverse of this slope is called the inverse subthreshold slope or, in short, the subthreshold slope, and usually noted S . From equation (2.6) and (2.8), the expression of the subthreshold slope is given by:

$$S = \frac{\partial V_{GS}}{\partial \log(I_{DS})} = n \frac{k_B T}{q} \ln(10) \quad (2.9)$$

The ideal value of S is 60 mV/decade, which is achieved when $n \approx 1$ ($\gamma \approx 0$). For the thin-film fully depleted SOI devices, the value of S is very close of the ideal case. However, the partially depleted transistors cannot exhibit a subthreshold slope as good as fully depleted devices do.

2.4.3.1 Drain-source current

When the SOI MOSFET works in high-inversion regime, the drain-current is dominated by the drift of the minority carriers. In this case, the expression of the high-inversion current in a long channel SOI MOSFET is

$$I_{DS} = \mu C_{ox1} \frac{W}{L_g} \left[(V_{GS} - V_{TH}) V_{DS} - \frac{1+\alpha}{2} V_{DS}^2 \right] \quad (2.10)$$

where V_{TH} and V_{DS} are the threshold voltage and drain-source bias, respectively. the coefficient α is approximatively equal, in case of fully and partially depleted SOI MOSFET, to

$$\alpha(FD) \approx \frac{C_{si} C_{ox2}}{C_{ox1} (C_{si} + C_{ox2})} \quad (2.11)$$

$$\alpha(PD) \approx \frac{C_{dep}}{C_{ox1}} \quad (2.12)$$

The effect of the parameter α is often neglected in case of fully depleted SOI MOSFET ($\alpha \approx 0$) and in case of partially depleted, $0.3 \leq \alpha \leq 0.5$ [1].

In saturation region ($V_{DS} \geq V_{DS,limit}$), the drain-current in a SOI MOSFET can be expressed as:

$$I_{DS} = \frac{W}{L_g} \frac{\mu C_{ox1}}{2(1+\alpha)} (V_{GS} - V_{TH})^2 \quad (2.13)$$

and $V_{DS,limit}$ is given by:

$$V_{DS,limit} \approx \frac{V_{GS} - V_{TH}}{1 + \alpha} \quad (2.14)$$

It is important to note that the fully depleted SOI MOSFET exhibits a higher drain-current than the partially depleted transistor for the same device size. This is due to the value of the coefficient α which is smaller for fully depleted than for partially depleted SOI MOSFETs. This has as a consequence a higher transconductance g_m for FD than for PD. The expression of transconductance is given by:

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \frac{W}{L_g} \frac{\mu C_{ox1}}{1 + \alpha} (V_{GS} - V_{TH}) \quad (2.15)$$

Replacing $V_{GS} - V_{TH}$ by its expression given in equation (2.12), the transconductance becomes:

$$g_m = \left(2 \frac{W}{L_g} \frac{\mu C_{ox1}}{1 + \alpha} I_{DS} \right)^{1/2} \quad (2.16)$$

2.4.4 Floating body effects in PD SOI MOSFET

FD MOSFETs are known to provide superior characteristics than their PD counterparts in terms of cut-off frequencies, transconductance and noise [24] [25] [26]. However, the fabrication of FD devices is more challenging than PD devices, since FD devices are very sensitive to film thickness variations and inherently present higher source/drain resistances. On the other hand, PD CMOS SOI processing techniques can be easily imported from planar bulk technologies, thus leading to significantly lower processing cost. For this last reason all major foundries currently producing SOI wafers have adopted the PD architecture. However, PD SOI MOSFETs present the detrimental well-known floating body effects (FBE) [4] [27]. The floating body effects are associated with the body region in the silicon film that is left unconnected or floating. The potential of the body is then mainly controlled by external mechanisms, such as capacitive coupling with the other electrodes and charge injection. The FBE is responsible of many surprising behaviors in SOI MOSFETs and circuits, such as the well known parasitic kink effect which can be seen in saturation region in the output conductance and transconductance characteristics [28] [29].

In saturated regime, holes generated by impact ionization accumulate in the body, which leads to an increase of the body potential (V_{BS}). This potential is raised until the source/body junction becomes forward biased, which allows the additional

hole flow to leave the body region or recombine with incoming electrons in the junctions [30]. The effective threshold voltage of the MOSFET is reduced, as the potential of the body increases, inducing an increase of both the output current and the output conductance as illustrated in Fig. 2.11 which can have negative impacts on the performance of analogue circuits [31] [32]. It can be suppressed when the body is connected to a fixed potential [33].

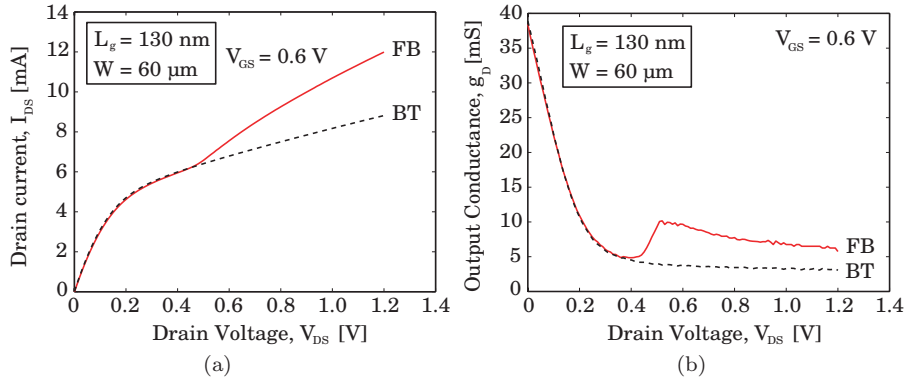


Figure 2.11: Illustration of the kink effect in a partially depleted SOI MOSFET in output characteristic ($I_{DS} - V_{DS}$) (a) and output conductance ($g_D - V_{DS}$) with a gate length $L = 0.13$ μm and a total width $W = 60$ μm .

On the other side, gate tunneling current becomes significant for gate bias values sufficiently large as to reduce the potential barrier for electrons across the gate oxide. The increase of drain current in this case affects the $I_{DS} - V_{GS}$ characteristic and produces a second “kink” in the $g_m - V_{GS}$ characteristic, which is called linear kink effect (LKE) [34] [27] or gate-induced floating body effect (GIFBE) [35]. The GIFBE is illustrated in Fig. 2.12. The GIFBE does not take place when the body is contacted.

2.4.5 PD SOI MOSFET technology

The geometry of a PD SOI MOSFET transistor is shown in Fig. 2.9. The quasi-neutral region (body) sandwiched between the space-charge regions extending from the front, lateral and back oxide/Si interfaces and Source/Drain junctions, is usually left electrically unconnected or floating (to form a Floating Body transistor). The body of the SOI MOSFET can also be connected to the source (to form a Body Contacted) and to the gate (to form a DTMOS). In the following, the three types of transistors will be analyzed.

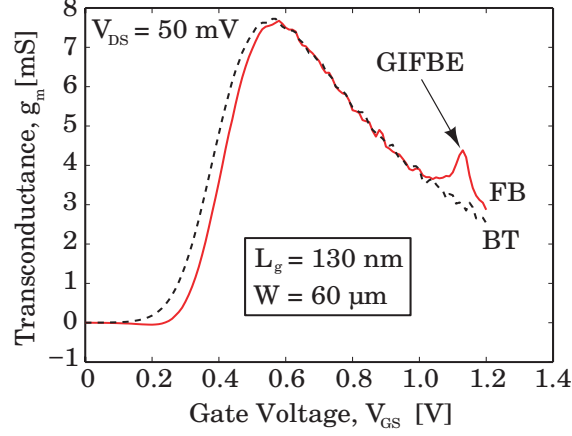


Figure 2.12: Illustration of the GIFBE (linear kink effect) in a partially depleted SOI MOSFET in transconductance characteristic ($g_m - V_{GS}$) (a) with a gate length $L = 0.13 \mu m$ and a total width $W = 60 \mu m$.

2.4.5.1 Floating body transistor

In SOI technology, the partially depleted (PD) SOI process scales well to smaller dimensions. However, the presence of the buried oxide layer results in a floating body region and the low thermal conductivity of the oxide causes self heating effects. Because of FB, SOI devices exhibit premature bipolar conduction (relative to bulk silicon devices) which coupled with the increase in the body voltage causes kink seen in the output characteristics of the partially depleted SOI n-MOSFETs. However, the kink is usually absent from p-channel SOI devices and in bulk MOSFETs when substrate or well contacts are provided (the base of the bipolar parasitic transistor is then connected to the ground) [1]. The kink effect constitutes a big disadvantage of the floating body transistor and limits its applications. In CMOS SOI technology, there are mainly two ways to provide body contact in SOI CMOS technology, as presented hereafter.

2.4.5.2 Body contacted transistor

Several approaches have been proposed to minimize the floating body effects in PD SOI based on either the reduction of the life-time of generated holes by introducing traps or the P+ body contacts for n-MOSFETs. The latter approach includes H-gate body contact, which has considerably large foot-print while allowing independent control of the body voltage [36]. On the other hand, introducing P+ regions in the source end of the device allows low resistance path to the holes at the expense of

reduced current drive. There are a number of ways to provide body contact, but the most common one resembles the structure shown in Fig. 2.13(b). The aim of this contact is to suppress the kink effect.

2.4.5.3 Dynamic threshold Transistor

The DTMOS SOI transistor is a partially depleted device with a contact between the gate and the body. DTMOS are fabricated using standard SOI PD CMOS processes [4]. The body of the SOI MOSFET is connected to the gate using a P+/-metal contact, as shown in Fig. 2.13(c). A DTMOS is a body contacted SOI transistor whose Threshold Voltage is dynamically controlled by connecting the body to the gate. As the body-source voltage V_{bs} is controlled, there is no floating body effect, and the threshold voltage swing is maximized, improving the I_{ON}/I_{OFF} ratio [24]. For higher voltages, the drain/body diode starts conducting and current limiters have to be introduced. Nevertheless, DTMOS transistors have two main drawbacks. Some of them are, a much larger layout area, and a larger gate capacitance [37].

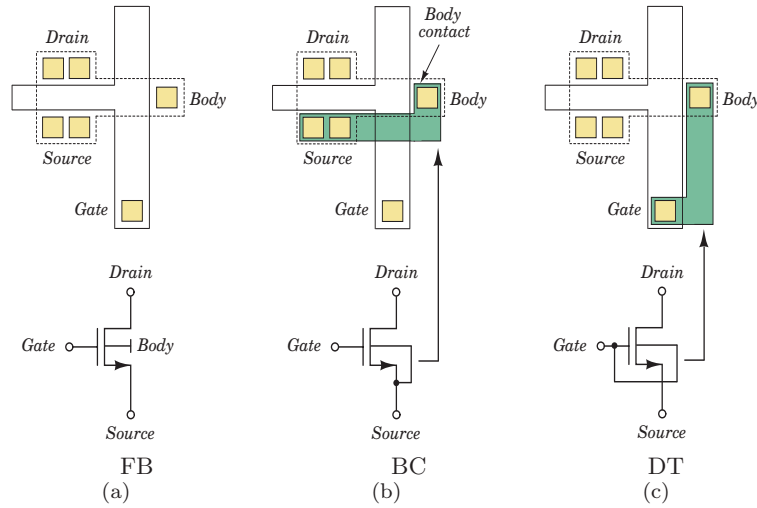


Figure 2.13: Illustration of different connecting body approach in PD SOI MOSFET: (a) Floating Body (FB), (b) Body Contacted (BC) and (c) Dynamic Threshold (DT) MOSFETs.

2.5 Conclusion

In this chapter, we introduced the SOI technologies that have been used in this work. SOI substrates can be fabricated by either oxygen implant/anneal (SIMOX) or bond/etch back (BESOI) techniques. Both methods have gained acceptance in the marketplace. Anticipated wafer volumes are in the range of 500,000 per year ramping to 2 million per year by 2005. This milestone signifies the general acceptance of CMOS SOI as the next generation technology choice because large volume production is the best way to ensure continuous price reduction and quality improvement. Honeywell, IBM, AMD and many other companies are actively working to further develop and implement this technology, thereby giving CMOS SOI a significant advantage over other insulated materials, such as SOS (Silicon-on-Sapphire).

Low power consumption is particularly important in mobile communications due to limited battery life. One approach to meet this challenge is to create a reduced power RF system-on-chip that contains digital, analog and RF portions of the design on the same die. In this context, SOI appears as a technology of choice for mixed signal RF CMOS applications. Due to its lower junction capacitance and reduced leakage current, SOI provides reduced static and dynamic power consumption of the digital logic. In terms of passive device integration the major benefit of SOI is the possibility of using high resistivity (HR) substrates.

Partially Depleted SOI technology present a reduced process complexity compared to Fully Depleted devices when their main drawbacks like the kink effect can be reduced by the possibility of connecting the body (thereby enabling to completely suppress floating body effects under DC conditions). The characteristics of Partially Depleted devices make them very attracting for low-power, high speed, high performance digital applications.

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CHAPTER 3

HT CHARACTERIZATION OF PASSIVE DEVICES

3.1 Introduction

The capability of radiowaves to provide instantaneous distant communications without interconnection wires has been a major factor in the explosive growth of communications during the twentieth century. In addition, the rapid multiplication of standard applications using radiowaves has dramatically increased the demand for universal wireless connectivity. In order for these standards and the companies that support them, to stay competitive, low-cost, small form-factor portable wireless communications devices are critical components.

In microwave monolithic integrated circuits (MMICs), passive elements are widely used. These can be distributed (transmission lines) or lumped (spiral inductors and MIM capacitors). The quality of the passive elements, in particular spiral inductors and transmission lines, in term of losses is predominant [1] [2] [3].

Moreover, more and more applications of radio-frequency (RF) integrated circuits require to operate over a wide temperature range. In the past decades, great efforts have been devoted to the modeling, optimization and design of the spiral inductors on silicon and GaAs substrates [4] [5]. Various approaches, such as using high resistivity substrate, high conductive metal layers and thick dielectric layers, selectively etching off substrates, stacking metal layers [6] [7], and even using differentially driven inductors, have been reported [8] [9]. However, no systematic study of the performance trends of spiral inductors with temperature has been reported in the literature, except in [10].

In this chapter, a brief analysis of the transmission lines is presented. Then, the temperature behavior of spiral inductors implemented on 130 nm SOI technology provided by ST-Microelectronics is analyzed. A physical π -model of spiral inductors on standard and high resistivity silicon substrate will be introduced.

3.2 Multilayer 130 nm CMOS SOI technology

The inductors have been built on a 130 nm SOI CMOS process provided by ST-Microelectronics, which is a single poly CMOS process, using SOI UNIBOND wafers with either a standard resistivity ($\rho_{Si} \approx 8\text{--}22 \text{ } \Omega\cdot\text{cm}$) or high resistivity ($\rho_{Si} > 2 \text{ k}\Omega\cdot\text{cm}$) substrate. This process features lines with six copper metal layers (M1

to M6) and an additional top metal layer (M7) in Aluminum (Alucap). The bottom metal layer M1 is above an oxide dielectric layer STI (Shallow Trench Isolation) and an oxide+nitride dielectric layer PMD (Pre-Metal Dielectric) as shown in Fig. 3.1. The characterized square spiral inductor is achieved by staking the top four metal levels (M4, M5, M6 and M7). The metal layers M2 to M5 have a thickness of 350 nm each, and the metal layers M6 and M7 have a thickness of 900 nm and 880 nm, respectively.

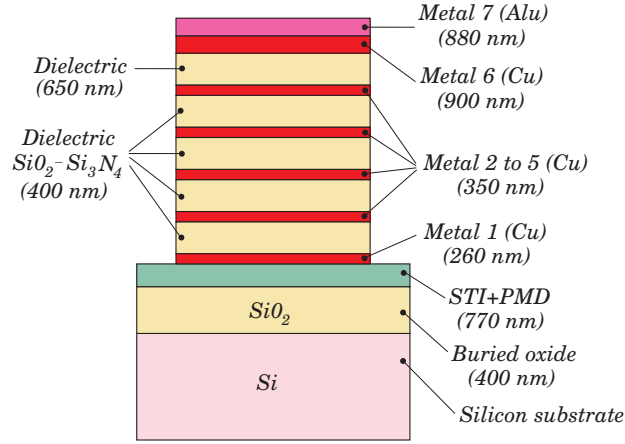


Figure 3.1: Illustration of a cross section in 130 nm ST-M SOI technology.

3.3 Transmission lines

In MMICs, the transmission lines constitute an important component of the circuits, where they are widely used as interconnects and matching networks. Therefore, it is necessary to study the behavior of the transmission line structures over wide frequency range. Moreover, the performance of the transmission lines depends on the temperature variation. It is also reported that at high temperature operation, the performances degradation of the MMICs is mainly due to temperature degradation of the transmission line losses [2] [11].

The behavior of thin film microstrip and coplanar waveguide transmission lines on both standard and high resistivity silicon-on-insulator (SOI) substrates versus high temperature is briefly presented in this section. The various lines types that can be used in MMICs are (Fig. 3.2):

- Microstrip line: the signal is located on the top of the substrate while the ground plane is located at the bottom.

3.3 TRANSMISSION LINES

- Coplanar waveguide line: the signal is located on the central conductor which is surrounded by two ground planes.
- Conductor backed coplanar: the ground plane is present both on the top and at the bottom of the structure.

Among all existing transmission line structures, it appears that microstrip lines and coplanar waveguides are the most attractive for use in MMICs due to the convenient field configuration and superior electrical characteristics of those two line topologies [1] [12]. The transmission lines are characterized by their lineic losses, usually noted α . The lineic losses are of two kinds : conductor losses (α_c), due to the resistivity of the metal conductor and substrate losses (α_{sub}) due to dielectric substrate. The total losses in a transmission line can be expressed by:

$$\alpha = \alpha_c + \alpha_{sub} \quad (3.1)$$

In case of quasi-TEM mode, a transmission line can be represented by a simple distributed RLCG model as shown in Fig. 3.3. In case of transmission lines used on SOI substrate, G_p and C_p are approximatively equivalent to G_{Si} and C_{Si} , respectively, where the G_{Si} and C_{Si} are silicon conductance and parasitic silicon capacitance, respectively. The lineic losses are defined as the real part of the propagation constant γ . In the case of TEM or quasi-TEM modes, the propagation constant can be defined as:

$$\gamma = \alpha + j\beta = \sqrt{(R_s + jL_s\omega)(G_p + jC_p\omega)} \quad (3.2)$$

For the lines with low losses (mandatory for quasi-TEM lines), where $R_s \ll jL_s\omega$ and $G_p \ll jC_p\omega$, the total losses can be expressed as:

$$\alpha \approx \frac{R_s}{2} \sqrt{\frac{C_p}{L_s}} + \frac{G_p}{2} \sqrt{\frac{L_s}{C_p}} \approx \frac{R_s}{2Z_c} + \frac{G_p}{2} Z_c \quad (3.3)$$

where $Z_c \approx \sqrt{L_s/C_p}$ is the line characteristic impedance (at high frequency).

In the following measurements performed on thin film microstrip lines (TFMS) and coplanar waveguides (CPW) are presented. The tested structures have been implemented on the 130 nm SOI process of ST-Microelectronics described in section 3.2. The lines are designed to have a characteristic impedance of 50 Ω , on high resistivity (HR) and standard resistivity (STD) SOI substrate wafers. The performances are presented at room and high temperature. The advantages and drawbacks of both

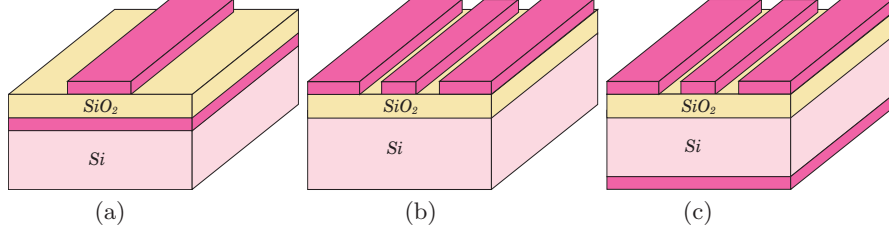


Figure 3.2: Illustration of the most widely used transmission line topologies in CMOS technology: (a) TFMS line, (b) coplanar waveguide and (c) conductor backed CPW.

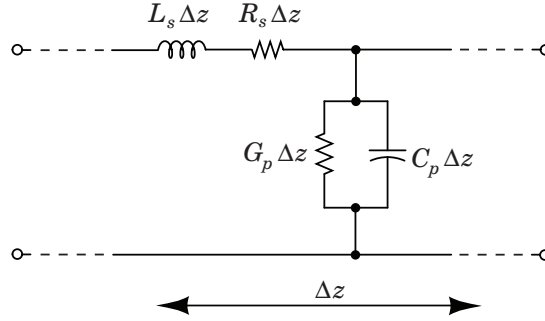


Figure 3.3: Distributed equivalent circuit of an incremental length Δz microstrip line in Quasi-TEM mode.

topologies are given and discussed.

3.3.1 Thin film microstrip lines

3.3.1.1 TFMS on high and standard resistivity substrate

The measured TFMS structures are constituted of a metallic strip on the metal M6 (copper) layer. The ground plane is obtained by stacking the metal M1 and metal M2 together (vias density $\approx 30\%$). The top conductor and the ground plane are separated by a dielectric layer of $2.9 \mu\text{m}$ thick, composed of a multi-layered structure of silicon dioxide and silicon nitride spacers.

The TFMS measurements have been performed on a $2 \mu\text{m}$ strip-width line configuration and for the two available substrate resistivities (STD and HR). The cross section of the TFMS lines implemented on the SOI technology is shown in Fig. 3.4. The lineic losses of the TFMS topology implemented on high and standard resistivity substrates at ambient temperature are plotted in Fig. 3.5. No significant difference is observed between to two structures. This can be explained by the fact that, the ground plane (constituted by the stacked metals M1 and M2 together) shields the

Si-substrate and therefore avoids coupling between the signal and the lossy silicon substrate. Thus the properties of TFMS lines are independent of the substrate type used. In this case, the losses in TFMS lines are mainly due to the conductor losses. In this case, α can be approximated by:

$$\alpha \approx \alpha_c \approx \frac{R_s}{2} \sqrt{\frac{C_p}{L_s}} \quad (3.4)$$

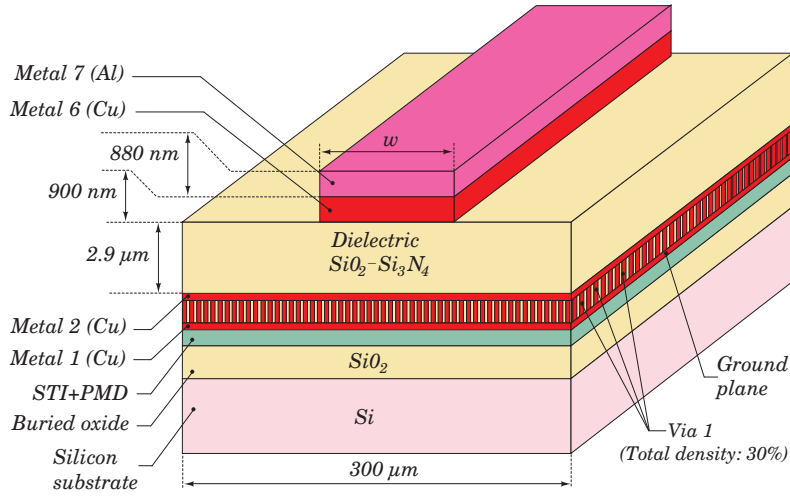


Figure 3.4: Illustration of the cross section of a TFMS line implemented on SOI technology.

3.3.1.2 Geometrical parameters of the TFMS lines

In this part the study of the influence of the geometrical parameters (the width and the thickness) in a TFMS structure, is performed. The TFMS structures are constituted of a metallic strip line designed on metal M6 (copper) layer with or without the stacked metal M7 (Aluminum) layer. The ground plane is obtained by staking the metal M1 and metal M2 together. The TFMS measurements have been performed for two strip-width line configurations ($W=7$ and $9 \mu\text{m}$) on high resistivity substrate. The cross section of the studied TFMS line implemented on SOI technology is shown in Fig. 3.4. As expected the losses in TFMS lines can be reduced by either increasing the strip width (W) or the conductor thickness (by stacking several metal layers together) (Fig. 3.6).

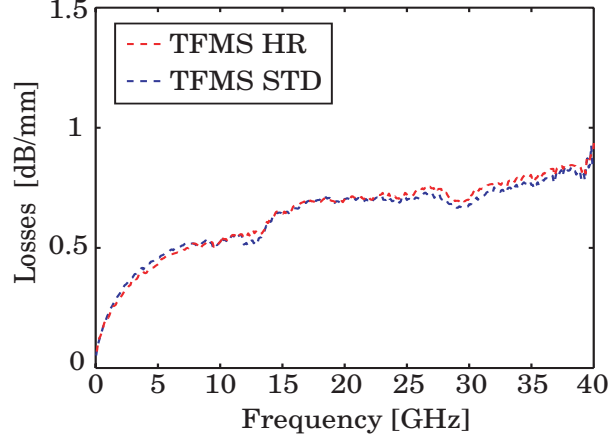


Figure 3.5: Measured lineic losses of TFMS lines having $2\ \mu\text{m}$ strip-width, implemented on standard (STD) and high resistivity (HR) SOI substrates.

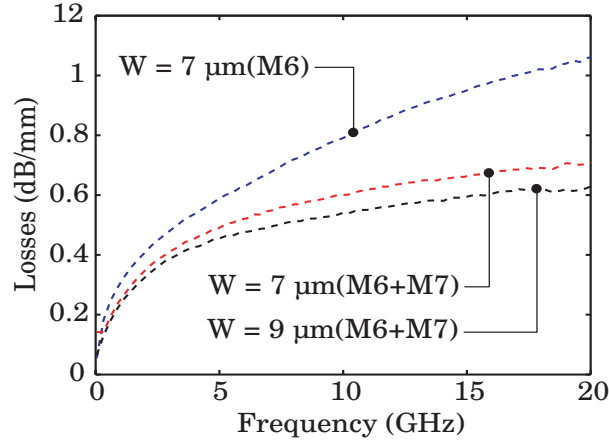


Figure 3.6: Measured lineic losses of TFMS line implemented on high resistivity (HR) SOI substrate for different geometrical parameters.

3.3.2 Coplanar waveguide

3.3.2.1 CPW on high and standard resistivity substrate

The CPW structures are constituted of a central conductor surrounded by two ground planes. The CPW lines have been designed on the 130 nm SOI process. The central conductor as well as the planar grounds were defined in metal 6 (copper). The characteristic impedance of CPW can be selected in a wide range by changing the width of the central conductor (W), and/or the spacing between the central conductor

and the ground planes (S). The width and the spacing of the CPW structures were fixed to $40\text{ }\mu\text{m}$ and $24\text{ }\mu\text{m}$, respectively, for each structure (on HR and STD resistivity substrates). These dimensions allow to obtain a characteristic impedance close to $50\text{ }\Omega$ for a wide frequency range. The CPW measurements have been performed for the two available substrate resistivities (standard and high resistivity substrate). The cross section of the CPW lines implemented on SOI technology is shown in Fig. 3.7. The CPW structures do not have a ground plane allowing to shield the Si-substrate, so the losses in CPWs are of two kinds: conductor losses, due to the resistivity of the metal conductor and substrate losses, due to the extension of the electric field in the oxide and the silicon substrate [1] [8]. The lineic losses of the CPW line implemented on high and standard resistivity substrate at ambient temperature are plotted in Fig. 3.8. We clearly note the advantage of the CPW implemented on HR substrate, compared to the CPW implemented on STD substrate. This is due to the quality of HR substrate, in term of impurities, which contributes to reduce drastically the substrate losses [1]. In the case of CPW implemented on standard resistivity, the substrate losses (α_{sub}) are predominant and for high frequency the total losses can be approximated as $\alpha \approx \alpha_{sub}$.

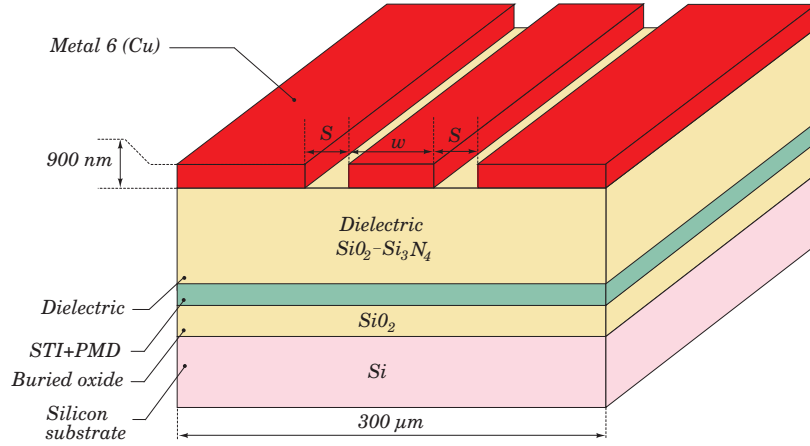


Figure 3.7: CPW cross section implemented on SOI technology.

3.3.2.2 TFMS vs CPW line structures

By comparing the results presented in Fig. 3.6 and 3.8, we note that the CPW lines implemented on HR substrate exhibit less losses than TFMS lines. This is mainly due to the smaller geometry of the TFMS structures in particular the strip line width which cannot be chosen without impact on the characteristic impedance [13] [14]. A

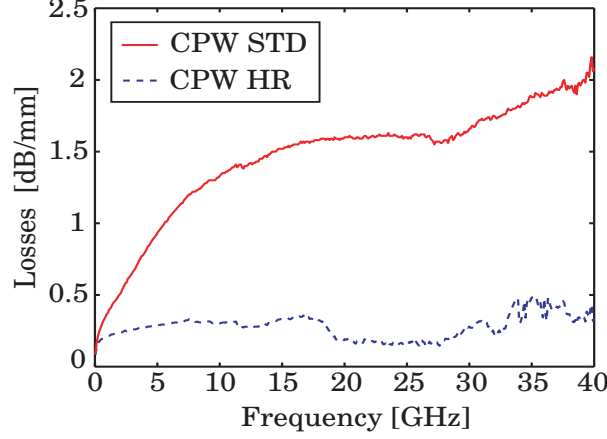


Figure 3.8: Measured lineic losses in case of CPW line implemented on standard (STD) and high resistivity (HR) SOI substrates ($W=40\ \mu\text{m}$ and $S=24\text{-}\mu\text{m}$).

small strip width of the TFMS lines has induced a high line series resistance. However, the measurements indicate that the TFMS lines offer better performance in matter of losses than CPW lines implemented on standard resistivity. Note that for both topologies (CPW HR and TFMS), the dominant component is the conductor losses. The series resistance in a metal conductor line, $R_{s,m}$ at low frequencies, depends on the geometrical parameters from the well known expression:

$$R_{s,m} = \frac{\rho_m \cdot l_m}{w_m \cdot t_m} \quad (3.5)$$

where ρ_m , l_m , w_m and t_m are the resistivity, overall length, the line width and the metal thickness, respectively.

3.3.3 Temperature behavior of TFMS and CPW

In this section, lineic losses are measured versus frequency and for various temperature conditions. The on-wafer measurements were performed with a Anritsu 37369A vector network analyzer. Temperature control is provided by a Temptronics 8-in temperature chuck up to 250°C . $100\ \mu\text{m}$ -pitch ground-signal-ground (GSG) high frequency coplanar $|Z|$ probes from $Süss^{TM}$ have been used for signal measurement (Fig. 3.9). The measurements were done over the temperature range from 25 to 250°C . In order to cancel the effects introduced by the transitions between the tested line structures and the coplanar access, a TRL (Thru-Reflect-Line) calibration was used. Fig. 3.10 shows typical standards necessary for a TRL calibration. The strip

3.3 TRANSMISSION LINES

line is embedded in CPW to Strip line transitions. Their effects are canceled by the TRL calibration.



Figure 3.9: On-wafer probing station.

The measurements were performed for the CPW on HR and STD substrates, and TFMS lines on HR substrate. The measured losses and characteristic impedance of the TFMS line are presented in Fig. 3.11. The measurement shows a minor temperature dependence of characteristic impedance, and a high degradation of the losses due to the increase of temperature (the losses increase by 70% when the temperature varies from 25 to 250°C). Because the losses of TFMS lines are mainly due to the conductor losses, we can confirm that the temperature degradation of the TFMS losses are due to the increase of the metal resistivity with the temperature. It is well known that the resistivity of a metal conductor (ρ_m) varies with temperature according to the empirical equation [15]:

$$\rho_m(T) = \rho_m(T_0) [1 + \lambda_m (T - T_0)] \quad (3.6)$$

where $\rho_m(T_0)$ is the metal resistivity at ambient temperature, the parameter λ_m is the temperature coefficient in $^{\circ}C^{-1}$ and T_0 is the ambient temperature. λ_m is given by:

$$\lambda_m = \frac{1}{\rho_m(T_0)} \cdot \frac{\partial \rho_m(T)}{\partial T} \quad (3.7)$$

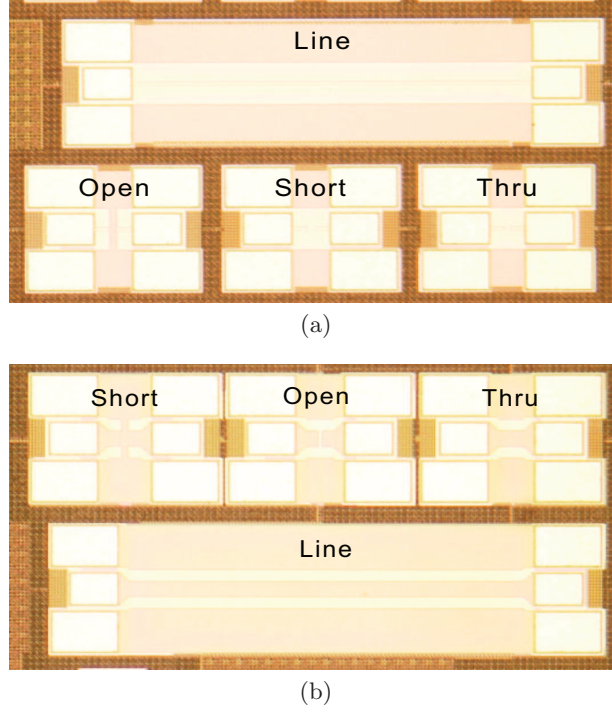


Figure 3.10: Chip microphotograph of the designed calibration kit: (a) TFMS and (b) CPW.

The series resistance in a metal conductor line, $R_{s,m}$ at low frequencies varies with the temperature according to:

$$R_{s,m}(T) = \frac{\rho_m(T) \cdot l_m}{w_m \cdot t_m} = \frac{\rho_m(T_0) \cdot l_m}{w_m \cdot t_m} [1 + \lambda_m (T - T_0)] \quad (3.8)$$

$$= R_{s,m}(T_0) [1 + \lambda_m (T - T_0)] \quad (3.9)$$

where $R_{s,m}$ is series resistance at ambient temperature and defined as:

$$R_{s,m}(T_0) = \frac{\rho_m(T_0) \cdot l_m}{w_m \cdot t_m} \quad (3.10)$$

The extracted losses and characteristic impedance of CPW (HR and STD) versus frequency and for various temperature conditions (from $25^\circ C$ to $250^\circ C$) are plotted in Fig. 3.12. The comparison between lineic losses of CPW (HR and STD) and TFMS (HR), at 10 GHz, versus temperature is represented in Fig. 3.13. The TFMS losses

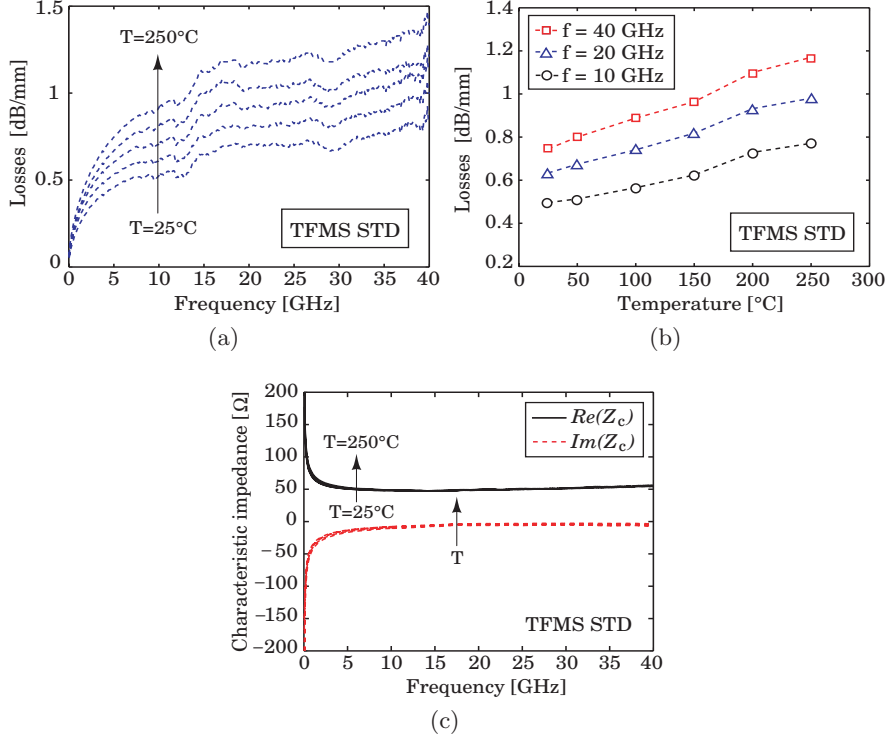


Figure 3.11: Measured lineic losses for a TFMS line implemented on STD SOI substrate: (a) versus frequency and over a temperature range from 25 to 250°C , (b) versus temperature for 10 GHz, 20 GHz and 40 GHz, and (c) the characteristic impedance of the TFMS line.

are dominated by the conductor losses which increase linearly (approximately) with temperature as mentioned in equation (3.9). The same conclusion can be drawn for the CPW line implemented on HR SOI substrate which however, shows less loss compared to TFMS HR line because CPW structures enable the use of wider lines to achieve the same characteristic impedance. This allows reducing the metallic losses as mentioned earlier. As expected, the lineic losses of TFMS and CPW implemented on HR increase with the temperature. An important increase of losses above 200°C in the case of CPW line on HR is observed. This is due to the increase of the substrate losses (the substrate resistivity ρ_{Si} decreases when the temperature increases due to the increasing of Si intrinsic concentration in the substrate at higher temperature [13], see section 3.4.5.2). Note that the characteristic impedances of the CPW lines do not show a significant variation with temperature.

We also note a decrease of the losses in the case of CPW STD up to 200°C ,

due to the decrease of the substrate losses ($\partial\alpha_{sub}/\partial T < 0$, the substrate resistivity increases when the temperature increases due to the mobility reduction of free carriers in the substrate at higher temperature), which is more important than metallic losses increase. Around $200^\circ C$, the total losses of CPW STD are constant. Above $200^\circ C$, due to the increases of the metallic losses which become predominant, the losses start to increase.

The variation of the lineic losses for a temperature variation in the range 25 to $250^\circ C$ is defined as $\epsilon_\alpha = 100 \cdot [\alpha(250^\circ C) - \alpha(25^\circ C)] / \alpha(25^\circ C)$ (in %) and is represented for TFMS and CPW lines versus frequency in Fig. 3.14. The values of ϵ_α , in the frequency range 5 – 40 GHz for all the studied line configurations are summarized in Table 3.1. A temperature degradation of 200% and 70% is noted for the CPW line implemented on HR and for TFMS line in the considered frequency band. However, in the case of CPW line implemented on STD substrate, a 35% improvement of ϵ_α is noted.

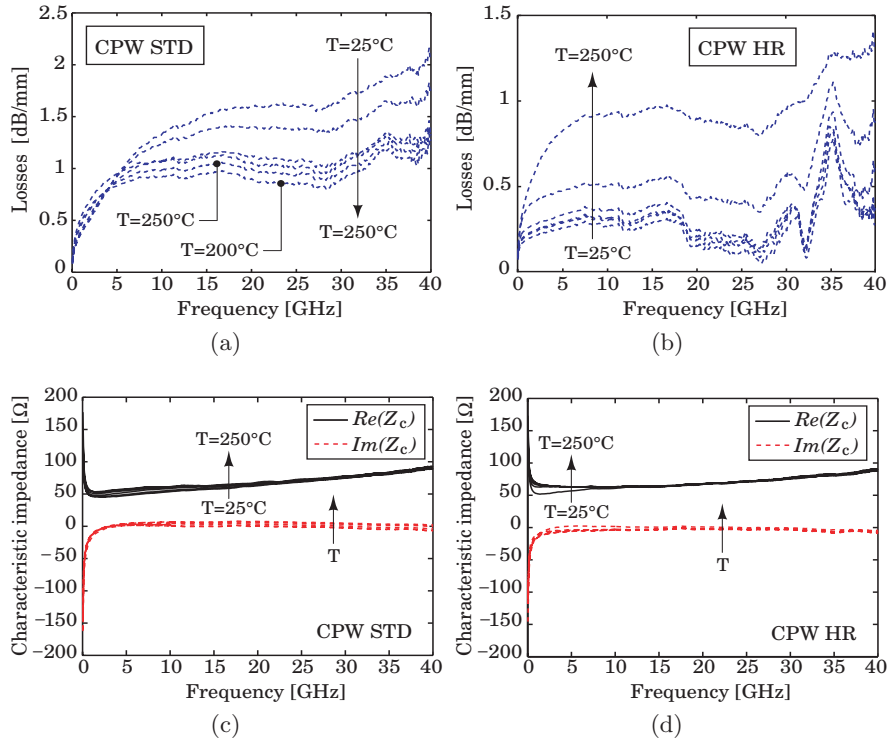


Figure 3.12: Measured lineic losses and characteristic impedance of the CPW lines versus frequency and over the temperature range 25 to $250^\circ C$, implemented on: (a,c) STD and (b,d) HR resistivity SOI substrates.

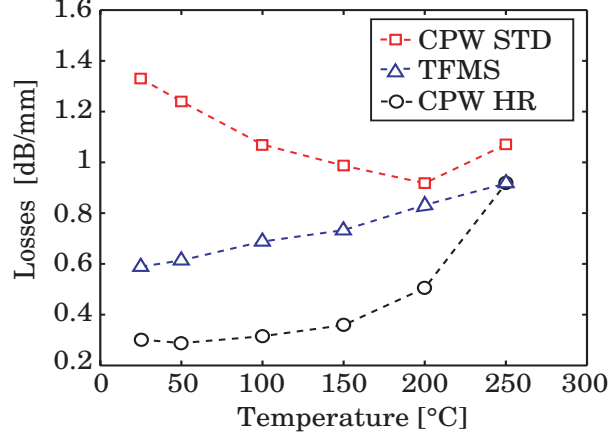


Figure 3.13: The total lineic losses of CPW (HR and STD) and TFMS lines versus temperature at 10 GHz.

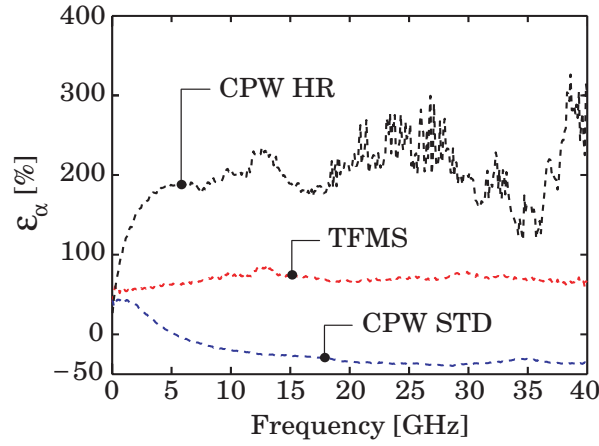


Figure 3.14: The measured variation of lineic losses of CPW (HR and STD) and TFMS lines when the temperature varies from 25 to 250°C.

3.3.4 Discussion

TFMS are independent of the substrate used because the ground plane avoids coupling between the signal and the substrate. This makes possible the use of a standard resistivity SOI substrate which is cheaper than HR.

Thanks to the possibility of using wider signal lines, allowing to reduce the metallic losses, the CPW lines implemented on HR substrate exhibit less losses than TFMS lines. In the case of transmission lines implemented on standard resistivity, TFMS

	<i>TFMS HR</i>	<i>CPW HR</i>	<i>TFMS STD</i>	<i>CPW STD</i>
Losses (T=25°C)	0.6	0.3	0.6	1.7
Losses (T=250°C) [dB/mm]	1.0	0.9	1.0	1.1
Variation, ϵ_α	+67%	+200%	+67%	-35%

Table 3.1: Summary of the measured lineic losses variations (ϵ_α) of CPW and TFMS lines when the temperature varies from 25 to 250°C, in the 5 – 40 GHz frequency band.

lines offer lower losses than CPW lines, due to the presence of the ground plane.

The losses in TFMS lines can be reduced by either increasing the strip width (W) or the conductor thickness (by stacking several metal layers together). But the increase of the strip width has an impact on the capacitance between the conductor and the ground plane, thus an impact on the characteristic impedance Z_c . In this last case, one should recall that for a given dielectric thickness, the strip width of the TFMS line is usually determined by characteristic impedance considerations. Therefore, for a specified Z_c value an increase of the line width can only be achieved along with a corresponding increase of dielectric thickness, and thus, by increasing the number metal levels in the back-end. It therefore appears that the properties of the TFMS lines in multilayer technologies are critically conditioned by the technology in which they are implemented.

However, because both the central conductor width (W) and the spacing between conductors (S) can be independently adjusted to achieve the desired characteristic impedance value, the conductor losses of CPW structures implemented on SOI technology are not so much constrained by technological parameters. This indicates that the CPW lines can be fabricated with much lower series losses than TFMS lines and so conferring a significant advantage of CPW lines over TFMS lines [1] [16].

The losses increase with respect to the temperature except for the STD CPW where the substrate resistivity increases with the increase of the temperature, compensating the increase of the metallic losses and thus making the CPW losses decrease with respect to temperature up to 200°C [17].

3.4 Integrated spiral inductors

3.4.1 Introduction

Monolithic microwave integrated circuits will be used to a large extent in future mass consumer and space applications thanks to the high degree of integration, high performances and small size. Spiral inductors are extensively used in MMIC-design, es-

pecially for matching input and output impedances in Low Noise Amplifier (LNA) or forming the LC tank of Voltage-Controlled-Oscillators (VCO) as they allow to drastically reduce the size of the circuits. The design of integrated inductors with optimum quality factor is important for increasing the RF performances of circuits [18] [19]. The temperature behavior of integrated inductors implemented on SOI technology have not been extensively studied at present. Depending on the required inductance, MMIC inductors can be either realized as a meander lines, or as spiral inductors.

This section presents a wideband and wide temperature range characterization of integrated spiral inductors implemented on silicon SOI substrate. Square and octagonal topologies were studied and characterized over the temperature range 25 – 200°C. Their performances, in term of quality factor, are presented, in both low and high resistivity silicon substrates. A simple π -model is compared with measurements for different topologies.

3.4.2 Physical model of a spiral inductor

In most cases, integrated spiral inductors are used in a frequency range that is far below its first self-resonance frequency (SRF). In this case, integrated spiral inductors on silicon can be accurately characterized by a physical π -model as shown in Fig. 3.15(b) [20] [21] [22].

The inductance and resistance of the spiral and underpass are represented by the series inductance, L_s , and the series resistance, R_s , respectively. The overlap between the spiral and the underpass leads to direct capacitive coupling between the two terminals of the inductor. This feed-through path is modeled by the series capacitance, C_s . The oxide capacitance between the spiral and the silicon substrate is modeled by C_{ox1} and C_{ox2} . The capacitance and resistance of the silicon substrate are modeled by C_{Si1} , C_{Si2} , and R_{Si1} , R_{Si2} , respectively. These values mainly vary with the overall track area for given substrate and inductive structure. The parameters C_{ox1} , C_{ox2} , C_{Si1} , C_{Si2} , R_{Si1} , and R_{Si2} depend on the geometrical and electrical characteristics of silicon substrate.

3.4.2.1 Inductance and parasitic series resistance

L_s and R_s are subject to eddy current effects in the conductor. At high frequencies, the penetration of the magnetic field into the conductor is attenuated, which causes reduction in the magnetic flux internal to the conductor [23]. However, L_s does not decrease significantly with increasing frequency because it is predominantly determined by the magnetic flux external to the conductor. The current density in a wire is uniform at low-frequencies. However, as frequency increases, the current density

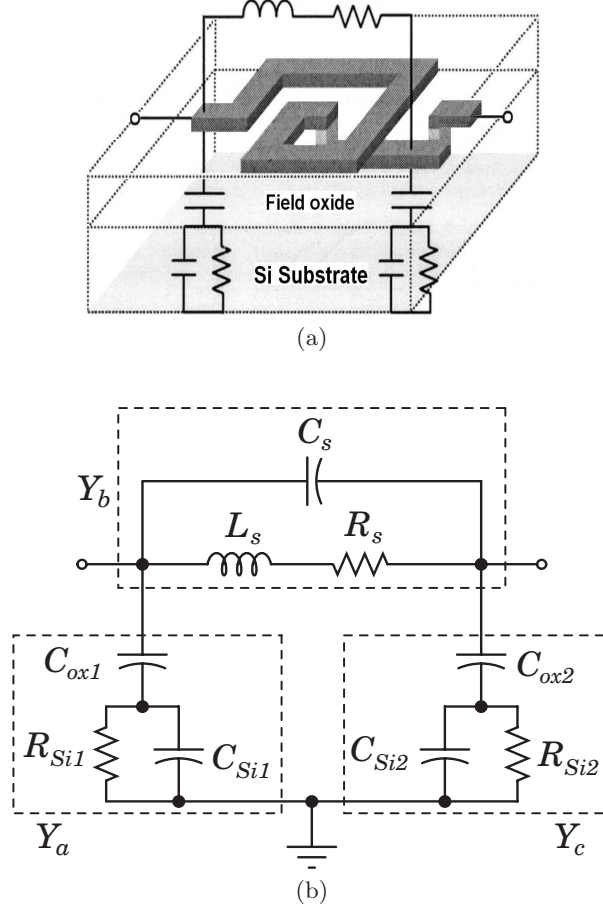


Figure 3.15: (a) 3-D view and (b) lumped physical equivalent model of a spiral inductor on silicon.

becomes nonuniform due to the formation of eddy currents [21] [24]. Eddy currents manifest themselves as skin and proximity effects. In the case of the skin effect, the time-varying magnetic field due to the current flow in a conductor induces eddy currents in the conductor itself. The proximity effect takes place when a conductor is under the influence of a time-varying field produced by a nearby conductor carrying a time-varying current. The dependence of the series resistance R_s with the skin effect is given by

$$R_s = \frac{\rho \cdot l}{w \cdot \delta \cdot (1 - e^{-t/\delta})} \quad (3.11)$$

where the parameter δ is the skin depth. The parameters l , w and t are the length,

the width and the thickness of the microstrip line.

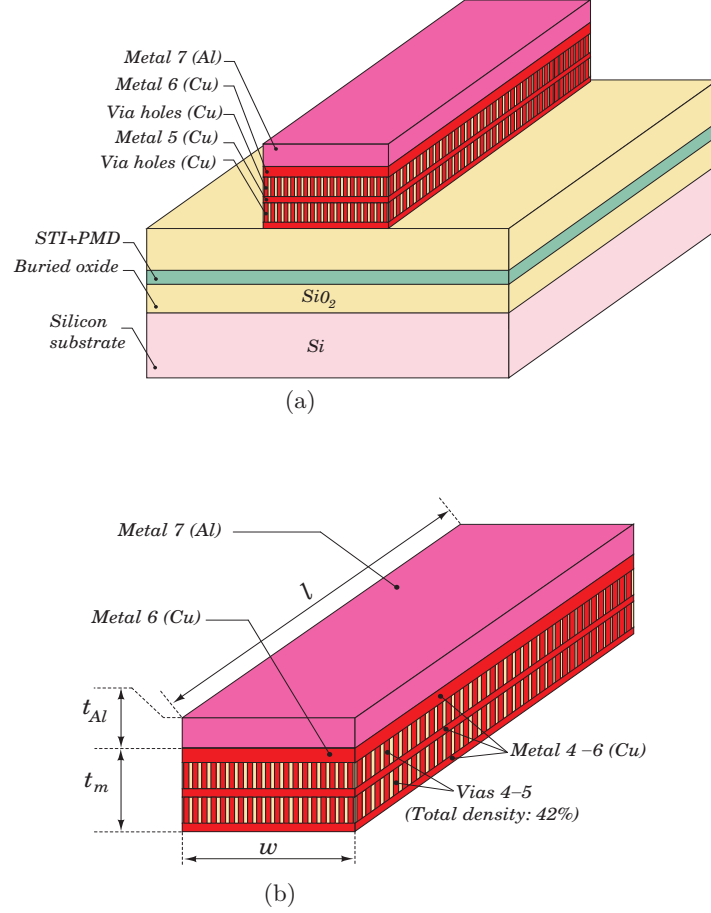


Figure 3.16: Illustration of a microstrip line in SOI technology: (a) elementary microstrip line of the on-chip square spiral inductor, (b) stack of the metal conductors.

3.4.2.2 Parasitic series capacitance

The series capacitance C_s is due to the parasitic coupling between input and output ports of the inductor, it takes account both the crosstalk between adjacent turns and the overlap between the spiral and the underpass. However, the effect of the crosstalk capacitance is usually negligible compared to the underpass capacitance. The spacing between each turn being constant, it is sufficient to model C_s as the sum of all overlap capacitances, which is equal to

$$C_s = n \cdot w^2 \frac{\epsilon_0 \cdot \epsilon_{ox}}{d_{ox, M4-M6}} \quad (3.12)$$

where n is the number of overlap, w is the spiral line width, and $d_{ox, M4-M6}$ is the oxide thickness between the spiral and the underpass.

3.4.2.3 Substrate parasitics

Integrated spiral inductors can be considered as simple microstrip structures (Fig. 3.16). It is shown that, usually, a MOS microstrip structure can be modeled by a three-element network (C_{ox} , C_{Si} and R_{Si}) as seen in Fig. 3.15. C_{ox} , represents the oxide capacitance, C_{Si} and R_{Si} model the resistance and capacitance of the silicon substrate, respectively. The physical origin of R_{Si} is the silicon conductivity which is predominately determined by the majority carrier concentration. C_{Si} models the capacitance effects occurring in the semiconductor at high frequencies. C_{ox} , C_{Si} and R_{Si} can be considered as proportional to the area occupied by the inductor and can be expressed as:

$$C_{ox} = \frac{1}{2} \cdot w \cdot l \cdot \frac{\epsilon_0 \cdot \epsilon_{ox}}{d_{ox}} \quad (3.13)$$

$$C_{Si} = \frac{1}{2} \cdot \kappa \cdot w \cdot l \cdot \frac{\epsilon_0 \cdot \epsilon_{Si}}{d_{Si}} \quad (3.14)$$

$$R_{Si} = 2 \cdot \kappa \cdot \frac{\rho_{Si} \cdot d_{Si}}{w \cdot l} \quad (3.15)$$

where l is overall length of spiral, w is the line width, d_{ox} is the oxide thickness between spiral and silicon substrate, ρ_{Si} is the silicon substrate resistivity and κ is the fringing effect coefficient. The factors of 1/2 in equations (3.13), (3.14) and 2 in (3.15) take account for the fact that the substrate parasitics are assumed to be distributed at the two terminals of the inductor.

3.4.3 Extraction methodology

From the π -model shown in Fig. 3.15(c), the admittance of a two port system can be expressed as:

$$[Y] = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} = \begin{bmatrix} 1/Z_a + Y_b & -Y_b \\ -Y_b & 1/Z_c + Y_b \end{bmatrix} \quad (3.16)$$

where Z_a , Y_a and Z_c can be expressed from the equivalent π -model as:

$$Z_a = \frac{1}{Y_a} = \frac{1}{Y_{11} + Y_{12}} \quad (3.17)$$

$$= \frac{1}{jC_{ox1}\omega} + \frac{R_{Si1}}{1 + jR_{Si1}C_{Si1}\omega} \quad (3.18)$$

$$Y_b = -Y_{21} = jC_s\omega + \frac{1}{jL_s\omega + R_s} \quad (3.19)$$

$$Z_c = \frac{1}{Y_c} = \frac{1}{Y_{22} + Y_{21}} \quad (3.20)$$

$$= \frac{1}{jC_{ox2}\omega} + \frac{R_{Si2}}{1 + jR_{Si2}C_{Si2}\omega} \quad (3.21)$$

The parameters L_s , R_s , C_{ox} are extracted at low frequency, and then C_{Si1} , C_{Si2} and R_{Si} are extracted at high frequency. The parameter C_s is extracted at self-resonance frequency of the inductor [20]. This corresponds to the frequency for which $\Im m(Y_{21}) = 0$. The extraction procedure of the π -model parameters is summarized in Fig. 3.17.

3.4.4 Analysis of the temperature behavior of a square spiral inductor

In this section, a temperature characterization of a square spiral inductor is presented. The inductor has been characterized over a temperature range from 25 to 200°C and a frequency band up to 20 GHz. The tested inductor has a conductor width W of 12 μm , conductor spacing S of 3 μm , inner diameter D_i of 100 μm and number of turns N_T of 4.5. The square spiral inductor are fabricated on a 130 nm SOI CMOS technology using a high resistivity substrate ($\rho > 2$ k Ω .cm). The cross section view and chip microphotograph of the studied four metal interconnect layers spiral inductor are represented in Fig. 3.18.

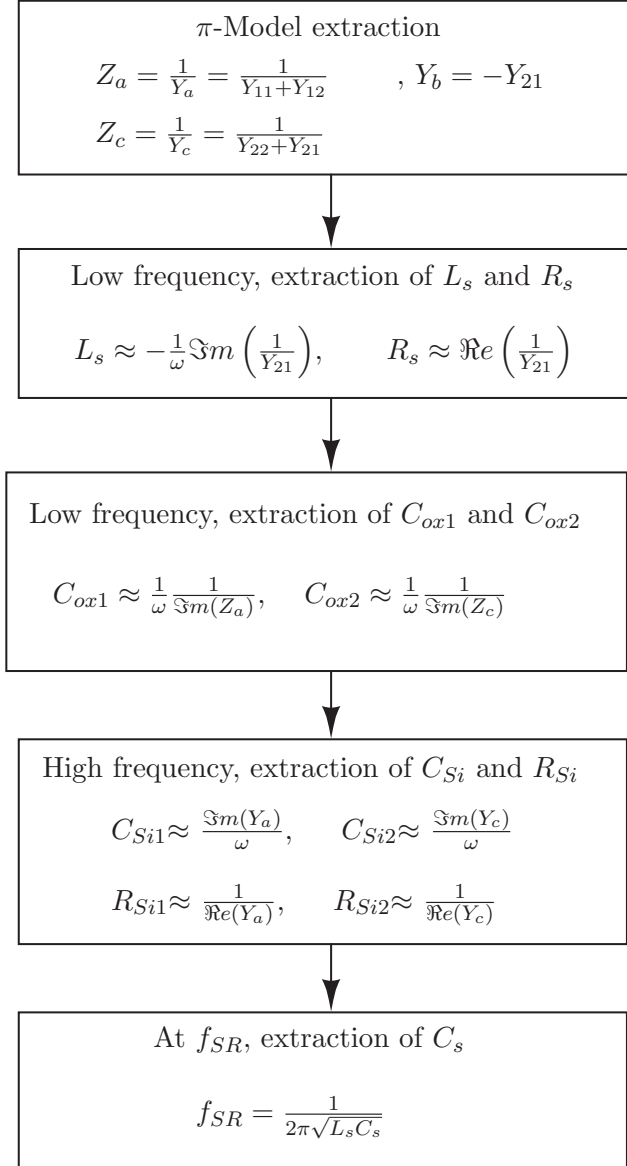


Figure 3.17: π -model parameter formulas and extraction flow chart.

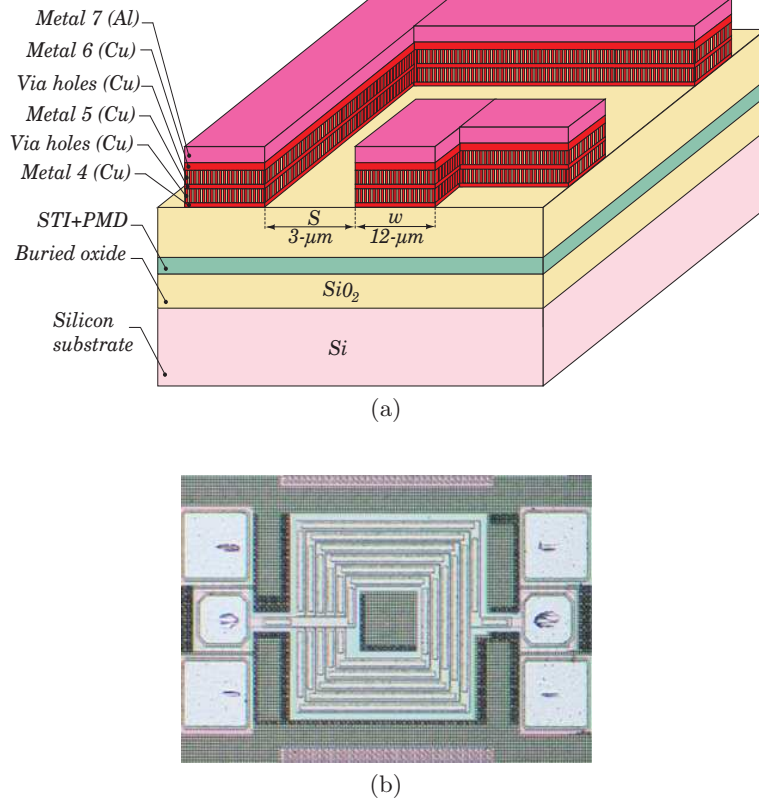


Figure 3.18: (a) 3-D view, and (b) Chip microphotographs of the square spiral inductor on silicon.

After the VNA calibration and the appropriate de-embedding, we extract first the parameters L_s , R_s , C_{ox} and R_{Si} at low frequency, and then C_{Si1} and C_{Si2} at high frequency. The parameter C_s is extracted at the self-resonance frequency of the inductor (frequency for which $\Im m(Y_{21}) = 0$) [20]. The measured results include the contact resistance of the probe. However, as it can be seen in Fig. 3.19, the used probe (infinity probe) provide a very low DC resistance contact and can be neglected ($< 0.05 \Omega$ on Al).

The parameters of π -model extracted from the measurements for various temperature conditions are plotted in Fig. 3.20. The measurements show a large impact of temperature on the parasitic series resistance R_s (degradation of 52% is noted when temperature varies from 25 to 200°C). The extracted quality factor Q , defined by $Q = -\text{imag}(Y_{11})/\text{real}(Y_{11})$, for various temperatures is presented in Fig. 3.21. The measurements show a degradation of 32% of the maximum quality factor when tem-

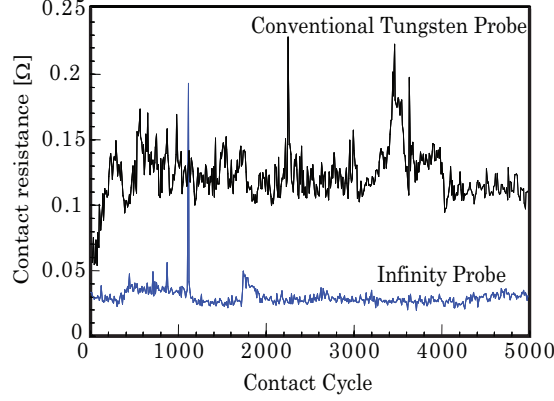


Figure 3.19: Measured contact resistance of the infinity and the conventional tungsten probes.

perature varies from 25 to 200°C. The temperature degradation of Q is mainly due to the increases of parasitic series resistance R_s with the rise of the temperature. The R_s , Q and L_s characteristics versus temperature are plotted in Fig. 3.22. As expected, R_s increases linearly with temperature according the empirical law:

$$R_s(T) \approx R_s(T_0) [1 + \lambda(T - T_0)] \quad (3.22)$$

where $R_s(T_0)$ is the series parasitic resistance at ambient temperature and the parameter $\lambda = (1/R_s(T_0)) \cdot \partial R_s(T) / \partial T \approx 3.6 \cdot 10^{-3} \cdot ^\circ C^{-1}$.

The different parasitic capacitances show a negligible temperature dependence (7% for the considered temperature range). The temperature variation does not impact the substrate and oxide dielectrics (ϵ_{Si} and ϵ_{ox}). So the temperature dependence of C_{ox} and C_{Si} is mainly due to the geometrical variation of the DUT with temperature (expansion of the tested die with temperature).

The extracted π -model parameters (from the measurement) at $T=25^\circ C$ and at $200^\circ C$ are summarized in Table 3.2. The experimental and simulation results show the validity of the proposed model for a wide temperature range considering only the temperature variation of the parameter $R_s(T)$ as presented in Fig. 3.23. The simulations are performed using the π -model (Fig. 3.15(b)) which takes into account the temperature variation of $R_s(T)$ according to the empirical law described in (4.22) (all other parameters of model are independent with temperature and are extracted at ambient temperature). The results show a good agreement over the whole frequency band between simulation and measurement results. Note that the variation of the

3.4 INTEGRATED SPIRAL INDUCTORS

substrate resistivity with respect to temperature does not impact the behavior of the spiral inductor. In fact, the substrate resistivity decreases with respect to the temperature in the case of HR substrate, but the value of R_{Si} at $200^{\circ}C$ is still quite high and does not substantially effect the temperature behavior of the spiral inductor. However, it is expected that temperature effect on the substrate resistivity could not be neglected at higher temperatures ($300^{\circ}C$) where the value of R_{Si} becomes very weak when compared to its value at ambient temperature.

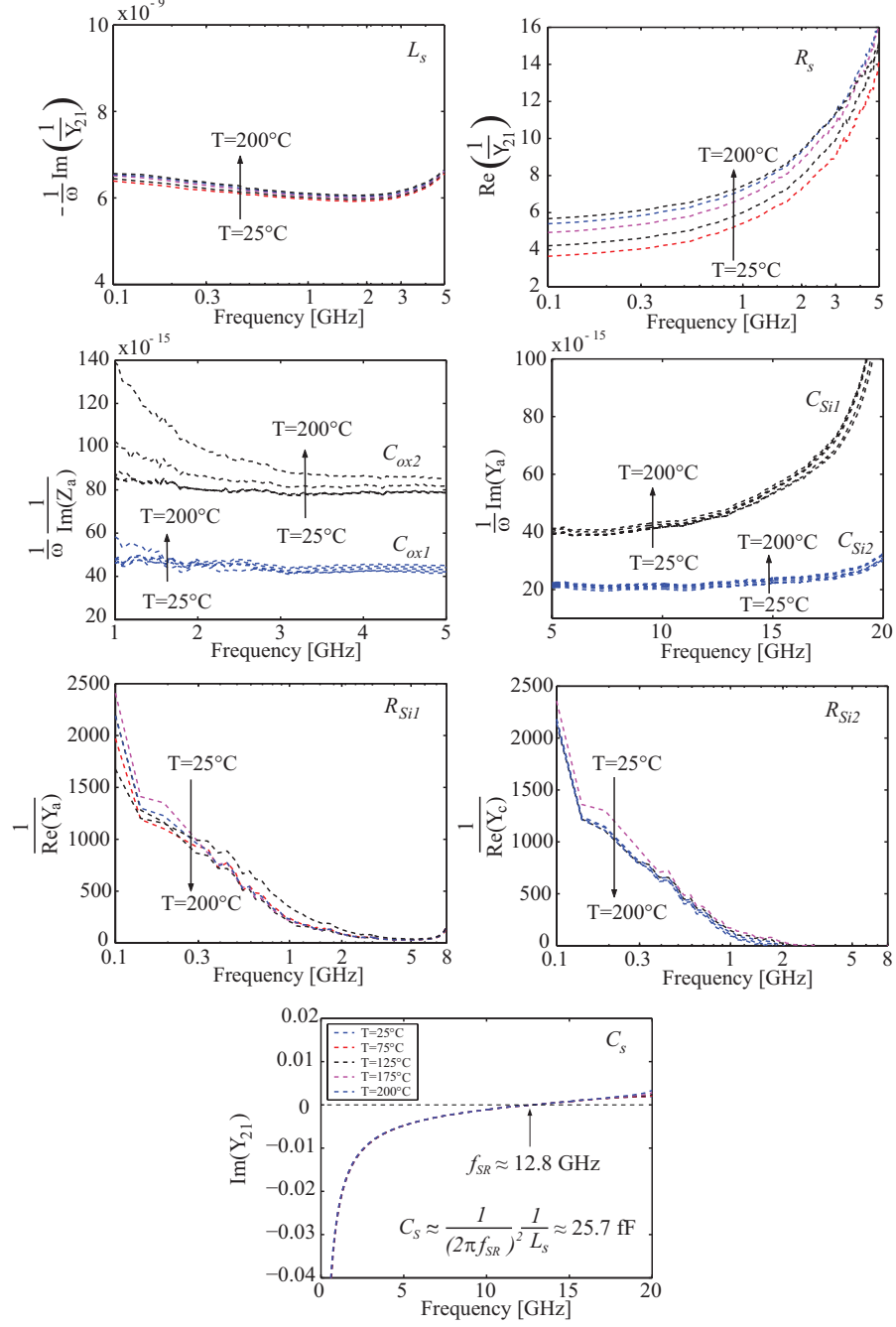


Figure 3.20: Measured π -model parameters of a 4.5-turn inductor for various temperatures.

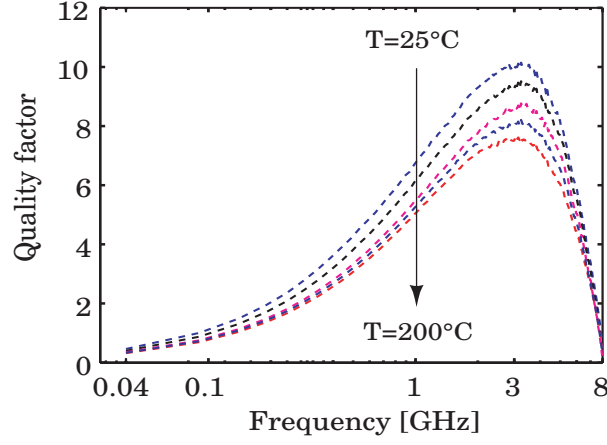


Figure 3.21: Measured quality factor of spiral inductor for various temperatures.

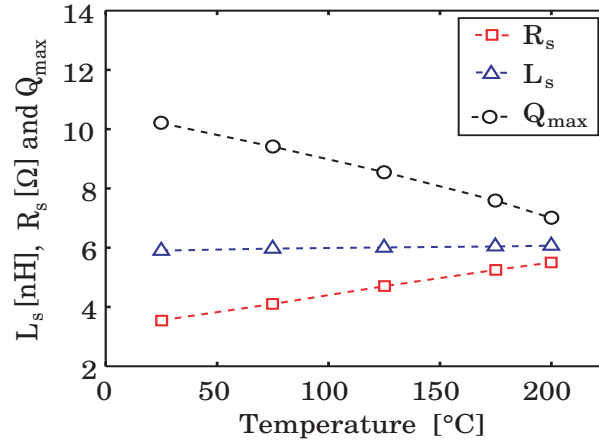


Figure 3.22: Measured quality factor, inductance and parasitic series resistance of spiral inductor for various temperatures.

	L_s [nH]	R_s [Ω]	C_{ox1} [fF]	C_{ox2} [fF]	C_{Si1} [fF]	C_{Si2} [fF]	Q_{max}
T=25°C	5.9	3.5	41	79	20.5	39	10.2
T=200°C	6.07	5.7	43	83	22	41	7
ϵ [%]	2.9%	52%	4.9%	5.1%	7.3%	5.1%	32%

Table 3.2: Summary of the π -model extracted parameters of the spiral inductor at room temperature and 200°C. ϵ is the calculated degradation in (%) of the π -model parameters when the temperature varies from 25 to 200°C.

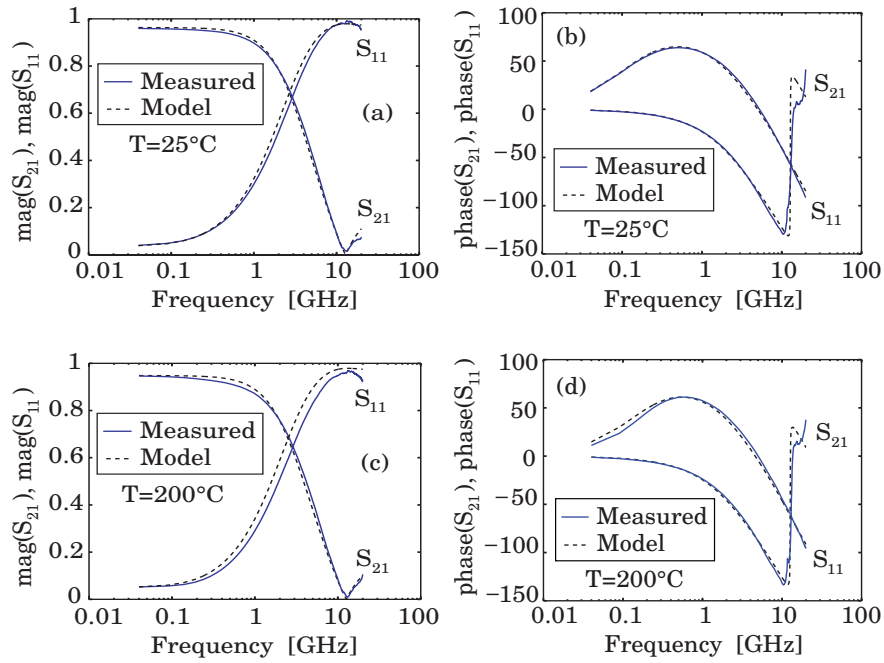


Figure 3.23: Comparison of S -parameters (magnitude and phase) between π -model simulation and measurements, (a) and (b) for T=25°C, (c) and (d) for T=200°C for 4.5-turn spiral inductor.

3.4.5 Spiral inductors on HR and STD SOI substrates

There are two kinds of losses in integrated spiral inductors: conductor losses due to the resistivity of the metal, and substrate losses due to the coupling between the central conductor and the silicon substrate [25] [26] [27]. As mentioned earlier, one of the important advantage of the SOI with respect to the conventional bulk technology is the possibility to have a very high resistivity substrate, characterized by a very low doping and a very low density of free carriers [1] [28]. In order to estimate the substantial loss reduction obtained with the high resistivity substrate, a 2-turns octagonal spiral inductor has been designed and measured on both substrate types (HR and standard resistivity substrates) with and without patterned ground shield (PGS). In the case of high resistivity substrate, the nominal value of silicon substrate resistivity (ρ_{Si}) is typically higher than $2\text{ k}\Omega\cdot\text{cm}$ when the standard silicon substrate exhibits a typical resistivity of $20\text{ }\Omega\cdot\text{cm}$.

The tested inductors have one port connection (the second port is connected to the ground). The equivalent model and the layout of the studied inductors are shown in Fig. 3.24 and 3.25, respectively. The four octagonal spiral inductor have been fabricated on 130 nm SOI CMOS technology. The inductors have been characterized over the temperature range $25 - 200^\circ\text{C}$.

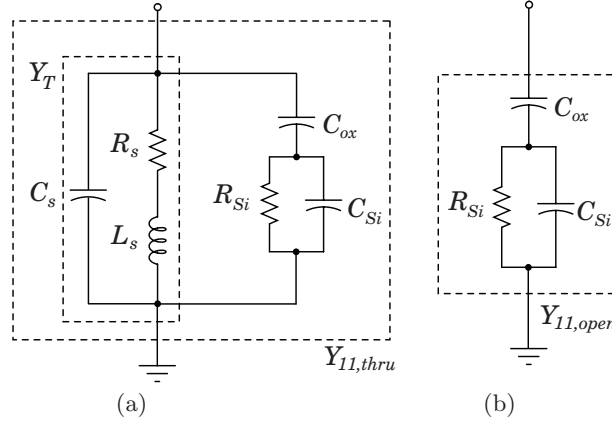


Figure 3.24: The lumped physical equivalent model of the octagonal spiral inductor when (a) the second port connected to the ground and its equivalent model when (b) the second port is floating.

3.4.5.1 Extraction methodology

From the model shown in Fig. 3.24, the admittance of the one port system can be expressed as:

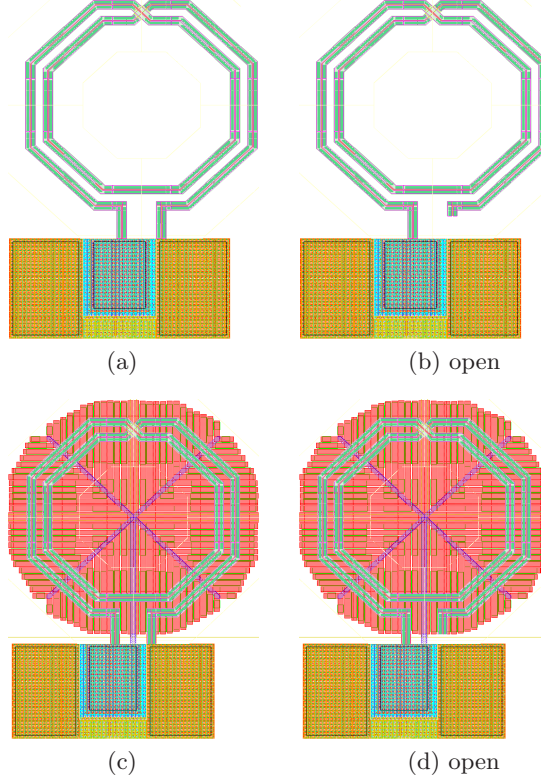


Figure 3.25: Layout of the designed inductors, (a) and (b) without patterned ground shield ((a): the second port is connected to the ground and (b): when the second port is floating), (c) and (d) configuration with patterned ground shield ((c): the second port is connected to the ground and (d): when the second port is floating).

$$Y_{11,thru} = Y_{11,open} + Y_T \quad (3.23)$$

where $Y_{11,open}$ and Y_T can be expressed from the equivalent model as:

$$Y_T = Y_{11,thru} - Y_{11,open} \quad (3.24)$$

$$= jC_s\omega + \frac{1}{jL_s\omega + R_s} \quad (3.25)$$

$$Y_{11,open} = \frac{1}{\frac{1}{jC_{ox}\omega} + \frac{R_{Si}}{1+jR_{Si}C_{Si}\omega}} \quad (3.26)$$

3.4 INTEGRATED SPIRAL INDUCTORS

As in the case of the square spiral inductor, the parameters L_s , R_s , C_{ox} of the octagonal inductor are extracted at low frequency (from Y_T and $Y_{11,open}$), and then C_{Si} and R_{Si} at high frequency (from $Y_{11,open}$). The parameter C_s is extracted at self-resonance frequency of the inductor (frequency for which $\Im m(Y_{21}) = 0$). The extraction procedure of the model parameters of the octagonal inductor is summarized in Fig. 3.26.

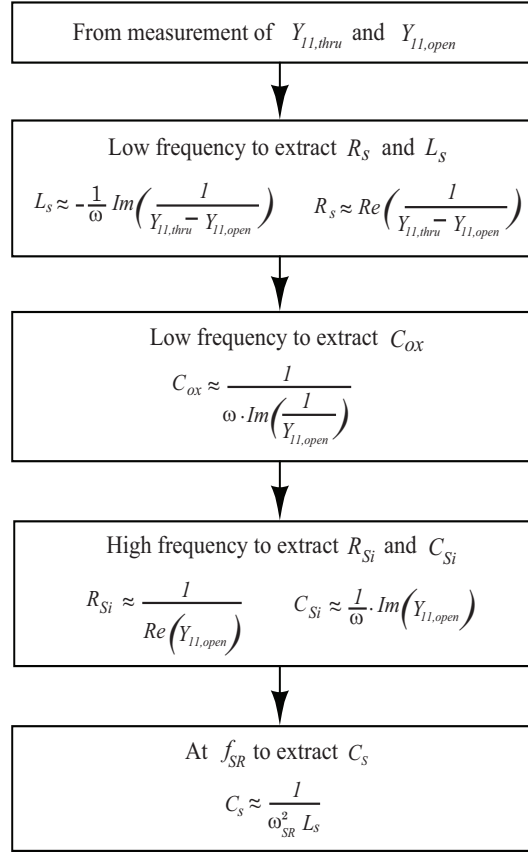


Figure 3.26: Model parameter formulas and extraction flow chart of the one port octagonal inductor.

3.4.5.2 Measurement results

The measured quality factor of the 2–turns octagonal spiral inductors designed on standard resistivity (STD), high resistivity (HR), standard resistivity with patterned ground shield (STD-PGS) and high resistivity with patterned ground shield (HR-PGS) at ambient temperature are plotted in Fig. 3.27.

As expected, we note the clear advantage of the HR substrate compared to the STD substrate in term of quality factor. A 80% increase of the maximum quality factor Q_{max} at ambient temperature is observed when high resistivity substrate (HR) is used instead of STD, as already mentionned in several works [29] [1]. This is due to the quality of HR substrate, in term of impurities, which contributes to drastically reduce the substrate losses. The patterned ground shield is widely used in the case of STD substrate to improve the quality factor of passive devices. We can observe an improvement of Q_{max} by 34% at ambient temperature in the case of STD with PGS structure. For inductors with PGS structure, the signal conductor is shielded from the substrate, avoiding coupling effects and thus the inductors electrical characteristics are not related to the substrate resistivity. However, the inductor implemented on HR-PGS shows a higher value of Q_{max} when compared to the inductor implemented on STD-PGS. This could be related to the fact that the patterned ground shield does not provide a total isolation from the silicon substrate.

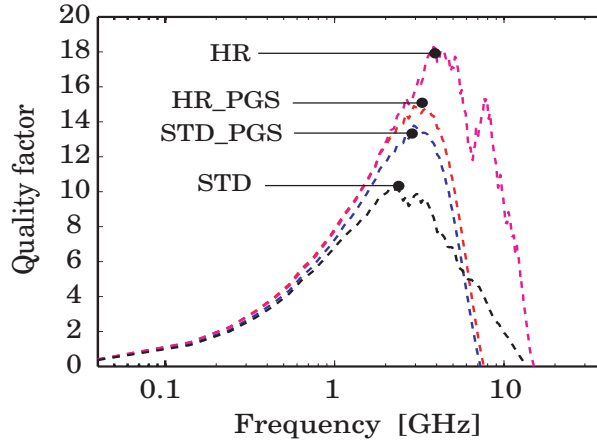


Figure 3.27: Measured quality factor for 2–turns octagonal spiral inductor on high resistivity substrate with and without patterned ground shield (HR-PGS and HR), standard resistivity with and without patterned ground shield (STD-PGS and STD) at ambient temperature.

The measured quality factor for a 2–turns octagonal spiral inductor on HR sub-

strate with and without patterned ground shield (HR-PGS and HR), standard resistivity with and without patterned ground shield (STD-PGS and STD), are plotted in Fig. 3.28 for various temperature conditions. The temperature behavior of the maximum quality factors for the different inductor configurations is summarized in Fig. 3.29. As expected, we note a decrease of the quality factor for the four inductors with temperature. In the case of HR, HR-PGS and STD-PGS, the temperature degradation of the quality factor is mainly related to the increase of the metallic losses (series parasitic resistance, R_s). In the case of the inductor configurations with PGS, there are no substrate losses because the signal conductor is shielded from the substrate. However, for the configurations without PGS, we note a temperature dependence of the substrate resistance R_{Si} as shown in Fig. 3.30.

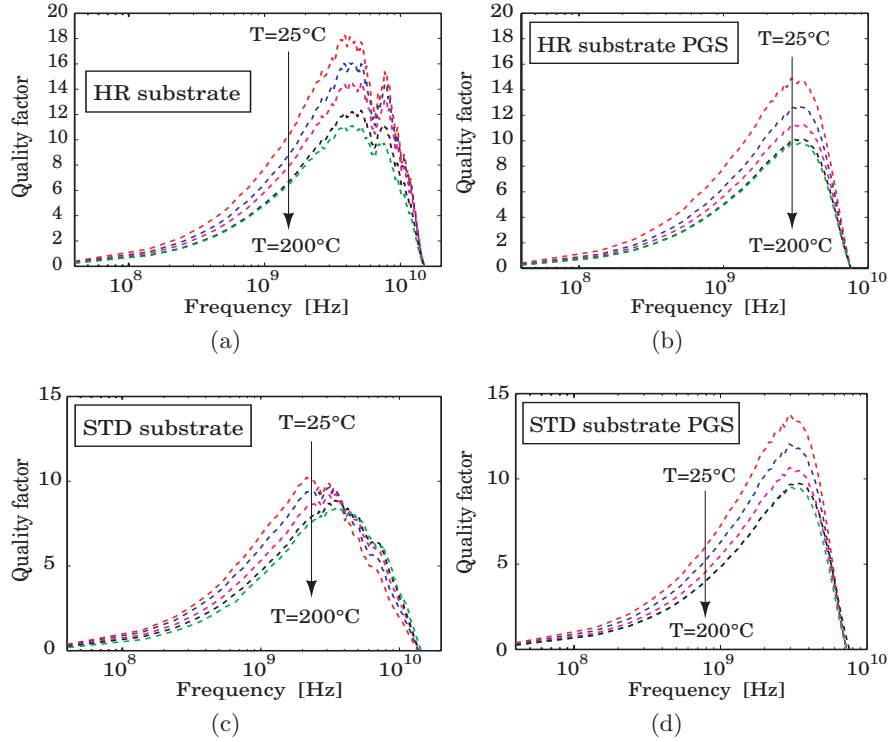


Figure 3.28: Measured quality factor for 2–turns octagonal spiral inductor on high resistivity substrate without and with patterned ground shield (a and b) and standard resistivity substrate without and with patterned ground shield (c and d) for various temperature.

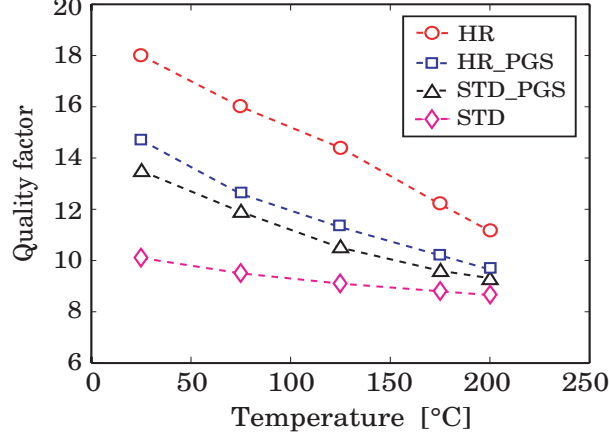


Figure 3.29: Measured maximum quality factor for 2–turns octagonal spiral inductor on high resistivity substrate with and without patterned ground shield (HR-PGS and HR), standard resistivity substrate with and without patterned ground shield (STD-PGS and STD) over the temperature range 25 – 200°C.

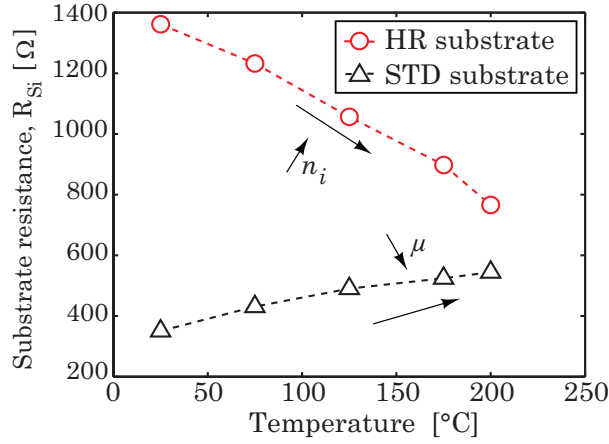


Figure 3.30: Extracted substrate resistance for 2–turns octagonal spiral inductor on high and standard resistivity substrates versus temperature, from 25 to 200°C.

The measured quality factor for a 2–turns octagonal spiral inductor on HR substrate without patterned ground shield when temperature increases from 25 to 200°C, then decreases from 25 to 200°C is plotted in Fig. 3.31. As it can be seen, the substrate resistivity is not affected by a thermal cycle and the high resistivity substrate keep its electrical properties.

The measurement of the quality factor at ambient temperature and at 200°C, for

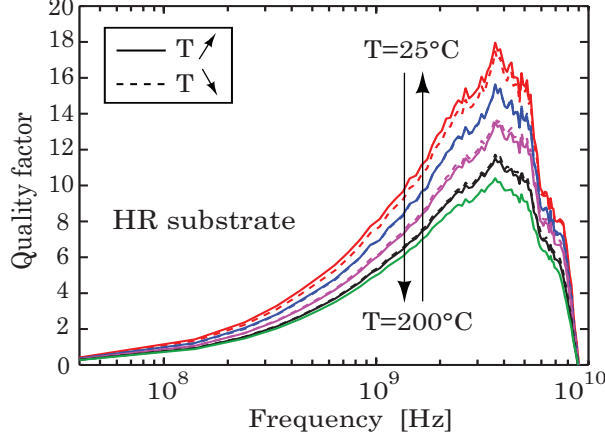


Figure 3.31: Measured quality factor for 2-turns octagonal spiral inductor on high resistivity substrate without patterned ground shield when temperature increases from 25 to 200°C, then decreases from 25 to 200°C.

all the inductor configurations, are summarized in Table 3.3. We note a degradation of Q (ϵ) higher than 30% for all the inductors, except in the case of the inductor implemented on STD resistive substrate. In the case of the inductor implemented on STD, the substrate resistivity increases when temperature rises thanks to the mobility degradation of free carries inside the Si-substrate [17] which compensates the metallic losses and thus minimizes the degradation of STD quality factor with respect to temperature. The inductors implemented on STD with PGS structures (STD-PGS) do not take benefit from the substrate resistivity increase when temperature raises because this inductor is isolated from the silicon substrate and is thus not affected by the substrate effects.

	<i>HRS</i>	<i>HRS PGS</i>	<i>STD</i>	<i>STD PGS</i>
$Q(T=25^{\circ}C)$	18	14.8	10.1	13.5
$Q(T=200^{\circ}C)$	11	9.8	8.6	9.4
Variation, ϵ	-39.0%	-34.0%	-14.3%	-30.3%

Table 3.3: Summary of the quality factors at ambient temperature and at 200°C for the different inductors.

The comparison between model and measurement versus frequency at 200°C for the HR and STD spiral inductors is plotted in Fig. 3.32. We note that for HR substrate, a temperature model including only the variation of the parameter $R_s(T)$ with temperature according to (3.22) (all other parameters of model being independent of

the temperature and extracted at ambient temperature) gives values in good agreement with the measurements. The estimated model error, E_{rr} extracted from Q and defined as $Err = \left| \frac{Q_{meas} - Q_{model}}{Q_{meas}} \right|$ (in %), is plotted in Fig. 3.33, 3.34 and 3.35. Fig. 3.33 shows a maximum error of 30% in the case of the inductor implemented on HR substrate at $200^\circ C$. However, in the case of the STD substrate and in order to minimize E_{rr} , the temperature model must take into account the temperature variation of the substrate resistance $R_{Si}(T)$ in addition to $R_s(T)$, in this case a maximum error of 16% is noted in Fig. 3.35 where two models are presented: the first one taking into account the variation of R_s only (model $R_s(200^\circ C)$) and the second one taking into account the temperature variation of R_{Si} and R_s as well (model R_s, R_{Si}). The physical parameters which depend with the temperature are summarized in Table 3.4 and in Fig. 3.36.

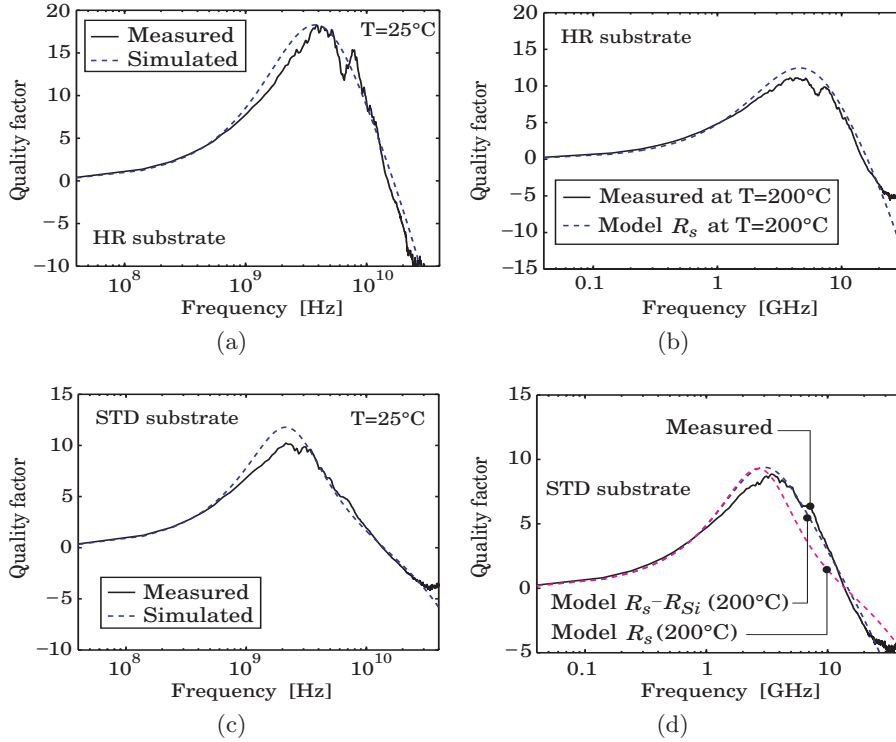


Figure 3.32: Comparison between measurement and model of the quality factor for 2-turns octagonal spiral inductor, (a) on HR substrate at $T = 25^\circ C$, (b) on HR substrate at $T = 200^\circ C$, (c) on STD substrate at $T = 25^\circ C$, and (d) on STD substrate at $T = 200^\circ C$.

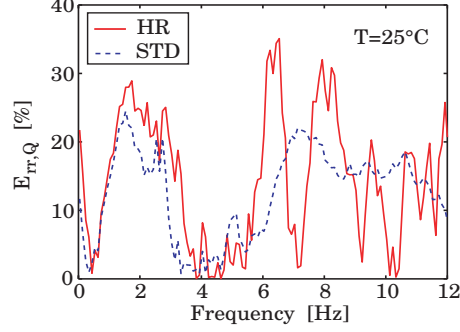


Figure 3.33: Estimated model error of the quality factor at 25°C for the 2–turns octagonal spiral inductor implemented on HR and STD substrates.

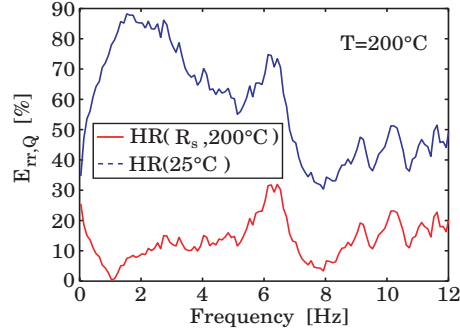


Figure 3.34: Estimated model error of the quality factor at 200°C for the 2–turns octagonal spiral inductor implemented on HR and STD substrates.

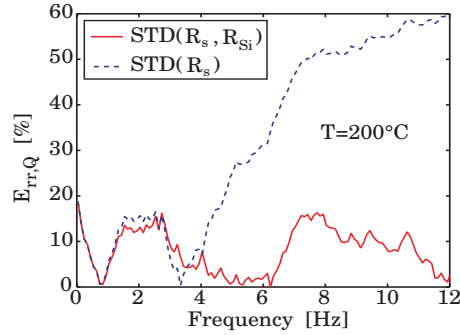


Figure 3.35: Estimated model error of the quality factor at 200°C for the 2–turns octagonal spiral inductor implemented on STD substrate.

	L_s	R_s	C_{ox}	C_{Si}	R_{Si}	C_s
HR	—	X	—	—	—	—
HR-PGS	—	X	—	—	—	—
STD	—	X	—	—	X	—
STD-PGS	—	X	—	—	—	—

Table 3.4: Temperature dependence of the model parameters of the integrated spiral inductor on silicon substrate. The parameters presenting a temperature dependence are noted by a cross “X”.

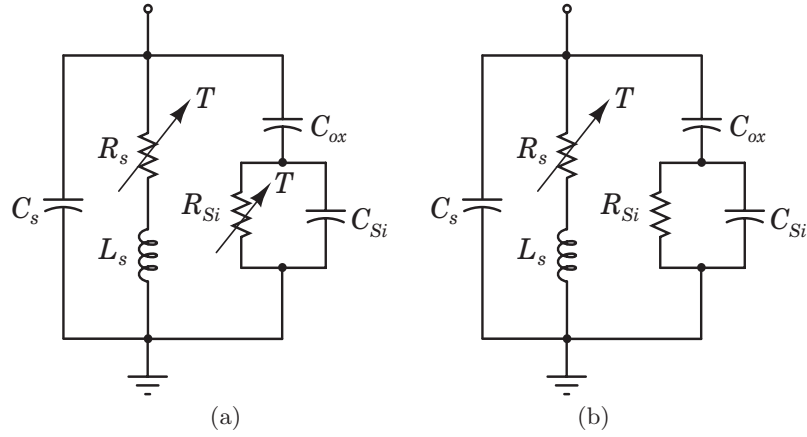


Figure 3.36: Temperature dependence of lumped physical equivalent model of the octagonal spiral inductor when the second port is connected to the ground: (a) case of STD substrate without PGS and (b) case of HR substrate and structures with PGS.

3.5 Conclusion

In this chapter, we have analyzed the impact of temperature on different transmission line structures and on integrated spiral inductors implemented on high and standard resistivity substrates. First, the two main transmission line topologies, usually used in MMIC design were compared. The losses of transmission line structures implemented on high resistivity substrate are mainly due to the metallic losses (metal resistivity). The losses of transmission line structures implemented on standard resistivity substrate are due to both metallic and substrate losses.

The losses of TFMS and CPW structures implemented on standard and high resistivity substrate were investigated over a wide range of temperature. As expected, the losses increase with respect to the temperature except for the CPW line implemented on standard resistivity substrate for which the decrease of substrate losses compensate the increase of metallic losses when temperature rises. The TFMS line

3.5 CONCLUSION

structures can then be an interesting topology if the losses can be lowered to the same level as CPW made on HR SOI, because the TFMS line structures do not depend on the under-laying substrate. Standard resistivity SOI substrates can be used, being cheaper than HR case.

To reduce the metallic losses, the width and the thickness of the conductor must be increased, but the capacitance between the conductor and the ground plane must be kept constant ensuring the same characteristic impedance Z_c . To achieve this goal, the thickness of the dielectric layer must be increased, or low-k dielectric must be used instead of silicon dioxide. These solutions are in agreement with the tendencies of semiconductor industries. Indeed, more and more metal levels are used, allowing a thicker isolator layer between the top conductor and the ground plane.

We also studied the impact of temperature on the model parameters of integrated square and octagonal spiral inductors implemented on the same SOI CMOS technology. The use of high resistivity substrate allows to improve substantially the quality factor (80% improvement at room temperature compared to STD resistivity substrate). The use of patterned ground shield in the case of STD substrate leads to a 34% improvement on the maximum Q at ambient temperature. The inductors implemented on standard resistivity substrate show a minor temperature degradation on their quality factor. In the case of inductors on HR substrate, an decrease of the substrate resistivity with respect to temperature has been observed but does not impact substantially the temperature behavior of the quality factor since the value of R_{Si} at $200^\circ C$ is still high.

For an accurate modeling versus temperature in the case of HR resistivity substrate, only $R_s(T)$ must be considered as dependent on temperature, whereas in STD resistivity substrate $\rho_{Si}(T)$ must be considered as well. These results demonstrate the feasibility and practical applicability of different passive structures in circuit design for both room and high-temperature applications.

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CHAPTER 4

HT CHARACTERIZATION OF 130-NM PD SOI MOSFET

4.1 *Introduction*

With improvement in state-of-the-art electronic systems and the huge demand for low-cost high-speed mixed-signal integrated systems, a considerable effort has recently been made to migrate several high-frequency elementary circuit blocks from GaAs to CMOS Silicon process. Since CMOS Silicon-on-Insulator (SOI) devices present a very good high frequency behavior and a low power consumption, it is of great interest to use them in RF circuit design [1]. In the last decade, the MOS transistor channel length was scaled down to deep submicron to improve device performance in term of cut-off frequency. Recently, many designs of RF blocs such as LNA, VCO and mixer have demonstrated the interest of this technology for low-voltage and low-power applications.

Some applications (well logging, avionics, automotive, ...) require electronic circuits capable of operating at temperatures up to $300^{\circ}C$ [1]. The use of the CMOS MOSFET's at high-temperature is limited by latch-up due to the leakage current through the well junctions which becomes very large at high temperature [2]. The capability of SOI circuits to expand the operating temperature range of integrated circuits up to $300^{\circ}C$ has been demonstrated. The SOI CMOS technology can be a viable alternative because the almost perfect isolation of nMOS and pMOS is afforded by the elimination of the CMOS well junctions which results in a latch-up-free operation [1] [3]. Moreover, the SOI MOSFET's present less temperature sensitive threshold voltage, when compared to the conventional Bulk devices usually operating at moderate temperatures.

In the past decades, great efforts have been devoted to the characterization and modeling of MOSFETs on silicon and GaAs substrates [4] [5]. However, no systematic study on the performance trend of SOI MOSFETs with temperature has been reported. The knowledge of the equivalent circuit elements is interesting to develop circuit design methodologies, or to determine which parameters have a strong influence on the performances of MOSFETs. With the motivations to predict the temperature behavior of the MOSFETs implemented on CMOS SOI technology, this chapter presents a discussion on temperature measurement performed on the three classical n-MOSFETs available in SOI technology. Temperature performances and comparison of the three MOSFET types is proposed.

4.2 Figures-of-merit versus temperature

Important temperature-dependent MOSFETs parameters are usually the threshold voltage, the leakage current and the subthreshold slope [6] [7]. These parameters constitute important figures-of-merit in CMOS technologies. In the present section the main figures-of-merit will be analyzed over a wide temperature range (from 25 to 250°C) and for the three usual partially depleted SOI transistors.

Fig. 4.1 shows the geometry of a partially depleted (PD) SOI MOSFET. The quasi-neutral region (called “body”) sandwiched between the space-charge regions extending from the front and back oxide/Si interfaces and Source/Drain junctions, and is usually left electrically unconnected or floating. In the last case, we talk about a Floating Body (FB) transistor. The body of the SOI MOSFET can also be connected: to the source (to form a Body Contacted) or to the gate (to form a DTMOS). The standard models and relations existing for bulk Si MOSFET apply, without any major modification, to partially depleted SOI transistors.

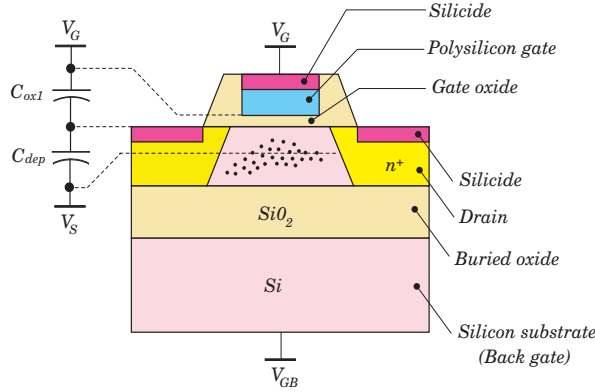


Figure 4.1: Illustration of a simplified capacitive network seen from the gate of a partially depleted SOI MOSFET.

4.2.1 Threshold voltage

In the SOI MOSFET, the threshold voltage V_{TH} is defined as the gate voltage required to induce a conducting channel under the CMOS gate. V_{TH} is defined in the same way for a conventional bulk MOSFET and is expressed as [1]:

$$V_{TH} = \phi_{MS} - \frac{Q_{ox}}{C_{ox}} + 2\phi_F + \frac{\sqrt{4\epsilon_0\epsilon_{Si}qN_a\phi_F}}{C_{ox}} \quad (4.1)$$

4.2 FIGURES-OF-MERIT VERSUS TEMPERATURE

where ϕ_F is the Fermi potential of the bulk Si, q is the electron charge, N_a is the substrate doping, Q_{ox} is the fixed charge density at the front $Si - SiO_2$ interface, C_{ox} is the gate oxide capacitance, ϵ_0 is the vacuum permittivity, ϵ_{Si} is the relative permittivity of silicon and ϕ_{MS} is the Fermi potential difference between the gate and bulk material. The parameter ϕ_{MS} depends on the energy gap E_g according to:

$$\phi_{MS} = -\frac{E_g}{2q} - \phi_F \quad (4.2)$$

Hence, the threshold voltage expression can be written as:

$$V_{TH} = -\frac{E_g}{2q} + \phi_F - \frac{Q_{ox}}{C_{ox}} + \frac{\sqrt{4\epsilon_0\epsilon_{Si}qN_a\phi_F}}{C_{ox}} \quad (4.3)$$

Assuming that the oxide charge density is independent of temperature, the temperature dependence of the threshold voltage is related to the temperature dependence of the energy gap E_g and of the Fermi potential ϕ_F :

$$\frac{\partial V_{TH}}{\partial T} = -\frac{1}{2q} \frac{\partial E_g}{\partial T} + \frac{\partial \phi_F}{\partial T} + \frac{1}{\sqrt{\phi_F}} \frac{\partial \phi_F}{\partial T} \frac{\sqrt{\epsilon_0\epsilon_{Si}qN_a}}{C_{ox}} \quad (4.4)$$

In the temperature range 25 to 250°C, E_g can be considered as constant. In this case the temperature dependence of threshold voltage of the thin-film SOI MOSFET can be written as [1]:

$$\frac{\partial V_{TH}}{\partial T} = \frac{\partial \phi_F}{\partial T} \left(1 + \frac{1}{\sqrt{\phi_F}} \frac{\sqrt{\epsilon_0\epsilon_{Si}qN_a}}{C_{ox}} \right) \quad (4.5)$$

where the Fermi potential ϕ_F is equal to

$$\phi_F = \frac{k_B T}{q} \ln \left(\frac{N_a}{n_i} \right) \quad (4.6)$$

and n_i is the Si intrinsic concentration defined as $n_i = \sqrt{N_c N_v} e^{\frac{-E_g}{2k_B T}}$.

Therefore,

$$\frac{\partial V_{TH}}{\partial T} = \frac{\partial \phi_F}{\partial T} \left(1 + \frac{q}{C_{ox}} \sqrt{\frac{\epsilon_0\epsilon_{Si}N_a}{k_B T \cdot \ln(N_a/n_i)}} \right) \quad (4.7)$$

where the temperature dependence of the Fermi potential ϕ_F can be expressed as:

$$\frac{\partial \phi_F}{\partial T} = \frac{\partial}{\partial T} \left[\frac{k_B T}{q} \cdot \ln \left(\frac{N_a}{\sqrt{N_c N_v} e^{\frac{-E_g}{2k_B T}}} \right) \right] \quad (4.8)$$

$$= \frac{k_B}{q} \cdot \ln \left(\frac{N_a}{\sqrt{N_c N_v}} \right) - \frac{k_B T}{q \sqrt{N_c N_v}} \frac{\partial \sqrt{N_c N_v}}{\partial T} \quad (4.9)$$

where N_c and N_v are both proportional to $T^{3/2}$. If we set $N_c = N_{co} \cdot T^{3/2}$ and $N_v = N_{vo} \cdot T^{3/2}$, the second term in (4.9) can be simplified as

$$\frac{k_B T}{q \sqrt{N_c N_v}} \cdot \frac{\partial \sqrt{N_c N_v}}{\partial T} = \frac{k_B T}{q \sqrt{N_{co} N_{vo}} \cdot T^{3/2}} \cdot \frac{3}{2} \sqrt{N_{co} N_{vo}} \cdot T^{1/2} \quad (4.10)$$

$$= \frac{3}{2} \frac{k_B}{q} \quad (4.11)$$

The second term in (4.9) is indeed caused by the temperature-induced variation of the depletion zone depth. Note that the variation of the depletion layer width in strong inversion is nonexistent in case of fully depleted SOI device, the threshold voltage shift with the temperature is due to the temperature dependence of ϕ_F ($\frac{\partial V_{TH}}{\partial T} \approx \frac{\partial \phi_F}{\partial T}$). Taking account the last simplification, the temperature dependence of Fermi potential ϕ_F becomes:

$$\frac{\partial \phi_F}{\partial T} = \frac{k_B}{q} \left[\ln \left(\frac{N_a}{\sqrt{N_c N_v}} \right) - \frac{3}{2} \right] \quad (4.12)$$

$$= \frac{k_B}{q} \left[\ln(N_a) - \ln \sqrt{N_{co} N_{vo}} - \frac{3}{2} [1 + \ln(T)] \right] \quad (4.13)$$

Fig. 4.2 shows the simulation of the temperature dependence of the threshold voltage for n-channel device implemented on silicon material according to the equation (4.7) and where the typical characteristics of the technology are: $\sqrt{N_{co} N_{vo}} \approx 3.9 \cdot 10^{16}$, $N_a \approx 1.2 \cdot 10^{17} - 1.6 \cdot 10^{17}$, $\epsilon_{Si} \approx 11.7$, $t_{ox} \approx 400 \text{ nm}$. The temperature coefficient of the threshold voltage $\partial V_{TH}/\partial T$ in SOI partially depleted devices is expected to be approximatively around -0.7 mV/K .

The linear extrapolation method with the drain current measured as a function of gate voltage at a low drain voltage ($V_{DS} \approx 50 \text{ mV}$) to ensure operation in the linear MOSFET region [8] has been used to extract the threshold voltage V_{TH} . The threshold voltage characteristics versus temperature for the three conventional transistors available in partially depleted SOI technology: floating body (FB), body contacted (BC) and dynamic threshold (DT) are plotted in Fig. 4.3. The floating body and body contacted show approximatively the same slope. It is also shows that V_{TH}

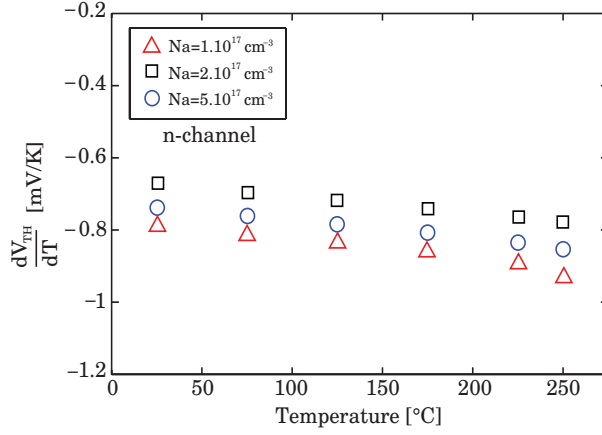


Figure 4.2: Threshold voltage versus temperature calculated by the linear extrapolation technique for $V_{DS} = 50 \text{ mV}$.

varies linearly versus the temperature according to:

$$V_{TH} \approx V_{TH}(T_0) + \lambda(T - T_0) \quad (4.14)$$

where $V_{TH}(T_0)$ is the threshold voltage at ambient temperature ($T_0 = 25^\circ\text{C}$) and the constant parameter λ is the temperature sensitivity of the threshold voltage equal to $\partial V_{TH}(T)/\partial T \approx -0.68 \text{ mV}/^\circ\text{C}^{-1}$, that is in a good agreement with the value of $-0.7 \text{ mV}/^\circ\text{C}$ predicted by the equation (4.7).

4.2.2 Leakage current

The increase of the junction leakage current is one of the main causes of failure in bulk silicon CMOS devices and circuits operating at high temperature. The junction leakage current is proportional to the area of junction. Much smaller high-temperature leakage currents are expected in CMOS SOI devices due to smaller source-drain junction areas and due to elimination of very large well-to-substrate junction leakages. It has been reported that at high temperature, where diffusion current dominates, the leakage current is three orders of magnitude lower in the SOI devices than in the bulk devices [1]. In CMOS SOI MOSFET, the leakage current I_{leak} is basically composed of two components, a generation current (I_{gen}) in the depletion region of the reverse-biased drain junction and a diffusion current I_{diff} from the undepleted portion of the film. In a n-channel SOI device, the generation current is expressed as [7] [9]:

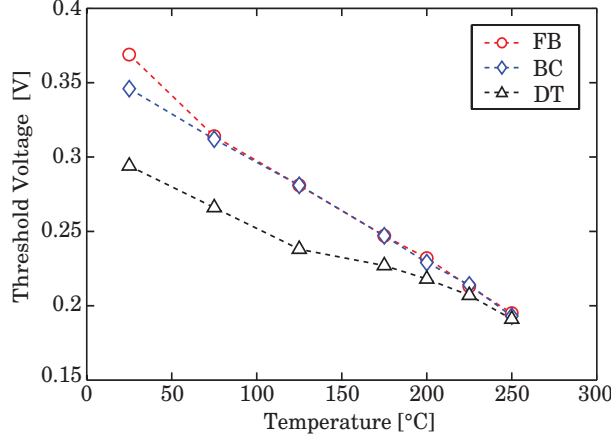


Figure 4.3: Threshold voltage versus temperature extracted from measurements by the linear extrapolation technique for $V_{DS} = 50 \text{ mV}$.

$$I_{gen} = \frac{qn_i W_g}{\tau_g} d_{Si} W_D \quad (4.15)$$

where W_g is the generation layer width, τ_g is the minority carrier generation lifetime which is related to the thermal generation process in the depletion region, d_{Si} is the Si film thickness and W_D is the total device width.

The diffusion current in n-channel SOI MOSFET can be expressed as [7]:

$$I_{diff} = qW_D \sqrt{\frac{D_n}{\tau_n}} \left(1 - e^{-\frac{qV_D}{k_B T}} \right) \int_0^{d_{Si}} \frac{n_i^2}{N_a} e^{\frac{q\varphi(x)}{k_B T}} dx \quad (4.16)$$

where D_n is the electron diffusion coefficient, τ_n is the electron lifetime in p-type neutral Si, $\varphi(x)$ is the potential distribution across the Si film thickness in undepleted body film and V_D is the potential of the drain junction.

The equations (5.15) and (5.16) indicate that the diffusion current is proportional to n_i^2 and the generation current is proportional to n_i . It has been experimentally observed that the leakage current in case of SOI MOSFETs varies with temperature as n_i below a temperature of $100 - 150^\circ\text{C}$ (meaning that the generation current mechanism dominates) and at temperature above 100°C the leakage current varies with temperature as n_i^2 indicating that the diffusion current becomes predominates [1].

Fig. 4.7 shows the measured leakage current of the 130 nm partially depleted n-channel MOSFETs versus temperature, for the three conventional types (floating

4.2 FIGURES-OF-MERIT VERSUS TEMPERATURE

body, body contacted and dynamic threshold transistors). Leakage current is measured when the MOSFET is turned off, which in this case is taken for negative values of gate-source bias and in saturation region ($V_{DS}=1.2$ V). It is clearly noticed that the floating body MOSFETs show the highest leakage current at high temperature. The dynamic threshold devices show a very interesting behavior and very low leakage current at high temperature when compared to floating body and body contacted devices [5]. It can be also observed that up to temperature of 100°C , the different transistors show similar leakage current values. However, starting from 150°C , where the diffusion current becomes predominant, the floating body device shows much higher leakage current due to the floating body effect (FBE) which is present in the saturation region [10] [11]. The generation of electron-hole pairs in the neutral region of the body of the FB MOSFETs increases with temperature, and so the accumulation of charges in the region may increase the diffusion current in the source-body junction [12].

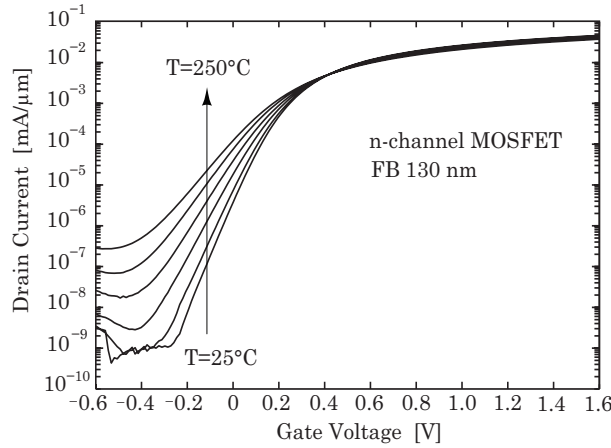


Figure 4.4: The temperature dependence of the leakage current per unit gate width in 130 nm partially depleted SOI devices measured for the floating body transistor and for $V_{DS}=1.2$ V.

4.2.3 Subthreshold slope

The subthreshold slope S (or subthreshold swing) should vary linearly with temperature according to:

$$S = \frac{\partial V_{GS}}{\partial \log(I_{DS})} \approx \frac{k_B T}{q} \ln(10) \left(1 + \frac{C_D}{C_{ox}} \right) \quad (4.17)$$

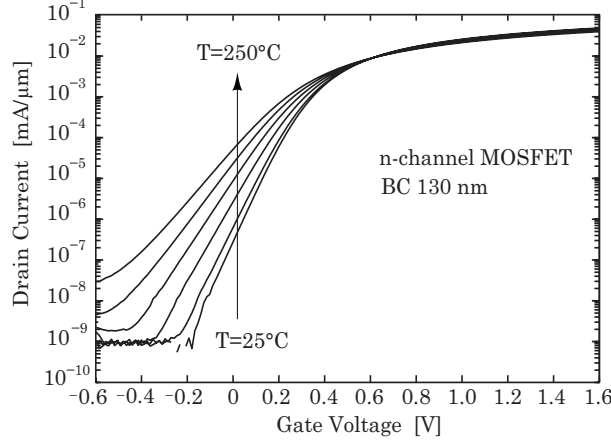


Figure 4.5: The temperature dependence of the leakage current per unit gate width in 130 nm partially depleted SOI devices measured for the body contacted transistor and for $V_{DS}=1.2$ V.

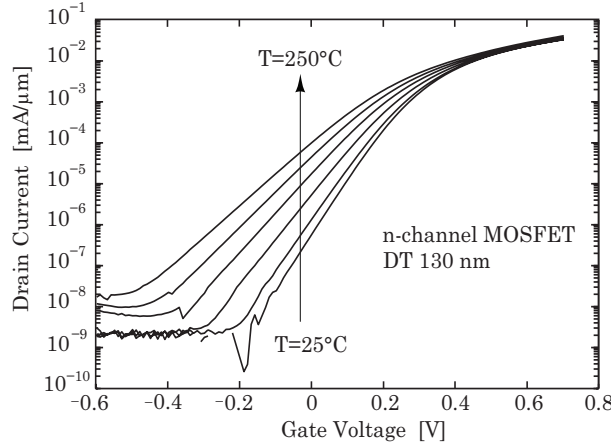


Figure 4.6: The temperature dependence of the leakage current per unit gate width in 130 nm partially depleted SOI devices measured for the dynamic threshold transistor and for $V_{DS}=1.2$ V.

where C_D is the capacitance of the depleted silicon film ($C_D = \epsilon_{Si}/d_{Si}$) and C_{ox} is the gate oxide capacitance.

Fig. 4.8 shows the measured evolution of the subthreshold slope S for the 130 nm partially depleted n-channel MOSFETs with temperature and for the three conventional MOSFETs (floating body, body contacted and dynamic threshold transistors). As expected, the subthreshold slope of the three device types is remarkably linear over

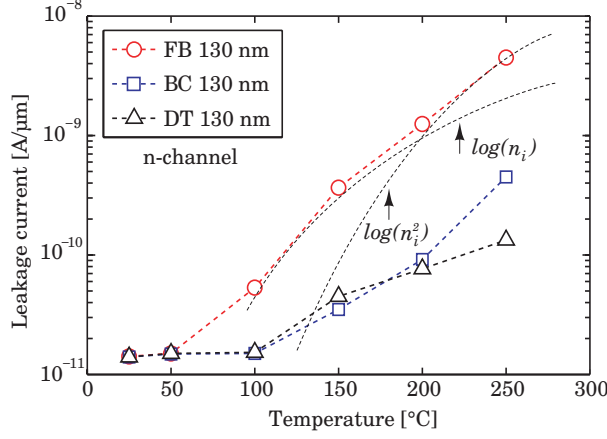


Figure 4.7: The temperature dependence of the leakage current per unit gate width in 130 nm partially depleted SOI devices measured for the three conventional transistors (FB, BC and DT) and for $V_{DS}=1.2$ V.

the temperature range 25 to 250°C. DT MOSFET shows a near ideal subthreshold slope at room temperature as already reported in several works [7] [13] [14]. For the BC and FB transistors, the subthreshold swing exhibits the expected linear temperature dependence only up to 150°C and above this temperature point, S show an exponential variation arising from the thermal activation of the leakage current [15].

$$S = S_{linear} + A \cdot \exp\left(-\frac{E_g}{2k_B T}\right) \quad (4.18)$$

4.2.4 I_{ON} to I_{OFF} Ratio

The I_{ON} -to- I_{OFF} ratio is an important figure of merit for digital circuits. It is well known that the SOI devices provide much better I_{ON}/I_{OFF} than the conventional bulk devices. This is due to the fact that the area of source and drain junctions are much smaller in SOI than bulk. This contributes to radically reduce the overall standby current consumption of SOI devices and circuits when compared to the conventional bulk devices. The OFF current of the SOI device is equal to the reverse-biased drain junction in enhancement-mode SOI MOSFETs. It is well smaller in SOI than in bulk devices owing to the reduced junction area and to the increase of the Si intrinsic concentration (n_i) with the temperature [7] [2].

Fig. 4.9 shows the measured I_{ON}/I_{OFF} ratio for the 130 nm partially depleted n-channel MOSFETs versus temperature (from 25 to 250°C) and for the three con-

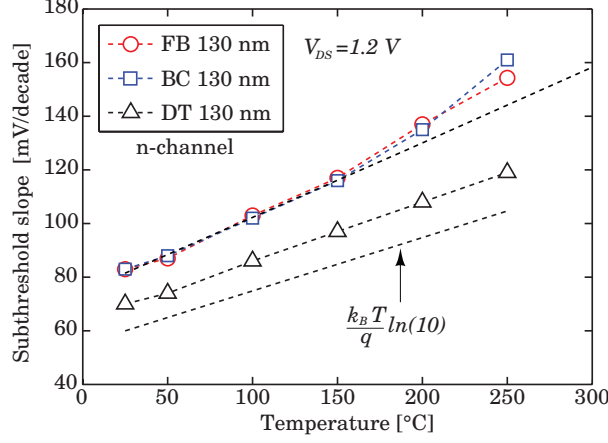


Figure 4.8: The temperature dependence of the subthreshold slope in 130 nm partially depleted SOI devices measured for the three conventional transistors (FB, BC and DT) and for $V_{DS}=1.2$ V.

ventional MOSFETs (FB, BC and DT transistors). The measurements are performed at $V_{GS} = 0$ V and $V_{DS} = 1.2$ V for devices with a channel length of 130 nm and a width of $60 \mu\text{m}$ (30 gate fingers of $2 \mu\text{m}$ each). At low temperature, it is clear that the FB transistors exhibit lower I_{ON}/I_{OFF} ratio I_{OFF} when compared to BC and DT devices. This is due to the larger I_{OFF} of FB MOSFET caused by the floating body effect (FBE) [3] [16]. Thanks to a lower leakage current and the absence of FBE, the body contacted and dynamic threshold devices show higher I_{ON}/I_{OFF} ratio. It should also be noticed that, at high temperature, the I_{ON}/I_{OFF} ratio of all devices tends to very close values. This can be explained by the fact that, when the temperature increases, the holes generated near the drain are injected into the floating body, and henceforth raise the body bias V_{BS} and so, the floating body effect becomes less severe when the temperature increases. Thus, the floating body induced increase of I_{OFF} is suppressed at high temperature and the FB devices show the same I_{ON}/I_{OFF} ratio and the same behavior as the BC devices [17].

4.2.5 Conclusion

Table 4.1 summarizes the degradation of the main figures of merit of the three conventional SOI MOSFETs when the temperature varies from 25 to 250°C . The dynamic threshold transistor exhibits the best results and the lowest temperature degradation when compared to the floating body and body contacted MOSFETs.

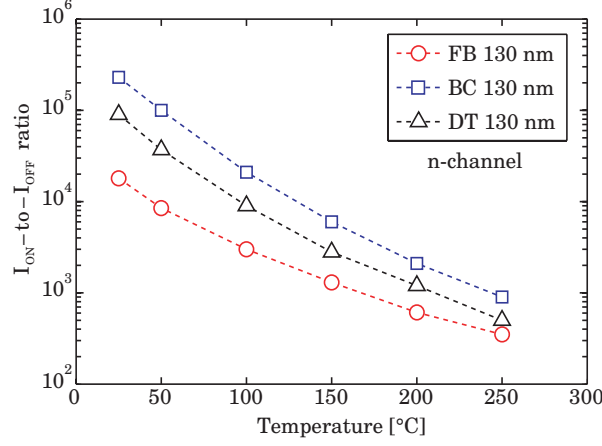


Figure 4.9: Temperature dependence of the I_{ON}/I_{OFF} ratio in 130 nm partially depleted SOI devices measured for the three conventional SOI transistors (FB, BC and DT)

	V_{TH}	S	I_{ON}/I_{OFF}	I_{Leak}
ϵ_{FB}	44%	88%	98%	332 10 ² %
ϵ_{BC}	43%	94%	99%	32 10 ² %
ϵ_{DT}	32%	71%	99%	9 10 ² %

Table 4.1: Temperature degradation of the main figures of merit in SOI devices.

4.3 High temperature DC characterization of MOSFETs

4.3.1 Introduction

The drain current temperature dependence of SOI CMOS transistors is driven by three main sources: the threshold voltage (V_{TH}), the inversion layer charge concentration (n_i) and the mobility (μ). The threshold voltage varies linearly with the temperature according (4.14). The mobility depends on temperature according to [18]:

$$\mu = \mu_0 \left(\frac{T_0}{T} \right)^\eta \quad (4.19)$$

where η is typically between 1 and 2 (typically 1.5). This causes the mobility to decrease by about half percent per degree. The expression for the channel mobility

can be further complicated by introducing velocity saturation and mobility degradation due to the applied transverse electric field. This would mean that the mobility depends upon the gate bias voltage and the threshold voltage and hence upon temperature again.

Assuming a long channel transistor, the drain current of a SOI MOSFET in the linear region ($V_{DS} < V_{DS,lim}$) is given by [19]:

$$I_{DS,lin} = \mu(T) C_{ox1} \frac{W}{L_g} \left[(V_{GS} - V_{TH}(T)) V_{DS} - \frac{1 + \alpha(T)}{2} V_{DS}^2 \right] \quad (4.20)$$

In the saturation region the drain-current $I_{DS,sat}$ and the transconductance $g_{m,sat}$ of the SOI n-MOSFET are expressed as [19]:

$$I_{DS,sat} = \frac{W}{L_g} \frac{\mu(T) C_{ox1}}{2(1 + \alpha(T))} [V_{GS} - V_{TH}(T)]^2 \quad (4.21)$$

$$g_{m,sat} = \frac{\partial I_{DS}}{\partial V_{GS}} = \frac{W}{L_g} \frac{\mu(T) C_{ox1}}{1 + \alpha(T)} [V_{GS} - V_{TH}(T)] \quad (4.22)$$

where the threshold voltage, the mobility and the body factor (α) depend on temperature.

In this section, the most important DC characteristics in linear and saturation regions are presented for the three types of transistors, in addition to other important figures-of-merit like g_m/I_{DS} , the temperature dependence of maximum of transconductance ($g_{m,max}$) and the Zero-Temperature-Coefficient (ZTC). Finally, an investigation of the possibility to tune the Zero-Temperature-Coefficient point by controlling the body-source forward bias V_{BS} will be proposed. The measured devices are n-channel MOSFETs fabricated in 130 nm partially depleted SOI technology. The measurements are done over the temperature range $25 - 250^\circ C$.

4.3.2 Dynamic characteristics

Fig. 4.10 shows the measured dynamic characteristics of the three conventional partially depleted transistors in linear ($V_{DS} = 50 \text{ mV}$) and saturation ($V_{DS} = 1.2 \text{ V}$) regions, for various temperature conditions. We note a bias gate voltage V_{GS} for which the drain current remains constant when temperature varies [20] [21]. The Zero-Temperature-Coefficient (ZTC) point has been identified experimentally for SOI MOSFET's by Jeon and co-workers [22], and Groeseneken and co-workers [23]. The ZTC bias points are defined as the bias at which the drain current or the transduc-

tance exhibits a zero variation with temperature. In other terms, at ZTC transconductance point (ZTC_{g_m}), $\partial g_m(T)/\partial T = 0$ and at ZTC current point ($ZTC_{I_{DS}}$), $\partial I_{DS}(T)/\partial T = 0$. The ZTC_{g_m} and $ZTC_{I_{DS}}$ bias points can be seen as factors of merit in analog circuit design for high temperature applications.

The so-called Zero Temperature Coefficient (ZTC) point, which appears in both linear and saturation regime of operation as shown in Fig. 4.10, is a value of V_{GS} at which the reduction of the threshold voltage and the reduction of the mobility are approximately compensated, and as a result, the value of the drain current and the value of the transconductance remain constant as the temperature varies. For gate voltages lower than ZTC, the decrease of the threshold voltage is dominant and so the drain current increases with temperature, while for gate voltages higher than ZTC, the mobility degradation predominates and the drain current decreases with temperature. As can be seen, the ZTC point of SOI devices is approximately constant with temperature (up to $250^\circ C$ in our study) due to low leakage current and a constant threshold voltage shift where in the case of bulk MOSFETs, ZTC point (ZTC_{g_m} and $ZTC_{I_{DS}}$) is approximately constant up to $150^\circ C$ only [24].

The ZTC point constitutes an important issue for the design of ICs operating at high temperature. We note a gate-voltage giving the drain-current ZTC ($V_{GS,ZTC_{I_{DS}}}$) of 0.51 V for the three transistors in linear region. The DTMOS does not show any ZTC point in saturation region. Dynamic threshold transistor shows less temperature dependence than the two other structures.

Fig. 4.11 shows the measured transconductance characteristics of the three conventional partially depleted transistors in linear and saturation regions and for various temperature conditions (from 25 to $250^\circ C$). As can be seen, the transconductance characteristic exhibit a ZTC point of 0.37 V for the three MOSFETs in the linear region. The values of the V_{GS} bias for which the transconductance and drain current of the three conventional devices exhibit ZTC points are summarized in the Table 4.2.

In saturation region, the transconductance is proportional to $\mu(T)(V_{GS} - V_{TH}(T))$ and because the DT transistor has a lower $V_{TH}(T)$, it shows higher saturation transconductance values and lesser dependence on temperature compared to FB and BC transistors. This makes the DT MOSFET more attractive for analogue design in high temperature applications. Note that the transconductance ZTC bias point ($V_{GS,ZTC_{g_m}}$) is lower than the current ZTC bias ($V_{GS,ZTC_{I_{DS}}}$). Thus, when a device is biased at saturation region current ZTC point, its g_m will decrease with temperature. The ZTC_{g_m} point can find applications in the design of amplifiers with a minimum gain variation when operated at high temperature.

Important improvements of the DTMOS when compared to nMOSFET are observed. In a DTMOS, any change of the gate bias will lead to induce a variation of

the body potential, changing dynamically the threshold voltage. Indeed, as the gate voltage of the DTMOS increases, its threshold voltage V_{TH} is reduced. The amount of current driven by the DTMOS is then higher than for BC and FB transistors having the same gate voltage overdrive ($V_{GS}-V_{TH}$), as can be seen in Fig. 4.10. The dynamic modulation of the threshold has also a strong influence on the transconductance. Indeed, the DTMOS exhibits a higher transconductance than for a BC or FB nMOSFETs [13] [14].

However, as can be seen in the drain-current and the transconductance characteristics, the DTMOS at high V_{GS} shows a temperature behavior which is quite different than for BC or FB MOSFETs. This can be explain by the fact that the PN junction diodes body/source and body/drain (Fig. 4.12) would turn on as gate/body bias larger than a certain voltage values (0.7 V at ambient temperature) for a n-channel DTMOS. Moreover, $V_{GS,limit}$ corresponding to the bias between the gate and source above which the body-to-source junction conducts, decreases with temperature as shown in Fig. 4.13.

Considerably large leakage current due to the turn-on diode current between the body and source terminals is a disaster under dynamic threshold mode. Therefore, the power supply voltage for DTMOS ambient temperature applications is usually restricted to 0.7 V due to the turn-on behavior between the body and source junction above that voltage.

Note also the presence of the so-called gate-induced floating body effect (GIFBE) in linear transconductance characteristic of the floating body device [25] (see chapter 2). However because the FBE becomes less severe when temperature increases due to impact ionization [26] [27], the GIFBE becomes negligible at high temperature.

		ZTC g_m		ZTC I_{DS}	
		Lin	Sat	Lin	Sat
$V_{GS,ZTC}$ [V]	FB	0.38	0.23	0.52	0.42
	BC	0.38	0.40	0.43	0.61
	DT	0.35	0.42	0.52	–

Table 4.2: Summary of the ZTC points in linear ($V_{DS} = 50$ mV) and saturation region ($V_{DS} = 1.2$ V) for the three conventional SOI MOSFETs.

Fig. 4.14 shows the temperature dependence of the g_m/I_{DS} ratio versus gate voltage for various temperature conditions. The g_m/I_{DS} ratio does not depend on device dimensions [27]. It is noted that the temperature dependence of the g_m/I_{DS}

4.3 HIGH TEMPERATURE DC CHARACTERIZATION OF MOSFETS

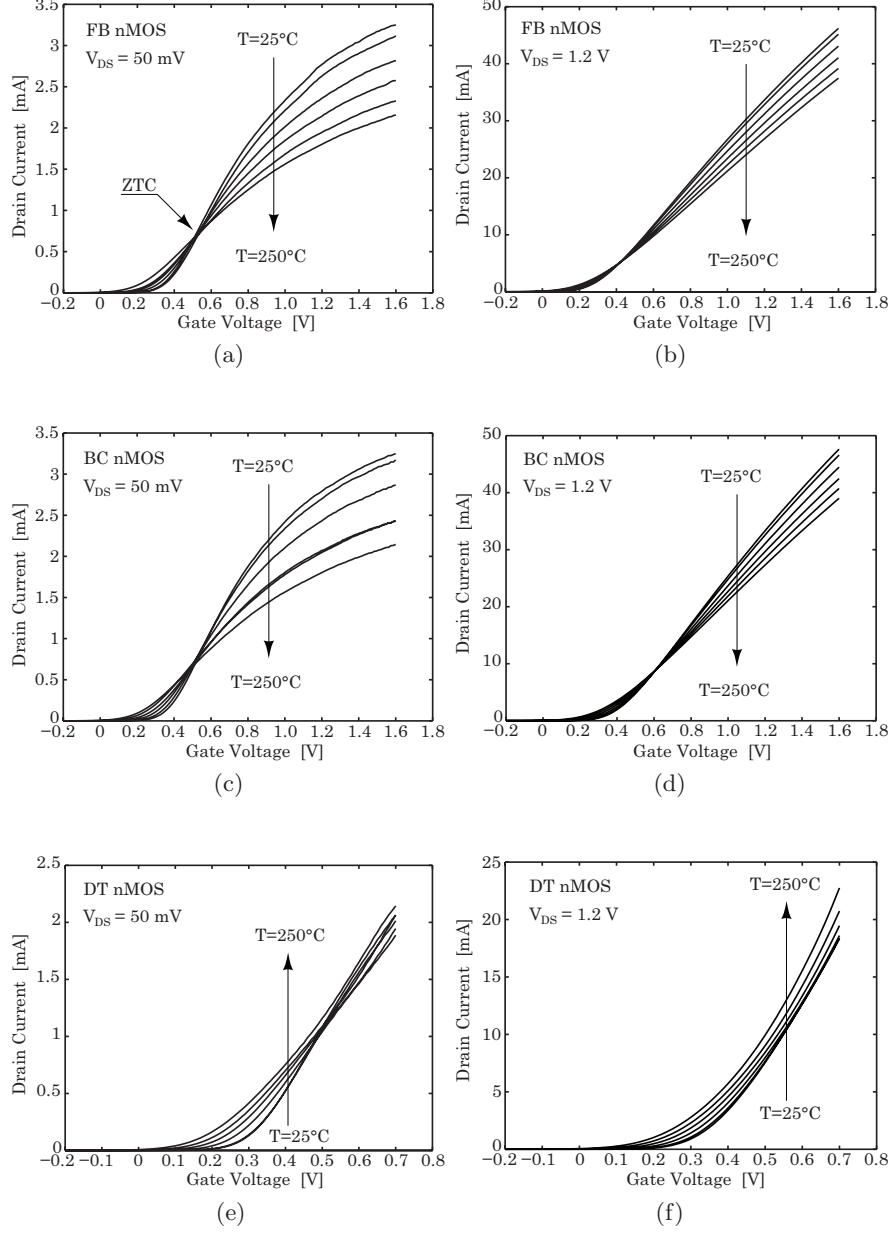


Figure 4.10: Temperature dependence of the $I_{DS} - V_{GS}$ characteristic for the (a) and (b) Floating-Body, (c) and (d) Body-Contacted, (e) and (f) Dynamic Threshold, nMOS SOI transistor with a channel length of 130 nm and a width of 60 μm (30 gate fingers of 2 μm each) in linear and saturation region.

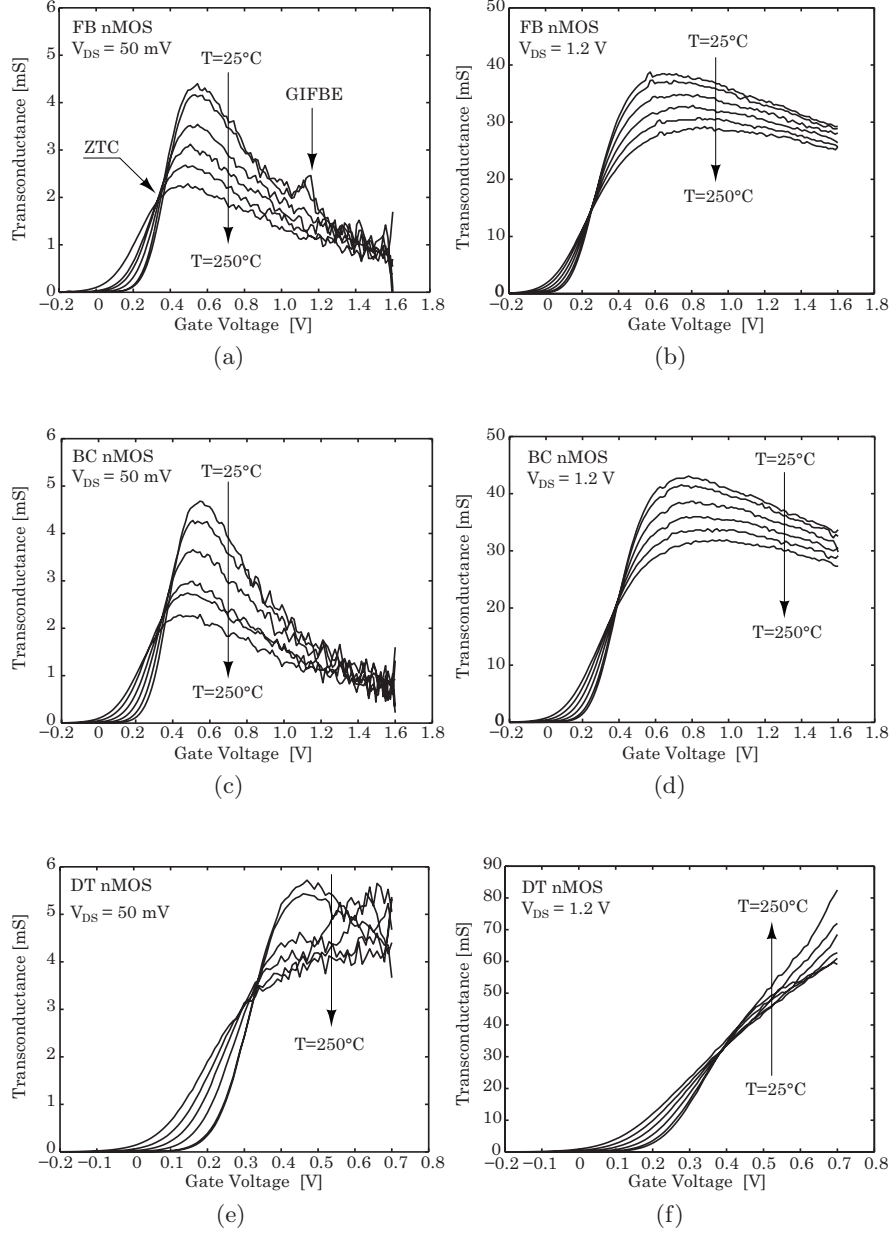


Figure 4.11: Temperature dependence of the $g_m - V_{GS}$ characteristic for the (a) and (b) Floating-Body, (c) and (d) Body-Contacted, (e) and (f) Dynamic Threshold, nMOS SOI with a channel length of 130 nm and a width of 60 μm (30 gate fingers of 2 μm each) in linear and saturation region.

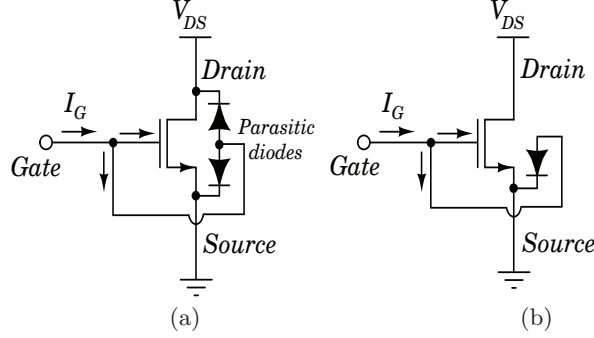


Figure 4.12: Simple equivalent model of DTMOS with the PN junction diodes (body/source and body/drain); (a) in linear and (b) in saturation regimes.

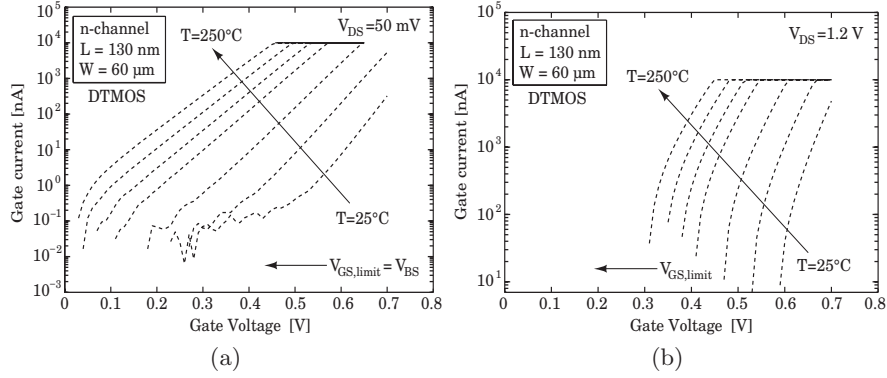


Figure 4.13: Gate current versus gate voltage characteristic in a Dynamic Threshold transistor, with a channel length of 130 nm and a width of 60 μ m (30 gate fingers of 2 μ m each), (a) in linear and (b) in saturation regions.

ratio can be neglected for V_{GS} higher than 0.6 V. Note that in saturation region and for $V_{GS} > V_{TH}$, the g_m/I_{DS} ratio is proportional to $1/(V_{GS} - V_{TH})$. Thus the g_m/I_{DS} ratio only depends on temperature via the threshold voltage $V_{TH}(T)$. The term $1/(V_{GS} - V_{TH})$ decreases when temperature increases because the threshold voltage decreases with the temperature. This explains why the g_m/I_{DS} ratio decreases with the rise of temperature. For high values of gate-voltage ($V_{GS} \gg V_{TH}$), the influence of the threshold voltage in the term $1/(V_{GS} - V_{TH})$ becomes negligible, thus the g_m/I_{DS} is proportional to $1/V_{GS}$ and the temperature dependence of g_m/I_{DS} ratio becomes negligible as shown in Fig. 4.14. In strong inversion and saturation regimes, the temperature dependence of g_m/I_{DS} is due to the variation of the drain current and mobility with temperature. Neglecting the leakage current, the g_m/I_{DS} ratio can be approximated in those regime as [27] [28]:

$$\frac{g_m(T)}{I_{DS}(T)} = \sqrt{\frac{W}{L_g} \frac{2\mu(T) C_{ox1}}{[1 + \alpha(T)] I_{DS}(T)}} \quad (4.23)$$

In weak inversion and saturation region, the effect of the temperature degradation of the leakage current and the subthreshold slope, flattens out the g_m/I_{DS} and limits his maximum. In weak inversion and neglecting the leakage current, the temperature degradation of the g_m/I_{DS} ratio depends only on temperature dependence of the subthreshold slope S and can be approximated as follows [28]:

$$\frac{g_m(T)}{I_{DS}(T)} \approx \frac{\ln(10)}{S(T)} \quad (4.24)$$

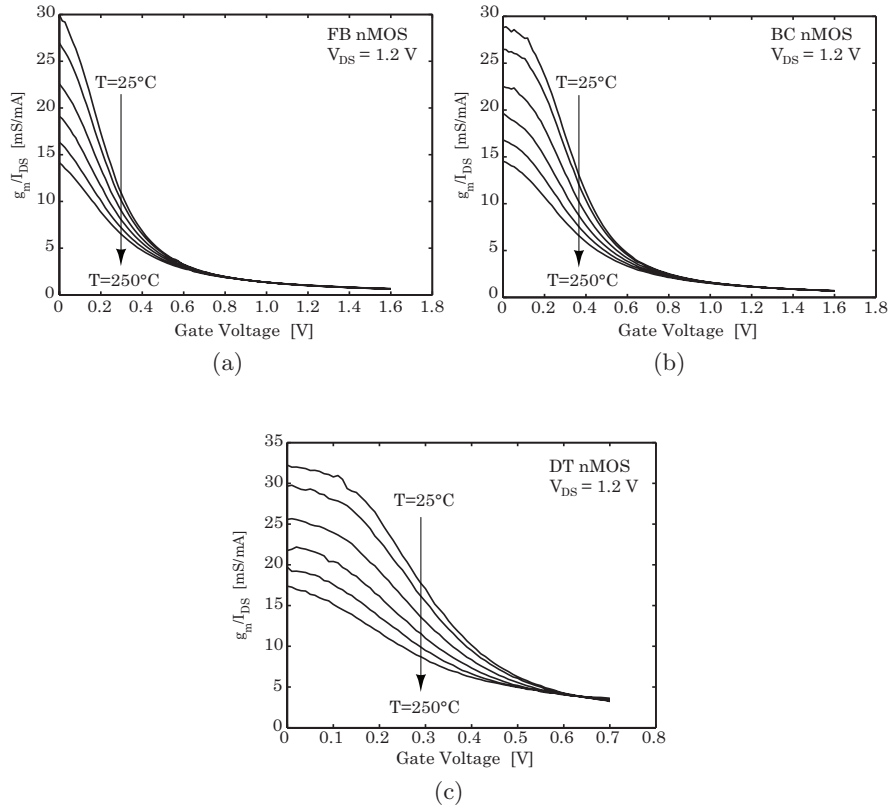


Figure 4.14: Temperature dependence of the g_m/I_{DS} characteristic for the (a) Floating-Body, (b) Body-Contacted and (c) Dynamic Threshold, SOI Partially-Depleted transistors in saturation region.

4.3.3 Static characteristics

Fig. 4.15 show the measured $I_{DS} - V_{DS}$ and $g_D - V_{DS}$ characteristics, respectively, of the three conventional partially depleted transistors for various temperature conditions (from 25 to 250°C). As mentioned before, because the impact ionization is reduced with temperature, the FBE is less pronounced at high temperature and the consequence is the reduction of the kink effect as can be seen in Fig. 4.15(a). The consequence is that the output conductance shows an important improvement at high temperature as can be seen in Fig. 4.15(b) [29]. This constitutes an important advantage compared to bulk devices where the output conductance is known to increase rapidly above 150°C due to the leakage current which shows a very important increase with the raise of temperature [30].

Without the kink effect which constitutes the main drawback of the FB transistor, it seems that the FB-SOI MOSFET can be the worst appropriate device for the analog application operating at high temperature. We also note a slight temperature dependence of the drain current with temperature for V_{GS} around 0.6 V over all the drain voltage range. This can be simply explained by the presence of the ZTC point around 0.6 V in $I_{DS} - V_{DS}$ characteristic, in saturation region.

As can be seen in Fig. 4.15, we also note an important improvement in output conductance of the DTMOS when the body potential increases. In fact, the depletion region under channel is reduced, providing for short channel DTMOS better output conductance than for FB and BC MOSFETs [31].

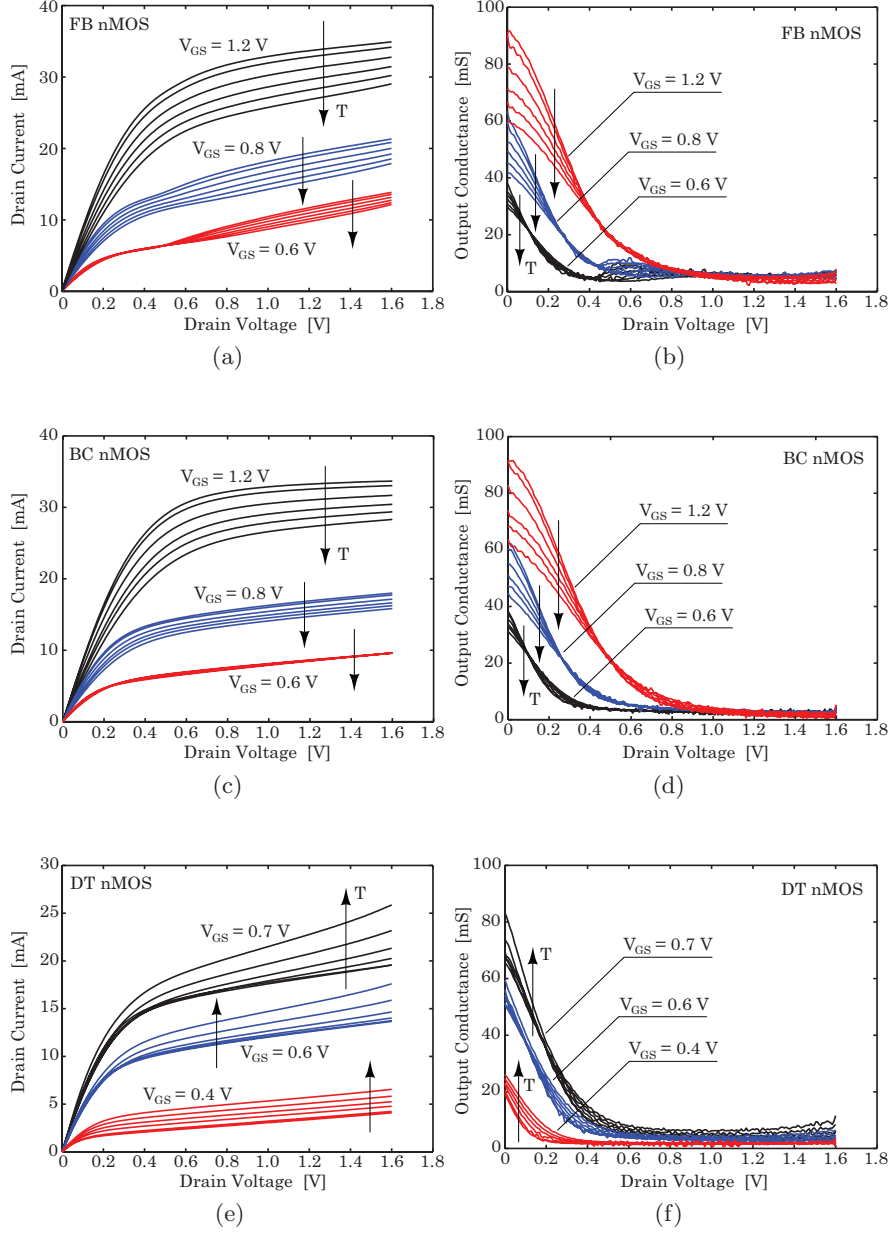


Figure 4.15: Temperature dependence of the $I_{DS} - V_{DS}$ and $g_D - V_{DS}$ characteristics for (a,b) Floating-Body, (c,d) Body-Contacted and (e,f) Dynamic Threshold, nMOS SOI with a channel length of 130 nm and a width of 60 μm (30 gate fingers of 2 μm each).

4.3.4 Temperature degradation

Fig. 4.16 and Fig. 4.17 show the variation of the drain-current $\epsilon_{I_{DS}}$ and the transconductance ϵ_{g_m} of the n-channel PD SOI MOSFET versus bias gate voltage V_{GS} when the temperature varies from $T_0 = 25^\circ C$ to $T_{max} = 250^\circ C$. The quantities $\epsilon_{I_{DS}}$ and ϵ_{g_m} are expressed in % and defined as:

$$\epsilon_{I_{DS}} = 100 \cdot \frac{I_{DS}(T_0) - I_{DS}(T_{max})}{I_{DS}(T_0)} \quad (4.25)$$

$$\epsilon_{g_m} = 100 \cdot \frac{g_m(T_0) - g_m(T_{max})}{g_m(T_0)} \quad (4.26)$$

where $g_m(T_0)$ and $g_m(T_{max})$ are the transconductance at $25^\circ C$ and at $250^\circ C$, respectively and $I_{DS}(T_0)$ and $I_{DS}(T_{max})$ are the drain current at $25^\circ C$ and at $250^\circ C$, respectively.

The factors $\epsilon_{I_{DS}}$ and ϵ_{g_m} give the information on the improvement or degradation of I_{DS} and g_m when the temperature passes from 25 to $250^\circ C$. It can be noted that the degradation of the transconductance (ϵ_{g_m}) due to the temperature variation can be minimized by fixing the gate bias point at $V_{GS,ZTC}$. The main inconvenient of this strategy is the important increases of drain current (100% for FB and BC transistors and 50% for DT MOSFET). We note an important improvement of the g_m in the total gate-voltage range in the case of the DT MOSFET. This improvement can be explained by the increase of the drain current with the raise of temperature for this device structure.

In strong inversion, the quantities $\epsilon_{I_{DS}}$ and ϵ_{g_m} can be approximated as:

$$\epsilon_{I_{DS}} = 100 \left[1 - \frac{I_{DS}(T_{max})}{I_{DS}(T_0)} \right] \quad (4.27)$$

$$= 100 \left[1 - \frac{\mu(T_{max})}{\mu(T_0)} \cdot \frac{1 + \alpha(T_0)}{1 + \alpha(T_{max})} \cdot \left(\frac{V_{GS} - V_{TH}(T_{max})}{V_{GS} - V_{TH}(T_0)} \right)^2 \right] \quad (4.28)$$

$$\epsilon_{g_m} = 100 \left[1 - \frac{g_m(T_{max})}{g_m(T_0)} \right] \quad (4.29)$$

$$= 100 \left[1 - \frac{\mu(T_{max})}{\mu(T_0)} \cdot \frac{1 + \alpha(T_0)}{1 + \alpha(T_{max})} \cdot \frac{V_{GS} - V_{TH}(T_{max})}{V_{GS} - V_{TH}(T_0)} \right] \quad (4.30)$$

and for higher values of gate-source voltage ($V_{GS} \gg V_{TH}$), $V_{GS} - V_{TH}(T)$ is approximatively equivalent to V_{GS} (this approximation is better at high temperature

where $V_{TH}(T)$ decreases with the raise of temperature). Considering this simplification, ϵ_{IDS} and ϵ_{gm} can be approximated as:

$$\epsilon_{IDS} = \epsilon_{gm} \approx 100 \left[1 - \left(\frac{T_0}{T_{max}} \right)^\eta \cdot \frac{1 + \alpha(T_0)}{1 + \alpha(T_{max})} \right] \quad (4.31)$$

The last expression shows that, in strong inversion, the degradations of ϵ_{IDS} and ϵ_{gm} in case of FB and BC transistors are independent with V_{GS} as shown in Fig. 4.16 and Fig. 4.17. As expected, the extracted ϵ_{IDS} and ϵ_{gm} factors are constant up to $V_{GS} > 0.8$ V and approximatively equal to 20% for the FB and BC devices. It is noted that the FB and BC devices show a maximum degradation of transconductance at $V_{GS} \approx 0.42$ V and $V_{GS} \approx 0.8$ V, respectively, corresponding to $V_{GS,ZTC_{IDS}}$ of each devices. This shows a serious comprimize between the choice of the two ZTC points. So it is necessary to choose to bias the circuit at one of the ZTC points.

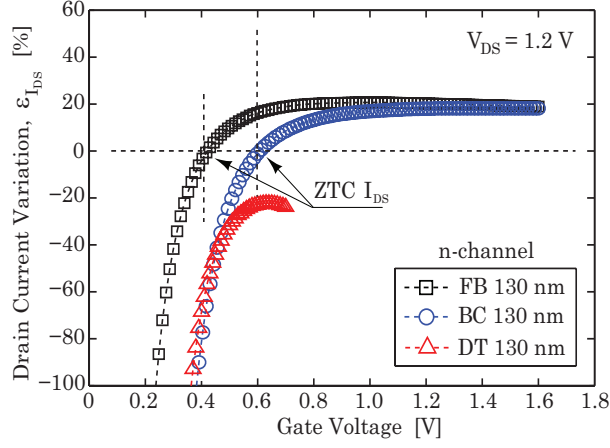


Figure 4.16: Degradation of the drain current when temperature varies from $T_0 = 25^\circ\text{C}$ to $T_{max} = 250^\circ\text{C}$ of n-channel PD SOI MOSFET for the three conventional transistors.

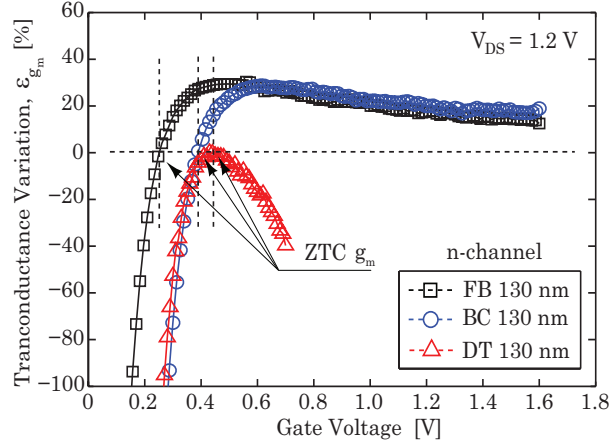


Figure 4.17: Degradation of the transconductance when temperature varies from $T_0 = 25^\circ\text{C}$ to $T_{max} = 250^\circ\text{C}$ of n-channel PD SOI MOSFET for the three conventional transistors.

Fig. 4.18 shows the variation of the g_m/I_{DS} ratio for the n-channel PD SOI MOSFET versus bias gate voltage V_{GS} when the temperature varies from $T_0 = 25^\circ C$ to $T_{max} = 250^\circ C$. The term $\epsilon_{g_m/I_{DS}}$ shows a large temperature impact on the g_m/I_{DS} ratio in weak inversion due to the degradation of the subthreshold slope which is predominant in weak inversion and increases with the raise of temperature [27]. Neglecting the leakage current, the $\epsilon_{g_m/I_{DS}}$ factor can be approximated, in the saturation region and weak inversion, by:

$$\epsilon_{g_m/I_{DS}} \approx 100 \cdot \left[1 - \frac{S(T_0)}{S(T_{max})} \right] \quad (4.32)$$

$$\approx 100 \cdot \left[1 - \frac{T_0}{T_{max}} \cdot \frac{\alpha(T_0)}{\alpha(T_{max})} \right] \quad (4.33)$$

This expression indicates that the devices having a minimum variation of subthreshold slope with temperature seem to exhibit a minimum temperature degradation of the g_m/I_{DS} ratio. This explains the lower $\epsilon_{g_m/I_{DS}}$ of DT transistor (45%) compared to the FB and BC devices (which exhibit a $\epsilon_{g_m/I_{DS}}$ of 50% and 55%, respectively). In strong inversion, g_m/I_{DS} ratio exhibits a minimum and negligible temperature degradation. However, the analog circuits are usually designed in weak inversion in order to optimize the g_m/I_{DS} ratio. The choice of strong inversion to minimize the temperature degradation of the g_m/I_{DS} ratio seems to set a serious compromise.

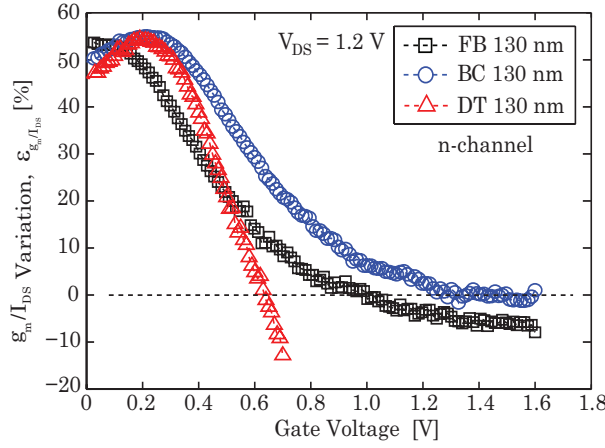


Figure 4.18: The degradation of g_m/I_{DS} ratio when temperature varies from $T_0 = 25^\circ C$ to $T_{max} = 250^\circ C$ of n-channel PD SOI MOSFET for the three conventional transistors.

4.3.5 Zero-Temperature-Coefficient point analysis

4.3.5.1 Introduction

Recently, there has been a growing interest in designing circuits that operate reliably at high temperature [28]. It is desirable to drive circuits designed for high temperature applications at a point where the drain current shows zero or very small variation with temperature [20]. The ZTC point constitutes one important issue for the IC design operated at high temperature applications. Moreover, the ZTC point is valid for SOI up to 300°C whereas in CMOS bulk it is valid up to 150°C. The extended temperature range in case of SOI MOSFET's is due to the suppression of leakage currents by the insulating layer (BOX: Buried Oxide) between the body and substrate [1].

However, the ZTC bias point is reached for a constant and unique gate-voltage (V_{GS}) when conventional SOI MOSFET architectures are used (floating body or body tied MOSFET) [20] [32]. This imposes the bias point of the circuit and then does not offer to designers different optimization possibilities (low power, low noise, high speed...) and does not offer, for example the possibility to reach a high gain and minimum temperature degradation together and imposes a compromise between these factors of merit. Note also that for the three conventional devices analyzed (FB, BC and DT nMOSFETs), the ZTC_{g_m} is achieved for a very weak values of V_{GS} (as low as 0.42 V), limiting the transconductance values (15, 20 and 32 mS for FB, BC and DT MOSFETs, respectively).

Moreover, the ZTC points are usually affected by process variations and it is not possible to obtain the ZTC_{g_m} and $ZTC_{I_{DS}}$ bias conditions together (the value of g_m at current ZTC bias point at 250°C is almost 30% its value at 25°C). All these inconvenients, make the ZTC points choice more delicate and inappropriate for many applications. To solve this problem, it would be interesting to control the drain current ZTC and g_m ZTC points in a large gate bias range. A solution, described in the next section, consists in biasing the body node of the MOSFET to vary the threshold voltage, and thus the ZTC points.

4.3.5.2 Body bias control

The ZTC point is reached when the temperature mobility reduction compensates the threshold voltage shift. So, theoretically, it is possible to vary the gate voltage giving the ZTC point ($V_{GS,ZTC}$) by varying the threshold voltage. A possibility consists in biasing the body node to control the threshold voltage (V_{TH}). The threshold voltage of SOI MOSFET is given by [23]:

$$V_{TH} = -\frac{E_g}{2q} - \frac{Q_{ox}}{C_{ox}} + \phi_F + \frac{\sqrt{2\epsilon_0\epsilon_{Si}qN_a(2\phi_F - V_{BS})}}{C_{ox}} \quad (4.34)$$

This equation depicts the dependence of threshold voltage on body effect. When a negative bias is applied to the body (with respect to the source), the threshold voltage increases as a square-root function of the body bias. Assuming that the oxide charge density is independent of temperature, the temperature dependence of the threshold voltage is related to the temperature dependence of the energy gap E_g and of the Fermi potential ϕ_F :

$$\frac{\partial V_{TH}}{\partial T} \approx \frac{\partial \phi_F}{\partial T} \left(1 + \frac{1}{C_{ox}} \sqrt{\frac{2\epsilon_0\epsilon_{Si}qN_a}{2\phi_F - V_{BS}}} \right) \quad (4.35)$$

Fig. 4.19 shows the calculated temperature dependence of the threshold voltage versus the back gate voltage (according to (4.35)) at room temperature for n-channel devices and for a gate oxide thickness of $0.4 \mu m$ and a channel doping of $1 \times 10^{17} cm^{-3}$. It should be noticed that for a body bias gate $V_{BS} < 0$, the temperature dependence, $\partial V_{TH}(T)/\partial T$ is constant and does not show any dependence with respect to V_{BS} .

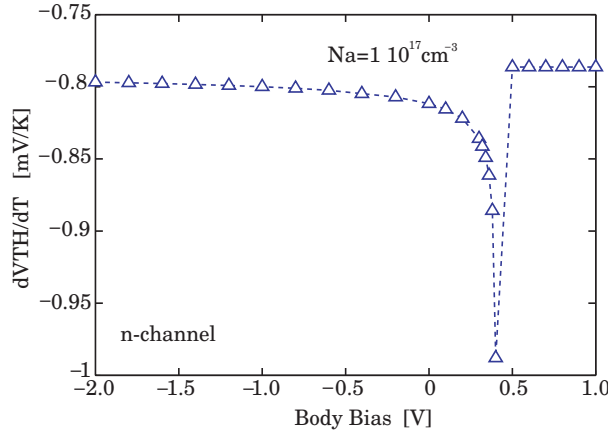


Figure 4.19: Calculated temperature dependence of the threshold voltage $\partial V_{TH}(T)/\partial T$, at room temperature, versus the body back-gate voltage, for a nMOS SOI transistor.

Fig. 4.20 shows the threshold voltage versus temperature ($V_{TH}(T)$) for various values of the body voltage (V_{BS}). It shows that V_{TH} varies almost linearly versus temperature [23]. The temperature variation of the threshold voltage can be experimentally and approximatively modeled by the simple expression:

$$V_{TH}(T) \approx V_{TH}(T_0) + \lambda(T - T_0) \quad (4.36)$$

where $V_{TH}(T_0)$ (≈ 0.34 V for $V_{BS} = 0$ V) is the threshold voltage at ambient temperature ($T_0 = 25^\circ\text{C}$) and the constant parameter λ is the temperature sensitivity, $\lambda = \Delta V_{TH}(T) / \Delta T$ (≈ -0.63 mV. $^\circ\text{C}^{-1}$ for $V_{BS} = 0$ V). It shows that the influence of V_{BS} on the threshold voltage has a big impact on $V_{TH}(T_0)$ and a small impact on the parameter λ . In this case (neglecting the impact of V_{BS} on the parameter λ), V_{TH} can be simply expressed as

$$V_{TH}(T, V_{BS}) \approx V_{TH}(T_0, V_{BS}) + \lambda(T - T_0) \quad (4.37)$$

where the parameter $V_{TH}(T_0, V_{BS}) = V_{TH}(V_{BS})$ at $T = T_0 = 25^\circ\text{C}$ is governed by the body bias according to a square-root function described by equation (4.34).

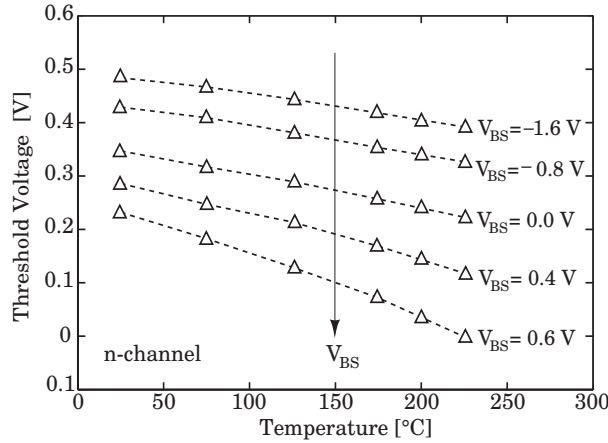


Figure 4.20: Measured $V_{TH}(T)$ -characteristic for various values of the back-gate voltage, for nMOS SOI transistor with a channel length of 130 nm and a width of 60 μm (30 gate fingers of 2 μm each).

The measured transconductance characteristic of the three-port nMOS of $\frac{W}{L} = \frac{60}{0.13}$ fabricated on 0.13 μm SOI CMOS process at various temperatures (from 25 to 225 $^\circ\text{C}$) and for different conditions of body bias is shown in Fig. 4.23. We observe that the gate-voltage giving the transconductance ZTC point ($V_{GS,ZTC_{gm}}$) decreases when V_{BS} increases. It confirms the influence of the body bias on the front channel threshold voltage. The position of the transconductance peak is shifted following the variation of $V_{TH}(V_{BS})$. The extracted characteristics $V_{GS,ZTC_{gm}}$ and $V_{GS,ZTC_{IDS}}$ versus V_{BS}

are shown in Fig. 4.24. When the body bias varies from -1.6 to 0.7 V, the tuning range of $V_{GS,ZTC_{gm}}$ and $V_{GS,ZTC_{IDS}}$ reaches 52% and 71%, respectively, of the ZTC gate bias of the body contacted transistor.

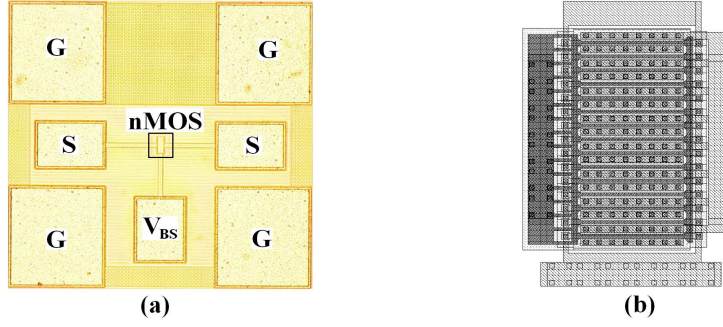


Figure 4.21: (a) Top view of a 3-port PD SOI MOSFET embedded in its RF pads, (b) core view of the device.

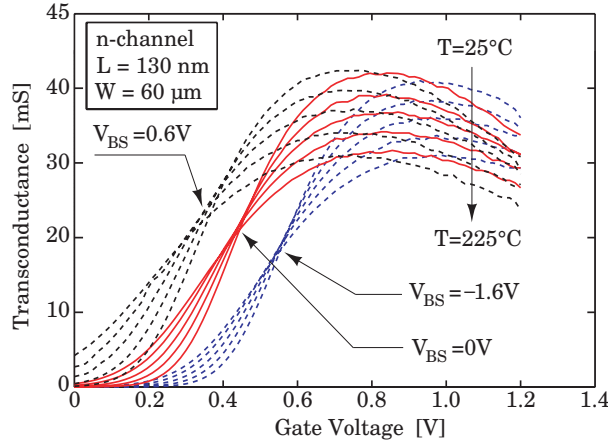


Figure 4.22: Measured $g_m - V_{GS}$ characteristic for $V_{DS} = 0.6$ V, at various temperatures and for tree bias body (V_{BS}) conditions for nMOSFET with a channel length of 130 nm and a width of $60 \mu\text{m}$.

4.3.5.3 ZTC applications

The ZTC_{gm} and ZTC_{IDS} bias points can be seen as factors of merit in analog circuit design for high temperature applications. A variety of circuit design method, can be used to improve high temperature performance of microelectronics [33]. For analog applications, the stability of the circuit performance in terms of gain, match-

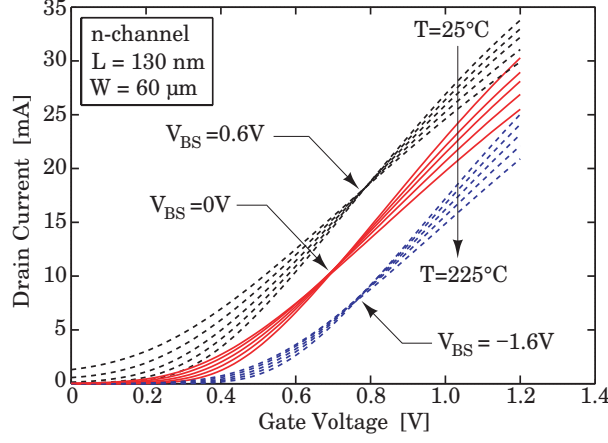


Figure 4.23: Measured $I_{DS} - V_{GS}$ characteristic for $V_{DS} = 0.6 \text{ V}$, at various temperatures and for tree bias body (V_{BS}) conditions for nMOSFET with a channel length of 130 nm and a width of 60 μm .

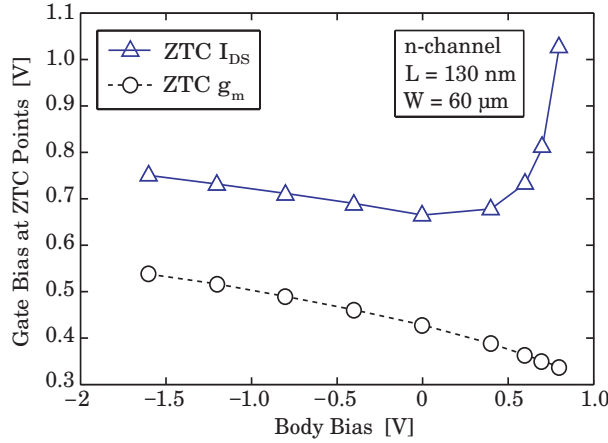


Figure 4.24: (a) Measured gate bias at transconductance ZTC (ZTC_{g_m}) and at drain current ZTC ($ZTC_{I_{DS}}$) for $V_{DS} = 0.6 \text{ V}$ with body bias (V_{BS}) for nMOSFET with a channel length of 130 nm and a width of 60 μm .

ing, bandwidth, etc. versus temperature is of first importance [34]. In operational amplifier design for example, devices used in biasing string can be biased at current ZTC points to maintain constant DC current levels While, the input devices can be biased at ZTC_{g_m} point to achieve stable circuit parameters which mainly depend on small signal parameters.

Moreover, promising perspectives are available with the possibility to bias the

body node to control the ZTC points of the transistors. This can be more interesting if we have the possibility to offer to the MOSFET an automatic control of its ZTC points by adding an internal circuit between the gate and the body nodes of the MOSFET as shown in Fig. 4.25. The internal circuit has the function to govern the ZTC points by providing different voltages according to the evolution of $V_{BS} = f(V_{GS})$. For example, if we consider the case of the ZTC_{gm} , the evolution of $V_{BS} = f(V_{GS})$ represented in Fig. 4.24 can be simply approximated by the simple linear law: $V_{BS} \approx \alpha - \beta V_{GS}$, where α and β are constant. In this case, the internal circuit can be realized by a simple analog subtractor as shown in Fig. 4.26, and which will control the ZTC_{gm} point by providing in its output the exact voltage to apply at the body node. The output of the internal analog subtractor circuit is given by

$$V_{BS} = \left(1 + \frac{R_4}{R_3}\right) \frac{R_1}{R_1 + R_2} V_{ref} - \frac{R_4}{R_3} V_{GS} \quad (4.38)$$

However, the ZTC auto-bias have some inconvenients, such as the complexity, the power consumption (internal circuit) and the size area of the internal circuit implementation. That solution will be of interest when the control circuit of the V_{BS} will apply to a certain number of MOSFETs.

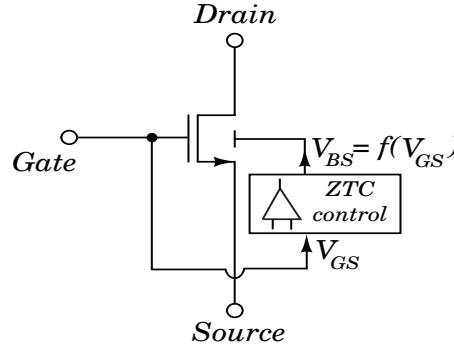


Figure 4.25: Auto-ZTC alternative implementation with auto-DC biasing of the body node.

4.3.5.4 Conclusion

The SOI MOSFET characteristics in saturation and linear region have an optional ZTC point for which the temperature mobility reduction compensates the threshold voltage shift. The ZTC point in SOI MOSFETs is valid up to 300°C due to the suppression of leakage currents by the insulating layer between the body and sub-

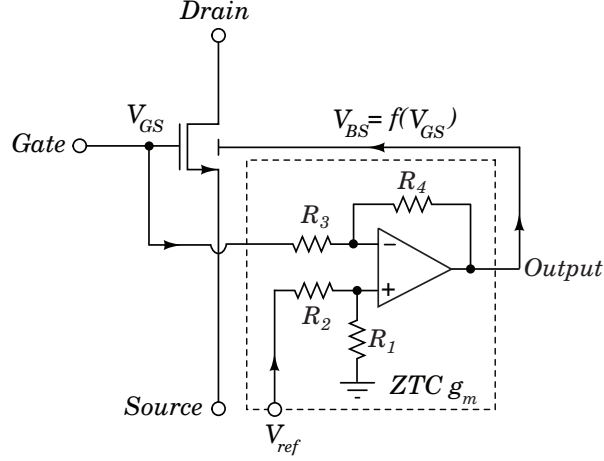


Figure 4.26: Auto- ZTC_{g_m} alternative implementation with internal auto-DC bias circuit using a simple analog subtractor.

strate. Moreover, thanks to a small junction area and the absence of diffusion leakage toward the substrate, the measured junction leakage current is remarkably smaller in SOI technology. Working at high temperature ameliorates the FBE, and the floating body transistor can be more appropriately used for applications operating in a high temperature environment. The SOI CMOS technology is now a mature technology for the realization of high-temperature integrated circuits. The temperature dependency of the body contacted n-channel transistors are more sensitive than that of the floating body nMOSFETs.

4.4 Microwave characterization at high temperature

4.4.1 Introduction

In the past decades, great efforts have been devoted to the modeling, optimization and design of the MOSFET devices on silicon and GaAs substrates [35] [4]. However, no systematic study of the performance trend of integrated MOSFETs with temperature has been reported in the literature. The high frequency models of MOSFETs devices are usually of two kinds: the polynomial and physical models. The polynomial models are extracted from measurement. They describe the behavior of devices, as black boxes and are easily introduced in simulators. The physical small signal equivalent circuits are composed of elements representing each physical phenomena [5]. A small signal equivalent circuit based on the device physics is proposed in this section, in order to model the behavior of common source n-channel PD MOSFET at high

frequencies. In this analysis the intrinsic and extrinsic elements of the device are presented for various temperature conditions.

4.4.2 Small signal model for the SOI MOSFET

The small signal equivalent circuit of common source PD MOSFET is presented in Fig. 4.27. It is composed of two part: intrinsic and extrinsic. The intrinsic elements are a simplified representation of the physical phenomena, that occur inside the transistor channel. The extrinsic elements are associated with the geometry of external connexions and accesses.

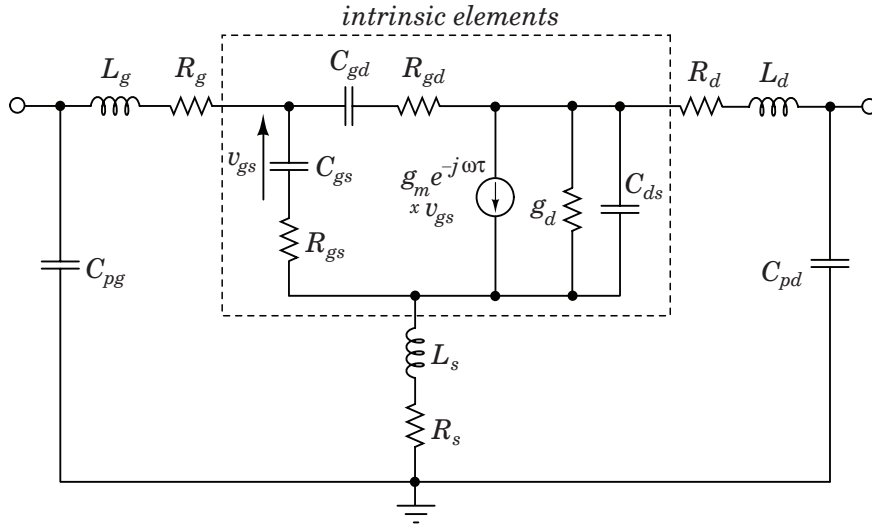


Figure 4.27: The non-quasi-static small signal equivalent circuit of a common source MOSFET.

4.4.2.1 Intrinsic elements

As explained in various works [4] [5] [35] [36], the intrinsic elements are bias dependent and are related to variations of charges or currents when a small signal is applied on the device. The definitions of the intrinsic gate-source (C_{gs}), gate-drain (C_{gd}) and drain-source (C_{ds}) capacitances are given by:

$$C_{gs} = - \left[\frac{\partial Q_g(V_{gs}, V_{ds})}{\partial V_{gs}} \right]_{V_{ds}=cst} \quad (4.39)$$

$$C_{gd} = - \left[\frac{\partial Q_g (V_{gs}, V_{ds})}{\partial V_{ds}} \right]_{V_{gs}=cst} \quad (4.40)$$

$$C_{ds} = - \left[\frac{\partial Q_d (V_{gs}, V_{ds})}{\partial V_{gs}} \right]_{V_{gs}=cst} \quad (4.41)$$

The definitions of the output conductance (g_d), which models the imperfect current sources and of the gate transconductance (g_m) are given by:

$$g_d = \left[\frac{\partial I_{ds} (V_{ds}, V_{ds})}{\partial V_{ds}} \right]_{V_{gs}=cst} = \left[\frac{\partial i_{ds}}{\partial v_{ds}} \right]_{v_{gs}=0} \quad (4.42)$$

$$g_m = \left[\frac{\partial I_{ds} (V_{gs}, V_{ds})}{\partial V_{gs}} \right]_{V_{ds}=cst} = \left[\frac{\partial i_{ds}}{\partial v_{gs}} \right]_{v_{ds}=0} \quad (4.43)$$

The non-quasi-static effects are modeled by introducing intrinsic resistances R_{gs} and R_{gd} in series with each intrinsic capacitances C_{gs} and C_{gd} , and a time delay τ affecting the transconductance. The intrinsic elements depend on the device dimension and on the applied bias.

4.4.2.2 Extrinsic elements

The geometry of the MOSFET induces some parasitic elements, surrounding the active part of the device. The gate, source and drain of the MOSFET are connected to the outside world by gate, source and drain fingers. These fingers having a given resistivity, they are distributed resistances and modeled by equivalent resistances R_g , R_s and R_d connected to the gate, the source, and the drain respectively as shows the Fig. 4.27. The resistances R_s and R_d include the metallic losses and the contact resistances between the metal and the source and drain implants. They are proportional to the inverse of the transistor width. The resistance R_g includes the resistance of the gate fingers, which is proportional to the transistor width. In most of the cases, this resistance is much higher than the R_s and R_d . Using the same approach, parasitic inductances can be defined. They are named L_g , L_d and L_s in the small signal model (Fig. 4.27). For sub-micron MOSFETs, these inductances are usually a few pico-Henry and are nearly negligible within the frequency band of operation. The extrinsic resistances and inductances are bias independent. Finally, the parasitic effects of the interconnections of the gate and drain are usually modeled by

two capacitances and are bias and size independent. These two elements are modeled in the small signal model (Fig. 4.27) by the capacitance C_{pg} and C_{pd} [35] [4] [37].

4.4.3 Extraction of the small signal model parameters

The extraction of the small signal parameters for different temperature conditions will be presented in this section. After a brief presentation of the extraction methodology, measurements of the intrinsic and extrinsic elements of the floating body and body contacted MOSFETs performed for a large temperature range from 25 to 250°C are compared.

4.4.3.1 Extrinsic parameters

The extraction of the interconnections parasitic capacitances of the gate and drain C_{pg} and C_{pd} are achieved by biasing the gate of the devices (V_{GS}) below the threshold voltage ($V_{GS} \ll V_{TH}$), for $V_{DS} = 0$ V. In this case, most intrinsic parameters of the device are neglected. The equivalent circuit of the MOSFET under these bias conditions is shown in Fig. 4.28. Considering the MOSFET as a symmetrical structure ($C_{gs} \approx C_{gd}$) and neglecting the drain-source capacitance C_{ds} , the access capacitances can be deduced from the measured Y-parameters as [38] [5]:

$$C_{pg} = \frac{1}{\omega} \cdot \Im m(Y_{11} + 2 \cdot Y_{12}) \quad (4.44)$$

$$C_{pd} = \frac{1}{\omega} \cdot \Im m(Y_{22} + Y_{12}) \quad (4.45)$$

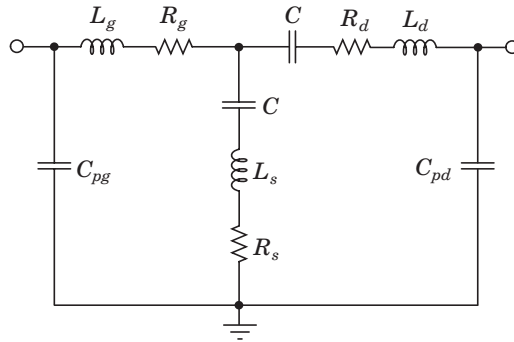


Figure 4.28: Simplified small signal equivalent circuit of MOSFET for $V_{DS} = 0$ V and $V_{GS} \ll V_{TH}$.

The access capacitances deduced from the measurement for two temperature conditions are shown in Fig. 4.29. A slight increase of the access capacitances with temperature is noticed. The extracted values of the extrinsic capacitances C_{pg} and C_{pd} are equal to 4 fF and 20 fF, respectively for the floating body and 11 fF and 30 fF, respectively for the body contacted MOSFET. The temperature variation does not impact the dielectrics and the small temperature dependence of C_{pg} and C_{pd} is probably due to the geometrical variation of DUT at high temperature (expansion of the tested devices with temperature).

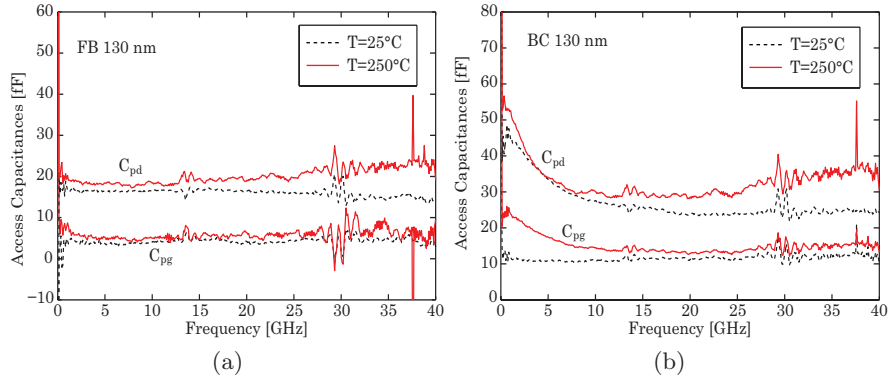


Figure 4.29: Extraction of access capacitance in, (a) FB and (b) BC SOI nMOSFET with a channel length of 130 nm and a total width of 60 μm for $T = 25^\circ\text{C}$ and 250°C at $V_{DS} = 0\text{ V}$ and $V_{GS} = -2\text{ V}$.

The extraction of the extrinsic resistances R_g , R_d and R_s was performed using the method proposed by Bracale [39]. The resistances are extracted in cold-FET conditions ($V_{DS} = 0\text{ V}$) and in strong inversion ($V_{GS} \gg V_{TH}$). Several measurements of the MOSFET with different gate voltage conditions are required. Considering that the MOSFET is working in the linear region, its equivalent circuit is simplified (Fig. 4.30). From this simplified equivalent model and considering the MOSFET as a symmetrical structure ($C_{gs} \approx C_{gd}$), the Z-parameters can be approximated by:

$$\Re(Z_{12}) \approx R_s + \frac{1}{2g_d} \quad (4.46)$$

$$\Re(Z_{11} - Z_{12}) \approx R_g - \frac{1}{4g_d} \quad (4.47)$$

$$\Re(Z_{22} - Z_{12}) \approx R_d + \frac{1}{2g_d} \quad (4.48)$$

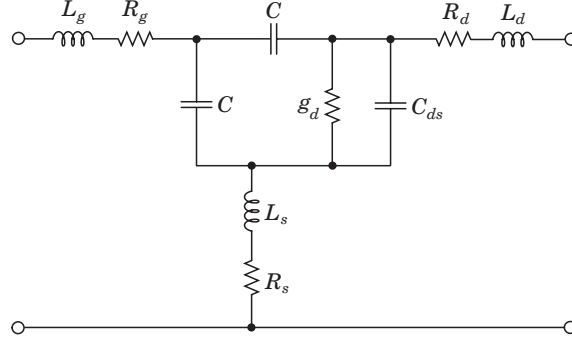


Figure 4.30: Simplified small signal equivalent circuit of MOSFET when $V_{DS} = 0$ V and $V_{GS} \gg V_{TH}$.

In the linear region, the output conductance of a MOSFET is proportional to the gate voltage and is given by:

$$g_d = \frac{\mu W C_{ox}}{L_g (1 + \alpha)} (V_{GS} - V_{TH}) \quad (4.49)$$

The real part of Z-parameters are proportional to $1/(V_{GS} - V_{TH})$ and are given by:

$$\Re(Z_{12}) \approx R_s + \frac{1}{2K (V_{GS} - V_{TH})} \quad (4.50)$$

$$\Re(Z_{11} - Z_{12}) \approx R_g - \frac{1}{4K (V_{GS} - V_{TH})} \quad (4.51)$$

$$\Re(Z_{22} - Z_{12}) \approx R_d + \frac{1}{2K (V_{GS} - V_{TH})} \quad (4.52)$$

where the coefficient K is equal to $\frac{\mu W C_{ox}}{L_g (1 + \alpha)}$. The extrinsic resistances are extracted using linear regressions of the real part of Z-parameters versus $1/(V_{GS} - V_{TH})$.

Note that the best results are obtained with Bracale's method when the extraction

is made for high values of V_{GS} (at least twice as big as the threshold voltage) [5].

The extraction results of the extrinsic resistances versus temperature are shown in Fig. 4.31. Minor temperature impact on extrinsic resistances is noticed. In a first approximation, it is possible to neglect the influence of the temperature on the extrinsic parameters of the MOSFET small signal model.

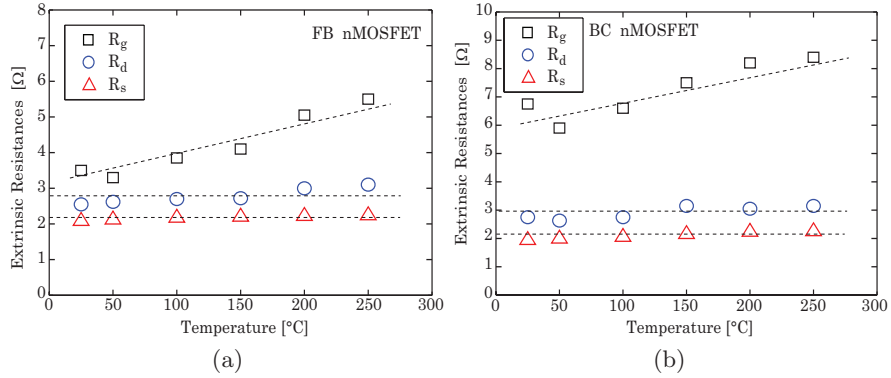


Figure 4.31: Extraction results of the extrinsic resistances versus temperature for, (a) FB and (b) BC SOI nMOSFET with a channel length of 130 nm and a width of 60 μm .

4.4.3.2 Intrinsic parameters

In this section the extraction of the intrinsic parameters of the small signal equivalent circuit shown in Fig. 4.27 is presented.

After the extraction of the extrinsic parameters, the intrinsic part of the device can be identified. The intrinsic Y-parameters (Y_i) of the MOSFET are given by [4] [35]:

$$[Y_i] = \begin{bmatrix} Y_{11i} & Y_{12i} \\ Y_{21i} & Y_{22i} \end{bmatrix} \quad (4.53)$$

$$= \begin{bmatrix} j\omega \left(\frac{C_{gs}}{1+j\omega R_{gs}C_{gs}} + \frac{C_{gd}}{1+j\omega R_{gd}C_{gd}} \right) & -j\omega \frac{C_{gd}}{1+j\omega R_{gd}C_{gd}} \\ \frac{g_m \exp(j\omega\tau)}{1+j\omega R_{gs}C_{gs}} - j\omega \frac{C_{gd}}{1+j\omega R_{gd}C_{gd}} & g_d + j\omega \left(C_{ds} + \frac{C_{gd}}{1+j\omega R_{gd}C_{gd}} \right) \end{bmatrix} \quad (4.54)$$

From Y_i , the values of intrinsic parameters are given by:

$$g_m = - \left| \frac{Y_{21i} - Y_{12i}}{Y_{11i} + Y_{12i}} \right| \frac{1}{\Im \left[\frac{1}{Y_{11i} + Y_{12i}} \right]} \quad (4.55)$$

$$g_d = \Re[Y_{22i} + Y_{12i}] \quad (4.56)$$

$$C_{gs} = -\frac{1}{\omega} \Im \left[\frac{1}{Y_{11i} + Y_{12i}} \right] \quad (4.57)$$

$$C_{gd} = \frac{1}{\omega \Im \left[\frac{1}{Y_{12i}} \right]} \quad (4.58)$$

$$C_{ds} = \frac{\Im[Y_{22i} + Y_{12i}]}{\omega} \quad (4.59)$$

$$R_{gd} = -\Re \left[\frac{1}{Y_{12i}} \right] \quad (4.60)$$

$$R_{gs} = \Re \left[\frac{1}{Y_{11i} + Y_{12i}} \right] \quad (4.61)$$

$$\tau = \frac{1}{\omega} \arctan \left[\frac{\Im \{(Y_{21i} - Y_{12i}) / (1 + j\omega R_{gs} C_{gs})\}}{\Re \{(Y_{21i} - Y_{12i}) / (1 + j\omega R_{gs} C_{gs})\}} \right] \quad (4.62)$$

The extracted intrinsic parameters are shown in Fig. 4.32 for different temperature conditions. The extracted capacitances show a slight dependence on temperature. The FB MOSFET shows lower C_{gs} values than the BC transistor, which explains the higher cutoff frequency of FB with respect to BC MOSFETs. Due to the connection between the body and the source which adds a considerable parasitic capacitance, the BC transistor shows a higher drain-source capacitance C_{ds} (about 36%) than in the case of the FB transistor. The intrinsic resistance R_{gs} shows a small variation with temperature for the two devices. The intrinsic resistances R_{gs} and R_{gd} show nearly constant values with temperature for the two devices, but R_{gd} looks incorrect with negative values.

As expected the transconductance g_m of the FB and BC devices decreases when

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temperature increases. This is because the transconductance depends on the choice of the gate bias and in our case, the transconductance was extracted in saturation region and for $V_{GS} = 1\text{ V}$, bias point for which g_m exhibits a temperature degradation about 25% in DC. However, the temperature degradation of g_m can be minimized by fixing the gate voltage close the g_m ZTC point. Finally, Table 4.3 summarizes the temperature dependence of the intrinsic parameters, the transconductance and the output conductance. This two last elements present a high dependence with respect to temperature. This is because they depend on the drain current which is highly influenced by temperature.

	C_{gs}	C_{gd}	C_{ds}	g_m	g_d	R_{gd}	R_{gs}
ϵ_{FB}	5%	7%	10%	15.2%	22.4%	33%	25%
ϵ_{BC}	5.4%	8%	9.4%	27%	11%	—	28%

Table 4.3: Temperature degradation of intrinsic parameters of the small signal SOI MOSFET.

4.4.4 Cut-off frequencies

The most important factor of merit of MOSFETs at microwave frequencies is the current gain ($|H_{21}|$), which is given by:

$$|H_{21}| = \frac{|Y_{21}|}{|Y_{11}|} \quad (4.63)$$

This current gain has some interesting properties as it is independent of the extrinsic resistance of the MOSFET. However, the current gain is extracted from the measured S-parameters when the output termination of the device is a short circuit and this factor is therefore not representative of the power gain that can be expected.

For this reason the Maximum Available Gain (MAG) is more often used. It is defined as the maximum power gain that can be extracted from a given transistor. According to power transfer theory, it is obtained under conjugate matching conditions at both input and output ports of the device. The MAG can be written in terms of the device S-parameters as:

$$\left| \frac{S_{21}}{S_{11}} \right|^2 \left(k - \sqrt{k^2 - 1} \right) \quad (4.64)$$

where k is Rollet's stability factor of transistors defined by:

$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2 |S_{12}| |S_{21}|} \quad (4.65)$$

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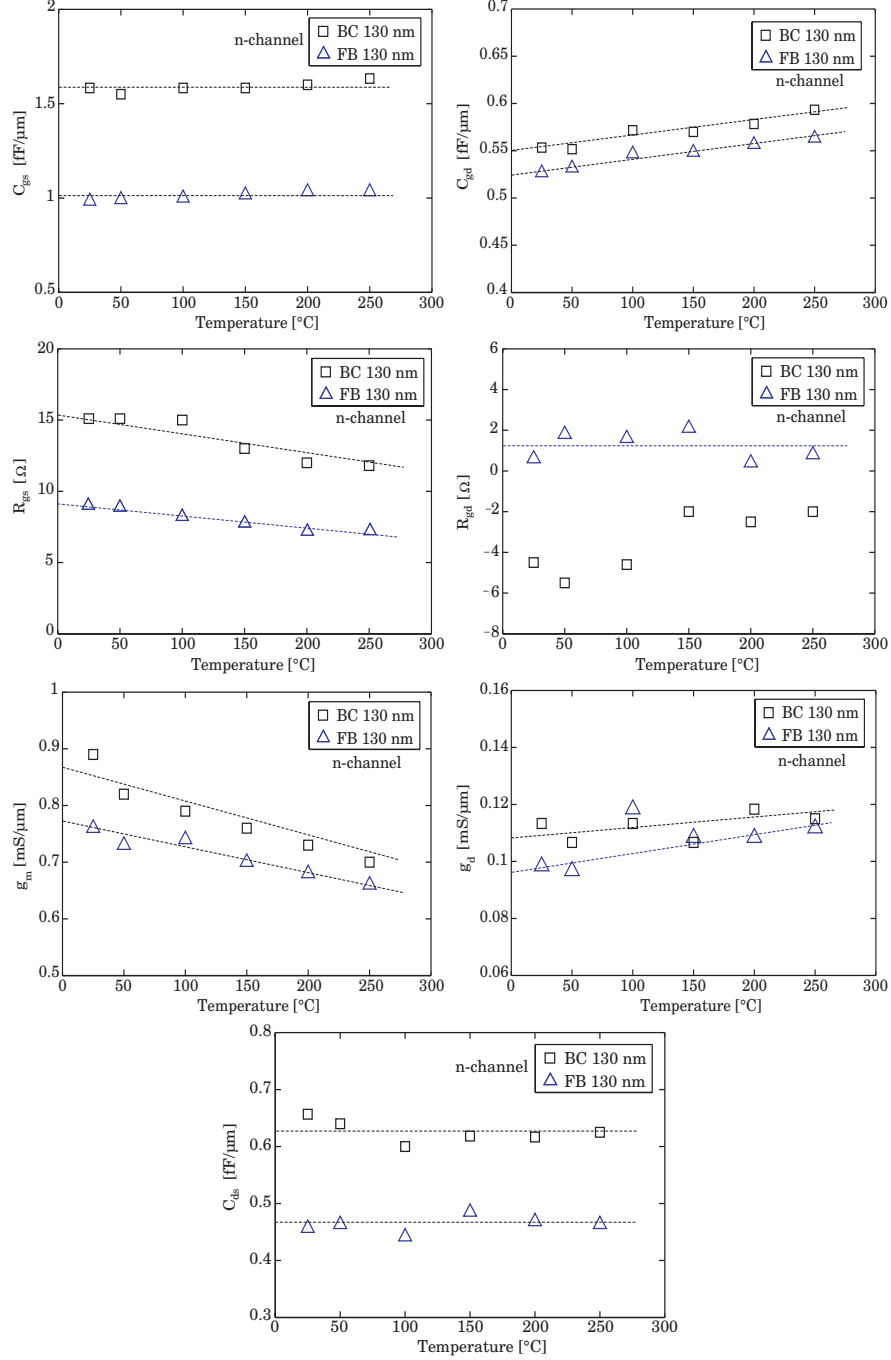


Figure 4.32: Temperature dependence of the intrinsic parameters for floating-fody and body-contacted n-channel MOSEFTs SOI with a channel length of 130 nm at $V_{DS} = 1.2$ V and $V_{GS} = 0.8$ V.

with $\Delta = S_{11}S_{22} - S_{21}S_{12}$. The maximum available gain definition is only valid in the case of a stable device.

Another important definition is the unilateral gain (ULG) which is defined as the maximal available gain of a device when the stability is ensured by using a lossless feedback network to cancel the reverse transmission of the device. This gain is defined as:

$$ULG = \frac{1}{2} \frac{\left| \frac{S_{21}}{S_{12}} - 1 \right|^2}{k \left| \frac{S_{21}}{S_{12}} \right| - \Re \left(\frac{S_{21}}{S_{12}} \right)} \quad (4.66)$$

From the different gain expressions defined above, it is possible to introduce two important figures-of-merit: the cut-off frequency of the current gain (f_T) and the cut-off frequency of the maximum power gain, also referred to as the maximum oscillation frequency (f_{MAX}).

f_T is extracted from current gain and defined as the frequency for which $|H_{21}|$ becomes equal to unity or 0 dB. Considering the simplified small signal equivalent circuit presented in Fig. 4.33, f_T can be approximated by the following relation:

$$f_T \approx \frac{g_m}{C_{gs} + C_{gd}} \quad (4.67)$$

Note that f_T is only dependent on the intrinsic parameters of the MOSFET. It is then an important factor to compare different technologies and devices.

The maximum frequency of oscillation f_{MAX} is defined as the frequency for which the gain ULG becomes equal to unity and can be approximated, from the simplified small signal equivalent circuit, by the following relation [9]:

$$f_{MAX} \approx \frac{f_T}{2\sqrt{2\pi f_T R_g C_{gd} + g_d(R_g + R_s + R_{gs})}} \quad (4.68)$$

Fig. 4.34 shows the measurement of $|H_{21}|$ for the three conventional SOI transistors (FB, BC and DT) with a channel length of 130 nm and a width of 60 μm at room temperature. Thanks to the lower parasitic capacitance, the floating body MOSFETs exhibit a higher $|H_{21}|$. The contact added between the gate and the source in BC MOSFETs, increases the gate-source capacitance when compared to FB transistors.

The f_T of the three conventional SOI nMOSFETs versus drain-current and for $T = 25^\circ\text{C}$ and 250°C are shown in Fig. 4.35. The f_{max} of the studied devices is shown in Fig. 4.36. As expected it is clear that the FB transistor shows much higher

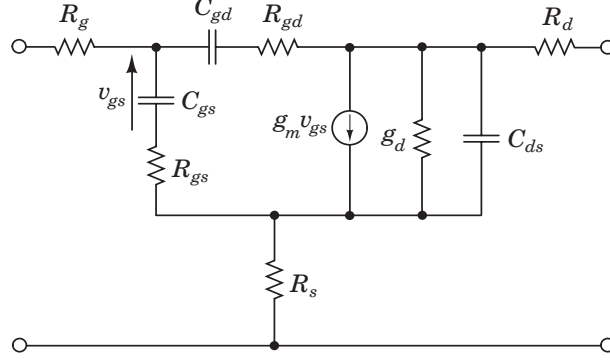


Figure 4.33: Simplified small signal equivalent circuit of common source MOSFET.

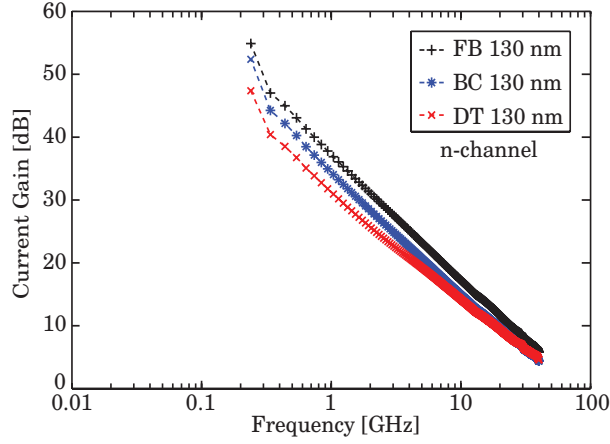


Figure 4.34: Measured $|H_{21}|$ for the three conventional SOI (FB, BC and DT) nMOSFETs with a channel length of 130 nm and a width of 60 μm , at room temperature and in saturation ($V_{DS} = 1.2 \text{ V}$ and $V_{GS} = 1.0 \text{ V}$).

f_T and f_{max} than the other transistors due its higher current gain. It can be seen that the temperature degradation of the current gain cut-off frequencies is due to the decrease of the transconductance g_m with the temperature in the saturation region.

4.5 Conclusion

In this chapter we investigated temperature behavior of the three conventional SOI transistors in both DC and RF domain. The main figures of merit in the DC regime as well as in the RF regime, besides the extraction of the equivalent circuit extrinsic and intrinsic parameters, have been shown.

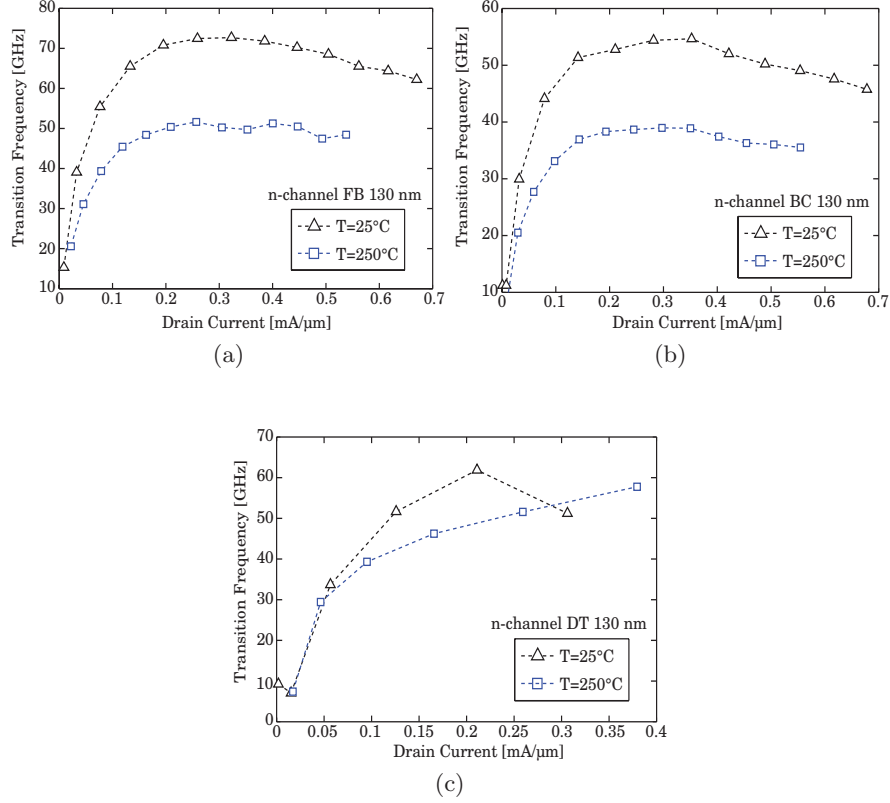


Figure 4.35: Measured f_T for, (a) FB, (b) BC and (c) DT SOI nMOSFETs with a channel length of 130 nm and a width of 60 μm, versus drain-current, for $T = 25^\circ\text{C}$ and 250°C ($V_{DS} = 1.2\text{ V}$ and $V_{GS} = 1.0\text{ V}$).

A superiority of body tied transistors (body-contacted and dynamic threshold devices) over floating body transistors is shown for some figures of merit, such as leakage current and I_{ON}/I_{OFF} ratio, while some other parameters show the superiority of floating body transistors, such as the cut-off frequency. Moreover, the main inconvenient of the floating body devices such as the floating body effect (FBE), which is known to play a critical role in partially depleted SOI and is less pronounced at high temperature. Without kink effect which constitutes the main drawback of the FB transistor, it seems that the FB SOI transistor can be more appropriate for applications operating in an environment of high temperature.

A high temperature degradation of the g_m/I_{DS} ratio is observed, reaching about 50% between room temperature and 250°C in weak inversion, for the three studied devices. However, this temperature degradation of the g_m/I_{DS} ratio can be minimized

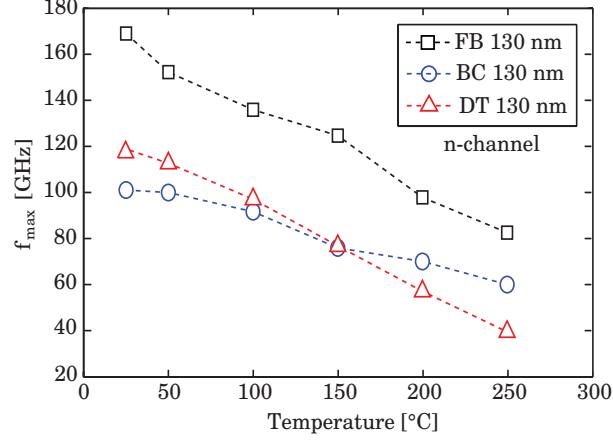


Figure 4.36: Measured f_T for the three conventional SOI nMOSFETs with a channel length of 130 nm and a width of 60 μm , versus temperature and in saturation ($V_{DS} = 1.2\text{ V}$ and $V_{GS} = 1.0\text{ V}$).

by biasing the devices in strong inversion.

Finally, the extrinsic and intrinsic parameters of the small signal equivalent model are extracted in a large temperature range (25 to 250°C). As expected, only the parameters which theoretically are dependent on the drain current (thus on the mobility and the threshold voltage), show a dependence on temperature.

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CHAPTER 5

EXAMPLE OF RF APPLICATION: 2.45-GHZ LNA DESIGN

5.1 Introduction

With advancement in state-of-the-art electronic systems and a huge demand for low-cost high-speed mixed-signal integrated systems, a considerable effort has recently been made to migrate several high-frequency elementary circuit blocks from GaAs to CMOS Silicon process. Since CMOS Silicon-on-Insulator (SOI) devices present a very good high frequency behavior and a low power consumption, it is of great interest to use them in RF circuit design [1]. Recently, many designs of different RF blocs such as LNA, VCO, Mixer have demonstrated the interest of this technology for low-voltage and low-power applications.

Power consumption is a major concern for high-performance digital systems and portable applications. The most efficient technological approach for reducing power consumption is power-supply voltage (V_{DD}) scaling. For this purpose SOI devices bring their unique inherent advantages over bulk devices: lower junction capacitance, lower junction leakage, no latch-up and full dielectric isolation [1].

As an example, the emerging IEEE 802.15.4 standard (ZigBee) in the 2.45 – 2.48 GHz frequency band is specially intended for low cost and low-power applications. The use of CMOS SOI technology to implement the front end in the ZigBee standard is therefore attractive because of the promise of integrating the whole system on a single chip which reduces considerably the power-consumption and the cost of the fabrication.

In a typical radio receiver, the low-noise amplifier (LNA) is one of the key components, as it is the critical element impacting the sensitivity of the receiver. The LNA design involves a trade off between noise figure (NF), gain, linearity, impedance matching, and power dissipation. Usually, the main goal of the LNA design is to achieve simultaneous low noise and input matching for a given power dissipation.

In order to provide some temperature performances of the RF CMOS SOI technology, a LNA design is proposed in this chapter as an example of RF applications. This chapter is structured as follows: a brief presentation of the basic noise characteristics in the MOSFET devices followed by the presentation of some classical LNA topologies. A LNA design using the inductive source degeneration topology is presented and measurement results are discussed. Finally, the importance of the circuit

protection against Electrostatic Discharges (ESD) is highlighted and a protected LNA is presented as example of ESD strategy protection.

5.2 Noise Figure

An important measurement of system noise performance is a parameter known as the noise factor (F) or the Noise Figure (NF) in dB. The noise figure parameter has been introduced in the 1940's by Friis [2]. The noise factor F is defined as the noise figure of a network, being the ratio of the signal-to-noise power ratio at the input to the signal-to-noise power ratio at the output:

$$F \triangleq \frac{(S/N)_{in}}{(S/N)_{out}} \quad (5.1)$$

A perfectly noise-free circuit would maintain the same signal-to-noise ratio at its input and output, and the noise factor would be equal to the unity ($F=1$ or $NF=0$ dB). However, in practice the circuit adds extra noise from its own components and degrades the signal-to-noise ratio. Therefore a low noise figure means that little noise is added by the circuit. An other important definition of the noise factor is given by:

$$F \triangleq \frac{\text{Total output noise}}{\text{Output noise due to the source}} \quad (5.2)$$

In a radio receiver, where the RF function blocks are cascaded (Fig. 5.1), the first stage has the biggest impact on the overall noise factor. It is so because the contribution of the excess noise of the following stages is attenuated by the combined gain of all the preceding stages. This is easily seen from the well-known Friis formula for the noise factor F of a cascaded system [2]:

$$F = 1 + \sum_{k=1}^n \frac{F_k - 1}{\prod_{i=1}^{k-1} G_i} \quad (5.3)$$

where F_k and G_i represent the noise factor and the gain of the k^{th} and i^{th} block in the receiver diagram, respectively.

Therefore, the first stage after the antenna is typically a low noise amplifier (LNA) with a minimum noise factor and a maximum gain. Sometimes, the LNA is preceded by a passive off-chip filter for image rejection in a heterodyne receiver or to attenuate strong signals in frequency bands nearby. The presence of such a filter often requires an additional constraint to be imposed on the LNA by limiting the input reflection

coefficient of the LNA.

The general requirements for a LNA are: a low noise contribution, a high linearity, a sufficiently high gain and a low power consumption. The degrees of freedom available to a designer are: the choice of the topology, the technology, the dimensioning of the active devices (usually the gate width and the bias point) and the value of the source impedance. The last point generally requires an input matching network if a limit is imposed on the reflection coefficients, as the source impedances are generally imposed. The output impedance is generally matched to 50Ω and necessitates an output matching network.

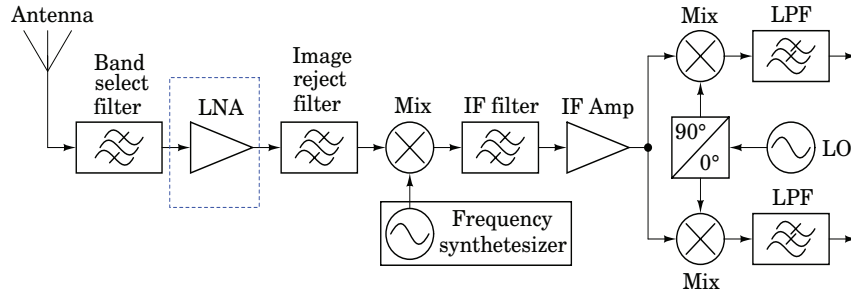


Figure 5.1: Bloc diagram of a RF receiver: place of the LNA.

5.2.1 High frequency noise sources in MOSFETs

In MOSFETs operating at RF frequencies, the $1/f$ -noise can often be neglected. There are two more important noise sources which are the channel thermal noise and the induced gate noise, also called the non-quasi-static gate noise.

The thermal noise in MOSFETs is due to the random thermal agitation of the carriers in the inversion layer. When one assumes that the total inversion layer charge, Q , does not change, this noise can be modeled as a current source between drain and source. The mean value of the square of this current is given by [3]:

$$\overline{i_{n,d}^2} = 4k_B T \frac{\mu}{L_g^2} (-Q) \Delta f \quad (5.4)$$

where μ is the carrier mobility and L_g the channel length. For a long channel devices, this reduces to

$$\overline{i_{n,d}^2} = 4k_B T \gamma g_{d0} \Delta f \quad (5.5)$$

where g_{d0} is the zero-bias drain conductance of the device, while γ is the thermal noise coefficient. The theoretical long-channel value of γ is $\frac{2}{3}$ when the device is operated in the saturation region and increases to 1 in the linear region [4]. For short channel devices it can be as large as 2 or 3 [5] [6]. In the case of short channel devices, the drain noise current is somewhat larger because of the channel length modulation and the presence of “hot” electrons. The channel length modulation is due to the reduction in the effective channel length as the drain depletion region extends into the channel when the drain bias exceeds the saturation drain voltage. The hot electrons are due to high electric fields at the drain: electrons may be left with a significantly higher temperature than the surrounding lattice structure. In order to minimize the short channel effects, the drain-source bias has to be kept as close as possible to saturation drain voltage.

The induced gate current noise is thermal noise that is induced by local fluctuations in the channel via capacitive coupling through the gate oxide. This noise is proportional to f^2 , owing to the ωC dependence, and dominates noise performance of MOSFETs at high frequencies, while drain noise is frequency independent (white noise). The drain and induced gate noise currents are not necessarily the same even if some correlation exists. The induced gate noise current is given by [3] [6]:

$$\overline{i_{n,g}^2} = 4k_B T \delta \frac{(\omega C_{gs})^2}{5g_{d0}} \Delta f \quad (5.6)$$

where δ is the gate noise coefficient. The theoretical long-channel value of δ is $\frac{4}{3}$. Like γ , the value of δ also increases in short channel devices and at high V_{GS} and V_{DS} .

Since both noise currents originate in the same physical noise source, namely the thermal channel noise, it is clear that they are at least partially correlated. The correlation coefficient c is defined as follows [3]:

$$c = \frac{\overline{i_{n,g} \cdot i_{n,d}^*}}{\sqrt{\overline{i_{n,g}^2} \cdot \overline{i_{n,d}^2}}} \quad (5.7)$$

The theoretical long-channel value of c is $c = 0.395j$. The value of c is purely imaginary, reflecting the capacitive coupling between the channel and gate-induced noise sources.

An additional noise source in MOSFET devices is the noise generated by the distributed gate resistance [7]. This noise source is modeled by a resistance in series with the capacitance C_{gs} between gate and source, as shown in Fig. 5.2. The mathematical

expression for this intrinsic channel resistance is approximatively given by [3]:

$$R_{gs} = \frac{1}{5g_{d0}} \quad (5.8)$$

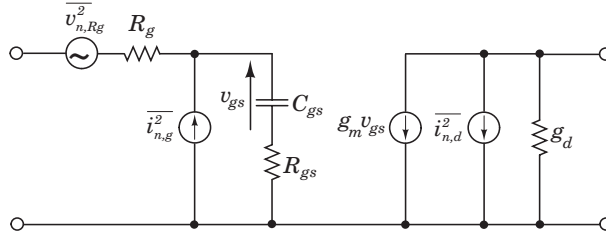


Figure 5.2: Simple MOSFET noise model.

5.2.2 The four noise parameters of MOSFETs

The noise factor of a system is not only determined by noise sources inside of the system but also determined by the source admittance driving the system. Classical two port noise theory yields the following expression for the noise factor:

$$F = 1 + \frac{G_u}{G_s} + \frac{R_n}{G_s} [(G_s + G_c)^2 + (B_s + B_c)^2] \quad (5.9)$$

where the parameters R_n , G_u , G_c and B_c are the parameters of an equivalent “noisy” network (Fig. 5.3). These parameters represent all internal noise sources referred to the input, in terms of the terminal current and voltage observed at the output. R_n is the equivalent noise resistance of the series voltage source, G_u is the equivalent noise admittance of the uncorrelated shunt current source, and $Y_c = G_c + jB_c$ is the correlation admittance relating the series voltage source with a fully correlated shunt current source.

The noise parameters of the MOSFET are investigated in many works [8], they are summarized in the Table 5.1.

5.3 Classical LNA topologies

In this section the classical LNA topologies are briefly presented. The selection of topologies to be discussed has been made with the criterion that the real part of their

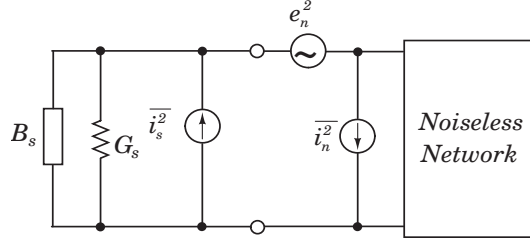


Figure 5.3: Equivalent circuit with internal noise source referred to input.

R_n	$\frac{\gamma}{\alpha} \frac{1}{g_m}$
G_{opt}	$\alpha \omega C_{gs} \sqrt{\frac{\delta}{5\gamma}} (1 - c ^2)$
B_{opt}	$-\omega C_{gs} \left(1 + \alpha c \sqrt{\frac{\delta}{5\gamma}}\right)$
F_{min}	$1 + \frac{2}{\sqrt{5}} \frac{\omega}{\omega_T} \sqrt{\gamma \delta (1 - c ^2)}$

Table 5.1: Noise parameters of the MOSFT.

input impedance can easily and directly be matched to real source impedance (here 50Ω) without the need for an extra, complete matching network [9] [10].

The resistive termination configuration is shown in Fig. 5.4(a). This topology simply uses a resistance across the input of a common source amplifier to achieve the required real part of the input admittance. The imaginary part due to the gate capacitance ($j\omega C_{gs}$) is usually much smaller than the real part ($1/R_s$). Therefore, this topology offers a very good source matching in a large frequency band. Its main drawback is the extra noise generated by the resistance itself, which is directly presented to the amplifier's input.

The second topology shown in Fig. 5.4(b) uses a common gate configuration MOSFET. This topology provides a good insulation between the input and output when compared to the common source topology. In order to match the input to 50Ω , the device transconductance g_m has to be set to $1/50\Omega$. The minimum noise figure in this configuration tends to be around 3 dB theoretically and greater in practice.

The third topology in Fig. 5.4(c) is the so called shunt-series feedback amplifier. This topology provides a good broadband match and does not exhibit the same drawback as the resistive termination configuration. Even if the resistive feed back network still generates noise, its noise will be lower as it does not present a noisy

attenuator directly at the amplifier's input. However, this architecture has a high power dissipation when compared to others. The high power dissipation is partially due to the fact that such amplifiers are naturally broadband, and hence techniques which reduce the power consumption through LC tuning are not applicable.

The last topology shown in Fig. 5.4(d) employs inductive source degeneration in order to generate a real term at the input impedance Z_{in} . With this architecture, it is possible to achieve a low noise under low consumption, for narrow-band applications [11]. The source inductor L_s provides the real part of the input impedance when the gate inductor L_g provides the desired band [12] [13]. This architecture gives an excellent input matching and the noise performance, are much better than the previous topologies because the real term of the input impedance is not due to any resistive component, which always generates noise.

Each of the presented topologies may be used in a single-ended form, or a differential form. Differential architectures require the use of a balun to transform the single-ended signal into a differential signal. Practical baluns introduce extra losses which add directly to the noise figure of the system, so usually single-ended architectures are preferred.

5.4 Design of a Low Noise Amplifier

In this section, a fully integrated Low-Noise Amplifier (LNA) is designed for low-power and narrow-band applications. It uses a cascode inductive source degeneration topology and is fabricated in a 130 nm CMOS SOI technology.

5.4.1 Topology of the LNA

The cascode inductive source degeneration topology was adopted for the design of the LNA. It allows a good trade-off between the input matching and the noise figure. The cascode configuration allows a good stability by achieving good insulation between the output and the input and reducing the Miller effect. The topology of the cascode inductive source degeneration is represented in Fig. 5.5.

5.4.2 Input matching technique

The small signal equivalent circuit seen at the input of the LNA is shown in Fig. 5.6. The input stage M_1 is followed by a cascode transistor M_2 in order to provide a sufficient reverse insulation and a reduction of the Miller effect on the gate of M_1 . In this case the impact of the gate-drain capacitance C_{gd} can be neglected. For simplicity of the formulas, a simple quasi-static model has been considered.

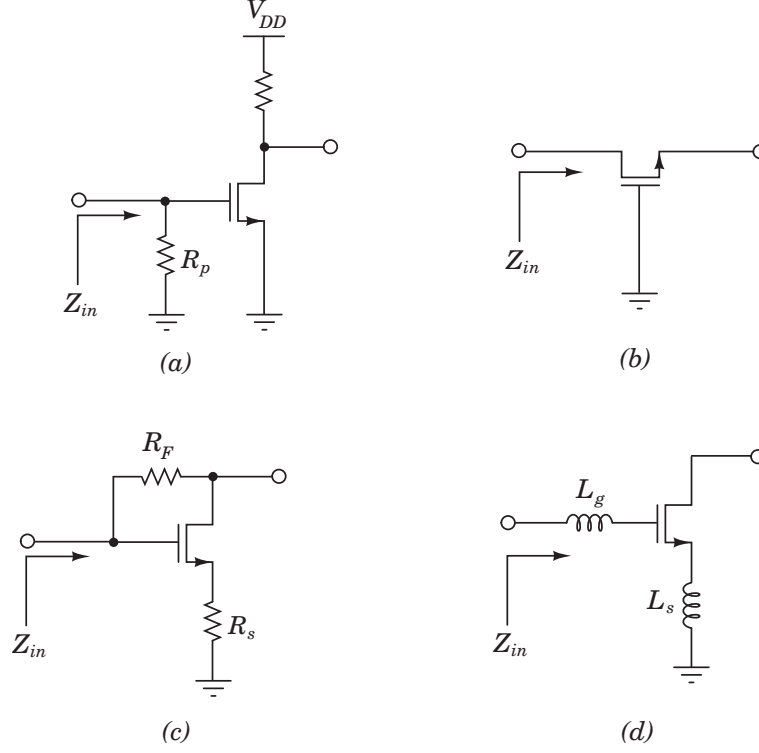


Figure 5.4: Classical LNA topologies: (a) resistive termination, (b) $1/g_m$ termination, (c) shunt-series feedback, and (d) inductive source degeneration.

From the signal model shown in Fig. 5.6, the expression of the input impedance can be written as:

$$Z_{in} = \sum(R) + L_s \omega_T + j\omega(L_s + L_g) + \frac{1}{j\omega C_{gs1}} \quad (5.10)$$

where

$$\sum(R) = R_{gs} + R_{Ls} + R_{Lg} \quad (5.11)$$

and

$$\omega_T = \frac{g_{m1}}{C_{gs1}} \quad (5.12)$$

where the parameters g_{m1} , C_{gs1} and R_{gs} are, respectively, the transconductance,

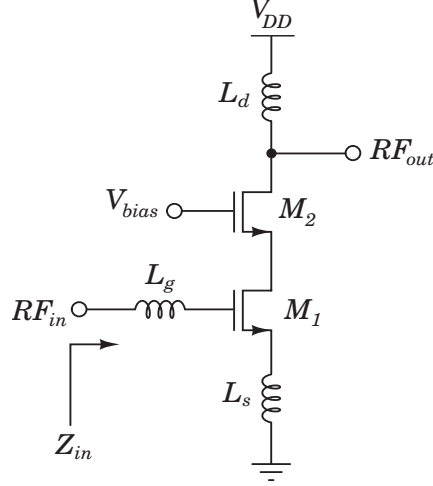


Figure 5.5: Common source amplifier with inductive degeneration.

the gate-source capacitance and the distributed intrinsic resistor of the transistor M_1 . R_{Ls} and R_{Lg} are, respectively, the parasitic series resistors of the spiral inductors L_s and L_g .

In source degeneration topology the input impedance at working frequency f_0 is purely real and proportional to L_s . Therefore, choosing appropriate value of the inductance L_s , the real term of the input impedance can be set equal to the source impedance R_s . From the small signal model shown in Fig. 5.6, the resonance condition for real input impedance is given by the relation [13]:

$$f_0 = \frac{1}{2\pi\sqrt{C_{gs1}(L_s + L_g)}} \quad (5.13)$$

Therefore choosing appropriate value of the inductance L_s , the real term of the input impedance can be set equal to the source impedance R_s and the gate inductance L_g is used to set the resonance frequency when L_s is chosen to satisfy the criterion of $50\ \Omega$ input impedance.

The noise factor of the LNA can be obtained by analyzing the equivalent circuit of Fig. 5.6. In this equivalent circuit, $\overline{i_{n,d}^2}$ and $\overline{i_{n,g}^2}$ represent the channel thermal noise and the gate-induced current noise of the MOSFET M_1 ; $\overline{v_{n,R_g}^2}$ and $\overline{v_{n,R_{Lg}}^2}$ are the thermal noise voltage of the parasitic gate resistance R_g and parasitic series resistance of the gate inductance, respectively. The analysis of the noise factor of the LNA considers only the noise contribution of the first stage; the noise contribution

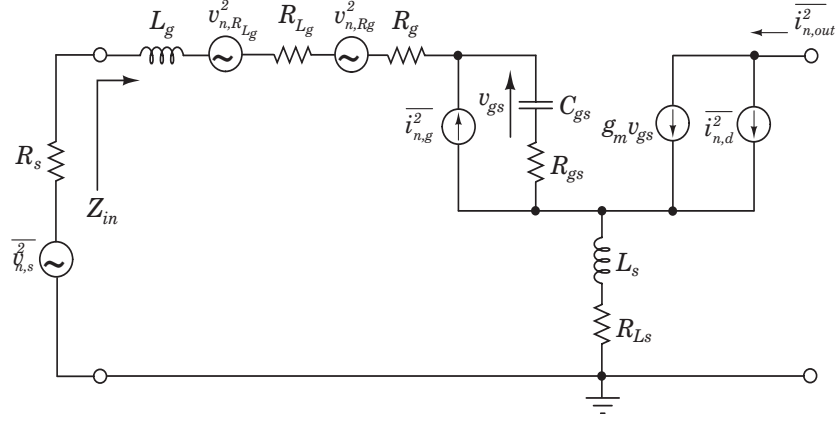


Figure 5.6: Equivalent schematic in the input of the LNA for the input impedance and noise calculations.

of the second stage formed by the transistor M_2 is neglected. This simplification is justifiable provided that the first stage possesses sufficient gain. The total noise factor of the two stages is then given by:

$$F_{LNA} = F_{stage1} + \frac{F_{stage2} - 1}{G_{stage1}} \approx F_{stage1} \quad (5.14)$$

The noise characterization of the cascode inductive source degeneration topology has been studied extensively. A first attempt to optimize the noise behavior has been proposed by Shaeffer et. al [9], who included the effect of gate induced noise. From the simple small signal equivalent circuit shown in Fig. 5.6 and neglecting noise contributions from the transistor M_2 , the noise figure for the studied topology is given by [9]:

$$F = 1 + \frac{R_{Ls}}{R_s} + \frac{R_{Lg}}{R_s} + \frac{R_g}{R_s} + \frac{\gamma}{\alpha} \frac{\chi}{Q_L} \left(\frac{\omega_0}{\omega_T} \right) \quad (5.15)$$

where

$$\chi = 1 + 2|c|Q_L \cdot \alpha \sqrt{\frac{\delta}{5\gamma}} + \frac{\alpha^2 \delta}{5\gamma} (1 + Q_L^2) \quad (5.16)$$

and

$$Q_L = \frac{(L_s + L_g)\omega_0}{R_s} = \frac{1}{\omega_0 R_s C_{gs}} \quad (5.17)$$

Because of the weak gate-source capacitance C_{gs1} of submicron transistors, the value of L_g calculated from (5.13) for the resonance condition at 2.4 GHz is usually larger than 20 nH . Large values of spiral inductors with high-Q are very difficult to integrate and occupy an important chip area. Some simple solutions exist to solve this problem like the increase of transistors size or the use of an off-chip inductor. The drawback of these solutions is the increase of power consumption. A more interesting solution to reduce the value of the inductance L_g consists in increasing artificially the value of the gate-source capacitance C_{gs1} . For that purpose, an external MIM capacitance C_{ex} is placed between the gate and the source of the transistor M1 as shown in Fig. 5.7 [13].

From the new small signal model shown in Fig. 5.7(b), the expression of the input impedance becomes:

$$Z'_{in} \approx \sum(R') + L_s \omega'_T + j\omega(L_s + L_g) + \frac{1}{j\omega(C_{gs1} + C_{ex})} \quad (5.18)$$

where

$$\sum(R') = \frac{R_{gs}}{1 + C_{ex}/C_{gs1}} + R_{Ls} + R_{Lg} \quad (5.19)$$

and

$$\omega'_T = \frac{g_{m1}}{C_{gs1} + C_{ex}} \quad (5.20)$$

The new resonance condition for real input impedance is given by the relation:

$$f_0 = \frac{1}{2\pi \sqrt{(C_{gs1} + C_{ex})(L_s + L_g)}} \quad (5.21)$$

5.4.3 Design methodology

In the following, a technique used for choosing the characteristics of the active and passive devices will be presented. The first step consists in choosing the dimensions and type of transistors, then evaluating the value of the spiral inductors and MIM

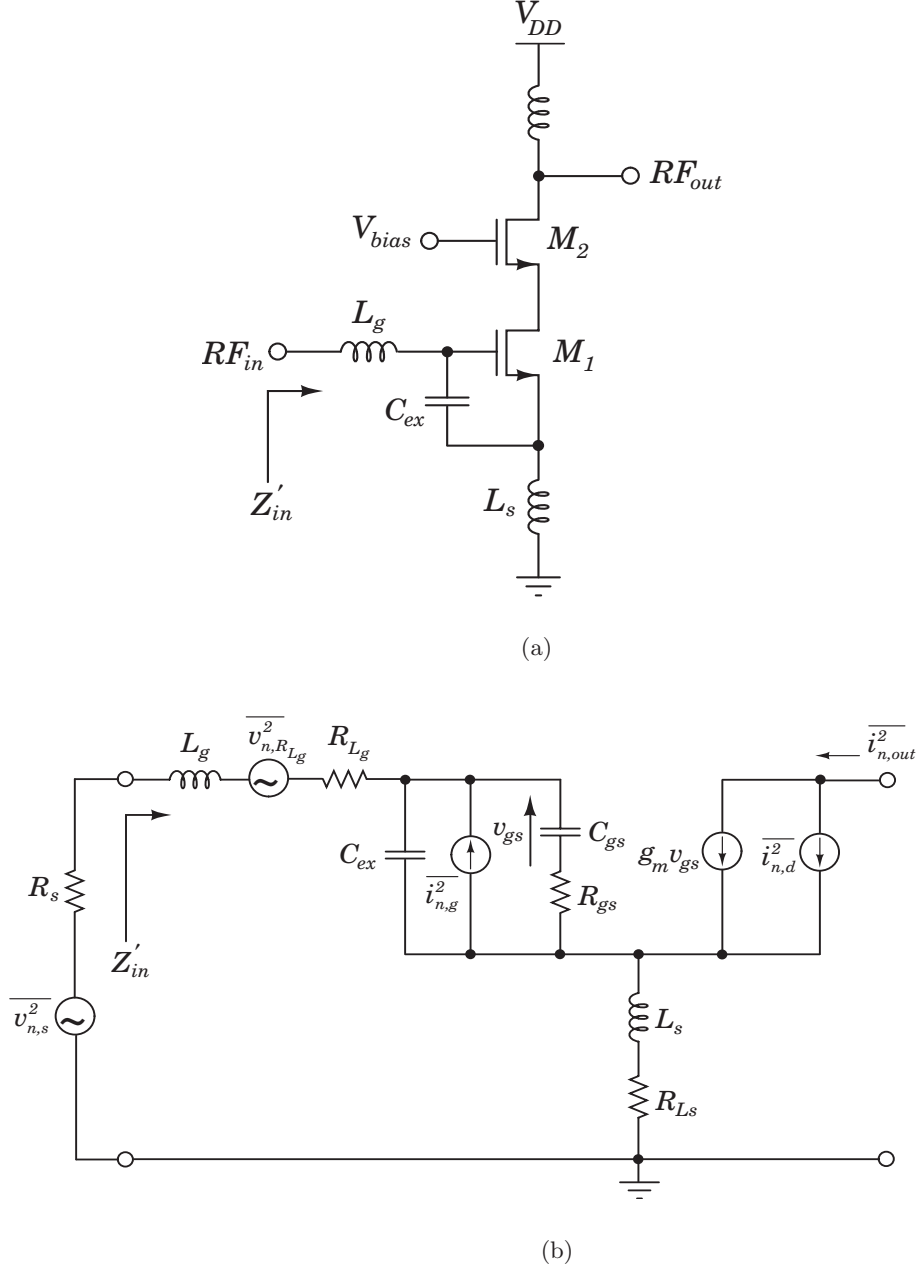


Figure 5.7: (a) Schematic of the optimized cascode inductive source degeneration LNA, (b) its simplified small-signal equivalent circuit as seen from the input.

capacitors needed to ensure the matching conditions of the LNA.

5.4.3.1 Choice of active devices

Fig. 5.8 shows the minimum noise figure (NF_{min}) of the floating body and body contacted SOI nMOS transistors. We also plot the gate resistivity versus gate width in Fig. 5.9. The increase of the gate resistivity with the gate reduction is due to the non-uniform polysilicon gate silicidation and the increase of the relative contribution of the contact gate resistance from each gate finger. Due to the distributed effect, the equivalent resistance of the gate electrode is given by [14]:

$$R_g = \frac{R_{\square} W}{K N_f L_{g,eff}} \quad (5.22)$$

where $R_{\square}$ is the sheet resistance of the gate material, W is the total gate width of the device, $L_{g,eff}$ is the effective gate length, and N_f is the number of gate fingers. The factor K arises from a distributed analysis of the gate. Its value is 1/3 when each gate finger is contacted only at one end, and reduces to 1/12 by contacting at both ends. Thus this contribution can be reduced by lowering the resistivity of the gate and interdigitating the gate electrodes.

The two transistors used are composed of 30 fingers having a width of $2 \mu m$ each and a channel length of 130 nm ($30 \times 2 \times 0.13$). The main small-signal equivalent elements for FB and BC MOSFETs are extracted and presented in Table 5.2. Because of higher gate resistance (Fig. 5.9) and parasitic capacitance due to the contact between the body to source, the body contacted transistor presents higher NF_{min} compared to the floating body MOSFET. For this reason, the floating body has been preferred to the body tied MOSFET for the LNA design.

SOI MOSET	V_T [V]	g_m [mS]	g_d [mS]	C_{gs} [fF]	NF_{min} [dB]	f_T [GHz]	f_{MAX} [GHz]
FB 30x2	0.34	28.8	6.3	52	0.7	89	125
BC 30x2	0.37	30	4.8	80	1.7	63	76

Table 5.2: Characteristics of the FB and BC transistors in 130 nm SOI technology ($V_{DS}=1.2$ V, $I_{DS}=10.2$ mA).

5.4.3.2 Choice of passive devices

The methodology consists in choosing inductors characterized by a maximum quality factor at the central frequency (f_0) of the LNA and considering the different capacitances [15]. A II-model has been extracted for various inductance values

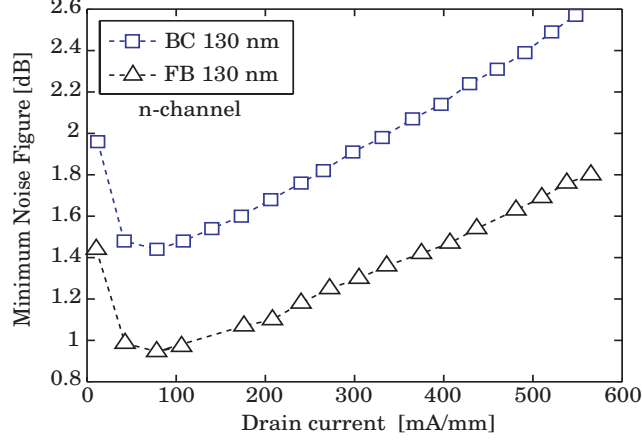


Figure 5.8: Measured minimum noise figure versus drain current for floating body (FB) and body contacted (BC) n-channel MOSFETs ($V_{DS}=1.2$ V).

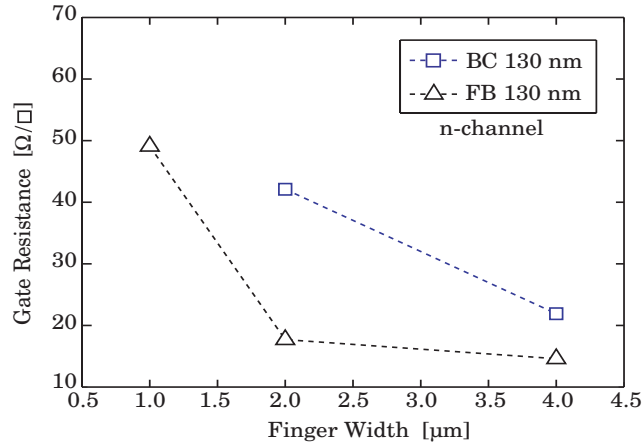


Figure 5.9: Measured gate resistivity versus gate finger width for floating body (FB) and body contacted (BC) nMOSFETs.

and simulated with ADS-Momentum software. The quality factors, defined by $Q = -\text{imag}(Y_{11})/\text{real}(Y_{11})$ and simulated for different inductors are presented in Fig. 5.10. The simulations show the optimum quality factors at 2.45 GHz for inductor values between 6 and 7 nH corresponding to number of turns N_T of 4.5 and 5.5, respectively.

From the expression of the input impedance (5.18), the value of the source inductor L_s allowing the real part of the input impedance Z'_{in} to be equal to the source impedance R_s is given by:

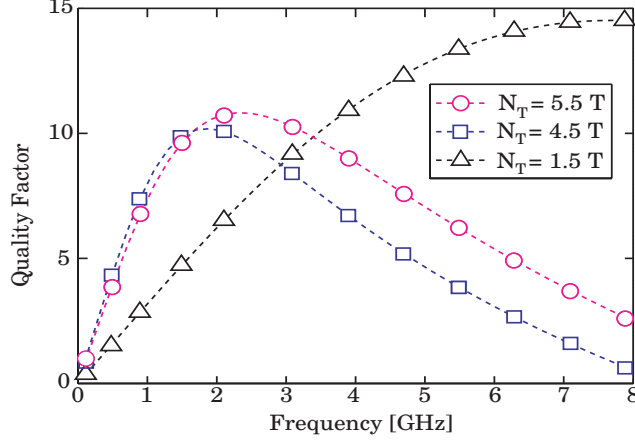


Figure 5.10: Simulated quality factors for three different values of inductor.

$$L_s \approx \frac{R'_{in} - R'_i}{\omega'_T} \quad (5.23)$$

where $R'_{in} \equiv R_s = 50 \, \Omega$ is the real part of input impedance Z'_{in} and $R'_i = R_i / (1 + C_{ex}/C_{gs1})$.

The value of the external capacitor C_{ex} is obtained by resolving the resonance equation defined by:

$$\Im m(Z'_{in}) \approx \omega_0(L_s + L_g) - \frac{1}{\omega_0(C_{gs1} + C_{ex})} = 0 \quad (5.24)$$

Replacing ω'_T and L_s , respectively, by (5.20) and (5.23), the resonance equation can be written as:

$$\omega_0^2 \left(\frac{R'_{in} - R'_i}{g_{m1}} \right) (C_{gs1} + C_{ex})^2 + L_g(C_{gs1} + C_{ex})\omega_0^2 - 1 = 0 \quad (5.25)$$

External capacitor C_{ex} giving the resonance condition at the frequency of interest f_0 is given by:

$$C_{ex} = \frac{\sqrt{1 + (\omega_0\tau)^2} - \omega_0\tau}{R\omega_0} - C_{gs1} \quad (5.26)$$

where

$$R = \sqrt{\frac{R'_{in}}{g_{m1}}} \quad (5.27)$$

and

$$\tau = \frac{1}{2} \frac{L_g}{R} \quad (5.28)$$

Fig. 5.11 shows the simulated gain and noise figure of the LNA using floating body devices, for a power consumption of 2.2 mW. The simulation (using a small signal model of MOSFETs developed by G. Dambrine, IEMN, Lille) results clearly indicate that the noise figure exhibits a minimum values for a capacitance values C_{ex} between 0.25 pF and 0.45 pF. But the gain of the LNA exhibits the highest values for lower capacitances and decreases when the capacitance C_{ex} increases. It is necessary to make a compromise between the gain performances and the noise figure. Moreover for the small values of C_{ex} , the gate inductance allowing the resonance condition at 2.45 GHz is usually large and difficult to integrate. For example, when C_{ex} is fixed to 0 pF the value of L_g is 20.2 nH and 11 nH when $C_{ex} = 0.2$ pF. The best compromise is achieved for $C_{ex} \approx 0.45$ pF. In this case, the needed gate inductance is 6 nH which is of course integrable and exhibits a maximum quality factor around 2.45 GHz. A larger value (≈ 7.2 nH) has been chosen for drain inductor L_d in order to get better DC isolation from V_{DD} .

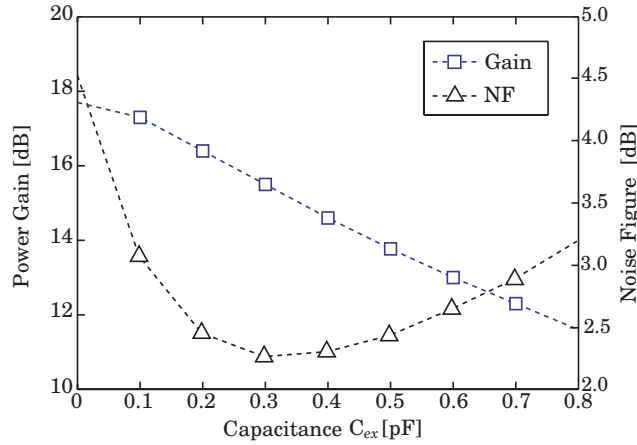


Figure 5.11: Simulated power gain and Noise Figure versus external capacitance C_{ex} .

Table 5.3 summarizes the simulation results of the three selected (L_s , L_g and L_d)

inductors. The parameter Q_{f_0} is the quality factor at working frequency and $f_{Q_{max}}$ the frequency for which the quality factor is maximum. The parameters W , S , D_i and N_T are, the conductor width, conductor spacing, inner diameter and number of turns for the spiral inductors, respectively.

	L_s	L_g	L_d
Nominal value [nH]	0.72	6.0	7.2
Q_{f_0}	5.1	9.0	8.2
$f_{Q_{max}}$ [GHz]	16	2.4	2.2
N_T [Turn Nb]	1.5	4.5	5.5
Size (W, S, D_i) [μm]	11.9, 3, 100		

Table 5.3: Physical dimension, inductance value and quality factor for various integrated inductors.

5.4.4 Circuit implementation and measurement results

The circuit was fabricated on 130 nm SOI CMOS provided by ST-Microelectronics (France) using a high resistivity ($\rho \approx 2 \text{ k}\Omega\cdot\text{cm}$) substrate in order to increase the quality factor of the passive elements. The schematic and die micrograph of the fabricated LNA are shown in Fig. 5.12. The chip dimension of the LNA is $1230 \times 650 \mu m^2$.

The LNA output matching uses the on-chip spiral inductor, L_d and two Metal-Insulator-Metal (MIM) capacitors C_1 and C_2 as shown in Fig. 5.12. These MIM capacitors are calculated and fixed to 0.6 and 1.2 pF, respectively. The active devices (M_1 and M_2) used in the design are floating body NMOS transistors composed of 30 fingers having a width of $2 \mu m$ each. The values of the on-chip spiral inductors L_g and L_d have been fixed, respectively, to 6 and 7.2 nH as explained before. The value of the capacitance C_{ex} is simulated and fixed to 0.45 pF.

The measured and simulated S-parameters and noise figure under 50Ω of the LNA are shown in Fig. 5.13. The LNA has a power gain of 10 dB with 3.1 dB NF at 2.4 GHz and a good input and output matching (S_{11} and $S_{22} \approx -10 \text{ dB}$) for a power consumption of 2 mW. The measured reverse isolation S_{12} is better than -20 dB at 2.4 GHz. This good isolation is mainly due to the cascode topology. Fig. 5.14 shows the measured input third-order intermodulation product (IIP3) of -2.5 dBm.

Table 5.4 summarizes the measurement results of the designed narrow-band LNA and compares them with previously published works. The proposed SOI LNA exhibits the best results in terms of ratio of the gain to the power consumption (S_{21}/P_{DC}) and in terms of the noise figure and the power consumption product ($NF \times P_{DC}$).

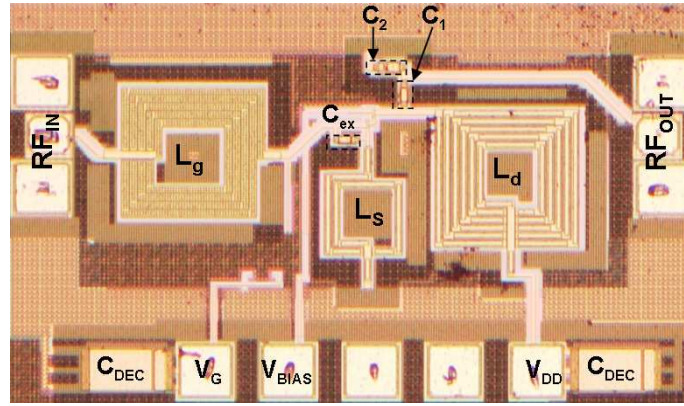
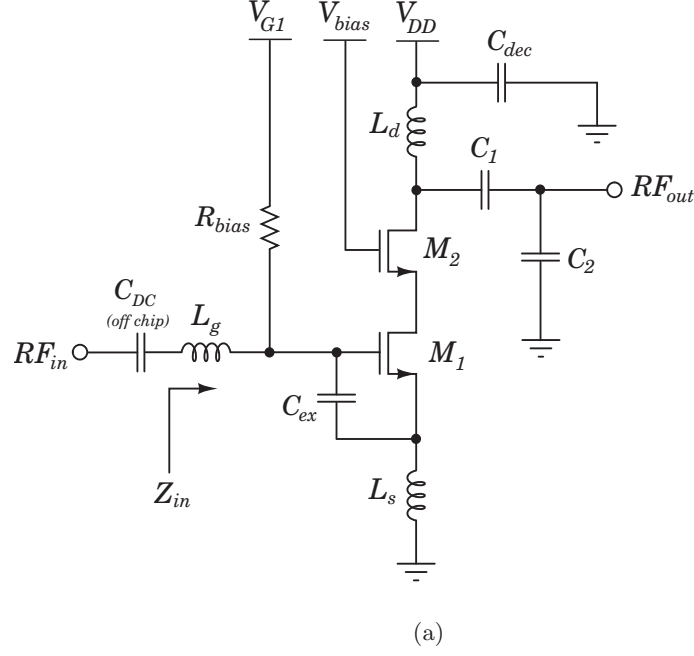


Figure 5.12: Schematic (a) and die micrograph (b) of the final optimized cascode inductive source degeneration LNA.

5.4.5 Conclusions

Narrow band LNAs were designed in a 130 nm SOI PD CMOS process, with floating body and body contacted devices. Thanks to the design methodology and the

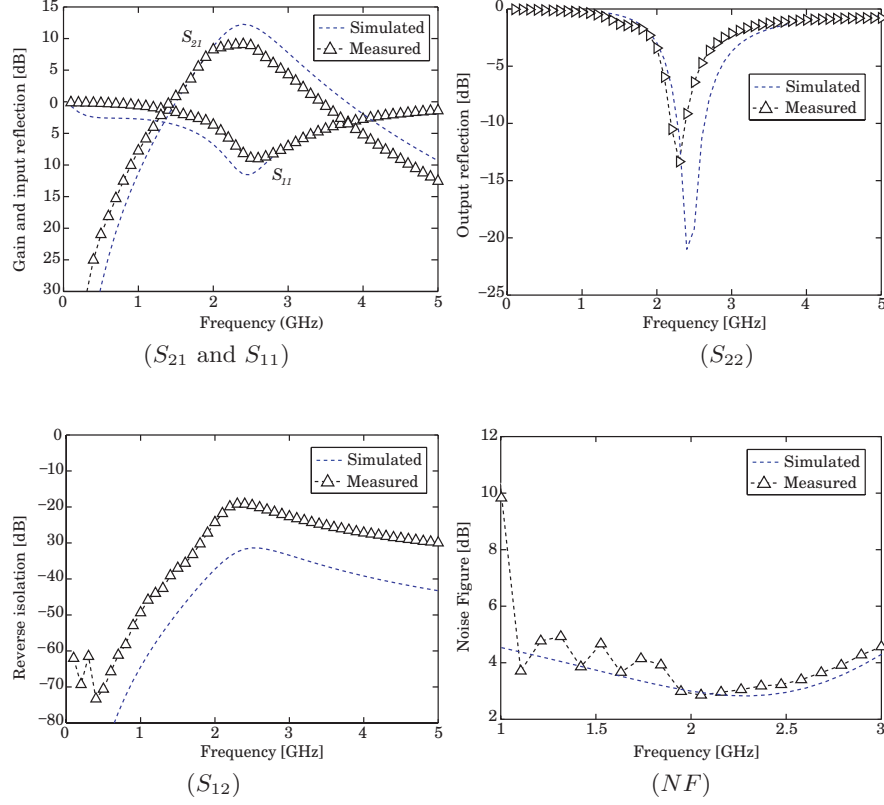


Figure 5.13: Measured and simulated S-parameters and noise figure of the designed LNA.

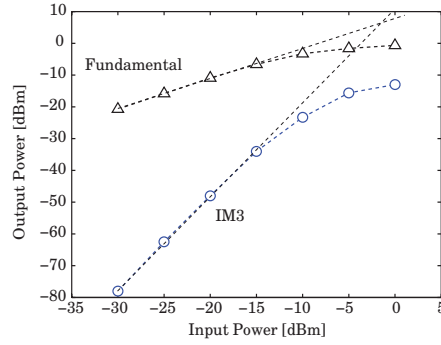


Figure 5.14: Measured IIP3 of the designed LNA at 2.4 GHz.

possibility of using CMOS SOI implemented on high resistivity substrates, the measurement results at ambient temperature show are good in terms of ratio of the gain

Ref.	Gain (dB)	NF (dB)	f_0 (GHz)	V_{DD} (V)	P_{DC} (mW)	CMOS Techno.
[16]	7	3.9	2.0	0.5	2	0.2 μm Bulk
[16]	10	3.5	2.0	1	10	0.2 μm Bulk
[17]	15	2.6	5	3	24	0.25 μm Bulk
[17]	8	4.7	5	3	6	0.25 μm Bulk
[18]	14	1.9	1.96	1	10.6	0.5 μm SOI
[19]	11.45	3.4	5.7	1.8	4	0.18 μm Bulk
This work	10	3.1	2.4	1.2	2	0.13 μm SOI

Table 5.4: Summary of the performances and comparison with previously published narrow-band LNA.

to the power consumption and in term of the product of noise-figure and power consumption.

5.5 ESD protection

Electrostatic Discharge (ESD) protection for Radio Frequency (RF) device applications is becoming increasingly important. Traditional ESD protection structures, whether on or off chip, are often responsible of performance degradation of RF blocks. SOI ESD protection networks have already made considerable progress in achieving industry-acceptable ESD protection levels using gated diodes, gate-coupled MOSFET's, and Zener diodes [20]. Introduction of systematic characterization benchmark strategies and new testing techniques (e.g., TLP: Transmission Line Pulse testing) will allow better understanding of the ESD robustness of advanced technologies [21]. Standard circuits operating at low frequencies or at low speed are relatively insensitive to the parasitic resistance, capacitance and inductance introduced by use of standard ESD protection structures. By contrast, high-frequency RF circuits are highly sensitive to any added parasitics, and traditional ESD protection approaches, when applied to RF devices, can generate impedance mismatches and losses, causing reflections of signals, decrease of gain, reduction in bandwidth, increased noise figure, etc. With the decrease of gate oxide thickness, CMOS circuits become more sensitive to stress from electrostatic discharge phenomena. LNA constitutes one of the most critical building block in RF front-end. It is usually connected to outside world through the antenna and can be exposed to ESD stress. The principle of full-chip ESD protection is illustrated with the ESD protection of the 2.4 GHz CMOS SOI LNA using diodes as ESD protection elements. The performance and the comparison between two LNAs (with/without ESD protection) are discussed.

5.5.1 Presentation of the ESD protected LNA

The circuit of the LNA with ESD protection is presented in Fig. 5.15. The ESD protection is achieved with the different diodes (D1 to D5) from which dual diodes with a power rail, and power clamp (PC). One of the advantages of this clamp is the fact that its parameters are tunable. It uses 4 trigger diodes in order to tune its trigger voltage (and leakage), and it uses 1 holding diode in order to increase its holding voltage for guaranteeing latch-up immunity. Each diode area is $140 \mu\text{m}^2$. During a positive ESD stress on RF_{IN} , with respect to ground, the ESD current is discharged through D2 diode and V_{DD} bus, then to the ground via the power clamp PC which is connected to V_{DD} and to the ground. Furthermore, the supply V_{DD} and ground pins are also protected by the power clamp and D1 diode from both positive and negative ESD stresses. During a negative ESD stress on RF_{IN} with respect to ground, the ESD current is discharged directly through D3 diode. The same ESD protection circuit configuration based on D4 and D5 diodes is considered at the output of the LNA (RF_{OUT}). The dimension of the input and output ESD protection circuits must be very small to significantly reduce the parasitic capacitances for high frequency applications [22].

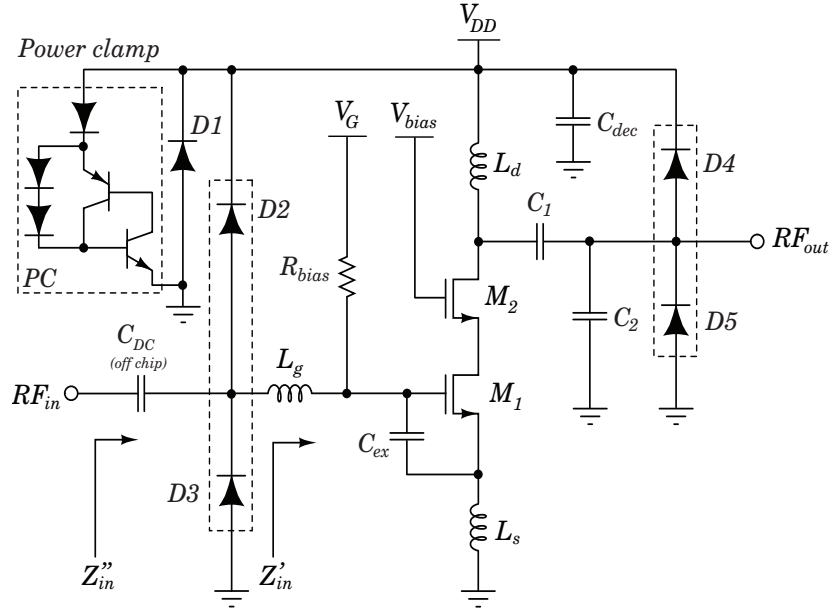


Figure 5.15: Schematic of the protected cascode inductive source degeneration LNA.

5.5.2 ESD protection diodes

The parasitic capacitances and resistances of the ESD protection circuit will degrade the LNA matching and noise figure. To avoid this, the ESD protection components should be built with low capacitances and high Q factors. The ESD protection devices in RF circuit should be chosen without large resistances and capacitances for noise and match concerns. Q factors are often used to evaluate the quality of the ESD protection devices. For our design, the ESD protection of the LNA consists of a pair of SOI low-cap diodes, provided by Sarnoff. The layout top view of this diode is shown in Fig. 5.16. This low-cap diode contributes to the parasitic capacitance for approximately 105 fF for an area of $140\text{ }\mu\text{m}^2$ (when the diode is off) in 130 nm SOI CMOS technology, as shown in Fig. 5.17.

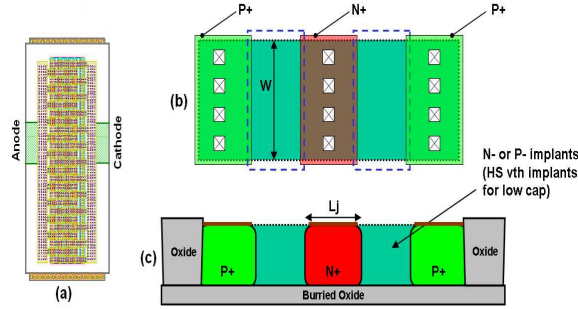


Figure 5.16: (a) Layout (b) top view and (c) cross section of the low-cap diode designed on 130 nm SOI CMOS process ($W = 35\text{ }\mu\text{m}$).

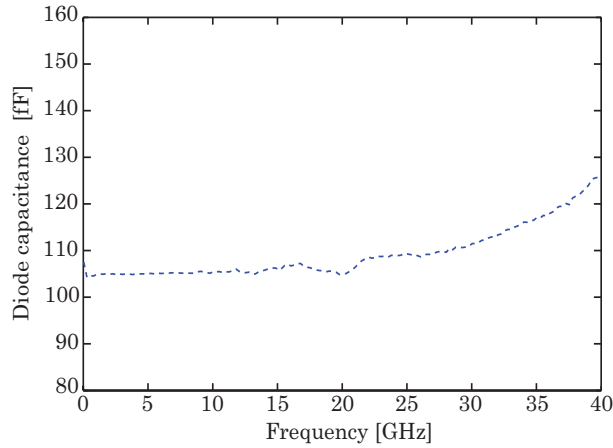


Figure 5.17: Measured capacitance of the ESD protection diode, after deembedding.

Fig. 5.18 shows the small signal model of the LNA with ESD protection, where C_T represents the parasitic capacitances due to D2 and D3 diodes. In order to study the impact of the different diodes on the matching input, the new expression of the input impedance Z''_{in} is given as

$$Z''_{in} = C_T / Z'_{in} = \frac{Z'_{in}}{1 + j\omega C_T Z'_{in}} \quad (5.29)$$

where

$$1 + j\omega C_T Z'_{in} = 1 + j\omega C_T \sum (R') + j\omega C_T L_s \omega'_T \quad (5.30)$$

$$-\omega^2 (L_s + L_g) C_T + \frac{C_T}{(C_{gs1} + C_{ex})} \approx 1 + \frac{C_T}{C_{gs1} + C_{ex}} \quad (5.31)$$

At resonance condition, Z'_{in} is purely real and equivalent to R'_{in} , the new input impedance Z''_{in} can be finally expressed as

$$Z''_{in} \approx \frac{R'_{in}}{1 + C_T / (C_{gs1} + C_{ex})} \approx 0.75 R'_{in} \quad (5.32)$$

The last expression shows a decrease of about 25% in input impedance due to the diodes D2 and D3.

5.5.3 ESD test methodology

The protection level of ESD is characterized using the Human Body Model (HBM) test [23]. The Human Body Model is the most commonly used model intended to represent a human discharging into an integrated circuits and devices. The protection levels are defined by a classes according to the HBM voltage levels. The summary of the main ESD classes is shown in Table 5.5.

The electrical model of the HBM test is shown in Fig. 5.19. It consists of a charged capacitance of 100 pF (C_c) that is discharged through a 1.5 k Ω resistor (R_s), connected to the device under test (DUT). The HBM test method is used for

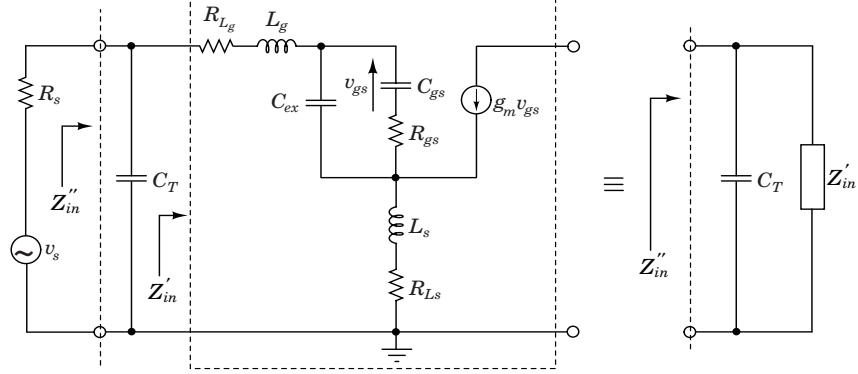


Figure 5.18: Small-signal equivalent circuit seen from the input of the LNA with ESD protection.

qualification of parts, meaning that the results only show a “pass” or a “fail” and do not provide any detailed information on the ESD protection circuit.

HBM voltage levels	Satisfied class
< 0.25 kV	Class 0
0.25 kV to 0.5 kV	Class 1A
0.5 kV to 1 kV	Class 1B
1 kV to 2 kV	Class 1C
2 kV to 3 kV	Class 2
4 kV to 8 kV	Class 3A
> 8 kV	Class 3B

Table 5.5: Illustration of the HBM test indicating the different classes.

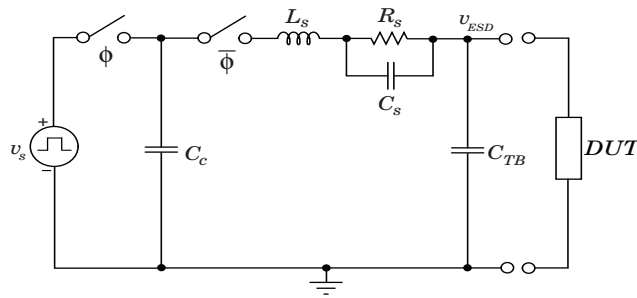


Figure 5.19: HBM electrical model testing.

The technique mainly used to characterize the ESD robustness is the transmission line pulse (TLP) [24] [25]. The principle of generating a square pulse by means of

discharging a pre-charged transmission line into a load device gave the name to this method introduced by Maloney and Khurana [24] for device characterization in the ESD-relevant, high-current domain.

An example of TLP test system is shown in Fig. 5.20 [26]. The 100 ns-TLP serves as a current source with an impedance of approximately 1 k Ω in order to emulate HBM-conditions (1.5 k Ω). A low-inductive 50 Ω -resistor terminates TL2 and transforms the low-impedance pulsed voltage source into a quasi-current source. Due to the purely resistive termination for both polarities, multiple reflections cannot occur. The transmission line TL2 separates the pulse generator from the remote pulse head and DUT. Both, current and voltage pulses are measured simultaneously, and as close as possible to the device. The $I - V$ diagram is constructed by plotting the average voltage value of the voltage waveform over the DUT, versus the average value of the current waveform through the DUT. During the consecutive TLP pulses, the pulse voltage increased is step-wise, and each pulse results into one $I - V$ point of the TLP $I - V$ curve. The $I - V$ characteristics serve as basis for many successful ESD protection design and technology hardening efforts [26].

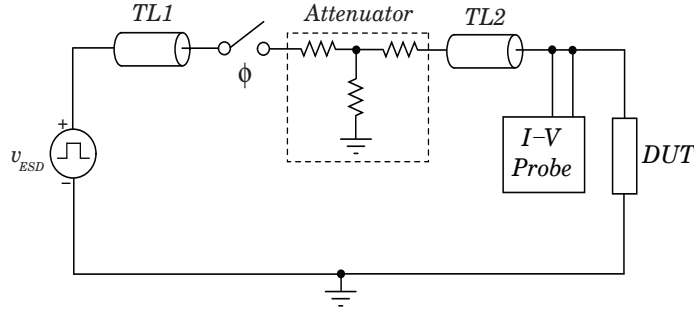


Figure 5.20: Basic TLP setup.

Using a BSIM model for each transistor and protection diode, it is possible to simulate the LNA protected in transient mode. Fig. 5.21 shows the voltage at the RF input node (RF_{IN}) and the voltage at the gate of transistor M1 ($V_{GATE}(M1)$) simulated when -2 kV HBM stress is applied on the RF input node. The voltage overshoot on the gate M1 (-1.6 V) does not exceed the maximum allowed gate-oxide voltage (4.5 V).

5.5.4 Circuit implementation and measurement results

The circuits (with and without ESD protection) were fabricated on 130 nm SOI CMOS provided by ST-Microelectronics (France) using a high resistivity ($\rho \approx 2$ k Ω .cm)

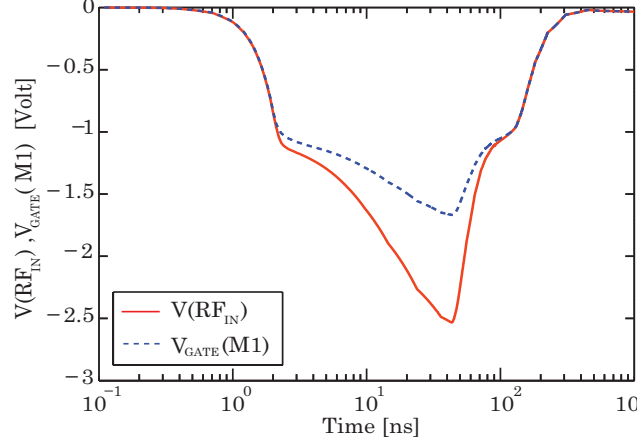


Figure 5.21: -2 kV HBM simulations of the protected LNA, stressed from the RF input pin (RF_{IN}) to the ground. The parameters $V(RF_{IN})$ and $V_{GATE}(M1)$ represent, respectively, a voltage overshoot on the RF input node and on the gate of the transistor M1.

substrate in order to increase the quality factor of the passive elements. The active devices (M1 and M2) used in the design are floating body NMOS transistors composed of 30 fingers having a width of $2 \mu\text{m}$ each. The photographs of the fabricated LNAs are shown in Fig. 5.22. The chip dimensions of both LNAs are $1230 \times 650 \mu\text{m}^2$.

5.5.4.1 RF measurement results

The measured S-parameters and noise figure (NF) under 50Ω of both LNAs are shown in Fig. 5.23. The LNA with ESD protection has a power gain of 13 dB at 2.4 GHz and a good output matching ($S_{22} \approx -10$ dB) for a power consumption of 6.5 mW. The noise figure of the LNAs are approximately 2.7 and 3.6 dB, respectively, at 2.4 GHz. A 0.9 dB increase in NF for the LNA with the ESD protection is mainly due to the parasitics of the diodes and the interconnects of the input/output ESD. The measured reverse isolation S_{12} is better than -20 dB at 2.4 GHz. Table 5.6 summarizes the performances of the ESD protected LNA for various bias conditions. Thanks to the small parasitic capacitance of the diodes, minor degradations of RF performance are noted when adding the ESD protection in the circuit.

Fig. 5.24 shows the measured real part of the input impedance of the LNAs (R'_{in} without and R''_{in} with ESD protection). The measured R'_{in} of the non-protected LNA (64Ω at 2.4 GHz) is more important than the expected value (50Ω). This increase is mainly due to parasitic resistance of the inductors L_g and L_s which have been underestimated and to the gate resistance of the transistor M1 which has been

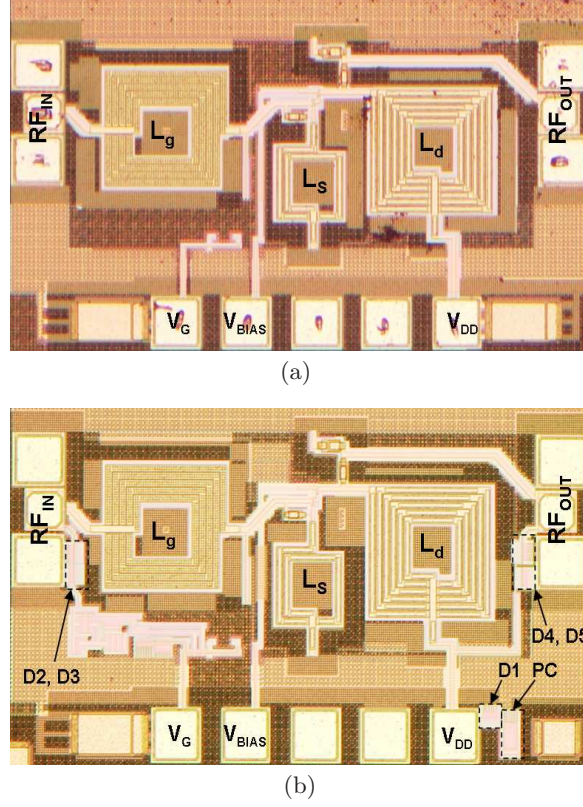


Figure 5.22: Chip microphotographs of the fully integrated LNA (a) without ESD protection, and (b) with “plug-and-play” diodes ESD protection.

neglected in the LNA optimization. As calculated in expression (6.32), the real part of the input impedance decreases when ESD protection is added. The value of R'_{in} is about $48\ \Omega$ at 2.4 GHz for the protected LNA. This value is closer to the source impedance ($R_s = 50\ \Omega$) and this explains the better input matching S_{11} (-10 and -13 dB) when ESD protection is added.

5.5.4.2 ESD measurement results

TLP and dynamic transmission-line pulse test systems are being commercially offered as a technique to characterize the robustness of semiconductor components and circuits. Positive and negative ESD stresses were applied to protected pads. When the Device Under Test (DUT) fails during the TLP test, one can extract a figure of merit that reflects the actual ESD hardness of the DUT. Fig. 5.25 shows the results of the TLP test achieved when a ESD stress is applied on V_{DD} , RF_{OUT} and RF_{IN}

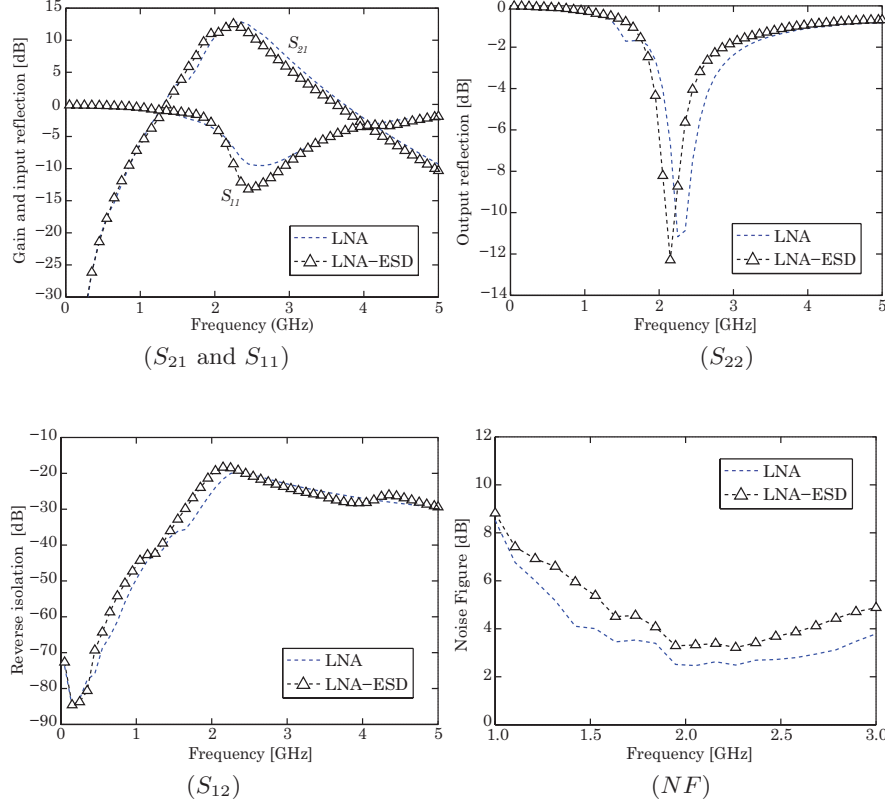


Figure 5.23: Measured and simulated S-parameters and Noise Figure of the designed LNAs (with and without ESD protection circuit).

pads. The measurements show that the V_{DD} pin is protected against ESD up to 1.4 A TLP current, corresponding to 2 kV HBM stress. The input and output terminals are protected against ESD up 0.9 and 0.8 A TLP current, respectively, corresponding typically to 1.4 and 1.2 kV HBM stress. The low ESD protection level of the input and output pads is due of the small area of the diodes. Increasing the area of protection diode allows a better ESD protection circuit but increases the parasitic capacitances of the diodes, thus degrades the RF performances of the LNA.

Additional protections have been added in order to protect the gates of the transistors M1 and M2 from the ESD coming from V_G and V_{bias} bias access pads as shown in Fig. 5.26. The V_G pin is protected by the D6, D7 and D8 diodes from both positive and negative ESD stresses. D7 and D8 diodes have been placed in series in order to improve the threshold voltage of their equivalent diode and make it insensitive to V_G bias. V_{bias} pin is protected by the D9, D10 diodes and local clamp (LC) from both

5.5 ESD PROTECTION

P_{DC} [mW]	Gain [dB]	NF [dB]	S_{11} [dB]	S_{22} [dB]	S_{12} [dB]
6.5	13.0	3.6	-14.0	-12.0	-19.0
3.1	11.0	3.8	-13.4	-12.0	-18.6
2.0	9.2	4.0	-13.1	-11.5	-18.0

Table 5.6: Summary of the measured LNA performance with ESD protection circuit.

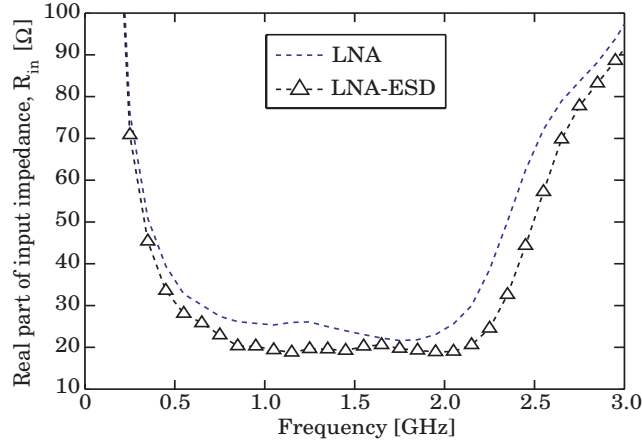


Figure 5.24: Measured real part of input impedance R_{in} of both LNAs (with and without ESD protection).

positive and negative ESD stresses.

Fig. 5.27 shows the results of the TLP test achieved when a positive ESD stress is applied on V_G and V_{bias} pads. The measurements show that the V_G and V_{bias} pins are protected against ESD stress up to 0.32 and 1.4 A TLP current, corresponding typically to up to 0.5 kV and 2 kV human body model stress, respectively.

Table 5.7 summarizes the measurement results and compares them with previously published works. The proposed SOI LNA with ESD protection circuit exhibits good results in term of the gain to the power consumption ratio.

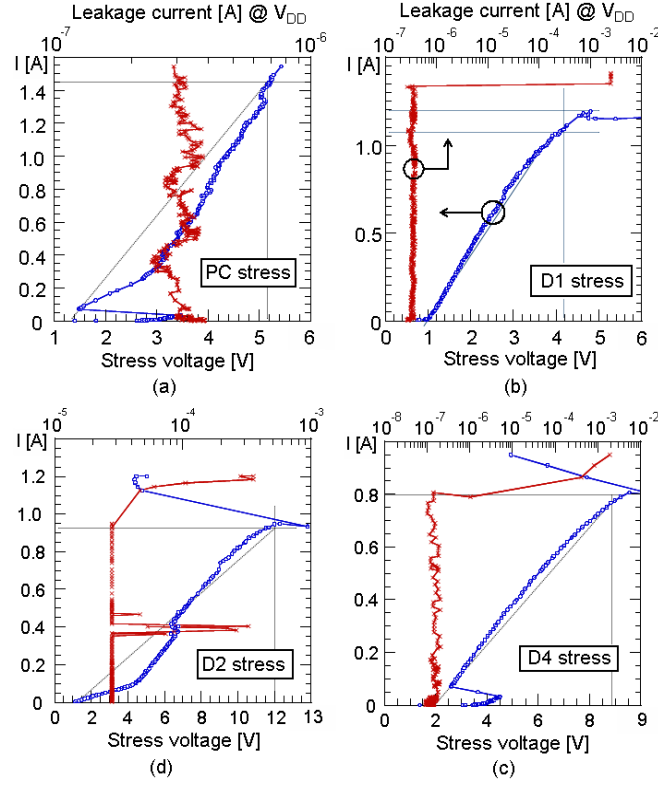
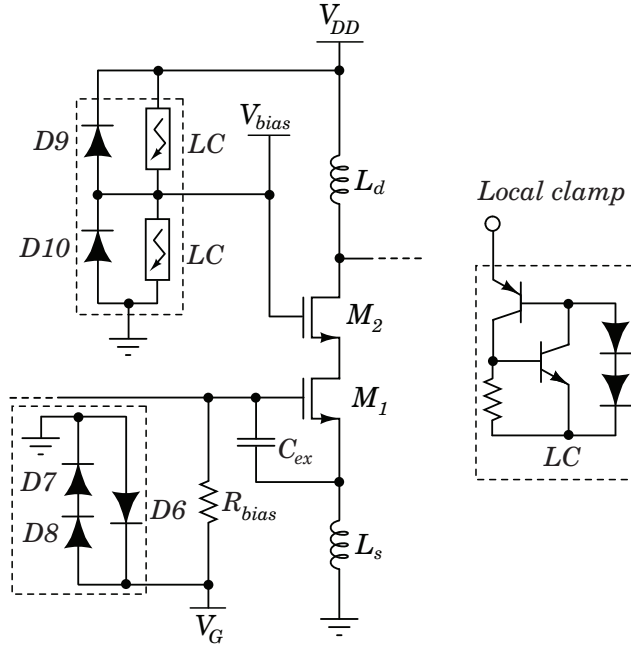
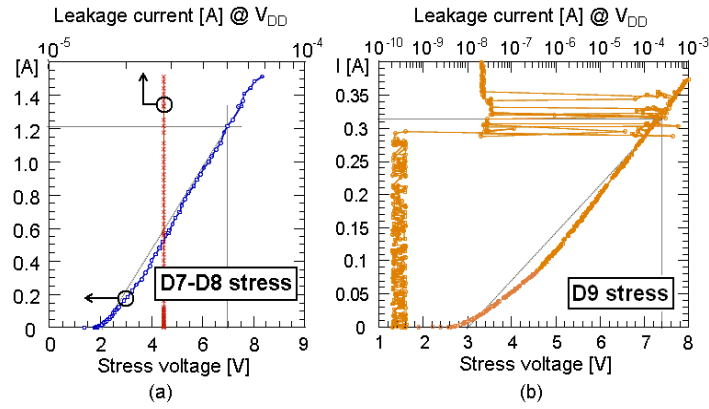


Figure 5.25: TLP test results of the LNA, when (a) positive and (b) negative ESD stresses are applied between V_{DD} and ground and when ESD stresses are applied (c) between RF output and ground and (d) between RF input and ground.

Ref.	Gain [dB]	NF [dB]	f_0 [GHz]	V_{DD} [V]	P_{DC} [mW]	HBM [kV]	CMOS Techno.
[27]*	13.3	2.9	5.5	1.2	9.72	2	0.09 μm Bulk
[28]*	12.1	2.77	2.0	1.0	10.0	2	0.15 μm Bulk
[17]	8.0	4.7	5.0	3.0	6.0	—	0.25 μm Bulk
[19]	11.45	3.4	5.7	1.8	4.0	—	0.18 μm Bulk
[29]*	21.9	2.56	2.4	1.0	12.9	4	0.09 μm Bulk
This work*	13	3.6	2.4	1.2	6.5	2	0.13 μm SOI

Table 5.7: Summary of the performance and comparison with previously published narrow-band LNA (*with ESD protection).


 Figure 5.26: ESD protection added to V_G and V_{bias} pads.

 Figure 5.27: TLP test results of the LNA, when positive ESD stresses are applied, (a) between V_G pin and ground and (b) between V_{bias} pin and ground.

5.6 Analysis of the LNA biased at g_m ZTC point

5.6.1 Introduction

Some applications (well logging, avionics, automotive, ...) require electronic circuits capable of operating at temperatures up to 300°C (Table 5.8). The capability of SOI circuits to expand the operating temperature range of integrated circuits up to 250°C has been demonstrated [1]. A variety of circuit design methods can be used to improve high temperature performances of microelectronics [30]. For analog applications, the stability of the circuit performance in terms of gain, matching, bandwidth, etc. versus temperature is of first importance [31] [32]. With the motivation of low-power and high-temperature applications, we present in this section the behavior of a low noise amplifier for 2.4 GHz high temperature applications based on 130 nm Partially Depleted SOI CMOS technology. The studied LNA is biased at transconductance ZTC.

<i>Applications</i>	<i>Temperatures</i>
Well logging	75-600C
Oil Wells	75-175C
Gas Wells	150-225C
Steam injection	200-300C
Geothermal energy	200-600C
Automotive	150-600C
Underhood	-50-600C
Engine sensors	up to 600C
Combustion and exhaust sensors	up to 600C
ABS	up to 600C
Aircraft	150-600C
Internal equipment	150-250C
Engine monitoring	300-600C
Surface controls	300-600C
Satellites (Venus probe)	150-600C
Commercial nuclear	30-550C

Table 5.8: Temperature requirements for electronic components used in various consumer or industrial applications [1].

5.6.2 ZTC g_m : design strategy

As mentioned in chapter 4, the CMOS MOSFETs exhibit a zero-temperature coefficient point for which the transconductance remains constant when temperature varies. This point is achieved for a single gate bias point. Fig. 5.28 shown the degradation of the transconductance, ϵ_{g_m} of body contacted and floating body NMOS transistors

versus bias gate voltage V_{GS} , when temperature varies from 25 to 250°C. The temperature degradation can be minimized by fixing the gate bias point to 0.42 V for the body contacted and 0.22 V for the floating body transistors. Because of its weak $V_{GS,ZTC}$ value, The FB MOSFET exhibit only a g_m of 14 mS at the ZTC_{g_m} point versus 21 mS for the BC MOSFET. For this reason, the LNA using BC MOSFETs has been selected to study the RF performances versus temperature at the ZTC_{g_m} bias point.

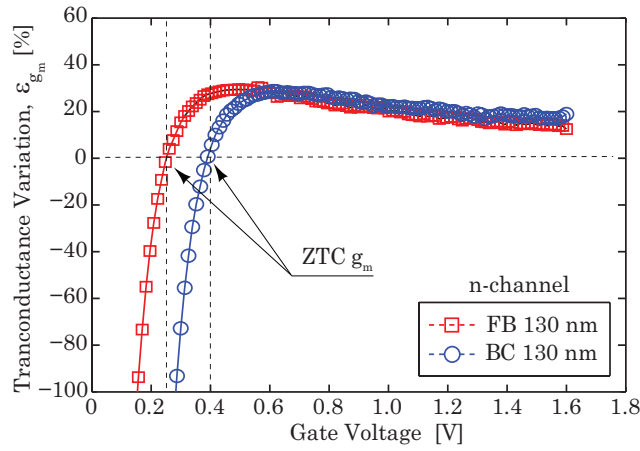


Figure 5.28: Degradation of the transconductance of n-channel SOI MOSFETs when temperature varies from 25 to 250°C ($V_{DS} = 0.6$ V).

For the temperature analysis, on-wafer measurements were performed on the BC LNA at ZTC_{g_m} bias point for each transistor M_1 and M_2 as shown in Fig. 5.29.

On-wafer measurements are performed, with an Anritsu 37369ATM vector network analyzer. Temperature control is provided by a Temptronics 8-in temperature chuck up to 250°C. Ground-signal-ground (GSG) (100 μm -pitch) high frequency coplanar |Z| Probes from SüssTM are used for signal measurement. The measurements are done over the temperature range from 25 to 200°C. In order to extract the S -parameters of the LNA, we perform a calibration step consists in defining the measurement reference planes at the CPW probe tips (VNA calibration). This is performed in measuring standards on a commercially available alumina substrate and applying the so called LLRM (line-line-reflect-match) calibration technique. The noise figure measurements are performed with an Agilent PSA E4440A spectrum analyzer. In order to extract the NF of the LNA, we perform a calibration step consists of a TRL calibration for each temperature value. The measurements include the parasitic effects of the RF pads.

The measured power gain (S_{21}) of the LNA over the temperature range 25 to 200°C is shown in Fig. 5.30. The LNA has a power gain of 10 dB at 2.4 GHz and at ambient temperature. Thanks to the ZTC_{gm} bias choice, the temperature degradation gain is minimized (less than 1 dB between the extreme temperatures corresponding to a degradation of less than 9%, with a power consumption of 2.3-mW at ambient temperature. However, as shown in Fig. 5.31 and Fig. 5.32, a degradation of 67% on noise figure and an increase of 67% of the power consumption is observed when temperature varies from 25 to 200°C. The temperature degradation of the gain and NF is due to the degradation of the quality factors of integrated spiral inductors present in the design.

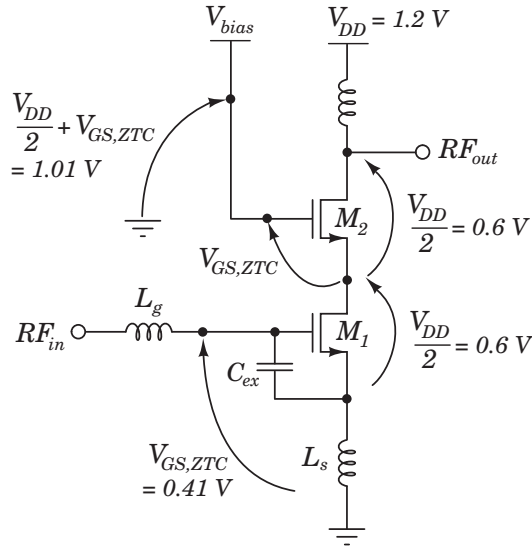


Figure 5.29: Schematic of the final optimized cascode inductive source degeneration LNA, biased at ZTC_{gm} point.

The temperature dependence of some important factors-of-merit is summarized in Table 5.9: ϵ representing the degradation of the gain (S_{21}), the power consumption (P_{DC}), the noise-figure (NF) of the LNA and the quality factor of the gate inductor (Q_{Lg}), when temperature varies from 25 to 200°C.

5.7 Conclusion

In this chapter we investigated the design and the characterization of a fully integrated Low-Noise Amplifier for low-power and narrow-band applications, using a cascode inductive source degeneration topology, and FB and BC transistor in 130 nm

5.7 CONCLUSION

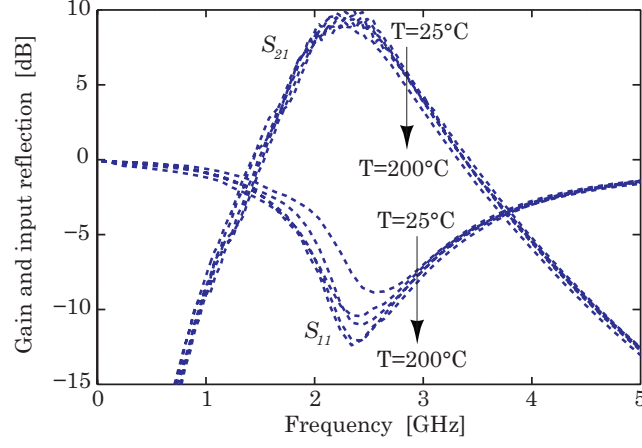


Figure 5.30: Measured gain of the LNA using body contacted n-channel MOSFETs for various temperatures and biased at transconductance ZTC point (ZTC_{gm}).

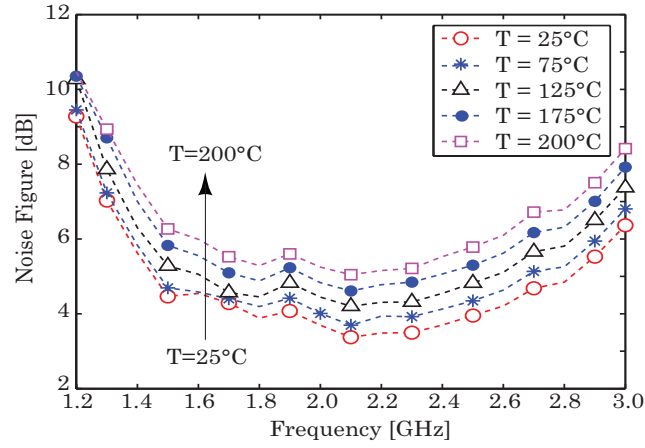


Figure 5.31: Measured noise figure of the designed LNA for various temperatures and biased at transconductance ZTC point (ZTC_{gm}).

	S_{21} [dB]	P_{DC} [mW]	NF [dB]	Q_{Lg}
$T = 25^{\circ}C$	10	2.2	3.4	10
$T = 200^{\circ}C$	9.1	3.7	5.7	6.4
variation, ϵ	-9%	+67%	+66%	-66%

Table 5.9: Temperature dependence of some factors of merit of the designed LNA at ZTC_{gm} bias point.

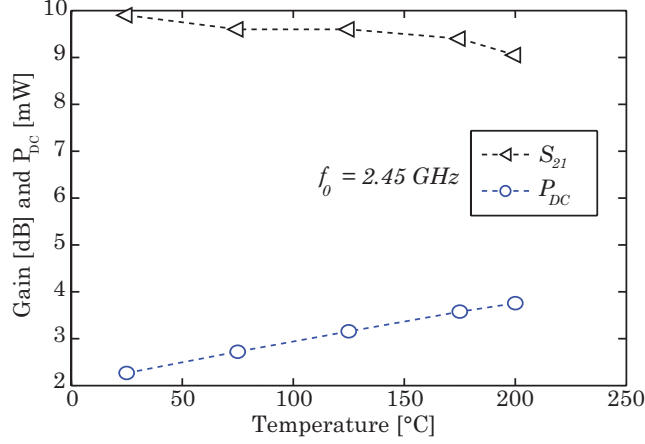


Figure 5.32: Measured gain and power consumption of the designed LNA at frequency work and for versus temperature at ZTC_{gm} bias point.

partially depleted CMOS SOI technology. Thanks to the SOI technology and design methodology, the designed LNAs shows promising results.

The BC LNA was characterized over a wide temperature range. Thanks to the ZTC_{gm} bias point choice, the temperature degradation of the gain is minimized (less than 1 dB between the extreme temperatures). The main drawback of the ZTC strategy design is the important increase of the power consumption (67%) when temperature varies from 25 to 200°C. These good results show that the SOI technology is now emerging as a good candidate for the realization of high-temperature integrated circuits.

The importance of the ESD protection in RF circuit was presented and LNA protected against ESD was proposed as example. The LNA with an on chip ESD protection was designed in a 130 nm SOI PD CMOS process. The LNA uses on-chip “plug-and-play” diodes protection in conjunction with a power clamp. The RF performances of the LNA are not degraded when adding the ESD protection to the circuit. However, the ESD measurements do not show the protection level expected in input and output of the circuit (2 kV HBM stress). This problem is due of the small area of the protection diodes. Increasing the area of protection diodes allows a better ESD protection circuit but increases the parasitic capacitances of diodes, degrading the RF performance of the LNA. There is a clear trade-off, between ESD and RF performance, but it is a deliberate choice of the authors to have the best RF performance at the cost of a little bit less ESD protection.

Finally, the LNA designed with body contacted devices has been measured in a

5.7 CONCLUSION

large temperature range and its factors-of-merit are presented. The LNA has a power gain of 10 dB at working frequency and ambient temperature. Thanks to the ZTC_{g_m} bias point choice, the temperature degradation gain is minimized (less than 1 dB between the extreme temperatures), -8 dB input reflection with a power consumption of 2.2 mW at ambient temperature. These good results show that the SOI technology is now emerging as a good candidate for the realization of high-temperature integrated circuits. However, as explained in chapter 5, the use of body-tied transistors does not offer the possibility to vary the ZTC_{g_m} point. It is not possible, for example to reach a high gain (maximum of g_m) and minimum temperature degradation together and impose a compromise between these factors-of-merit. The use of MOSFETs with body node access, disable this impossibility and should offer a sufficient margin to designers to optimize RF circuits with minimum temperature degradation.

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CHAPTER 6

CONCLUSION

Low power consumption becomes an important figure-of-merit in mobile communications due to limited battery life. One approach to meet this challenge is to create a reduced power RF system-on-chip that contains digital, analog and RF parts on the same die. In this context, SOI appears as an important technology for mixed signal RF CMOS applications. Due to its lower junction capacitance and reduced leakage current, SOI provides reduced static and dynamic power consumption of the digital logic. In terms of passive device integration the major benefit of SOI is the possibility of using high resistivity (HR) substrates.

This work has explored the performance of the SOI technology for current and future RF and high temperature applications. The investigation was performed by analyzing the temperature effects on passive and active devices, then on an RF circuit example.

In chapter 1, a brief presentation and discussion about the RF architectures was presented. A few receiver classical architectures have been explored with respect to integrability, performance and required building block specifications. Traditional heterodyne receivers are not optimal solutions for achieving low-cost and low-power because they require expensive and bulky off-chip filters resulting in a low degree of integration and increased power consumption. The homodyne architecture offers a high degree of integration and constitutes an excellent candidate for completely integrated receivers with good performances at low power and a small silicon area.

The SOI technology has been briefly introduced in the Chapter 2. Various SOI technologies and different existing process fabrications were presented. The general acceptance of CMOS SOI as the next generation technology choice because large volume production is the best way to ensure continuous price reductions and quality improvement. Most companies are actively working to further develop and implement this technology, thereby giving CMOS SOI a significant advantage over other insulated materials, such as SOS (Silicon-on-Sapphire).

The impact of temperature on different transmission line structures and on integrated spiral inductors implemented on high and standard resistivity substrate has been investigated in chapter 3. The behavior of the TFMS and CPW transmission line topologies, versus frequency and for standard and high silicon substrate resistivity was presented and compared. It has been clearly shown that CPW topologies made on high resistivity substrate exhibits better performances than TFMS, because CPW structures enable wider lines to achieve the same characteristic impedance, leading

to reduced metallic losses. However, TFMS allows the use of standard resistivity substrate because the back ground plane shields the Silicon substrate. The TFMS line structures can then be an interesting topology if the losses can be lowered to the same level than CPW made on HR SOI. To reduce the metallic losses, the width and the thickness of the conductor must be increased, but the capacitance between the conductor and the ground plane must be kept constant ensuring the same characteristic impedance. To achieve this goal, the thickness of the dielectric layer must be increased, or low-k dielectric must be used instead of silicon dioxide. These solutions are in agreement with the tendencies of semiconductor industries. Indeed, more and more metal levels are used, allowing a thicker isolator layer between the conductor, made with the top metal layer, and the ground plane. The losses of TFMS and CPW structures implemented on standard and high resistivity substrate were investigated over a wide range of temperature. As expected, the losses increase with temperature except for the CPW line implemented on standard resistivity substrate for which the decreases of substrate losses compensate the increases of metallic losses with the rise of temperature.

We also studied the impact of temperature on the model parameters of integrated square and octagonal spiral inductors implemented on a 130 nm SOI CMOS technology. The use of high resistivity substrate allows to improve substantially the quality factor. The use of patterned ground shield in the case of STD substrate allows a good isolation of the devices from the Si-substrate and leads an improvement of Q_{max} .

The temperature behavior of the three conventional SOI transistors (FB, BC and DT) in both DC and RF domain has been studied. The main figures-of-merit of the three conventional transistors have been compared and the extraction of the extrinsic and intrinsic parameters of the small signal equivalent model have been performed in the chapter 5. The superiority of body tied transistors (body-contacted and dynamic threshold devices) over floating body transistors has been reported for some figures of merit, such as leakage current and I_{ON}/I_{OFF} ratio, while some other parameters showed the superiority of floating body transistors such as the cut-off frequency. Moreover, the main inconvenient of the floating-body devices such as the floating body effects (FBE) that are known to play critical issues in partially depleted SOI technology are less pronounced at high temperature. Finally, the extrinsic and intrinsic parameters of the small signal equivalent model are extracted in a large temperature range. As expected, only the parameters which theoretically are a highly dependent on the drain current (thus on the mobility and threshold voltage) show a real dependence with the temperature variation.

As example of RF circuit applications of the SOI technology, a fully integrated Low-Noise Amplifier for low-power and narrow-band applications, using a cascode

inductive source degeneration topology has been investigated at room temperature. Then the LNA was characterized over a wide temperature range at zero-temperature-coefficient of transconductance bias point. Thanks to the SOI technology and design methodology, the LNA shows a promising results at ambient temperature and a minimum temperature degradation of the gain when biased at ZTC_{g_m} . These good results show that the SOI technology is now emerging as a good candidate for the realization of high-temperature integrated circuits. Finally, the importance of the ESD protection in RF circuits was briefly introduced and an example of ESD protected circuit was proposed. A LNA has been designed using on-chip “plug-and-play” diodes protection. The RF performances of the LNA have been presented and compared with previously published narrow-band LNA characteristics.

APPENDIX A

MOSFET MODELS

A.1 The high-frequency SOI MOSFET model

Two MOSFET models have been used in this thesis: the first one is the non-quasi-static small signal model developed by Prof. G. Dambrine from IEMN (France) [1] and the other one is a non-linear model developed by Dr. A. Siligaris (IEMN).

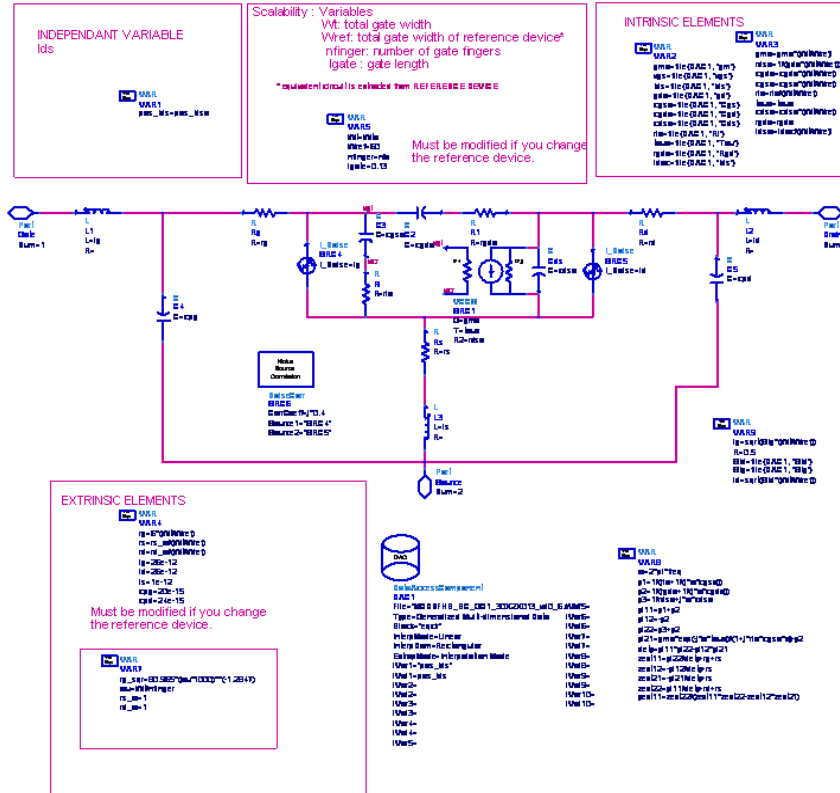
The non-quasi-static small signal model of the SOI MOSFET's (floating body and body contacted) is a table based model scalable and extracted from measurements done on the transistors. This model also includes the noise caused by the gate and the drain of the MOSFET (Fig. A.1). This model has been used in the LNA design (chapter 6) especially for the evaluation of the noise figure.

A.2 The non-linear model

This model describes accurately the electrical (DC-RF) characteristics of MOS devices. It includes a nonlinear drain current expression that is continuous and infinitely derivable, leading to the transconductance and the output conductance to be continuous. The capacitances are directly derived from a gate charge expression that ensures the charge conservation principle (Fig. A.2).

This model is an empirical nonlinear model, which is charge conservative, useful for large signal RF circuit simulation. This model is a compromise between compact models and look-up table models, and combines some advantages of each modeling technique. The electric equivalent circuit is similar to those used for all MOSFETs; it includes a nonlinear drain current expression and a nonlinear gate charge equation. The model shows very good DC and RF prediction of the nonlinearity and the harmonics level [2] [3].

APPENDIX A. MOSFET MODELS



A.2 THE NON-LINEAR MODEL

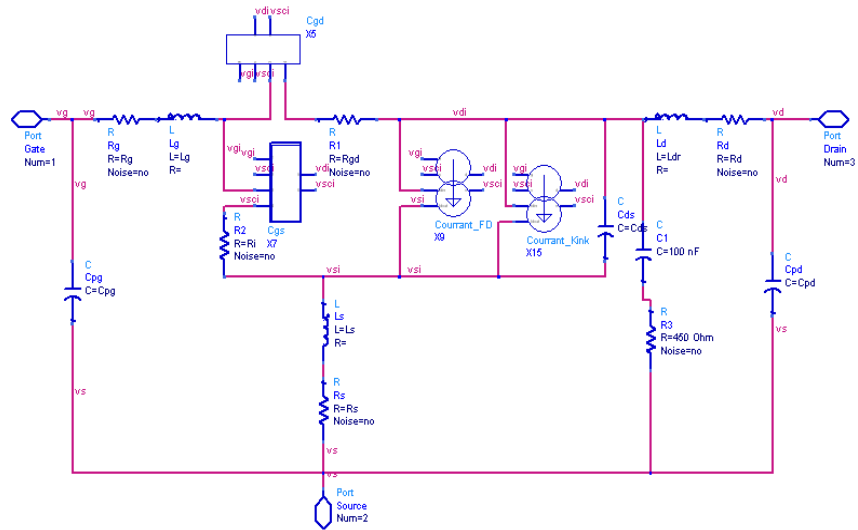


Figure A.2: Schematic of the non linear model of the SOI MOSFET implemented on ADS simulator.

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APPENDIX B

DENSITY OF VIAS

The 130 nm SOI CMOS process provided by ST-Microelectronics, is a single poly CMOS process, using SOI UNIBOND wafers with either a standard resistivity ($\rho_{Si} \approx 8-22 \Omega.cm$) or high resistivity ($\rho_{Si} > 2 \text{ k}\Omega.cm$) substrate. This process features lines with six copper metal layers (M1 to M6) and an additional top metal layer (M7) in Aluminum (Alucap). The bottom metal layer M1 is above an oxide dielectric layer STI (Shallow Trench Isolation) and an oxide+nitride dielectric layer PMD (Pre-Metal Dielectric) as shown in Fig. B.1. All metal levels can be connected by a high density of vias (via 1 to 5). The ground plane used for the implementation of the TFMS lines (chapter 3) is illustrated in Fig. B.2.

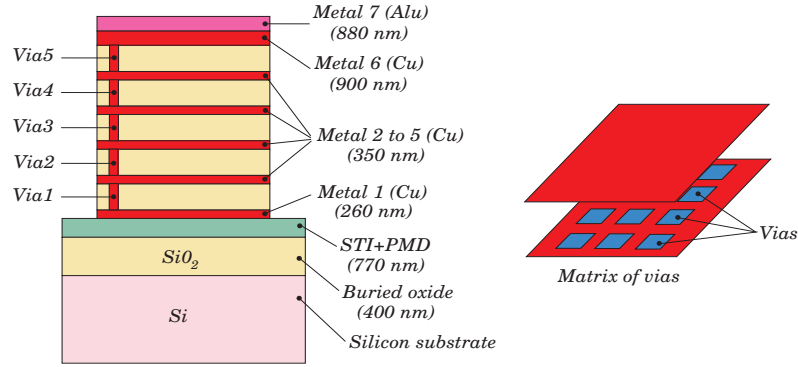


Figure B.1: Illustration of a cross section with vias in 130 nm ST-M SOI technology.

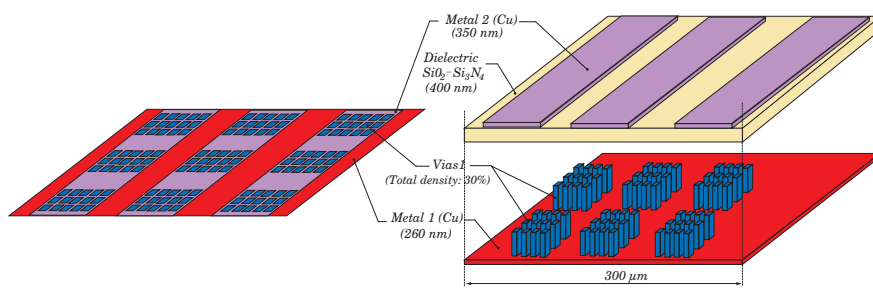


Figure B.2: Illustration of ground plane implemented on SOI technology.