Substrate noise mitigation using high resistivity base silicon wafer for a 14 GHz VCO on 28 nm FD-SOI

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***Abstract*—This paper studies the impact of substrate resistivity on the sideband spurs generated at the output of a 14 GHz voltage-controlled oscillator (VCO) because of noise signal propagation through the substrate. A VCO has been designed in the 28 nm fully depleted Silicon-on-Insulator (FD-SOI) technology and implemented on a standard (15 Ω.cm), a high resistivity (3 kΩ.cm with parasitic surface conduction) and a trap-rich (3 kΩ.cm without parasitic surface conduction) silicon base wafer. The output spectrum of the VCO (around f_{osc}) when injecting a 10 dBm noise signal at a frequency of 10 MHz (f_{noise}) into the substrate is simulated, showing spurs generated at $f_{osc}\pm f_{noise}$, and at other higher-order modulation products. The results obtained on the high resistivity substrate show a reduction of 10 dB of the $f_{osc}\pm f_{noise}$ sideband spurs compared to those on the standard resistivity substrate. The spurs are further reduced by more than 90 dB when a trap-rich SOI wafer is used. Those results highlight the important impact of substrate resistivity and parasitic surface conduction on the signal integrity of CMOS VCOs.**

Keywords— Voltage-Controlled Oscillators, substrate noise coupling, crosstalk, high resistivity substrates, parasitic surface conduction, Fully Depleted Silicon-on-Insulator, spur generation, electromagnetic simulation.

I. Introduction

With the emergence of new 5G systems, a particular interest in the co-integration of radio frequency (RF) and digital circuits is exhibited. Unfortunately, RF circuits do not benefit from the same immunity to external disturbing signals as digital circuits do, leading to them being sensitive to the co-integration with other potentially noisy circuits. Signals leaking into the substrate because of digital switching activity, which will be referred to as signal noise, are considered harmful noise to RF front ends such as voltage-controlled oscillators (VCO), and such coupling can be facilitated by the silicon substrate's conductive properties.

Digital leaking signals coupling to sensitive RF integrated circuit (IC) modules is an issue that degrades transceiver performance [1 - 7]. For example, in [7] parasitic coupling was analyzed for a 2.1 GHz long-term evolution (LTE)-compliant receiver channel in a 65 nm CMOS technology, confirming that the noise signal from baseband digital circuits propagating through the substrate creates in-band spurious tones in RF received bands. Such an issue, named substrate noise, could be strongly mitigated by the proper choice of the substrate's material properties. Indeed, substrate coupling between a noise injection pad and a MOS transistor at frequencies ranging from 500 kHz to 50 MHz was studied in [4 - 6]. In that work, by analyzing the power spectrum at the transistor's drain electrode, up to 35 dB in coupling isolation improvement was observed by considering an RF-optimized trap-rich (TR) SOI substrate solution compared with a non-optimized high-resistivity (HR) option (without any interface passivation, and hence suffering from the parasitic surface conduction (PSC) effect [8, 9]).

This paper investigates the effect of increasing substrate resistivity on noise coupling in the 28 nm FD-SOI technology from STMicroelectronics, where a 14 GHz LC-VCO is chosen as the test vehicle. Indeed, oscillators form critical RF blocks that are expected to deliver the purest possible signals, and, as discussed in this paper, VCO signal purity can be corrupted by noise signals coupling through the substrate.

The paper is organized as follows: first, the impact of substrate resistivity on noise coupling is discussed in Section II. Section III describes the VCO designed as an RF demonstrator circuit in this study. Section IV presents the methodology that was implemented to simulate the noise coupling to the VCO for various substrate resistivity values, as well as to quantify its impact on the VCO's performance. Finally, Section V summarizes the simulation results and draws conclusions regarding the use of HR substrate for mitigating the substrate noise.

II. Noise Propagation vs. Substrate Resistivity

A. Substrate noise considerations

Extensive studies have been carried out in the literature on the subject of substrate noise coupling between different circuits sharing the same handle silicon substrate [1 - 3] and the problem is often divided into three main categories (Fig. 1): generation, propagation, and impact on devices. Designers can intervene at any one of these levels to immunize the circuit to this kind of noise. This work focuses on the propagation part on which the impact of the silicon substrate resistivity is investigated. Indeed, the substrate can be viewed as an RC network linking any two points located on top of it [10].

B. High resistivity substrate

An HR substrate brings in many benefits when it comes to RF circuits, mainly by reducing losses and improving linearity in passive RF components [11, 12]. Integrating such low-loss substrates into a given CMOS process can be worth investigating depending on the applications targeted for a particular circuit.

Digital circuits typically switch at frequencies in the MHz range and, at these frequencies, a standard silicon substrate behaves more as a resistive network for which we can neglect the capacitive component. As a consequence, raising the nominal resistivity of the substrate results in

mitigating the propagation of any signals running through it, including noise that might have been generated at another location on the chip. Crosstalk simulations that elaborate more on this reasoning are shown in Section II.C.

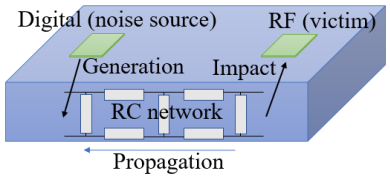


Figure 1. Noise coupling mechanism through the substrate.

Nevertheless, HR substrates in SOI technologies suffer from PSC (Fig. 2) [8, 9], a phenomenon that is present because of the buried oxide (BOX) layer, in which positive fixed charges attract electrons from the bulk, making that interface highly conductive, therefore inducing a vertical gradient of resistivity. This results in a much lower effective resistivity of the substrate despite having a very high bulk resistivity [8, 9, 13]. One of the solutions to this problem is the trap-rich (TR) layer [15], an undoped polysilicon layer characterized by many trap energy levels introduced beneath the BOX. In this work, simulated substrate resistivity profiles are chosen in order to represent the case of a standard resistivity (STD) substrate, an HR substrate suffering from the PSC, and an HR substrate with a TR passivation layer.

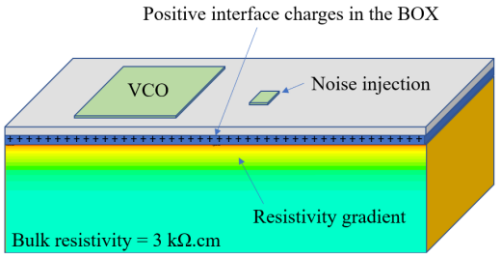


Figure 2. A 3 kΩ.cm substrate suffering from PSC.

Modeling these three cases essentially comes down to choosing a resistivity profile for the substrate, to be included in electromagnetic simulations that will account for the impedance networks through all substrate layers and any propagation of signals within them. The resistivity profile itself is derived from separate TCAD simulations [13, 14]. The TCAD simulations will be discussed in Section II.C.

C. Crosstalk simulations

To emphasize the link between substrate noise and high-resistivity substrates, crosstalk is simulated between two 50x100 µm² metallic pads, distanced by 235 µm, with vias penetrating through the BOX into the substrate (Fig. 3). The layout is chosen to roughly mimic the distance between the noise injection location and the active core of the VCO in the more complete simulations, which will be discussed in Section IV.B. This gives a preview of the substrate resistivity's effect on the propagation of signals between two arbitrarily chosen locations on the substrate.

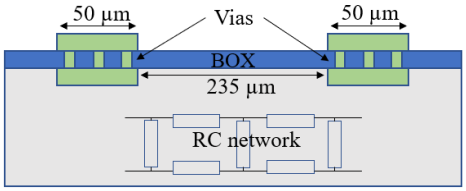
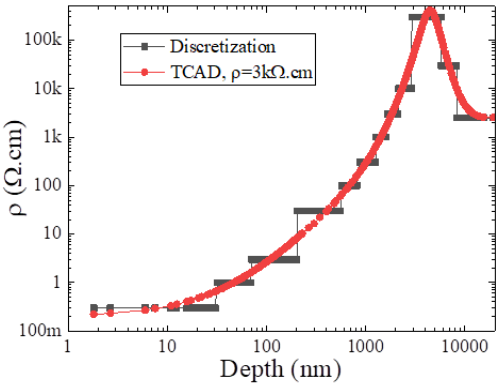
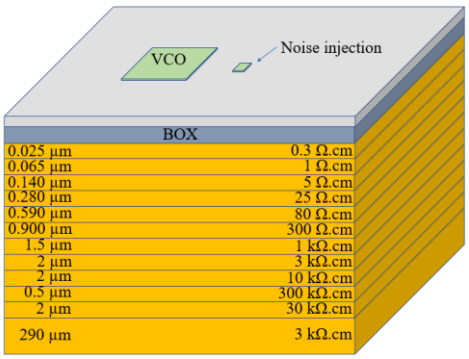


Figure 3. Crosstalk simulation setup.

Three substrates with different resistivity profiles are used for this simulation: a 15 Ω.cm STD substrate, a substrate with a vertical discretized gradient of resistivity representing the PSC effect (Fig. 4), and a 3 kΩ.cm TR substrate.



(a)



(b)

Figure 4. Discretization of the resistivity profile for an HR substrate with the PSC, (a) results of TCAD simulations (Atlas from Silvaco) showing the resistivity profile, (b) Depiction of the stack used in ADS Momentum for electromagnetic simulations.

The discretization of the resistivity profile is made according to the results of TCAD simulations (Atlas from Silvaco) [14] that give precise information about the gradient of electron concentration in the vicinity of the interface BOX-handle Si substrate (Fig. 4.a). This information is then injected in a dedicated substrate definition interface in the electromagnetic solver ADS Momentum (Fig. 4.b). A 2-port S-parameter simulation is performed and the parameter S_{21}, which characterizes power transmission between the two ports, is extracted (Fig. 5).

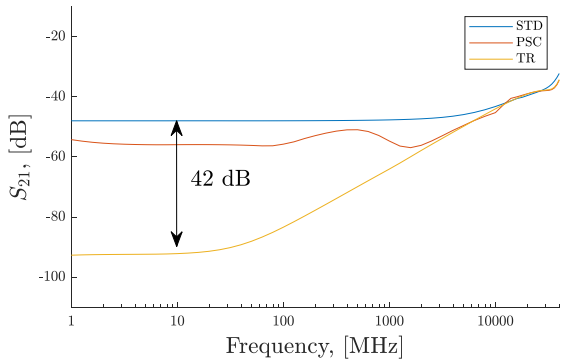


Figure 5. Crosstalk simulations from 1 MHz to 40 GHz.

Results show that there are two main types of behavior exhibited for all types of substrates, where the S_{21} parameter is initially flat and invariant with frequency (resistive behavior of the substrate impedance) until it reaches a cut-off where it starts to increase (capacitive behavior of the substrate impedance). The noise signal used for the simulations that will be presented in Section IV.C has a frequency of 10 MHz. At this frequency, the TR substrate has an S_{21} 42 dB lower than that of the STD substrate, justifying the investigation on the use of such substrates for external noise immunization of VCOs.

III. Substrate-Dependent VCO Designs

Two VCOs were designed for this study, one optimized for a standard resistivity substrate while the other one is optimized for an HR substrate. Indeed, optimizing the inductor for the highest quality factor results in different designs when performed on STD or HR substrates. This will be discussed in Section III.B.

A. VCO architecture

The architecture chosen for the two VCOs is a classic LC tank topology (Fig. 6), with a cross-coupled pair of transistors whose role is to provide the negative resistance and compensate the losses present in the oscillating LC network. The transistors are sized for optimal phase noise performance and to provide enough biasing current for the proper functioning of the circuit.

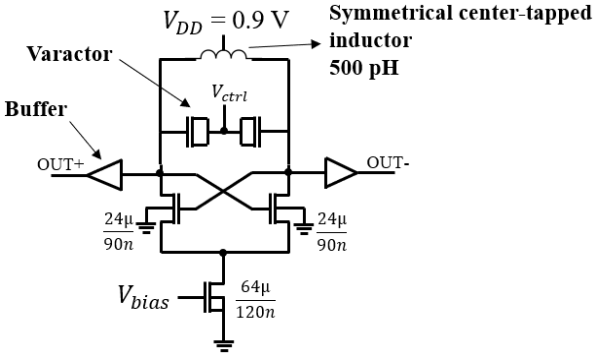


Figure 6. LC VCO architecture.

The two VCOs are designed such that they have exactly the same active core (transistors and varactors) and associated core layout, A simplified layout of one of the VCOs is shown in Fig. 7.

B. Inductor design considerations

The only difference between the two VCOs is in terms of the 500-pH inductor of the resonating tank. The VCO that is integrated on an HR substrate has a thicker metal track inductor, which means using several stacked metal layers. This is because an HR substrate is less lossy and therefore the designer has more freedom in terms of using lower-level metal layers as opposed to trying to stay as far away from it as possible for a STD silicon substrate. This allows the designer to stack up more metal layers, resulting in a lower track resistance and a higher quality factor. The value of the inductance also changes, and adaptation is needed in terms of width and the length of the track to readjust the inductance value in order to effectively have the same oscillating frequency for both VCOs. The optimal performance obtained on the STD substrate was achieved by shielding the substrate with a floating M1 metallic plane and by implementing the inductor coil in the stacked combination of IB and LB top metal layers, using an internal diameter of 270 µm. At 14 GHz a series inductance of 504 pH is obtained for a Q factor of 24.0. The design on the HR substrate uses a stacked combination of IA, IB, and LB with an inner diameter of 275 µm and without any metallic shielding plane below the coil. In this manner, at 14 GHz, a series inductance of 491 pH is obtained for a Q factor of 31.5.

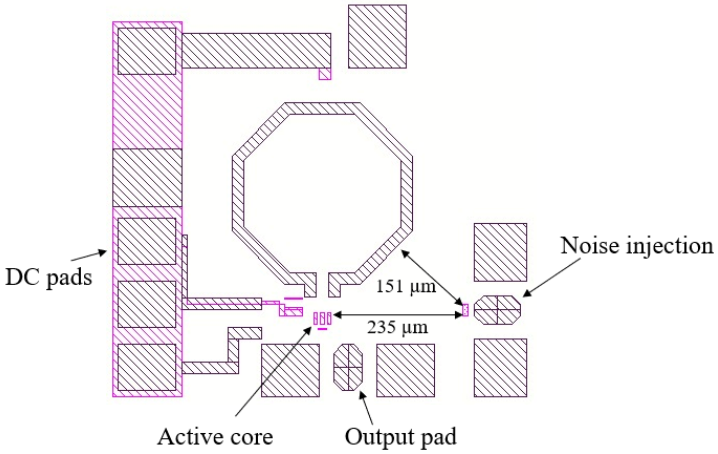


Figure 7. Simplified image of the VCO layout.

IV. Impact of Substrate Noise Coupling

A. Simulation methodology

The layout of the VCO is divided into two parts: a part that has all the passives, on-chip interconnects, and the substrate, and a part that only includes the active devices and a few lower-level metals in their vicinity. The first part is simulated using ADS Momentum, by choosing a different substrate resistivity profile for each case (STD, PSC, and TR). The second part is simulated using the Quantus parasitics extraction (PEX) tool. The results of the two simulations are then coupled together on the same testbench to fully capture the substrate effects under investigation.

The final testbench is created using an S-parameter box resulting from the ADS Momentum simulations, together with the model of the transistors extracted using Quantus PEX. After wiring all the nodes together, a 2-tone harmonic balance analysis is performed and results are extracted. The results of the standalone VCOs are summarized in Section

IV.B, while the results regarding spurs generation due to noise coupling are presented in Section IV.C.

B. VCO Figures of Merit

The VCO's figures of merit were simulated on the STD substrate. These results are obtained from post-layout simulations and account for the types of parasitic components present in a finalized design. The VCO is tunable between 13.2 and 16.1 GHz for a tuning range of 19.7%. The best achievable phase noise at a 1 MHz frequency offset is at -102.7 dBc/Hz. The DC power consumption is 7.5 mW for a differential output power of -6.9 dBm.

C. Substrate noise coupling levels

Beyond the standalone VCO simulations, the output spectrum of the VCOs can be analyzed while including the injection of a single-tone noise signal (10 dBm power at 10 MHz) into a dedicated substrate pin available in the electromagnetic S-parameter simulation file and located ~235 um away from the VCO core (Fig. 7).

Frequency modulation of the fundamental oscillating signal by the single-tone noise signal injected into the substrate occurs in the non-linear transistors. The spectrum of the output node (Fig. 8) shows the fundamental oscillating signal along with modulation products at $f_{osc} \pm n \times f_{noise}$, n being a natural positive number (only the first, second, and third modulation products are shown in Fig. 8 for clarity). Fig. 9 summarizes the results for different types of substrate. Only the power of the first two modulation products on the right side of the spectrum is reported for symmetry reasons. The highest power for the spurs being at roughly -52 dBm, is enough to compromise the purity of the output signal. For the HR substrate suffering from PSC, spurs are also generated in the same way at lower power of -62 dBm but still enough to have a degrading effect on the purity of the output signal. For the 3 kΩ.cm TR substrate, the simulated power value of the spurs generated because of the noise is at -155 dBm, essentially sitting below the noise floor of a real circuit, therefore, strongly improving the noise immunity and the purity of the fundamental oscillating output signal autonomously generated by the VCO.

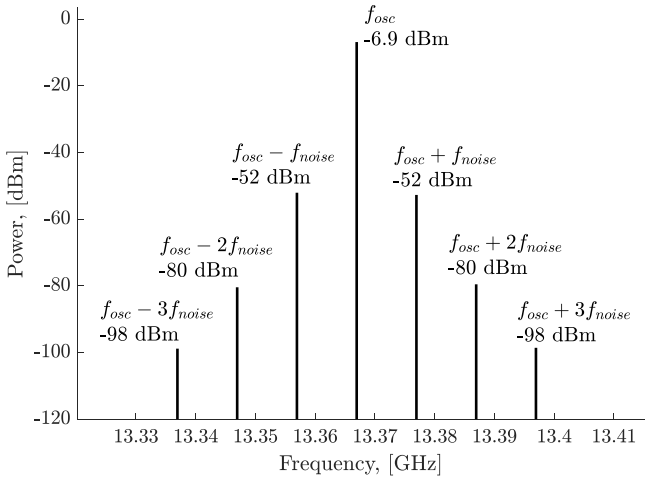


Figure 8. Spectrum of the output signal when a 10 MHz 10-dBm power signal is injected into the standard resistivity substrate.

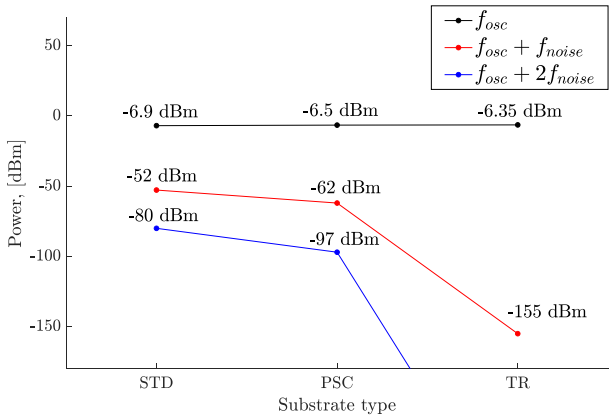


Figure 9. Power of the fundamental signal and the spurs generated by the VCO when a 10 MHz 10 dBm-power signal is injected into the substrate as a function of the substrate type.

Noise propagating through the substrate accesses the VCO nodes in different ways. It can propagate to the back-gate or bulk of the transistors, it can capacitively couple to the inductor parts in the circuit, or it can couple to the metallic ground plane and cause ground bounce. Many solutions to this problem found in the literature suggest using guard rings around transistors [16, 17] or shielding the inductor [10]. These are solutions used during the circuit design phase, assuming the propagation of the noise until it reaches the VCO nodes is inevitable. The results obtained in this work show how effective it can be to directly compromise the propagation itself of the noise signal thanks to the use of high-resistivity TR passivated SOI substrates seeing how they are effective in reducing crosstalk at the MHz frequency range. On such types of substrates in FD-SOI technology, the designer can worry less about design constraints related to protecting the circuit from external noise, since the solution proposed is a technological one.

V. CONCLUSION

This paper shows quantitative data issued from electrical and electromagnetic simulations in order to illustrate the effect of substrate resistivity on the isolation of CMOS RF front-end circuits like VCOs from externally generated substrate noise. Using a 14 GHz LC-VCO designed in 28 nm FD-SOI technology as a demonstrator, the spectrum of its output signal is investigated. It is demonstrated that the sideband spurs, generated by mixing of the VCO fundamental frequency and the noise signal, are lowered by 10 dB when using a HR substrate instead of a 15 Ω.cm standard resistivity substrate. They are further reduced by more than 90 dB when a trap-rich SOI wafer is used. Those results highlight the important impacts of substrate resistivity and parasitic surface conduction on the signal integrity of CMOS VCOs.

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REFERENCES

[1] C. Soens, G. Van der Plas, P. Wambacq and S. Donnay, "Performance degradation of an LC-tank VCO by impact of digital switching noise," Proceedings of the 30th European Solid-State Circuits Conference, 2004, pp. 119-122, doi: 10.1109/ESSCIR.2004.1356632.

[2] S. Bronckers, K. Scheir, G. Van der Plas, G. Vandersteen and Y. Rolain, "A Methodology to Predict the Impact of Substrate Noise in Analog/RF Systems," in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 28, no. 11, pp. 1613-1626, Nov. 2009, doi: 10.1109/TCAD.2009.2030360.

[3] Singh, Pawan Kumar & Sharma, Sanjay. (2011). Substrate noise coupling in NMOS transistor for RF/analog circuits. International Journal of the Physical Sciences.

[4] K. Ben Ali, C. Roda Neve, A. Gharsallah, and J.-P. Raskin, "Digital substrate noise coupling into trap-rich hr-soi substrate," in Proc. of the 9th Workshop of the Thematic Network on Silicon-On-Insulator Technology, Devices and Circuits, EUROSOI 2013, Paris, France, Jan 2013.

[5] K. Ben Ali, C. Roda Neve, A. Gharsallah, and J.-P. Raskin, "RF performance of SOI CMOS technology on commercial 200 mm high resistivity silicon trap-rich wafers", IEEE Transactions on Electron Devices, vol. 61, no. 3, pp. 722-728, March 2014, doi: 10.1109/TED.2014.2302685.

[6] J.-M. Le Meil, B. Aspar, E. Desbonnets and J.-P. Raskin, "Engineered substrates: The foundation to meet current and future RF requirements," 2015 International Symposium on VLSI Technology, Systems and Applications, 2015, pp. 1-4, doi: 10.1109/VLSI-TSA.2015.7117546.

[7] N. Azuma *et al*., "Measurements and simulation of substrate noise coupling in RF ICs with CMOS digital noise emulator," 2013 9th International Workshop on Electromagnetic Compatibility of Integrated Circuits (EMC Compo), 2013, pp. 42-46, doi: 10.1109/EMCCompo.2013.6735170.

[8] Y. Wu, S. Gamble, B. M. Armstrong, V. F. Fusco, and J. A. C. Stewart, "SiO2 interface layer effects on microwave loss of high-resistivity CPW line," IEEE Microw. Guided Wave Lett., vol. 9, no. 1, pp. 10–12, Jun. 1999, doi: 10.1109/75.752108.

[9] D. Lederer and J.-P. Raskin, "Effective resistivity of fully processed SOI substrates", Elsevier Science, Pergamon, Solid-State Electronics, no. 49, pp. 491-496, 2005, doi.org/10.1016/j.sse.2004.12.003.

[10] C. Soens, G. Van der Plas, P. Wambacq, S. Donnay and M. Kuijk, "Performance degradation of LC-tank VCOs by impact of digital switching noise in lightly doped substrates," in IEEE Journal of Solid-State Circuits, vol. 40, no. 7, pp. 1472-1481, July 2005, doi: 10.1109/JSSC.2005.847301.

[11] M. Rack and J.-P. Raskin, "SOI technologies for RF and millimeter wave applications" ECS Trans., vol. 92, no. 4, pp. 79-94, July 2019, doi: 10.1149/09204.0079ecst.

[12] C. Roda Neve and J.-P. Raskin, "RF harmonic distortion of CPW lines on HR-Si and trap-rich HR-Si substrates", IEEE Transactions on Electron Devices, vol. 59, no. 4, pp. 924-932, April 2012, doi: 10.1109/TED.2012.2183598.

[13] M. Rack and J.-P. Raskin, "SOI Devices and Substrates towards RF and Millimeter Wave ICs," 2020 4th IEEE Electron Devices Technology & Manufacturing Conference (EDTM), 2020, pp. 1-4, doi: 10.1109/EDTM47692.2020.9117977.

[14] M. Rack, F. Allibert, J.-P. Raskin, "RF modelling of trap-rich passivated semiconductor substrates: Part I - Static and dynamic physics of carriers and traps", IEEE Transactions on Electron Devices, vol. 68, no. 9, pp. 4598-4605, September 2021, doi: 10.1109/TED.2021.3096777.

[15] D. Lederer and J.-P. Raskin, "New substrate passivation method dedicated to HR SOI wafer fabrication with increased substrate resistivity," in IEEE Electron Device Letters, vol. 26, no. 11, pp. 805-807, Nov. 2005, doi: 10.1109/LED.2005.857730.

[16] N. Checka, D. D. Wentzloff, A. Chandrakasan and R. Reif, "The effect of substrate noise on VCO performance," 2005 IEEE Radio Frequency integrated Circuits (RFIC) Symposium - Digest of Papers, 2005, pp. 523-526, doi: 10.1109/RFIC.2005.1489864.

[17] Huailin Liao, S. C. Rustagi, Jinglin Shi and Yong Zhong Xiong, "Characterization and modeling of the substrate noise and its impact on the phase noise of VCO," IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, 2003, 2003, pp. 247-250, doi: 10.1109/RFIC.2003.121393