Gate-controllable negative differential conductance in graphene tunneling transistors

2012 Semicond. Sci. Technol. 27 105018

(http://iopscience.iop.org/0268-1242/27/10/105018)

Semicond. Sci. Technol. **27** (2012) 105018 (7pp) doi:10.1088/0268-1242/27/10/105018

Gate-controllable negative differential conductance in graphene tunneling transistors

V Hung Nguyen[1,2], **Y M Niquet**[1] **and P Dollfus**[3]

[1] L_-Sim, SP2M, UMR-E CEA/UJF-Grenoble 1, INAC, F-38054 Grenoble, France
[2] Center for Computational Physics, Institute of Physics, VAST, PO Box 429 Bo Ho, Hanoi 10000, Vietnam
[3] Institut d'Electronique Fondamentale, UMR8622, CNRS, Université Paris-Sud, F-91405 Orsay, France

E-mail: nvhungphys@gmail.com

Received 17 May 2012, in final form 13 July 2012
Published 7 August 2012
Online at stacks.iop.org/SST/27/105018

Abstract
The transport characteristics and the possibility of controlling the negative differential conductance (NDC) in graphene tunnel field-effect transistors are investigated by means of numerical simulation. We find that an NDC effect can be achieved while the peak current and the peak-to-valley ratio (PVR) are controllable by tuning the gate voltage. Moreover, compared to the case of P–N junctions (Esaki diodes), the controllability of the potential profile in the gated region is shown to make the peak current higher and the PVR much less sensitive to the transition length between the two highly doped zones of the source and drain contacts. This work can stimulate further applications of this device in the field of high-frequency circuits, besides its potential for low-power digital operation.

(Some figures may appear in colour only in the online journal)

1. Introduction

The tunnel field-effect transistor (TFET) is a device where the inter-band tunneling current from the p-doped source contact to the n-doped drain one can be turned ON and OFF by tuning the gate voltage. This kind of device has a strong potential for low-power digital applications because of low OFF current and steep subthreshold swing that can be less than 60 mV/decade at room temperature (see the recent review [1] and references therein). However, the choice of a good material for designing TFETs is still a debate due to various constraints regarding material properties, material quality and processing issues. For instance, a Si TFET has a low ON current due to the large Si bandgap, while materials with smaller bandgaps such as Ge can be used alternatively but at the expense of an increased OFF current [2]. In this context, carbon-based materials (i.e. carbon nanotube and graphene nanostructures) with various possibilities of bandgap engineering appear to be very promising for TFET applications [3–9] thanks to the Zener tunneling current higher than in conventional semiconductors [10].

Besides the characteristics above, the TFET is also a good candidate for RF electronic applications since it can exhibit a strong negative differential conductance (NDC) effect when a drain voltage is applied to the p-doped zone [11], as in the well-known Esaki tunnel diode [12]. Compared to the tunnel diodes, this device additionally provides the possibility of controlling the potential profile in the center zone between the two heavily doped contacts. On this basis, the TFET shows a good ability to control the inter-band tunneling current and the peak-to-valley ratio (PVR) with the gate, which may be very useful for high-frequency applications [1, 13–17].

Graphene-based TFETs have been already studied with a view to digital applications [5–9], but to our knowledge their ability to exhibit a gate-controllable NDC effect has not yet been investigated properly. This work aims at filling this gap by means of self-consistent simulations based on the Green function technique within an atomistic tight-binding model. In section 2, we present briefly the model used and the simulated device. We also discuss the possibilities of inducing the bandgap in graphene needed for TFET operation. We consider especially the case of graphene on a hexagonal boron nitride

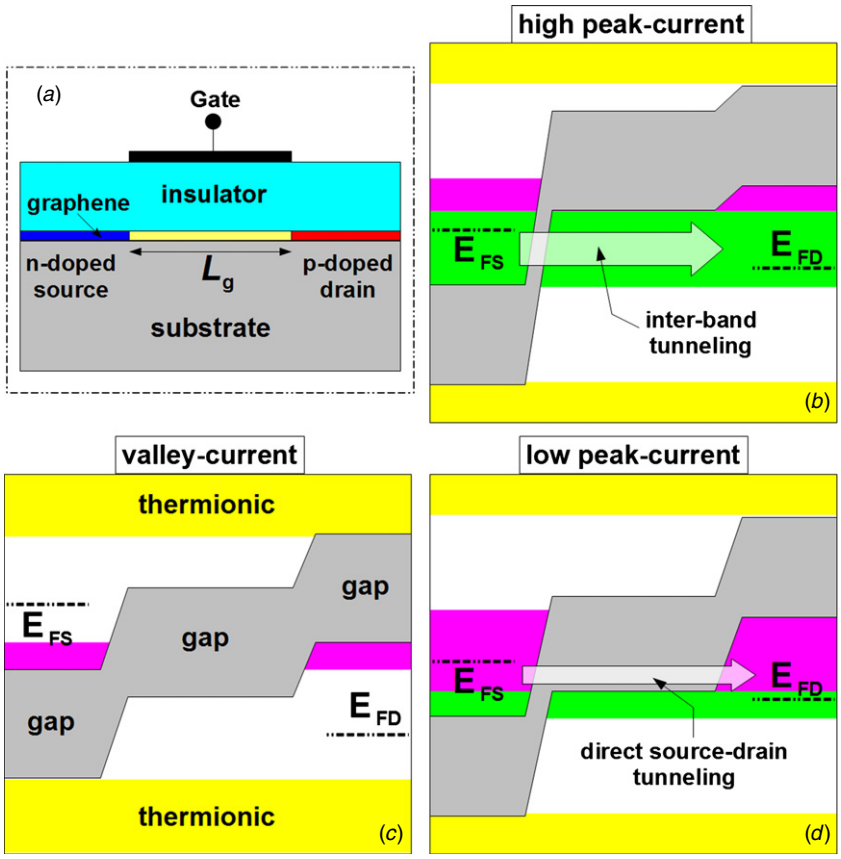

Figure 1. Sketch of the considered graphene TFET (*a*) and its band diagram in the different states of high peak current (*b*), low peak current (*d*) and valley current (*c*).

(h-BN) substrate. The results are presented and discussed in section 3, while the conclusion is drawn in section 4.

2. Model and simulated device

The simulated graphene TFET together with its band diagram in the different states of peak and valley currents are schematized in figure 1. Similar to what happens in the tunnel diodes [12, 18–20], at a low bias the peak current is mainly governed by the inter-band tunneling through the junction (see the diagrams in figures 1(*b*) and (*d*)). The valley current occurs at a high bias when the contribution of the inter-band tunneling is reduced (see the diagram in figure 1(*c*)). In addition, as illustrated schematically in the diagrams of figure 1 and demonstrated below, the inter-band tunneling in this device is also tunable by changing the gate voltage, which results in the possibility of controlling the peak current and the PVR.

We assume the transverse width of the graphene sheet to be much larger than the typical device length along the transport direction (i.e. a few tens of nanometers), so that Bloch periodic boundary conditions can be applied in the transverse direction [20]. Our approach is based on a nearest-neighbor tight-binding Hamiltonian [21] which is solved self-consistently with the 2D Poisson equation using the Green function technique [22]. To achieve the transport characteristics discussed above, a finite bandgap in graphene is a key point. Different methods have been proposed to generate such a bandgap in 2D graphene sheets, with the value ranging from a few to hundreds of meV [23–38], which has stimulated investigations of various graphene nanodevices [9, 18, 20, 39–42]. In particular, a bandgap can be achieved in graphene on an h-BN substrate [23–29], by doping and impurities [30, 31], by inserting a nanohole lattice into the graphene sheet [32], by applying a vertical electric field to bilayer graphene [33], or by some other methods [34–38]. In what follows, we especially focus on the device wherein the monolayer graphene channel is supported on an h-BN substrate. On the one hand, it has been predicted that in the case of Bernal stacking on h-BN, a bandgap can open in graphene and reach the value of 53 meV [23] or 100 meV [24]. The bandgap may even increase up to more than 200 meV under external pressure [25–27]. On the other hand, it has been recently shown that graphene on h-BN has higher mobility than on any other substrate [43], i.e. about 275 000 $cm^2\ Vs^{-1}$ at low temperature and 125 000 $cm^2\ Vs^{-1}$ at room temperature [44], which makes it reasonably possible to achieve ballistic transport in realistic devices. We thus propose to use this material as the substrate of simulated graphene TFETs to take advantages of both the bandgap engineering and the high-carrier mobility. Besides, similar to the case of bilayer graphene, it has been shown in [28] that the bandgap of monolayer graphene sandwiched between two h-BN layers can be tuned by a strong (typically $\sim$ 10 V nm^{-1}) electric

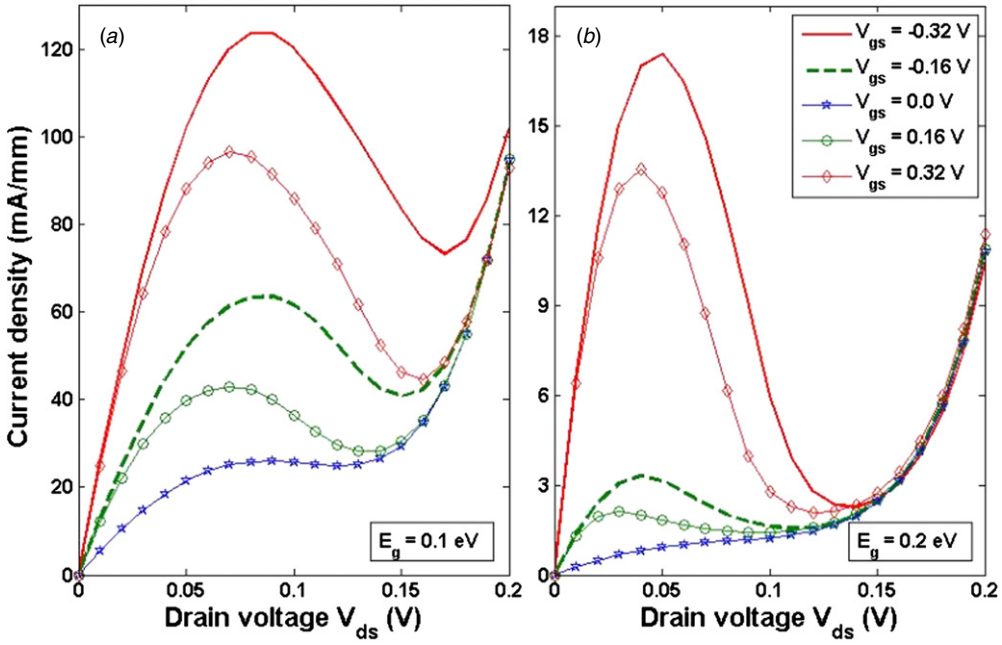

Figure 2. $I - V_{ds}$ characteristics of graphene TFET at different gate voltages V_{gs} and for different bandgaps: $E_g = 0.1$ eV (*a*) and 0.2 eV (*b*). Everywhere, the gate length is $L_g = 20$ nm, the gate insulator thickness $T_{\text{ins}} = 4$ nm and the doping concentration $N_D = 2.5 \times 10^{16}$ m^{-2} in the heavily doped contacts.

field (gate voltage). However, this effect shall be negligible [29] here, since the applied electric field is limited to about 0.1 V nm^{-1}. The bandgap of graphene was hence considered to be independent of the gate voltage and chosen in the energy range mentioned above, i.e. from 0.1 to 0.3 eV.

In conventional semiconducting devices, it is usually necessary to include the effect of different scattering mechanisms in the simulation such as the electron–phonon interaction. Additionally, in devices where bipolar transport occurs, carrier generation and recombination processes may play an important role. However, on the one hand, in 2D graphene sheets the mean free path of electrons is typically larger than 400 nm even at room temperature [45]. On the other hand, some investigations have shown that the generation/recombination time in graphene is typically longer than 1 ps [46]. With an average drift velocity $\langle v_d \rangle \simeq 5 \times 10^5$ ms^{-1} [47], the generation/recombination length is thus larger than 500 nm. Since these characteristic lengths are much longer than the typical size of the simulated device, both the electron–phonon scattering and the carrier generation/recombination processes were appropriately neglected here, i.e. our simulations have been performed in the ballistic approximation.

3. Results and discussion

We now go to explore the transport characteristics of graphene TFETs. All simulations were performed at room temperature. In figure 2, we display the obtained $I - V_{ds}$ curves at different gate voltages and for two different graphene bandgaps: $E_g = 0.1$ eV (figure 2(*a*)) and 0.2 eV (figure 2(*b*)). A gate-controllable NDC effect is clearly observed in figure 2. The peak current is high when the charge density in the gated region is high (e.g., see the cases of $V_{gs} = -0.32$ V for p-type carriers and 0.32 V for n-type ones), and the NDC effect disappears when the density is low (see the case of $V_{gs} = 0$ V). This feature is clearly explained by the diagrams of figure 1 as discussed above. In fact, the current through this device can be split into three components: the thermionic transmission, the direct source–drain (DSD) tunneling and the inter-band tunneling. While the first two components are always small but can contribute significantly as leakage in the valley regime, the latter one is generally high and can result in a high peak current. In principle, to efficiently switch off the valley current, a large bandgap is essentially required. Indeed, it is shown clearly in figure 2 that an increase of the bandgap strongly reduces the valley current. Therefore, though the peak current is reduced too, the NDC effect is more pronounced, i.e. the maximum value of PVR is about 2.2 in figure 2(*a*) for $E_g = 0.1$ eV and ∼8 in figure 2(*b*) for $E_g = 0.2$ eV. However, due to the reduced peak current, the PVR may reach a maximum value and then reduce when further increasing E_g. For instance, the PVR varies from ∼8 to ∼2 when changing E_g from 0.2 to 0.3 eV (not shown) in the same device. This result suggests that the best device operation (either a high peak current or a large PVR) is obtained for a moderate bandgap (e.g., ∼0.2 eV here) and, as discussed in [18] for graphene P–N junctions, with a potential-energy difference between the source and drain contacts at the zero bias about two times larger than E_g.

To see more clearly the gate-controllable NDC effect, we display in figure 3(*a*) the evolution of peak current J_p, valley current J_v and PVR with respect to the gate voltage for the optimum case $E_g = 0.2$ eV. Indeed, the $J_p - V_{gs}$ curve exhibits a typical form of gate-controlled current in TFETs [1]. Additionally, we find that the valley current J_v is reached at lower V_{ds} (see figure 2) and its value reduces when tuning the

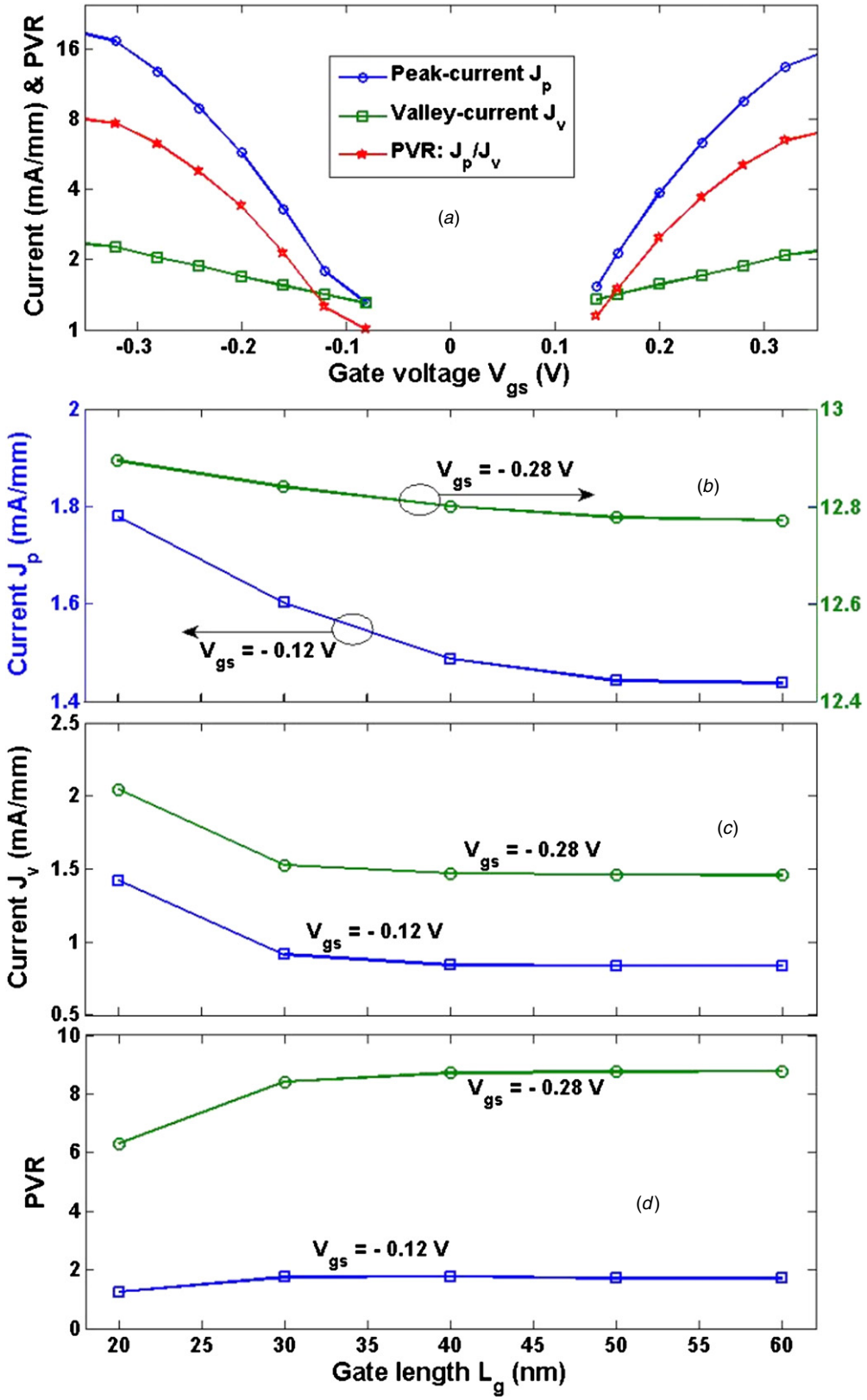

Figure 3. (*a*) The peak, the valley currents and the PVR as a function of V_{gs} for $L_g = 20$ nm. The peak (*b*), the valley (*c*) currents and the PVR (*d*) as a function of L_g for different V_{gs}. The other device parameters are the same as in figure 2(*b*).

gate voltage from the high peak-current state to the low peak-current state. However, thanks to the strong V_{gs} dependence of the peak current, the PVR is strongly tunable by the gate voltage.

Since the characteristics observed above are essentially due to the controllability of the potential profile in the gated region, the device operation may be influenced by the gate length, especially, in the short-channel case. To examine this

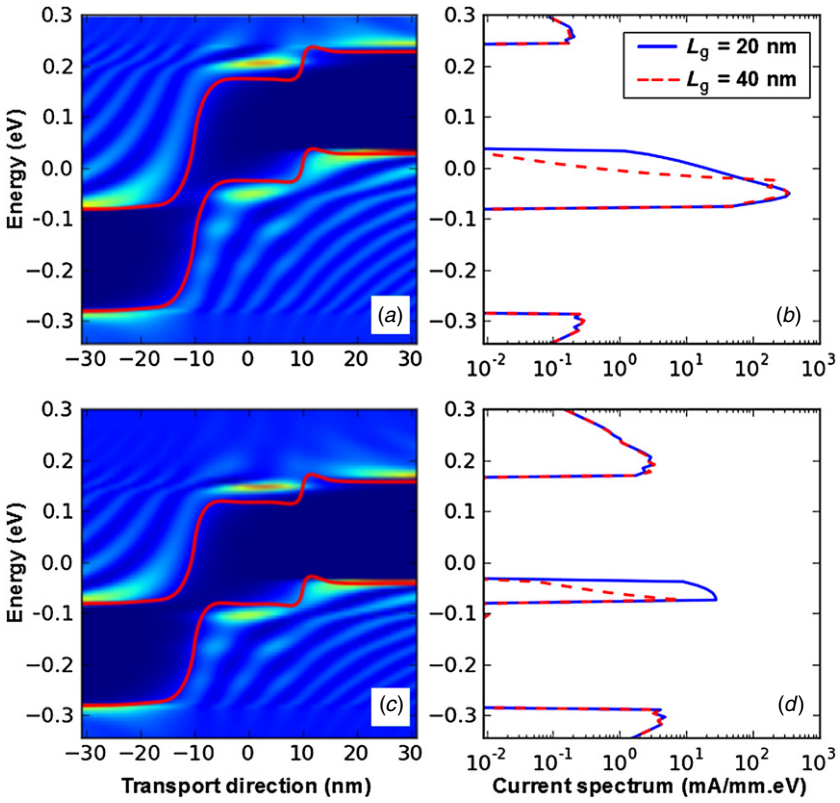

Figure 4. ((*a*) and (*c*)) Local density of states together with the band profile (red-solid lines). ((*b*) and (*d*)) Current spectrum plotted as a function of energy in the peak current ($V_{ds} = 50$ mV in (*a*,*b*)) and the valley-current ($V_{ds} = 120$ mV in (*c*,*d*)) regimes. The gate voltage $V_{gs} = -0.28$ V and the other device parameters are the same as in figure 2(*b*).

effect, we show the peak current, the valley current and the PVR as a function of gate length L_g in figures 3(*b*), (*c*) and (*d*), respectively. Generally speaking, it is shown that both the peak and the valley currents are reduced when increasing the gate length. It is nothing but the consequence of the reduced DSD tunneling, i.e. the short-channel effect. This feature is clearly illustrated by the pictures of current spectrum shown in figure 4: while the inter-band tunneling and thermionic components seem to be unchanged, the DSD tunneling current is strongly reduced when increasing L_g. When the gate is long enough, this DSD component vanishes and the total current reaches its saturation value (see in figures 3(*b*) and (*c*)). This saturation value is essentially determined by the remaining (inter-band and thermionic) components, which are L_g-independent (see in figures 4(*b*) and (*d*)). Moreover, we find from figure 3(*b*) that when the device is in the high peak-current state, the peak current is weakly sensitive to the gate length, i.e. when increasing L_g from 20 to 60 nm J_p is reduced by ~ 0.12 mA mm^{-1} for $V_{gs} = -0.28$ V, while it is reduced by ~ 0.36 mA mm^{-1} for $V_{gs} = -0.12$ V. This result is well explained by the relative contribution of DSD tunneling to the current, which is more important when the device is in the low peak-current state, as illustrated schematically by the diagrams of figures 1(*b*) and (*d*). Finally, due to the L_g dependence of the peak and the valley currents discussed above, we find from figure 3(*d*) that the PVR increases and reaches its saturation value when the gate length is large enough, e.g., larger than ~ 40 nm in the device considered here.

Another important point to consider is the influence of the transition region between the different doped zones on the device operation. An increase of the transition length is known to strongly degrade the value of peak current and PVR in the P–N junctions [18–20]. This is basically explained by the fact that the larger the transition length, the smaller the slope of potential profile and hence the stronger the influence of evanescent states in the transition region on the inter-band tunneling current. To investigate the effect of the transition region in TFETs, we compare in figure 5 their potential profile for different gate insulator thicknesses T_{ins} with that of an ungated P–N junction having the same distance between the two heavily doped zones. It appears that the slope of the potential profile in the transition region between the gated and the heavily doped zones of the TFETs increases when reducing the gate insulator thickness and is steeper than that in the transition region of the P–N junctions. Moreover, differently from the case of the P–N junctions, the slope of the potential profile seems not to be affected by an increase of the distance between the two heavily doped contacts if the gate voltage is applied over the whole channel, e.g., compare the two cases of $L_g = 20$ and 40 nm (with the same $T_{\text{ins}} = 4$ nm) in figure 5. This property leads to the fact that (i) a gate voltage applied to the tunnel FET can make the peak current and the PVR higher than those in the P–N junction (see in the inset of figure 5), and (ii) the NDC effect is weakly sensitive to L_g in the former device (see in figure 3), while the peak current and the PVR are strongly reduced when increasing the transition length in the latter one [18]. It suggests a good way to avoid the sensitivity of

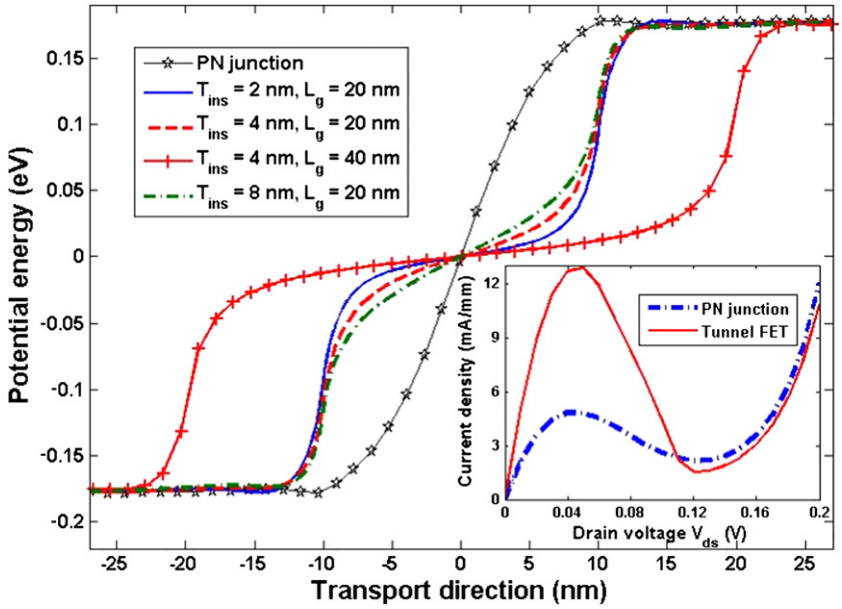

Figure 5. The potential profile of graphene TFET at $V_{ds} = V_{gs} = 0$ for different gate insulator thicknesses T_{ins} in comparison with that of a P–N junction. The inset shows the $I - V_{ds}$ characteristics at $V_{gs} = -0.28$ V of a tunnel FET in comparison with that in the P–N junction with the same length $L_g = 30$ nm. The other device parameters are the same as in figure 2(*b*).

the operation of P–N junction devices to the transition length without developing any technique to design complex graphene hetero-structures with a gapless transition region [19, 20].

4. Conclusion

In this work, we have investigated the transport characteristics of graphene tunnel FETs using atomistic quantum simulation and discussed the possibility of controlling the NDC effect. We find that a strong NDC effect at room temperature can be achieved in gapped graphene tunnel FETs, while the current peak and the PVR are controllable by tuning the gate voltage. The role of device parameters such as the gate length and the gate insulator thickness has been analyzed. As an important result, we have shown that, in comparison with the graphene P–N junction where the PVR is strongly dependent on the transition length, the gate controllability of the potential profile in the device channel makes the PVR in the TFET higher and weakly sensitive to the gate length (distance between the two highly doped contacts). Provided that the appropriate bandgap of about 0.2 eV may be generated in graphene, we believe that the proposed device is a valuable option to achieve circuits operating at very high frequency with limited problems of variability which are known to reduce the applicability of tunneling devices. The concept could be extended to other carbon-based nanostructures as carbon nanotubes, graphene nanoribbons, graphene nanomesh and bilayer graphene, or to other small bandgap and low effective mass semiconductors.

Acknowledgments

This work was partially supported by the French ANR through the projects NANOSIM-GRAPHENE (ANR-09-NANO-016) and MIGRAQUEL (ANR-10-BLAN-0304). One of the authors (VHN) acknowledges the Vietnam's National Foundation for Science and Technology Development (NAFOSTED) for financial support under the project no. 103.02-2010.33. The authors would like to thank Arnaud Bournel for fruitful discussions.

References

[1] Seabaugh A C and Zhang Q 2010 *Proc. IEEE* **98** 2095
[2] Toh E-H, Wang G H, Samudra G and Yeo Y-C 2008 *J. Appl. Phys.* **103** 104504
[3] Appenzeller J, Lin Y-M, Knoch J and Avouris Ph 2004 *Phys. Rev. Lett.* **93** 196805
[4] Koswatta S O, Lundstrom M S and Nikonov D E 2008 *Appl. Phys. Lett.* **92** 043125
Koswatta S O, Lundstrom M S and Nikonov D E 2009 *IEEE Trans. Electron Devices* **56** 456
[5] Zhang Q, Fang T, Xing H, Seabaugh A and Jena D 2008 *IEEE Electron Device Lett.* **29** 1344
[6] Zhao P, Chauhan J and Guo J 2009 *Nano Lett.* **9** 684
[7] Fiori G and Iannaccone G 2009 *IEEE Electron Device Lett.* **30** 1096
[8] Lam K-T, Seah D, Chin S-K, Kumar S B, Samudra G, Yeo Y-C and Liang G 2010 *IEEE Electron Device Lett.* **31** 555
[9] Michetti P, Cheli M and Iannaccone G 2010 *Appl. Phys. Lett.* **96** 133508
[10] Jena D, Fang T, Zhang Q and Xing H 2008 *Appl. Phys. Lett.* **93** 112106
[11] Leburton J P, Kolodzey J and Briggs S 1988 *Appl. Phys. Lett.* **52** 1608
[12] Esaki L 1958 *Phys. Rev.* **109** 603
[13] Uemura T and Baba T 1994 *Japan. J. Appl. Phys.* **33** L207
[14] Omura Y 1996 *Japan. J. Appl. Phys.* **35** L1401
[15] Uemura T and Baba T 1997 *IEEE Electron Device Lett.* **18** 225
[16] Koga J and Toriumi A 1997 *Appl. Phys. Lett.* **70** 2138
[17] Koga J and Toriumi A 1999 *IEEE Electron Device Lett.* **20** 529
[18] Hung Nguyen V, Bournel A and Dollfus P 2011 *J. Appl. Phys.* **109** 093706

[19] Hung Nguyen V, Mazzamuto F, Saint-Martin J, Bournel A and Dollfus P 2011 *Appl. Phys. Lett.* **99** 042105
[20] Hung Nguyen V, Mazzamuto F, Saint-Martin J, Bournel A and Dollfus P 2012 *Nanotechnology* **23** 065201
[21] Hung Nguyen V, V Nam Do, Bournel A, Lien Nguyen V and Dollfus P 2009 *J. Appl. Phys.* **106** 053710
[22] Hung Nguyen V, Mazzamuto F, Bournel A and Dollfus P 2012 arXiv:1201.4258v2
[23] Giovannetti G, Khomyakov P A, Brocks G, Kelly P J and van den Brink J 2007 *Phys. Rev.* B **76** 073103
[24] Kharche N and Nayak S K 2011 *Nano Lett.* **11** 5274
[25] Xu Y, Guo Z, Chen H, Yuan Y, Lou J, Lin X, Gao H, Chen H and Yu B 2011 *Appl. Phys. Lett.* **99** 133109
[26] Fan Y, Zhao M, Wang Z, Zhang X and Zhang H 2011 *Appl. Phys. Lett.* **98** 083103
[27] Kan E, Ren H, Wu F, Li Z, Lu R, Xiao C, Deng K and Yang J 2012 *J. Phys. Chem.* C **116** 3142
[28] Quhe R *et al* 2012 *NPG Asia Mater.* **4** e6
[29] Balu R, Zhong X, Pandey R and Karna S P 2012 *Appl. Phys. Lett.* **100** 052104
[30] Liu H, Liu Y and Zhu D 2011 *J. Mater. Chem.* **21** 3335
[31] Escaño, M. C. S., Nguyen T Q and Kasai H 2011 *Chem. Phys. Lett.* **515** 85
[32] Bai J, Zhong X, Jiang S, Huang Y and Duan X 2010 *Nat. Nanotechnol.* **5** 190
[33] Oostinga J B, Heersche H B, Liu X, Morpurgo A F and Vandersypen L M K 2008 *Nat. Mater.* **7** 151
[34] Vitali L, Riedl C, Ohmann R, Brihuega I, Starke U and Kern K 2008 *Surf. Sci.* **602** L127
[35] Liu L and Shen Z 2009 *Appl. Phys. Lett.* **95** 252104
[36] Dong X *et al* 2009 *Phys. Rev. Lett.* **102** 135501
[37] Zhou J, Wu M M, Zhou X and Sun Q 2009 *Appl. Phys. Lett.* **95** 103108
[38] Enderlein C, Kim Y S, Bostwick A, Rotenberg E and Horn K 2010 *New J. Phys.* **12** 033014
[39] Hung Nguyen V, Bournel A and Dollfus P 2010 *J. Phys.: Condens. Matter* **22** 115304
[40] Cheli M, Michetti P and Iannaccone G 2010 *IEEE Trans. Electron Devices* **57** 1936
[41] Giavaras G and Nori F 2010 *Appl. Phys. Lett.* **97** 243106
[42] Hung Nguyen V, Bournel A and Dollfus P 2011 *Semicond. Sci. Technol.* **26** 125012
[43] Dean C R *et al* 2010 *Nat. Nanotechnol.* **5** 722
[44] Zomer P J, Dash S P, Tombros N and van Wees B J 2011 *Appl. Phys. Lett.* **99** 232104
[45] Novoselov K S, Geim A K, Morozov S V, Jiang D, Zhang Y, Dubonos S V, Grigorieva I V and Firsov A A 2004 *Science* **306** 666
[46] Rana F 2007 *Phys. Rev.* B **76** 155431
Rana F, George P A, Strait J H, Dawlaty J, Shivaraman S, Chandrashekhar M and Spencer M G 2009 *Phys. Rev.* B **79** 115447
[47] Shishir R S, Ferry D K and Goodnick S M 2009 *J. Phys.: Conf. Ser.* **193** 012118