Thermal Coupling between FD-SOI FETs at Cryogenic Temperatures

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***Abstract*—This work studies the thermal cross-coupling between two side-by-side FD-SOI MOSFETs at liquid nitrogen temperature in comparison to the room temperature one. The temperature rise experienced by a device due to the self-heating of a neighbor one is estimated by making a comparison to a referenced g_m/I_d curve as a function of chuck temperature. The impact of thermal coupling effects is studied on main digital (SS, V_{th}, I_{on}, I_{off} and I_{on}/I_{off}) and analog (g_m and g_m/I_d) figures of merit. We demonstrate that electrical parameters degradation caused by the operation (heating) of the neighbor device can be up to 50 % more important at 77 K than at 295 K.**

Keywords- Cryogenic temperatures; FD-SOI; MOSFET, self-heating; thermal coupling.

I. Introduction

Quantum computers have the potential to solve problems computationally unfeasible on classical computers [1]. For proper operation, the qubits need to be cooled down to cryogenic temperatures with its control electronics placed in close vicinity. Fully depleted silicon-on-insulator (FD-SOI) CMOS technology is considered as an excellent platform for cryogenic applications such as spatial applications and quantum computing [2]. In spite of the numerous advantages of FD-SOI technology such as its outstanding electrostatic control, very low mismatch and low-power [3], [4], the lower thermal conductivity of the buried oxide w.r.t silicon makes it more subject to self-heating (SH) than their bulk counterparts [5]. Self-heating can raise the device temperature significantly above the ambient temperature and its surroundings [6], [7], which degrades device performance and can also alter qubit state. It is thus crucial to characterize self-heating down to cryogenic temperatures as the channel temperature rise displays a strongly non-linear dependence with dissipated power [8].

Furthermore, it is worth emphasizing that self-heating does not only impact the electrical characteristics of the device itself but also the electrical characteristics of neighboring devices. Indeed, the heat generated by the self-heated device propagates to the surroundings which results in thermal coupling effects. In our previous work [9], the impact of thermal coupling on the digital and analog figures of merit was analyzed at room temperature. Overall variations were demonstrated to remain limited with a maximum degradation observed on I_{off} (+ 30% increase).

In this paper, the impact of heat generated by one device operation on the characteristics of a neighbor device is studied at liquid nitrogen temperature in comparison to room temperature. The corresponding temperature rise is estimated and the impact of thermal coupling effects is studied on I_d-V_{gs} characteristics, digital and analog figures of merit.

II. Device Details and Experimental Setup

The devices under study are fabricated by an industrial FD-SOI process. They consist of two multi-fingers nFETs placed side-by-side at 2.76 µm distance from each other as schematically represented in Fig. 1: (i) FET 1 features a gate length (L) < 30 nm and a total width (W) of 8 µm and (ii) FET 2 (heater) features L < 30 nm and W of 32 µm. As FET 2 is larger and thus dissipates more power, it serves as the heating device to demonstrate thermal cross-coupling effects. LakeShore CPX cryogenic probe station is used to perform I-V measurements from room temperature (295 K) down to liquid nitrogen temperature (77 K) and I-V characteristics are measured using a Keysight B1500A semiconductor analyzer.

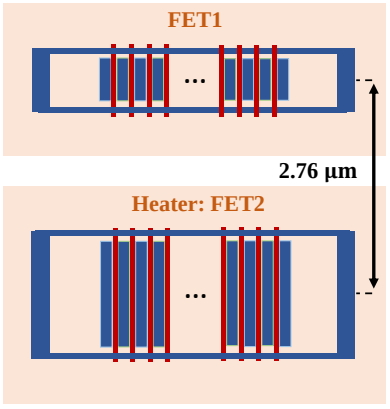

Fig. 1. Schematic (not to scale) of two multi-fingers FD-SOI nFETs placed 2.76 µm away from each other. Bottom FET is used to heat the top FET.

III. Results and Discussion

In order to evaluate the temperature increase ΔT resulting from thermal coupling effects, one first needs to

measure the electrical characteristics of FET 1 as a function of temperature. During this step, FET 2 terminals are left floating/unbiased while the chuck temperature is varied. These measurements serve as a temperature reference. Secondly, FET 1 is measured again but this time with FET 2 biased at different usual operation conditions. Thanks to the temperature reference, the temperature rise ΔT in FET 1 when FET 2 operates can be estimated.

A. *Temperature Characterization*

Fig. 2 shows I_d-V_{gs} characteristics of FET 1 biased in a linear regime (V_{ds} = 50 mV) at different temperatures, highlighting a strong temperature dependence, particularly visible in the subthreshold region. A threshold voltage shift of ΔV_{th} = 96 mV (Table I) is observed when moving from 295 K (V_{th} = 0.392 V) to 77 K (V_{th} = 0. 296 V). The threshold voltage is computed using the second derivative method [10].

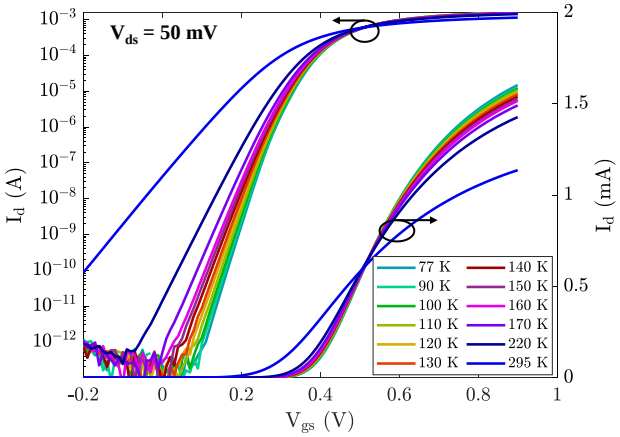

Fig. 2. Drain current I_d of FET 1 vs gate voltage V_{gs} in linear regime (V_{ds} = 50 mV) at different temperatures.

From I_d-V_{gs} characteristics of FET 1 (Fig. 2), one can compute g_m/I_d of FET 1 as function of temperature as shown in Fig. 3. The corresponding variations of g_m/I_d of FET 1 serve as a temperature reference to estimate afterwards the temperature rise in FET 1 when FET 2 operates and its heat propagates to the surroundings.

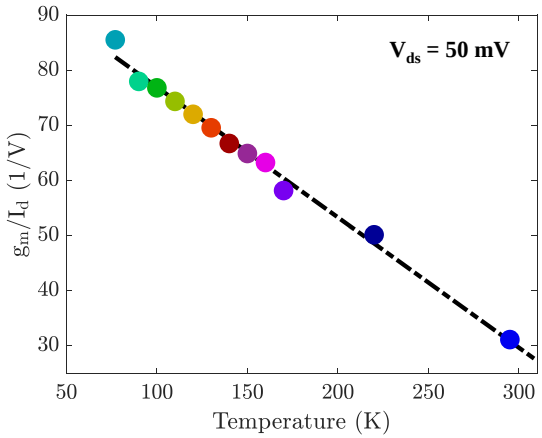

Fig. 3. g_m/I_d of FET 1 extracted at I_d = 10^{-9} A vs temperature in linear regime (V_{ds} = 50 mV).

B. *Thermal Coupling Effects*

Fig. 4 plots I_d-V_{gs} curves of FET 1 biased in a linear regime (V_{ds} = 50 mV) when FET 2 is biased in cold FET mode (V_2 = V_{gs2} = V_{ds2} = 0 V) and in different operation conditions in saturation and strong inversion regimes (V_2 = 0.5, 0.6, 0.8 and 0.9 V) at both 77 K and 295 K. Hold time for FET 1 is set to two minutes in order to ensure sufficient heating (and heat propagation) of/from FET 2 prior to measurements of FET 1. Indeed, stabilization of FET 1 drain current after heating of FET 2 was observed after around 70 seconds (not shown). It was decided to increase the hold time to 120 seconds to guarantee temperature/current stability.

As shown in Fig. 4, the subthreshold swing SS at 77 K is more impacted by thermal coupling (dissipated power of FET 2) than at 295 K. Indeed, a ~15% increase in SS at 77 K is observed (Table I) when FET 2 is biased at V_2 = 0.9 V compared to only ~4% at 295 K. The threshold voltage V_{th} is however less sensitive to thermal coupling effects at both 77 K and 295 K with variations limited $|\Delta V_{th}| < 10$ mV as shown in Table I.

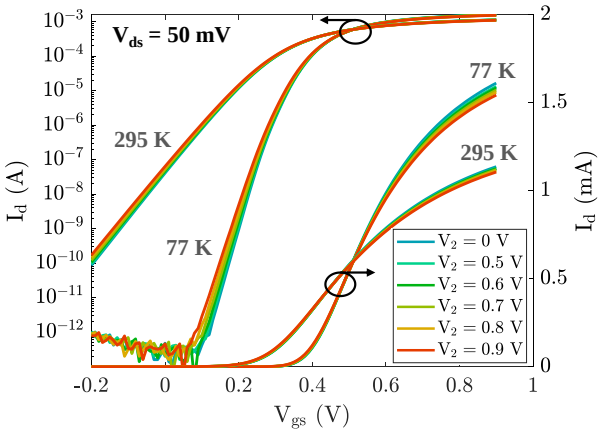

Fig. 4. I_d of FET 1 vs gate voltage V_{gs} in linear regime (V_{ds} = 50 mV) at 77 K and 295 K when FET 2 is under different bias conditions.

A linear reduction of g_m/I_d of FET 1 vs the power of FET 2 from 85.5 to 74.6 V^{-1} at 77 K and from 31.1 to 29.3 V^{-1} at 295 K is demonstrated in Fig. 5. By using g_m/I_d of FET 1 vs temperature plot (Fig. 3), one can estimate a temperature increase of ΔT = 33 K and 4 K for the case when V_2 = 0.9 V at 77 and 295 K, respectively, highlighting strong sensibility to thermal coupling (TC) effects at cryogenic temperature. It is worth mentioning that although the dissipated power of FET 2 at fixed V_2 is higher at 77 K than at 295 K (due to higher I_d at 77 K), the thermal coupling effects are still more important at cryogenic temperature. Indeed, at constant power P = 20 mW, g_m/I_d of FET 1 decreases by 8.4 % (from 85.5 to 78.3 V^{-1}) at 77 K while it only decreases by 2.9 % (from 31.1 to 30.2 V^{-1}) at 295 K.

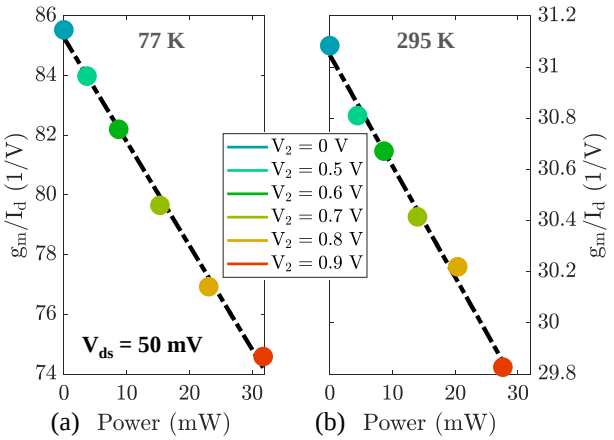

Fig. 5. g_m/I_d of FET 1 vs dissipated power of FET 2 at 77 K and 295 K, when FET 1 is biased at V_{ds} = 50 mV.

Keeping this in mind, the following part of this work is focused on the analysis of TC effects on various figures of merit (FoM) of FET 1, i.e. when it is operating in saturation regime. One of the main FoM for digital applications is the I_{on}/I_{off} ratio. While I_{off} is classically measured at V_{gs} = 0 V, I_d in this condition becomes very small (< 10^{-10} A) at 77 K, so it is decided to take I_{off} at V_{gs} = 0.1 V in the framework of this work, so that $I_{on} = I_d(V_{gs} = V_{ds} = 0.8$ V) and $I_{off} = I_d(V_{gs} = 0.1$ V, $V_{ds} = 0.8$ V). As shown in Fig. 6, I_{on}/I_{off} ratio suffers a significant 77 % reduction at 77 K when FET 2 is biased at V_2 = 0.9 V while this reduction is limited to 25 % at 295 K. This degradation of the I_{on}/I_{off} ratio is strongly related to the increase of I_{off} (Table I) whereas I_{on} reduction (Table I) remains small (< 1 %).

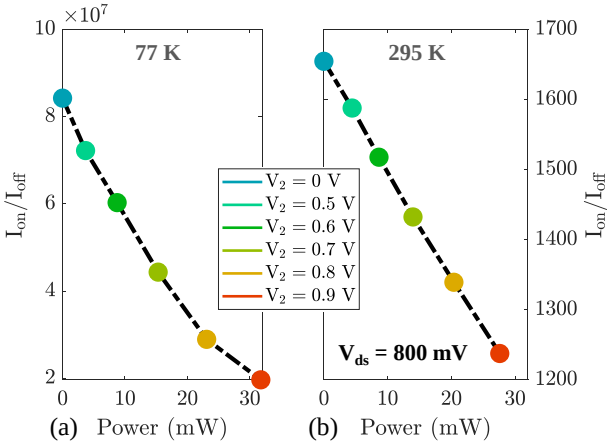

Fig. 6. I_{on}/I_{off} ratio of FET 1 vs dissipated power of FET 2 at 77 and 295 K, when FET 1 is biased at V_{ds} = 800 mV. I_{on} and I_{off} are respectively defined at V_{gs} of 0.8 and 0.1 V).

Another FoM, particularly important for analog applications, is the transconductance (here extracted as peak value at V_{ds} = 800 mV), which appears only slightly degraded by the operation of FET 2 with a reduction of 1.7 % (1.5 %) at 77 K (295 K) (Table I). Indeed, in saturation and inversion regimes FET 1 itself is subjected to self-heating making it less sensitive to external heat sources (e.g. cross-thermal coupling). In weak inversion regime (at V_{ds} = 800 mV) at $I_d = 10^{-7}$ A, g_m/I_d decreases with V_2 from 69.6 to 63 V^{-1} (-9.5 %) at 77 K and from 30.2 to 29.2 (-3.3 %) at 295 K (Table I).

An important remark is that the thermal coupling effects reported in Table I are specific to the configuration described in Section II. Indeed, thermal effects are strongly layout dependent. Different transistors dimensions/geometries and distances between neighboring devices can therefore result to smaller/stronger self-heating and thermal coupling as demonstrated in [8], [11].

IV. Conclusion

In this work, the importance of thermal coupling (and related temperature rise) particularly at cryogenic temperatures and its impact on different FoMs was demonstrated. Temperature rise in FET 1 due to operation of FET 2 was revealed to be stronger at 77 K (ΔT = 33 K) wrt 295 K (ΔT = 4 K). Similarly, the FoMs degradation is more important at 77 K comparing to its degradation at 295 K. The strongest impact was observed on I_{on}/I_{off} ratio with a 77% reduction at 77 K wrt 25 % at 295 K when the neighbor device is biased at $V_{gs2} = V_{ds2}$ = 0.9 V due to stronger temperature increase at 77 K. Electrical characterization over a wide range of temperatures and devices is thus crucial for the development of accurate compact models.

Acknowledgment

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References

[1] T. D. Ladd, F. Jelezko, R. Laflamme, Y. Nakamura, C. Monroe, and J. L. O'Brien, 'Quantum computers', *Nature*, vol. 464, no. 7285, pp. 45–53, Mar. 2010, doi: 10.1038/nature08812.

[2] E. Charbon, F. Sebastiano, A. Vladimirescu, H. Homulle, S. Visser, L. Song *et al.*, 'Cryo-CMOS for quantum computing', in *2016 IEEE International Electron Devices Meeting (IEDM)*, San Francisco, CA, USA: IEEE, Dec. 2016, p. 13.5.1-13.5.4. doi: 10.1109/IEDM.2016.7838410.

[3] S. Makovejev, B. Kazemi Esfeh, V. Barral, N. Planes, M. Haond, D. Flandre *et al.*, 'Wide frequency band assessment of 28 nm FDSOI technology platform for analogue and RF applications', in *2014 15th International Conference on Ultimate Integration on Silicon (ULIS)*, Apr. 2014, pp. 53–56. doi: 10.1109/ULIS.2014.6813904.

[4] B. C. Paz, L. Le Guevel, M. Cassé, G. Billiot, G. Pillonnet, A. G. M. Jansen *et al.*, 'Variability Evaluation of 28nm FD-SOI Technology at Cryogenic Temperatures down to 100mK for Quantum Computing', in *2020 IEEE Symposium on VLSI Technology*, Honolulu, HI, USA: IEEE, Jun. 2020, pp. 1–2. doi: 10.1109/VLSITechnology18217.2020.9265034.

[5] S. Makovejev, N. Planes, M. Haond, D. Flandre, J.-P. Raskin, and V. Kilchytska, 'Comparison of self-heating and its effect on analogue performance in 28nm bulk and FDSOI', *Solid-State Electronics*, vol. 115, pp. 219–224, Jan. 2016, doi: 10.1016/j.sse.2015.08.022.

[6] K. Triantopoulos, M. Cassé, S. Barraud, S. Haendler, E. Vincent, M. Vinet *et al.*, 'Self-Heating Effect in FDSOI Transistors Down to Cryogenic Operation at 4.2 K', *IEEE Transactions on Electron Devices*, vol. 66, no. 8, pp. 3498–3505, Aug. 2019, doi: 10.1109/TED.2019.2919924.

[7] P. A. T Hart, M. Babaie, A. Vladimirescu, and F. Sebastiano, 'Characterization and Modeling of Self-Heating in Nanometer Bulk-CMOS at Cryogenic Temperatures', *IEEE Journal of the*

Electron Devices Society, vol. 9, pp. 891–901, 2021, doi: 10.1109/JEDS.2021.3116975.

[8] F. E. Bergamaschi, T. M. Frutuoso, B. C. Paz, G. Billiot, A. G. M. Jansen, P. Galy *et al.*, 'Experimental Analysis and Modeling of Self-Heating and Thermal Coupling in 28 nm FD-SOI CMOS Transistors Down to Cryogenic Temperatures', *IEEE Trans. Electron Devices*, vol. 71, no. 4, pp. 2598–2604, Apr. 2024, doi: 10.1109/TED.2024.3367316.

[9] M. Vanbrabant, J.-P. Raskin, D. Flandre, and V. Kilchytska, 'Impact of thermal coupling effects on the digital and analog figures of merit of UTBB SOI MOSFET pairs', *Solid-State Electronics*, vol. 202, p. 108623, Apr. 2023, doi: 10.1016/j.sse.2023.108623.

[10] H.-S. Wong, M. H. White, T. J. Krutsick, and R. V. Booth, 'Modeling of transconductance degradation and extraction of threshold voltage in thin oxide MOSFET's', *Solid-State Electronics*, vol. 30, no. 9, pp. 953–968, Sep. 1987, doi: 10.1016/0038-1101(87)90132-8.

[11] M. Vanbrabant, J.-P. Raskin, D. Flandre, and V. Kilchytska, 'Experimental study of thermal coupling effects in FD-SOI MOSFET', *Solid-State Electronics*, vol. 194, p. 108362, Aug. 2022, doi: 10.1016/j.sse.2022.108362.

TABLE I THERMAL COUPLING IMPACT ON DIFFERENT FOM IN LINEAR AND SATURATION REGIMES.

FoM	**V_{ds} (V)**	**Temperature (K)**	**V_2 = 0 V**	**V_2 = 0.9 V**	**FoM(V_2 = 0.9 V) vs FoM(V_2 = 0 V)**
SS (mV/dec)	0.05	77	26.9	30.9	+ 14.9 %
		295	74.1	77.2	+ 4.2 %
V_{th} (V)		77	0.392	0.387	ΔV_{th} = - 0.005 V
		295	0.296	0.288	ΔV_{th} = - 0.008 V
I_{on} (A)	0.8	77	7.15×10^{-3}	7.08×10^{-3}	- 1 %
		295	6.27×10^{-3}	6.22×10^{-3}	- 0.8 %
I_{off} (A)		77	0.85×10^{-10}	3.60×10^{-10}	+ 323 %
		295	3.79×10^{-6}	5.03×10^{-6}	+ 32.7 %
I_{on}/I_{off}		77	84.2×10^{6}	19.6×10^{6}	- 76.7 %
		295	1.65×10^{3}	1.24×10^{3}	- 24.8 %
g_m (mS)		77	17.87	17.56	- 1.7 %
		295	13.58	13.37	- 1.5 %
g_m/I_d (1/V) @ $I_d = 10^{-7}$ A		77	69.6	63.0	- 9.5 %
		295	30.2	29.2	- 3.3 %