

Abstract #1182, 236th ECS Meeting, © 2019 The Electrochemical Society

(Invited) SOI Technologies for RF and Millimeter Wave Applications

Martin Rack^a, Jean-Pierre Raskin^a

^aUniversité catholique de Louvain

Silicon-on-Insulator (SOI) technology has taken the radio-frequency (RF) world by storm in the past decade. By offering high performance at low cost it has steadily displaced Gallium-Arsenide (GaAs) and Silicon-on-Sapphire (SOS) technologies to become the **mainstream technology for implementing the RF switch banks in mobile applications**. Indeed, in 2008 RF SOI accounted for less than 10% of switching modules in handsets, and today virtually 100% of all modern day smartphones include RF switches implemented in Partially Depleted SOI (PD SOI) on engineered and optimized trap-rich (TR) silicon based substrates.

The huge success of current PD SOI (130 nm) in today's RF market is due to significant **technological improvements**. First, the analog and high-frequency characteristics of the front-end of line (FEOL) **active devices**, i.e. advances at the transistor level, are presented, and second, the **quality of the back-end of line** (BEOL) process is reviewed.

The BEOL encompasses the metals, dielectric layers and semiconductor substrate of the manufacturing process. Substantial losses arise in silicon substrates at RF frequencies due to the conductive nature of silicon, and simply reducing the nominal doping of the handle wafer is insufficient, as a **parasitic conduction channel** is induced by (even low-level) parasitic charged defects present at all silicon/insulator interface. This effect -and ways to counter it- are described in depth as it is responsible for large amounts of **RF losses, parasitic coupling** and high levels of **non-linear signal distortion**.

In terms of CMOS FEOL, the RF characteristics of SOI devices are compared with those of other high-frequency technologies. It is shown that though **SOI devices provide attractive RF performances**, these alone do not account for SOI's dominance in the silicon RF market (over technologies such as planar bulk or FinFETs).

Indeed, on top of boasting high figures of merit (FoM) for RF applications, SOI technology owes its success to a **unique compatibility** with a passivation layer rich in traps that disables the aforementioned parasitic conduction channel below the buried oxide (BOX). The so called **"trap-rich" substrates**, that are composed of a high-defect polysilicon layer between the BOX and the high-resistivity silicon handle substrate, are **virtually lossless and highly linear** and are truly optimized for RF ICs.

A variety of essential RF passive elements (inductors, transmission lines, filters, antennas, etc.) are presented that benefit strongly from trap-rich silicon-substrate's properties, along with its beneficial impact on the key RF switching modules.

The future trends of SOI are then addressed. A summary is made on the progress of the most **advanced PD SOI** nodes (65 and 45 nm) as well as the **ultra-advanced Fully Depleted SOI (FD SOI)** nodes (22 and 28 nm) that are demonstrating their potential for **all kinds of RF and millimeter wave front-end circuit modules**, such as low-noise amplifiers (LNAs), voltage controlled oscillators (VCOs), mixers, etc. From these results SOI is expected to be a big contender as a technological platform to enable **mass production of 5G and IoT** devices and products in the very near future.

Finally, compatibility issues between advances FD SOI nodes and the trap-rich layer are discussed, and **alternative silicon-based substrate solutions** to overcome the problematic parasitic conduction channel are presented, such as porosification of the silicon handle, deep trap implantations, and smart PN doping patterns to fight against the unwanted conductive channel that degrades substrate RF performance, the latter technique being compatible with not only SOI but also with planar bulk technology.