A SPDT RF Switch Small- and Large-signal Characteristics on TR-HR SOI Substrates

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***Abstract*— This paper evaluates the small- and large-signal characteristics of a single pole double thru (SPDT) RF antenna switch including its insertion loss, isolation and non-linear behavior. It is fabricated on two different types of high resistivity (HR) Silicon-on-Insulator (SOI) substrates: one standard (HR-SOI) and one trap-rich (RFeSI80). Using a special test structure, the contribution of substrate and active devices is separated for both in small- and large-signal. It is shown that by using trap-rich substrate technology, a reduction of more than 17 dB of 2nd harmonic is achieved compared with HR SOI substrate.**

***Keywords*— RF switch; SOI; trap-rich (TR), RFeSI; SPDT; harmonic distortion; insertion loss; isolation.**

I. INTRODUCTION

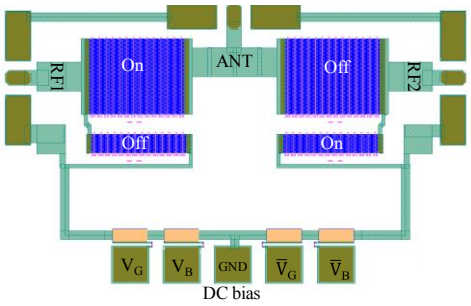
The market of cellular components has been shifting rapidly from GaAs pHEMT or SOS to silicon-based technology. CMOS SOI antenna switches - which are compatible with multimode GSM/EDGE, TD/WCDMA and LTE systems - exhibit higher integration levels and became the fastest growing mobile phone submarket [1]-[5]. An ideal RF antenna switch has low insertion loss in the signal path and high isolation from other paths. Other specifications such as linearity and time constant are also of high importance and should be accounted for carefully. R_{on}-C_{off} figure of merit is mainly process and device dependent. With the increasing number of throw counts from SPDT to SP9T and beyond, lower C_{off} and R_{on} are desired [4]. Advanced material engineering has been used to suppress the substrate contribution to the harmonics and intermodulation distortion. In this paper, the contribution of the transistors or the substrate to the nonlinear behavior of the studied RF switch (SPDT) is discriminated by measuring the second (H2) harmonic distortion levels achieved by large-signal measurements performed on the switch and its special test structure counterpart. R_{on}-C_{off}, insertion loss and isolation are extracted from small-signal measurements.

II. TECHNOLOGY DESCRIPTION

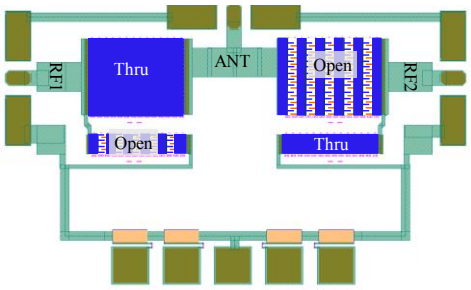
In this work, the SPDT RF antenna switch and its special test structure counterpart are fabricated using TowerJazz's 1st generation 0.18 µm, 4-metal layer SOI CMOS process (CS18 2.5 V) on top of 2 different types of RF-SOI substrates. This process is a thin-SOI partially depleted process supporting floating body and body contacted devices with a time constant ($\tau = R_{on}.C_{off}$) of 250 fs. The 2 types of substrates are labelled (i) HR-SOI, with a 1 µm-thick BOX and high resistivity handle wafer and (ii) RFeSI80 with a trap-rich layer inserted between the 400 nm BOX and HR handle wafer. They are characterized and compared for R_{on}-C_{off} and harmonic distortion levels.

III. RF ANTENNA SWITCH (SPDT)

The SDPT switch has one transmit port and one receive port which are symmetric. The on-state branches are biased with V_G= 2.5 V at the gate and V_B= 0 V at the body whereas the off-state branches are biased with V_G= V_B= -2.5 V at the gate and body to have minimum C_{off} and robust power handling in this condition [6]. The designed layout of the SPDT RF switch is shown in Fig. 1a. Because of the symmetry in the SPDT structure (identical Tx and Rx parts), we only measure and investigate the Tx part.



(a)



(b)

Figure 1. Layout of (a) SPDT switch and (b) Open/Thru test structure.

As illustrated in Fig. 1b, a special test structure named "Open/Thru" is designed and fabricated on the same chip as the SPDT. In this design, the transistors are removed to eliminate their contribution and bring forward the substrate's contribution to the measured characteristics.

The on-state is simulated by replacing the devices with metal-1 lines. The off-state is emulated by an open structure where all

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source-drain fingers are kept to better account for the extrinsic parasitic effects.

IV. Measurement Description and Results

A. Small-signal measurement

On-wafer small-signal measurements of the SPDT switch and Open/Thru test structure are performed in the frequency range between 10 MHz and 26.5 GHz. To eliminate the effects of cable losses and connections from S-parameters, the off-wafer line-reflect-reflect-match (LRRM) right angle calibration method is used. The RF insertion loss and isolation of both measured structures on 2 studied wafers are plotted in Fig. 2. The transmit insertion loss (Fig. 2a) is slightly higher in the SPDT than in the Thru structure because of higher transistor channel resistivity compared with metal-1.

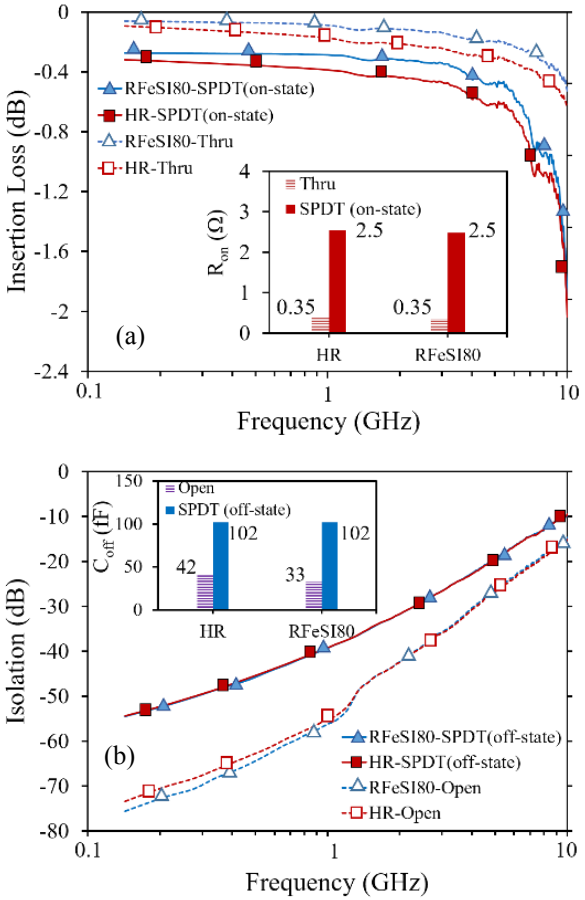

Figure 2. Comparison of (a) insertion loss, (b) isolation of the SPDT and the Open/Thru structure on both wafers. The extracted R_{on} and C_{off} at 900 MHz are shown in the insets of the figures.

At 900 MHz, the transmit insertion loss (S_{12}) in the SPDT switch is -0.28 dB and -0.38 dB for trap-rich and HR substrates, respectively. The extracted R_{on} ($1/\mathrm{Re}(-Y_{12})$) in the SPDT (2.5 Ω) and Thru structure (0.35 Ω) is identical for both substrates. Lower insertion loss shown in the RFeSI wafer compared with HR-SOI confirms lower substrate losses even if the BOX thickness of the RFeSI wafer is 2.5 times thinner than in the case of HR. The weaker isolation (Fig. 2b) in the SPDT switch than in the Open structure can be explained by higher total drain-source capacitance parasitic effect of the transistors in the series branch. Moreover, in the case of the Open structure the substrate effect is observable below 1 GHz whereas in the SPDT the high level of transistor C_{off} dominates the substrates' capacitance network thus the substrate coupling effect is not observed. The extracted C_{off} ($\mathrm{Im}(-Y_{12})/2\pi f$) at 900 MHz in the SPDT switch is about 100 fF whereas this value in the Open structure is about 32 fF and 42 fF for trap-rich and HR substrates, respectively. Therefore, the contribution of the RFeSI substrate in system isolation is well achieved by trap-rich technology even though the BOX is much thinner compared with HR wafer.

B. Large-signal measurement (HD)

Large-signal H2 measurement is done at the fundamental frequency of 900 MHz up to 40 dBm. As illustrated in Fig. 3a, the on-state SPDT on RFeSI substrates exhibits 17 dB lower H2 than on HRSOI at P_{in}=20 dBm, resulting in H2 values constantly below -85 dBc up to P_{in} = 40 dBm. The difference in H2 levels between on-state and Thru structures evidences a contribution of the transistors to the non-linearity of about 12 dB. In off-state (Fig. 3b) the transistor contribution reaches about 35 dB. This non-linearity is directly correlated with the C_{off} level which is proportional to parasitic drain-source capacitances in SPDT and Open structure. Non-linearity is mostly affected by C_{off} (intrinsic and extrinsic parts) of the active devices in off-state and not by the substrate. However, HR-SOI still shows 3 dB higher harmonic than RFeSI substrate in SPDT. The inset in Fig. 3b illustrates the output fundamental signal (H1) in off-state, showing the incident signal wave leak to the output due to the parasitic off capacitances.

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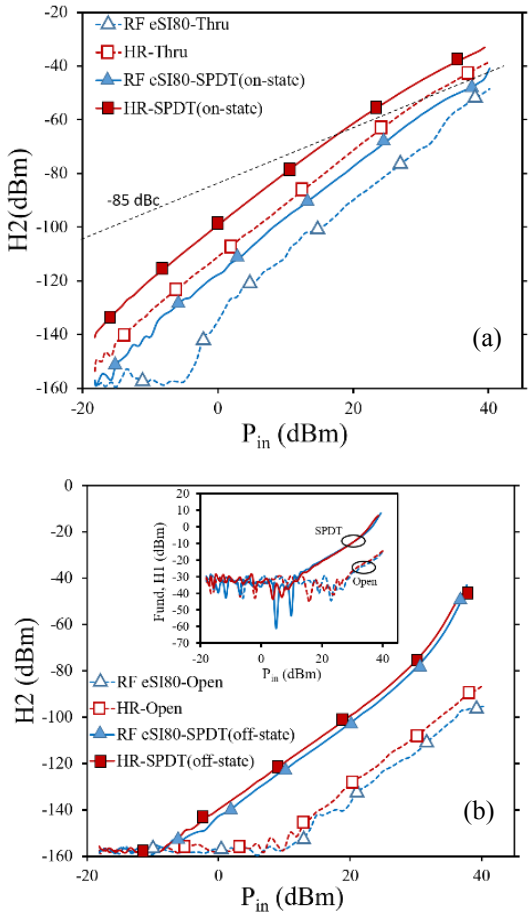

Figure 3. Measured on-state (a) and off-state (b) H2 of the studied SPDT and Open/Thru structures on both wafers at 900 MHz. The fundamental output in off-state SPDT and Open is shown in the inset.

V. Conclusion

In this paper, the relative contribution of active devices and substrate to the RF switch performance in terms of small- and large signal parameters is presented. RFeSI substrate significantly reduces the 2nd harmonic level in on-state. The harmonic levels in off-state mainly originate from the non-linearity behavior of the active devices. It is shown that RFeSI having a 2.5 times thinner BOX still outperforms HR substrate. It is worth mentioning that in SOI technology, BOX thinning is desired to achieve better thermal properties (lower self-heating effect) or back-gate control scheme in the transistors while maintaining low substrate cross-talk and losses.

Acknowledgment

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