Static and Dynamic Stochastic Analysis of a Temperature-Sensitive VO_2 Spiking Neuron

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***Abstract*—In this work, we investigate the intrinsic cycle-to-cycle variations in a spiking temperature-sensitive neuron, based on the resistive switching of a Vanadium dioxide (VO_2) two-terminal device. We study how this phenomenon impacts the spike rate jitter, and affects the spiking sensor precision. To do so, we combine a statistical analysis of the device DC characteristics, with measurements of the spiking neuron in dynamic operation from 41 to 47 °C. Using an analytical dynamic model, we reveal that the VO_2 cycle-to-cycle variations of the insulating resistance and insulator-to-metal threshold voltage dominate the stochastic processes. Our spiking sensor achieves large, linear sensitivity (1.71 kHz/°C) and high resolution (0.024 °C for a 10 ms-long observation), attributed to its small cycle-to-cycle variations.**

***Index Terms*—Spiking sensor, sensitive neuron, temperature sensor, stochasticity, cycle-to-cycle variations, Vanadium dioxide, resistive switching, phase-change material**

I. Introduction

Spiking Neural Networks (SNNs) open novel perspectives for performing learning, recognition and inference tasks in resource-constrained environments [1], towards energy-efficient in-sensor computing. Such neuromorphic implementations would benefit from input spiking neurons directly encoding stimuli in the time domain, as electrical spikes. Thanks to their electrically triggerable insulator-to-metal transition (IMT), Vanadium dioxide (VO_2) two-terminal devices can be integrated in compact one-transistor circuit interfaces to achieve such spiking behavior. Their phase transition being sensitive to several stimuli, rate-coded spikes have recently been demonstrated for RF, visible light, and temperature [2] [3] [4]. While these sensors demonstrate high linearity and sensitivity, their resolution is usually not investigated. Yet, this metric is affected by an inherent non-ideality of VO_2 two-terminal devices: akin to biological neurons, intrinsic cycle-to-cycle variations of their electrical characteristics induce jitter on their spike rate. In this work, we investigate this limitation in a VO_2 temperature spiking sensor working between 41 and 47 °C, a range representative of health risks such as heat strokes and burn injuries [5]. Section II details the fabrication of our VO_2 two-terminal device, the statistical study of its I-V characteristics, and the cycle-to-cycle distributions of its electrical properties. Section III presents the circuit interface required to bring the device in spiking regime, and the sensor dynamic operation under thermal stimulus. Section IV develops an analytical dynamic model for the spiking output, and leverages it to demonstrate that the cycle-to-cycle variations of two specific electrical properties dominate the spike rate jitter. Finally, Section V uses these findings to derive the sensor resolution for different averaging times, and benchmarks it against other VO_2 spiking temperature sensors.

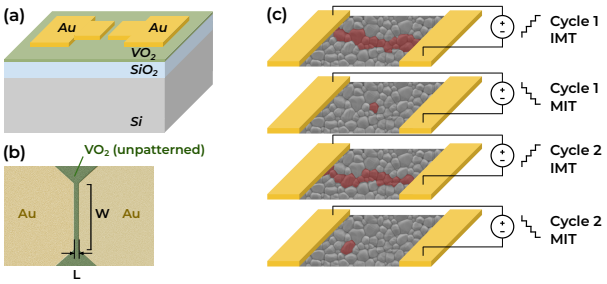

Fig. 1. VO_2 two-terminal device : **(a)** Schematic 3D view and **(b)** SEM picture, top view (colored). The device presented in this work has dimensions $L = 800\ nm$, $W = 3\ \mu m$. **(c)** Visualization of the filament formation during voltage-driven transitions, with subsequent stochastic relaxation process in the polycrystalline VO_2 film, yielding different filaments upon each transition.

II. Characterization of the VO_2 Device

A. Device fabrication

The VO_2 two-terminal device is fabricated by sputtering a 135 nm VO_2 thin film onto a SiO_2/Si substrate. The 400 nm SiO_2 layer is grown through wet thermal oxidation of a standard Si substrate of resistivity $\sim 10\ \Omega \cdot cm$. The DC reactive sputtering step is performed at room temperature from a Vanadium target (99.95 % purity), under an Ar/O_2 flow (43.5/6.5 sccm), at constant pressure of 5 mTorr and with 200 W plasma power. The as-deposited VO_2 layer is amorphous: an annealing step is needed to trigger crystallization. The later is performed at 500 °C for 1 hour, under an Ar flow of 30 sccm and at constant pressure of 165 mTorr, and yields a polycrystalline VO_2 layer. Following a lithography step, a bilayer of Ni/Au (5/100 nm) is evaporated on top of the VO_2 film, and patterned through liftoff. As the VO_2 layer is not patterned, the VO_2 resistance is defined by the electrodes width and length (see Fig. 1a-b). All measurements presented in this work have been performed on the very same device.

B. Cycle-to-cycle variations in I-V characteristic

When triggered electrically, the insulator-to-metal transition (IMT) has been shown to take place through a nucleation process [6], illustrated in Fig. 1c. When the voltage applied across the device exceeds a threshold V_{IMT}, first seed domains become metallic. This induces an increase in the electric field across the neighbouring domains, along with an increase in Joule heating. As a result, a metallic filament forms between the electrodes, causing a drastic reduction in

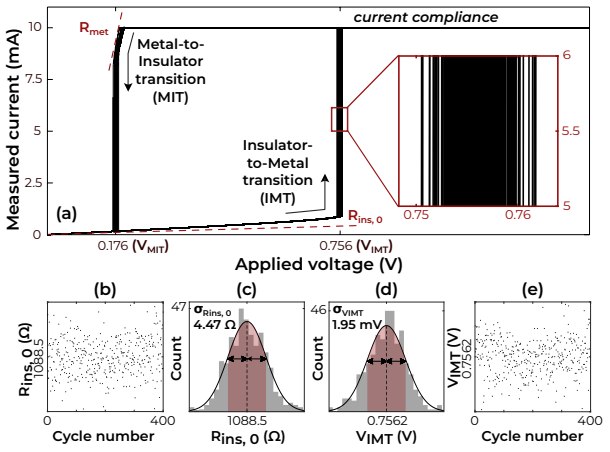

Fig. 2. **(a)** 400 consecutive voltage-driven DC sweeps measured on a single VO_2 device, at $T = 41°C$, with current compliance to protect the device. Close-up of the cycle-to-cycle variations in threshold voltage V_{IMT} shown in inset. **(b)-(e)** Distributions of the resistance in insulating regime $R_{ins,0}$ and the threshold voltage V_{IMT}, with their respective mean and standard deviation. Scatter plots show the absence of drift over the consecutive cycles.

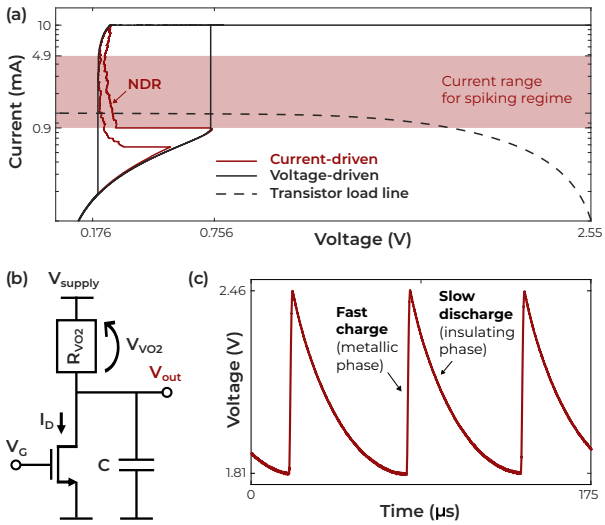

Fig. 3. **(a)** V- and I-driven characteristic of the VO_2 device, together with the NMOS load line, which falls in the current range for spiking regime (corresponding to the NDR). **(b)** Schematic of the spiking sensor circuit interface **(c)** Output spikes measured across the capacitance at $T = 41°C$.

the device resistance. During the relaxation process (metal-to-insulator transition MIT), the filament resorbs. Once the device resistance has returned to its initial value, isolated metallic domains can persist for timescales up to several milliseconds, serving as seeds for the next transition [7]. As a consequence, distinct filaments in the polycrystalline film are created from one sweep to the next [8]. This phenomenon causes cycle-to-cycle variations in the device I-V characteristics, more specifically the resistance in insulating and metallic regimes, noted respectively R_{ins} and R_{met}, as well as the two transition voltages V_{IMT} and V_{MIT}. To study these variations, we performed 400 high-resolution voltage-driven DC measurements of the device I-V characteristics (Fig. 2a). We then extracted the statistical distribution of the four representative electrical parameters. The insulating resistance is extracted close to zero bias, and noted as $R_{ins,0}$. Fig. 2b-e show the Gaussian fitting and absence of drift for V_{IMT} and $R_{ins,0}$, which will be proved to be the dominant causes of the spike rate jitter. We obtain normalized standard deviations σ_i/μ_i of 0.41, 0.42, 0.26 and 0.28 % for $R_{ins,0}$, R_{met}, V_{IMT} and V_{MIT}, respectively.

III. Study of Temperature-Dependent Spiking

A. Circuit topology

To enter spiking regime, the VO_2 resistor must be biased in an astable region so that it alternates between its metallic and insulating equilibrium points. To this end, the current flowing through the device must fall in its negative differential resistance range (NDR), visible in the current-driven measurement of the I-V characteristic (Fig. 3a). This constant bias I_D is set by the gate voltage V_G of a NMOS transistor working in saturation regime. An output capacitor C sets the spike rate, which is governed by the circuit RC time constant. The full circuit is shown in Fig. 3b. All measurements have been performed on a PCB implementation with $C = 33$ nF, supply voltage $V_{supply} = 2.55$ V, $V_G = 2.09$ V and $I_D = 1.025$ mA. The measurement of a typical output waveform is shown in Fig. 3c. During the abrupt charging phase, the VO_2 is in its metallic regime: C is charged by the large current flowing through the low VO_2 resistance, thus decreasing the voltage drop V_{VO2} across the device. Once V_{VO2} reaches the lower threshold voltage V_{IMT}, R_{VO2} switches back to its insulating regime: the capacitance slowly discharges through the NMOS. V_{VO2} thus increases up to the higher threshold voltage V_{IMT}, triggering the reverse phase transition and starting a new cycle.

B. Spike rate modulation with temperature

The spike rate is modulated by the variation of the VO_2 I-V characteristics with temperature, shown in Fig. 4a for $T = 41 - 47$ °C. The choice of a narrow temperature range with fine stepping is required for the sensor resolution investigation in Section V. Fig. 4b-c show the inversely proportional relationship of $R_{ins,0}$ and V_{IMT} to temperature. Two transduction mechanisms could be responsible for the V_{IMT} reduction [9]: (1) Joule heating-driven, and (2) electric field (Poole-Frenkel conduction-driven). Here, the almost linear V_{IMT} temperature dependence on a narrow range doesn't allow to discriminate the dominant contribution. Since the discharge phase (insulating regime) dominates the dynamic operation, the V_{IMT} and $R_{ins,0}$ reductions result in a linear increase in spike rate, as well as a decrease of the spikes amplitude (Fig. 4d). The two phenomena can be understood through the analytical model presented in the next section.

IV. Stochastic Analysis

To identify the device characteristics responsible for the spike rate jitter, we use the insight gained from our statistical analysis of the DC measurements to develop a stochastic dynamic model, which we then compare to our dynamic measurements. The analysis is presented for measurements at $T = 41°C$, but remains valid for other temperatures. We start by developing the deterministic version of the model.

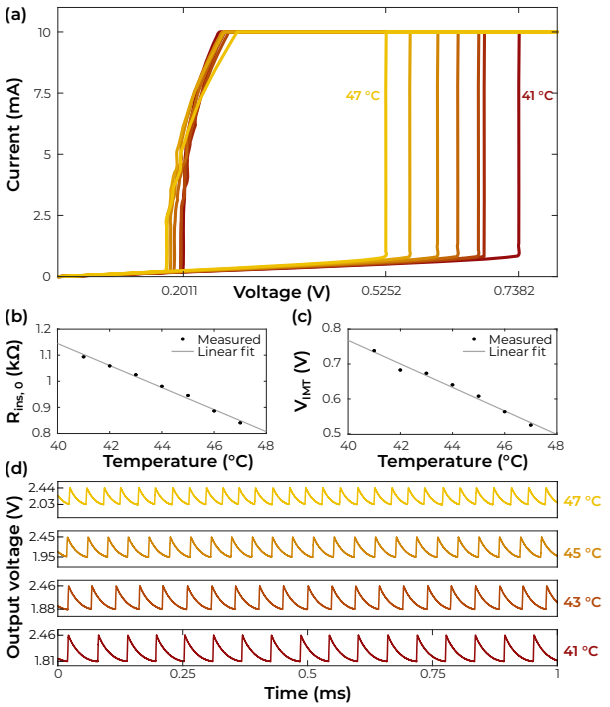

Fig. 4. **(a)** Voltage-driven I-V characteristics of the VO_2 device for $T = 41 - 47\ ^\circ C$. **(b)(c)** Evolution of $R_{ins,0}$ and V_{IMT} with temperature, with linear fit. **(d)** Output voltage of the spiking sensor circuit, showing spiking behavior in the $41 - 47\ ^\circ C$ range with spike frequency and amplitude adaptation.

A. Analytical dynamic model

The time-dependent equations for the output voltage of the spiking sensor can be derived from the fact the system essentially behaves as a RC circuit. We thus have, for the charge phase, while $V_{out} < V_{supply} - V_{MIT}$:

$$V_{out}(t) = (V_{supply} - V_{IMT}) + (V_{IMT} - R_{met}I_D)\left(1 - e^{-(t-t_c)/R_{met}C}\right);$$

and for the discharge phase, while $V_{out} > V_{supply} - V_{IMT}$:

$$V_{out}(t) = (R_{ins}I_D - V_{MIT})e^{-(t-t_d)/R_{ins}C} + (V_{supply} - R_{ins}I_D).$$

The model has been presented in previous work [2]; we extend it by including the voltage dependence of R_{ins}:

$$R_{ins}(V_{VO2}) = R_{ins,0} - ae^{bV_{VO2}}.$$

We fit the resistances on the I-V characteristic measured at 41 °C (Fig. 5a), and obtain $(50\ \Omega, 2.276\ V^{-1})$ for the fitting parameters (a, b), $R_{ins,0} = 1088.53\ \Omega$, and $R_{met} = 21\ \Omega$. The other circuit parameter (C, V_{supply}, and I_D) correspond to the

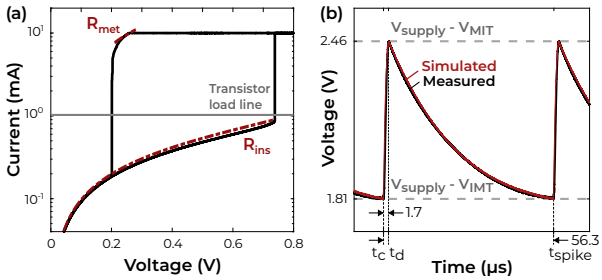

Fig. 5. **(a)** Measured voltage–driven DC sweep of the VO_2 device at $T = 41\ ^\circ C$. Superimposed: transistor drain current (approximated as constant) and fitted resistances in metallic (constant) and insulating (voltage-dependent) regimes, as used in the model. **(b)** Comparison between the dynamic model and the measured waveform.

operating parameters specified in Section III-A. The threshold voltages V_{IMT} and V_{MIT} are extracted from the average min. and max. values of the measured spikes, in coherence with the DC measurements. It now becomes obvious that the reduction in V_{IMT}, associated to a reduction in the hysteresis window of the I-V curve, results in a reduction of spike amplitude and increase in spike rate. Our deterministic, 9-parameters model reproduces a single spike with high fidelity (Fig. 5b).

B. Introducing stochastic processes

To distinguish the dominant causes of the spike rate jitter σ_f, we introduce several individual noise sources in our dynamic model. We then extract their respective impact $\sigma_{f,i}$ on this jitter, as summarized in Table I. Noise sources (1) to (4) are related the cycle-to-cycle variations of the VO_2 electrical parameters. At the beginning of each charge and discharge phase, we sample new values for (R_{met}, V_{MIT}) and (R_{ins}, V_{IMT}) using their Gaussian distributions. Their mean values are those used in our deterministic model, and their standard deviations are derived from the normalized values extracted from the 400 DC cycles in Section II-B. Three other noise sources are included using a transient Monte-Carlo approach. The thermal noise on the VO_2 resistance in both phases (5) and the noise on the transistor current (6) are modeled as parallel current sources, added to I_D:

$$I_D(t) = I_D + i_{th} + i_{NMOS}$$
$$\sigma_{th,met} = \sqrt{4k_BT\Delta f/R_{met}}, \quad \sigma_{th,ins} = \sqrt{4k_BT\Delta f/R_{ins}}$$
$$\sigma_{NMOS} = \sqrt{4k_B\gamma g_m T\Delta f}\quad ,$$

with $\gamma = 2/3$, $g_m = 1.8\ mS$ the NMOS transconductance, and $\Delta f = 62.5\ MHz$. To account for any other additive white gaussian noise (AWGN) sources coming from the electrical setup (7), we add a noise voltage to the output voltage :

$$V_{out}(t) = V_{out}(t) + v_{AWGN}$$

TABLE I
CONTRIBUTION OF THE DIFFERENT NOISE SOURCES TO THE SPIKE RATE JITTER AT T = 41 °C

Noise source	(1) Cycle-to-cycle variations in V_{MIT}	(2) Cycle-to-cycle variations in R_{met}	(3) Cycle-to-cycle variations in V_{IMT}	(4) Cycle-to-cycle variations in $R_{ins,0}$	(5) Thermal noise on R_{met} and R_{ins}	(6) Noise on transistor current	(7) Total AWGN extracted from setup	**Final model**	Measu-rements
Statistical parameters	$\mu_{VMIT} = 0.088\ V$ $\sigma_{VMIT} = 0.24\ mV$	$\mu_{Rmet} = 21\ \Omega$ $\sigma_{Rmet} = 0.87\ \Omega$	$\mu_{VIMT} = 0.74\ V$ $\sigma_{VIMT} = 1.95\ mV$	$\mu_{Rins,0} = 1088.53\ \Omega$ $\sigma_{Rins,0} = 4.47\ \Omega$	$\sigma_{th,met} = 227\ nA$ $\sigma_{th,ins} = 32\ nA$	σ_{NMOS} $= 36\ nA$	σ_{AWGN} $= 1.56\ mV$	**All noise sources combined**	
Simulated $\sigma_{f,i}$ (Hz)	4.43	20.00	232.32	263.37	2.68	2.56	0.81	$\sigma_{f,sim}$ $= 353.64$	$\sigma_{f,meas}$ $= 344.82$

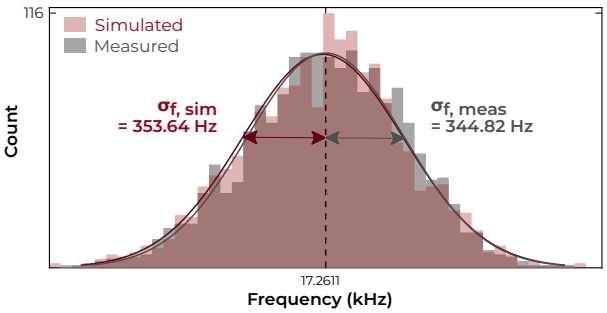

Fig. 6. Concordance between measured and simulated jitter on the spike rate, measured and simulated over 100 ms. All the noise sources of Table I have been included in the dynamic model.

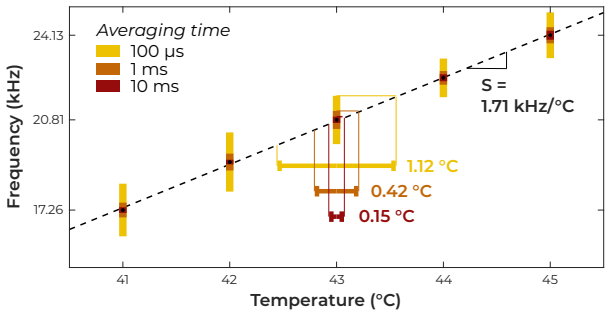

Fig. 7. Mean frequencies for $T = 41 - 45\ °C$, together with their 99.7% confidence interval, for three different averaging times (100 μs, 1 ms, 10 ms). Sensitivity derived from linear fit. Temperature resolution derived for worst case of spike rate jitter, i.e. T = 43 °C.

Its std σ_{AWGN} was extracted from the rms value of the measured output voltage, just below the spiking regime. The different noise sources can be considered mostly uncorrelated, as they satisfy $\sigma_f \simeq \sqrt{\Sigma\sigma_{f,i}^2}$. When considering all noise sources, the dynamic model can accurately reproduce the distribution of the spike rate jitter (Fig. 6). Its dominant causes are the cycle-to-cycle variations of V_{IMT} and R_{ins}, whereas previous work presented V_{IMT} as the sole source of the spike rate jitter [8]. Our model is able to capture the R_{ins} effect as it accounts for its voltage-dependence. Indeed, considering it constant throughout the discharge phase results in systematic underestimation of its variations impact. Additionally, our analysis does not generally support the hypothesis that the cycle-to-cycle variations in R_{met} and R_{ins} could be due to thermal noise [4]: the large difference in their effect on the spike rate proves they are distinct phenomena.

V. Benchmarking & Perspectives for Sensing

The linear dependence of the average spike rate with temperature yields a sensitivity S of 1.71 $kHz/°C$ (Fig. 7). To overcome the uncertainty related to the spike rate jitter, the instantaneous frequency can be averaged over a certain number of cycles, which will determine the duration of the observation. We can then define the spike rate resolution for a given averaging duration using a 99.7 % (3σ) confidence interval: from the sensitivity, it can be converted to a temperature resolution. Fig. 7 shows the results for the worst case (T = 43 °C): the resolution improves with the averaging time, from 1.12 °C for a 100 μs observation to 0.15 °C for a 10 ms observation. This indicates a clear resolution-energy trade-off. If we take the commonly accepted definition of the resolution (rms, one-sigma), this value falls to 0.024 °C for a 10 ms observation. Table II provides benchmarking of our sensor, compared with the two other existing implementations of spiking VO_2 temperature sensors, showing competitive sensitivity and static power consumption. Although none of them report on the temperature resolution, our work shows smaller cycle-to-cycle V_{IMT} variations; as well as higher signal to noise ratio, defined by [3] as $10log(\mu_f^2/\sigma_f^2)$.

VI. Conclusion

We presented the fabrication, modeling, static and dynamic operations of a spiking VO_2 temperature sensor. We investigate the impact of the VO_2 cycle-to-cycle variations on the spike rate jitter, through both DC and dynamic measurements. We link them using an analytical stochastic model, and discuss for the first time how this jitter affects the resolution. Our sensor demonstrates a high precision of 0.024 °C for a 10 ms observation, and shows lower cycle-to-cycle variations values than SoA VO_2 spiking sensors, making it a good candidate to be interfaced with SNNs for edge sensing applications.

TABLE II
Benchmarking with other spiking VO_2 temperature sensors

Ref.	V_{IMT} cycle -to-cycle variations (%)	Sensitivity kHz/°C	SNR (dB)	Resolution (rms) (°C)	Power consumption (mW)
[3]	0.73	2.8	29.92	/	$\sim 5^{\dagger}$
[4]	$\sim 1.1^{*}$	1.7	/	/	$\sim 0.1^{\dagger}$
This work	0.41	1.71	76.95	**0.260** °C (1 cycle) **0.024** °C (173 cycles)	2.6

∗: Estimated considering min. and max. as 3σ value
†: Static power, estimated from suppl. information and operating voltage/current.

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