28 FDSOI RF Figures of Merit down to 4.2 K

L. Nyssens[1], A. Halder[1], B. Kazemi Esfeh[1], N. Planes[2], D. Flandre[1], V. Kilchytska[1], J.-P. Raskin[1]
[1]ICTEAM, Université catholique de Louvain, 1348 Louvain-la-Neuve, Belgium
[2]ST, ST-Microelectronics, 850 rue J. Monnet, 38926 Crolles, France

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***Abstract*—This work presents a detailed RF characterization of 28 FDSOI nMOSFETs at cryogenic temperatures down to 4.2 K. Two main RF Figures of Merit (FoMs), i.e. current gain cutoff frequency (f_T) and maximum oscillation frequency (f_{max}), as well as parasitic elements of the small-signal equivalent circuit are extracted from the measured S-parameters. The observed behavior of RF FoMs versus temperature is discussed in terms of small-signal equivalent circuit elements, both intrinsic and extrinsic (parasitics). This study suggests 28 FDSOI nMOSFETs as a good candidate for future cryogenic applications down to 4.2 K and clarifies the origin and limitations of the performance.**

Keywords— FDSOI, UTBB MOSFETs, RF Figures of Merit (FoMs), liquid-helium temperature, parasitic elements

I. Introduction

Numerous studies focused on the cryogenic behavior of advanced CMOS technologies are mainly driven by the perspective of quantum computing applications [1-8]. Quantum computer operations are realized by quantum bits (or "qubits"), working at extremely low temperature, typically in the mK range, while the control and read-out circuitry is to be placed in a close proximity to the qubits, typically at liquid-helium temperatures [2]. Advanced CMOS technologies are known to be highly scalable and low-power. Furthermore, they feature a limited power dissipation during normal operation. Thus, these technologies are very promising for quantum computer electronics. This motivated numerous works [3-7] towards the analysis of the advanced MOSFETs behavior at cryogenic temperatures. Those works widely addressed static parameters, such as short-channel effects, threshold voltage, subthreshold swing, etc. The influence of cryogenic temperature on 28 nm bulk and FDSOI technologies with a main focus on analog parameters and modeling has been discussed in [3]-[5]. In [7] and [8], the above studies were completed by investigating the analog and RF figures of merit (FoM) in 28 FDSOI technology at cryogenic temperatures down to 77 K. Strong improvement of both analog and RF FoMs was demonstrated [7, 8].

This paper extends our previous work [8] down to 4.2 K, the liquid-helium temperature. RF FoMs of nMOSFETs from 28 FDSOI process with different gate lengths in a temperature (T) range of 4.2-300 K are extracted. Next to that, the full small-signal equivalent circuit of UTBB MOSFETs, including both intrinsic and extrinsic parasitic elements is reconstructed to support the performance analysis.

II. Experimental Details

Devices studied in this work originate from 28 FDSOI process of ST Microelectronics [9]. N-channel MOSFETs under study feature gate lengths (L_g) from 25 to 150 nm. The Si film, BOX and the equivalent gate oxide thicknesses are 7, 25 and 1.3 nm, respectively. Studied nMOSFETs incorporate 60 fingers of 2 µm width, embedded in CPW pads for RF characterization.

DC I-V and RF S-parameters in a frequency range from 10 MHz up to 67 GHz under saturation (V_{ds} = 1 V) and "cold" (V_{ds} = 0 V) conditions for different applied gate voltages (V_{gs}) are measured down to liquid-helium temperature (4.2 K). The back gate is kept grounded. The CPW feed line pads are de-embedded by a dedicated open structure for each device measured at every temperature. More details about the extraction methodology of equivalent circuit elements can be found in [10].

III. Results and Discussion

Fig. 1 shows the drain current (I_d) and transconductance (g_m) versus gate voltage (V_{gs}) for the shortest device (25 nm). As expected, one can observe an increase of the threshold voltage, I_d and maximum g_m with temperature reduction. Furthermore, the zero temperature coefficient (ZTC) point at which I_d stays invariable with T clearly appears at ~ 0.83 V. The maximum g_m behavior versus temperature is further detailed in Fig. 2. Both "extrinsic" g_m (i.e. as measured, $g_{m,e}$) and "intrinsic" (i.e. when parasitics are withdrawn after RF extractions, $g_{m,i}$) are shown. g_m increases with temperature lowering down to 100 K, thanks to an enhanced mobility (µ) resulting from a reduced phonon scattering, dominant in this temperature range. Then, as T decreases below 100 K, g_m reaches a plateau. This is because a concurrent µ mechanism, associated with impurity scattering (in the source and drain junctions and extension regions) and known to feature a µ reduction with T lowering, comes into a play. A similar trend is observed in the total source and drain resistance (R_{ds}) behavior versus T (Fig. 3), while the T at which the impurity scattering mechanism starts to dominate is shifted to lower temperatures and is more pronounced (due to higher impurities concentration in these regions w.r.t channel). Carriers freeze-out effect can also be assumed to contribute in the R_{ds} increase at T<50 K.

The increase in g_m is the main origin of the current gain cutoff frequency (f_T) improvement at cryogenic temperatures (Figs. 4, 5). The total gate capacitance exhibits only a slight decrease with T (~10 fF for all devices from 300 K to 4.2 K) and does not contribute significantly to the increase of f_T. Strong f_T improvement of about 130 GHz (~50% w.r.t. room temperature) is observed for the shortest device. Furthermore, small f_T reduction in the T range from 100 to 77 K, discussed in [8], does not persist at T<77 K but stabilizes instead. The maximum oscillation frequency (f_{max}) (Figs. 4, 6) also increases by a factor of 50-60 % from 300 K to 4.2 K. It is linked to both the increased g_m and the reduced gate resistance (R_g) with temperature (Fig. 3). R_g reduction can be explained in terms of the metal gate stack resistivity. Contrarily to previously reported R_g behaviour in 90 nm bulk CMOS devices [11] and our observations for R_{ds}, R_g reduction is monotone, without an increase in R_g at very low temperatures (4-50 K), observed in [11] and in our R_{ds}. This is due to a different gate stack, high-K – metal gate of the gate electrode in our case compared to a poly-Si gate in [11] and to a complex source/drain resistance combining extension regions, heavily doped epitaxially raised source/drain with silicidation. Indeed, [11] related the R_g increase in the 4-50 K T-range to

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carriers freeze-out in the poly-Si. Thus, contrarily to [11], f_{max} in our case does not decrease at 4.2 K (Fig. 4).

IV. Conclusion

In this work, the prospects of 28 FDSOI MOSFETs for future cryogenic RF applications has been assessed by the analysis of RF FoMs and complete small-signal equivalent circuit elements. The temperature reduction down to 4.2 K has been shown to result in a strong improvement of f_T (~130 GHz for 25 nm–long device) and f_{max} (~75 GHz). The temperature evolution of RF FoMs was discussed in terms of mobility and parasitic elements behavior. This was supported by the fact that the reconstructed f_T and f_{max} based on the MOSFET small-signal equivalent circuit model agree well with those extracted by extrapolation of H_{21} and the unilateral power gain in a temperature range down to 4.2 K.

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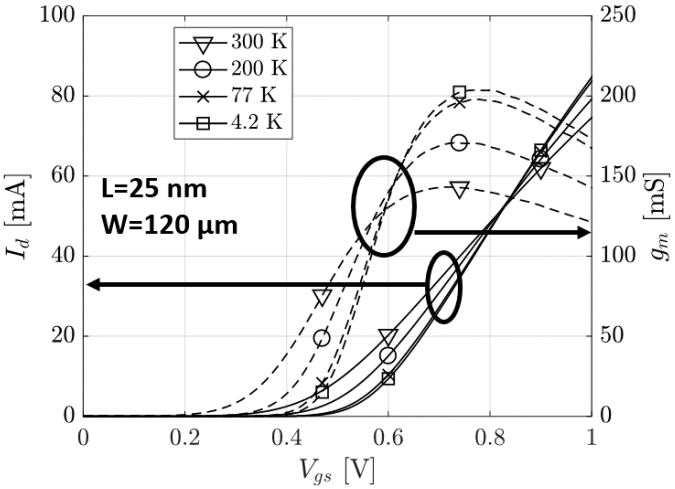


Fig. 1. I_d (left) and g_m (right) for different V_{gs} from 300 K down to 4.2 K.

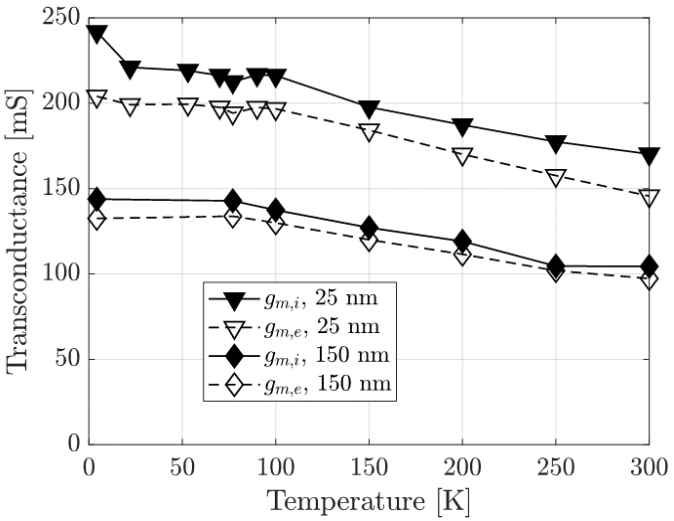


Fig. 2. Maximum $g_{m,i}$ and $g_{m,e}$ extracted from RF measurements.

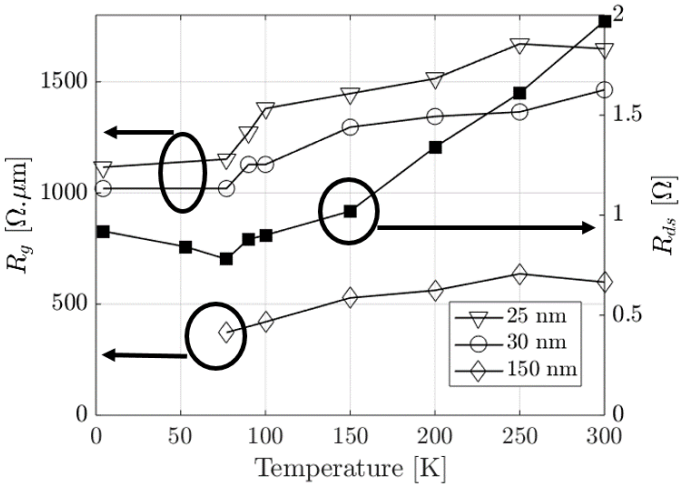


Fig. 3. Extrinsic R_g and R_{ds} at different T for three gate lengths.

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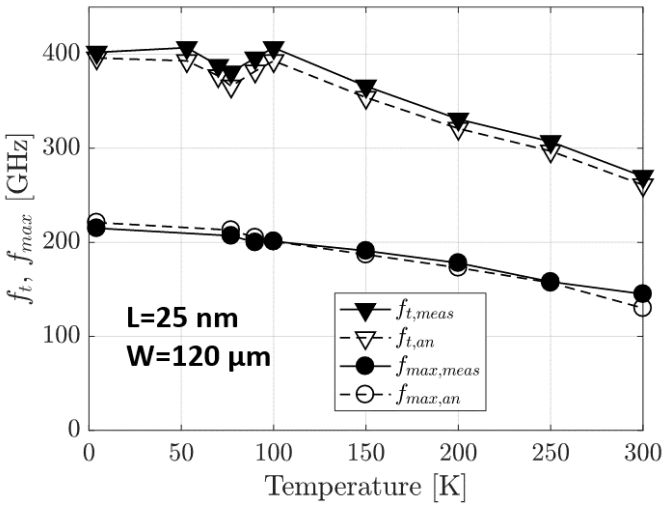


Fig. 4. Measured (meas) and reconstructed (an, cfr. insight Figs. 5 and 6) f_T and f_{max} of the shortest device for different temperatures.

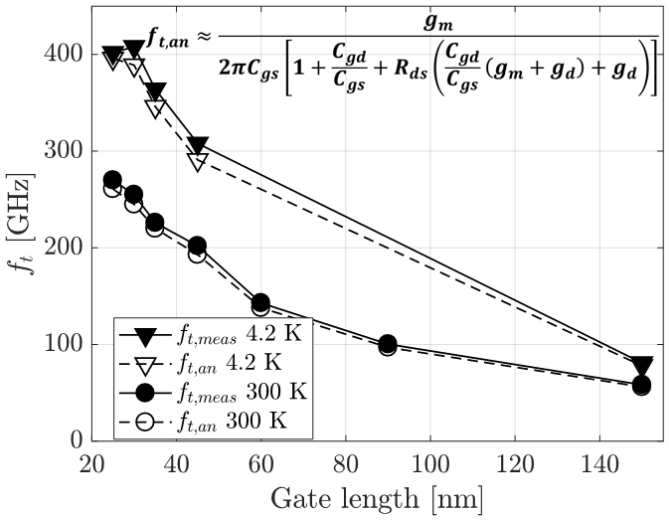


Fig. 5. f_T for different gate lengths at 300 K and 4.2 K and its analytical expression based on the small-signal equivalent circuit [10].

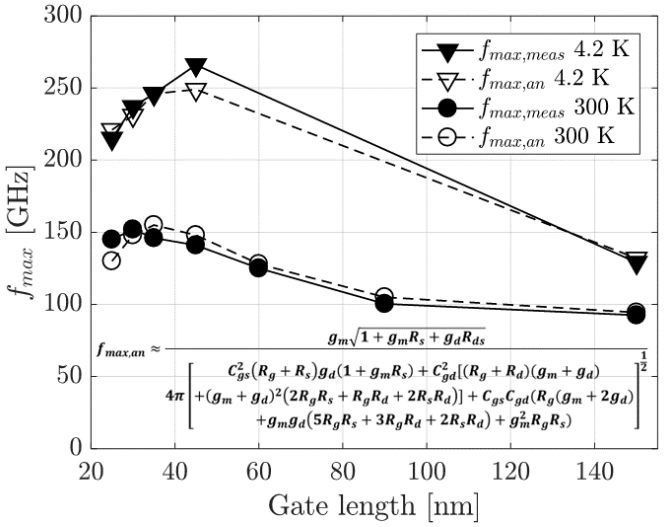


Fig. 6. f_{max} for different gate lengths at 300 K and 4.2 K and its analytical expression based on the small-signal equivalent circuit [12].

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