Advanced MOSFETs Electrical Characterization for Further Analog and RF applications

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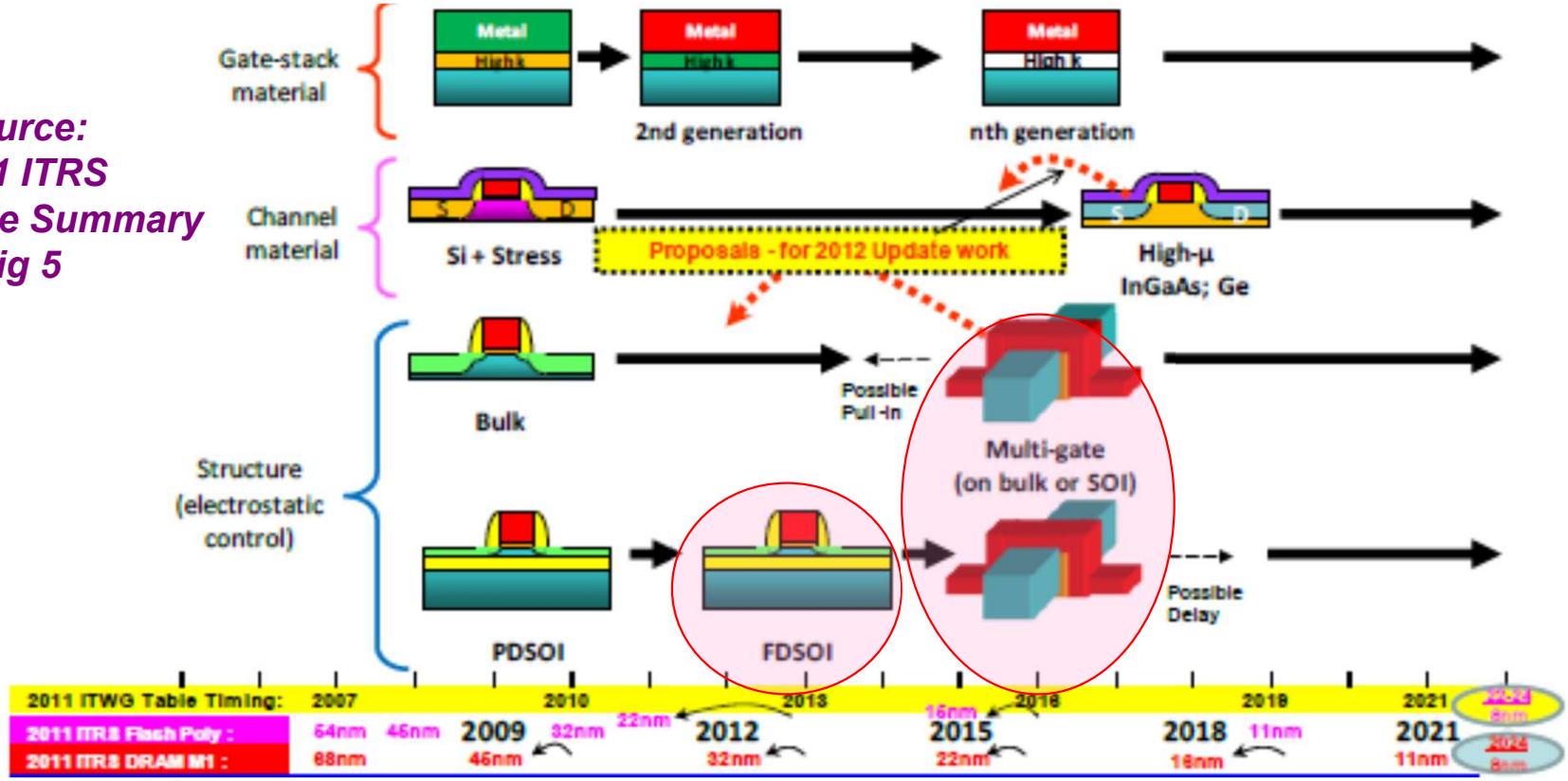
Outline

- ✓ **Introduction**
- ✓ **Analog/RF Figures of Merit**
- ✓ **Methodology used for device assessment**
  - ⇒ DC-based Techniques
  - ⇒ Wide frequency range measurements
  - ⇒ RF characterization methodology
- ✓ **Conclusions**

Introduction

- Device **downscaling** is accompanied by introduction of **new materials** and **new architectures**, affecting Analog/RF FoM
- Main contenders: **UTBB FDSOI** MOSFETs and **MuGFET** (*FinFETs, NWs,…*)
- We **do not target** to answer **"Which technology is better for Analog/RF?"**
- But **review methodological approaches** enabling a fair assessment

Source: 2011 ITRS Executive Summary Fig 5



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Analog / RF Figures of Merit

Key-factors:

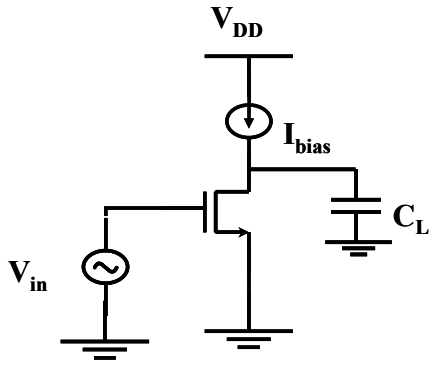
MOSFET-level

- $f_T = g_m/(2\cdot\pi\cdot C_{gg})$
- f_{max}
- $A_{v0} = g_m/g_d = (g_m/I_d)\cdot V_{EA}$

  $\neq$ const (f)

IC (amplifier)-level

- GBW = $g_m/(2\cdot\pi\cdot C_L)$ = $= (g_m/I_d)\cdot(I_d/(2\cdot\pi\cdot C_L))$



We link FoM with device physics

⇨ *depends on*

- Transconductance g_m
- Drive current, I_d
- Output conductance, g_d
- Early voltage, V_{EA} ($V_{EA}=I_d/g_d$)
- g_m/I_d ratio
- Gate capacitance, C_{gg}
- Parasitics (C, R)

$$f_T \approx \frac{g_m}{2\cdot\pi\cdot C_{gs}} \frac{1}{\left(1+\frac{C_{gd}}{C_{gs}}\right)+(R_s+R_d)\cdot\left(\frac{C_{gd}}{C_{gs}}\cdot(g_m+g_d)+g_d\right)}$$

$$f_{max} \approx \frac{g_m}{4\cdot\pi\cdot C_{gs}} \frac{1}{\left(1+\frac{C_{gd}}{C_{gs}}\right)\sqrt{g_d\cdot(R_g+R_s)+\frac{1}{2}\frac{C_{gd}}{C_{gs}}\cdot\left(R_s\cdot g_m+\frac{C_{gd}}{C_{gs}}\right)}}$$

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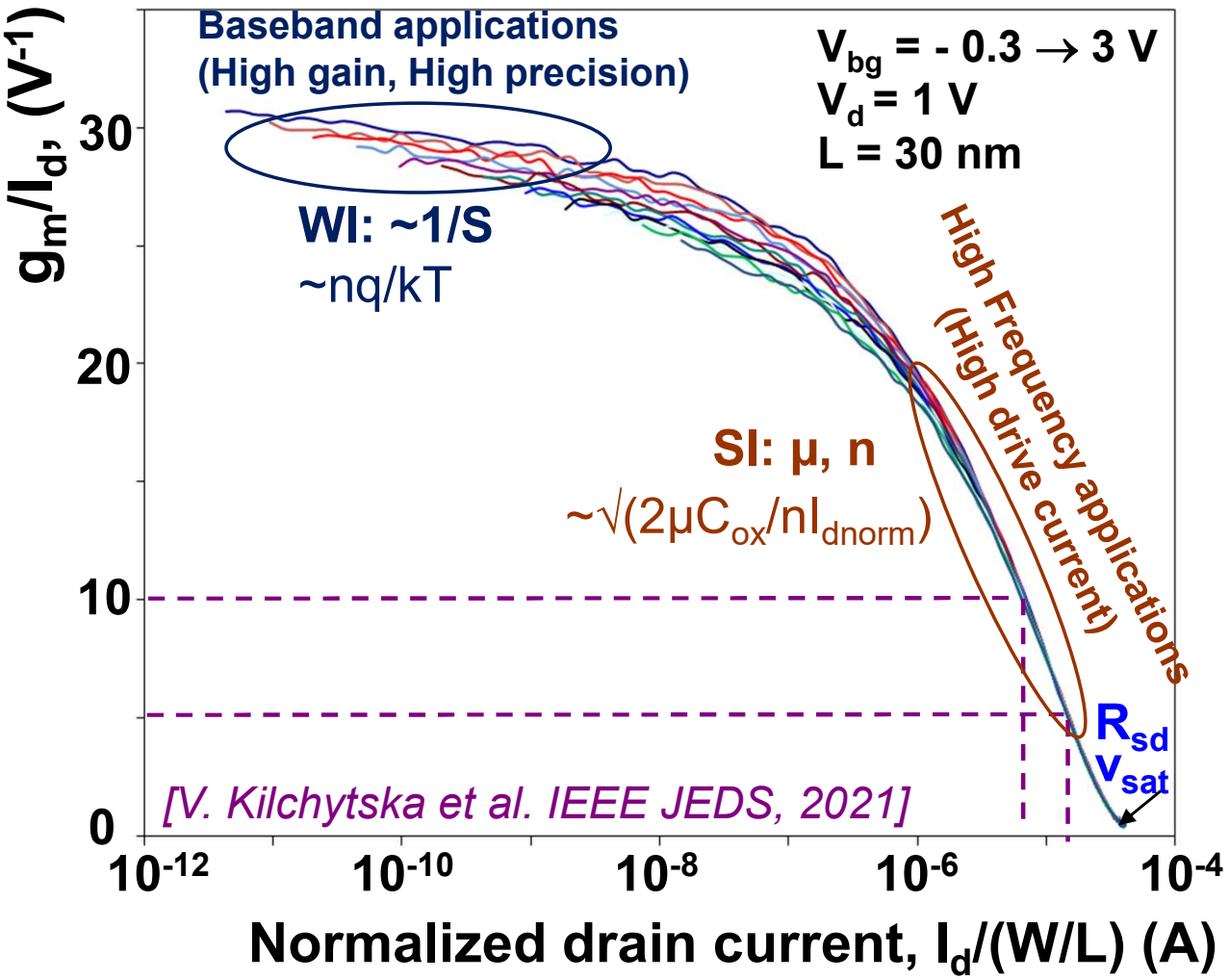
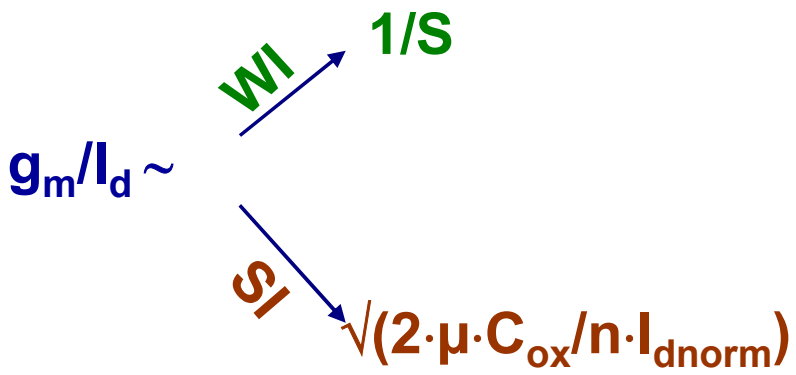
Methodology

g_m/I_d Technique





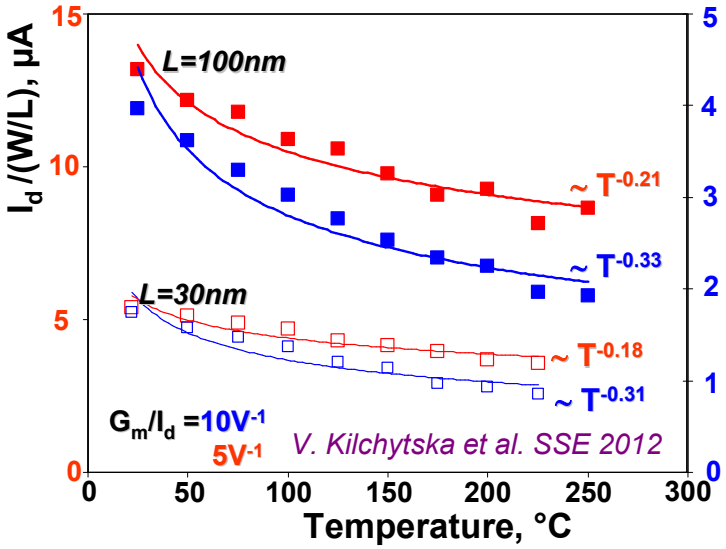
- independent on V_T
- independent on L (except SCE)
- ease comparison vs V_{sub} and vs T *(in terms of purely physical parameters)*

Allows fair comparison of different devices & at different conditions & T

g_m/I_d Technique

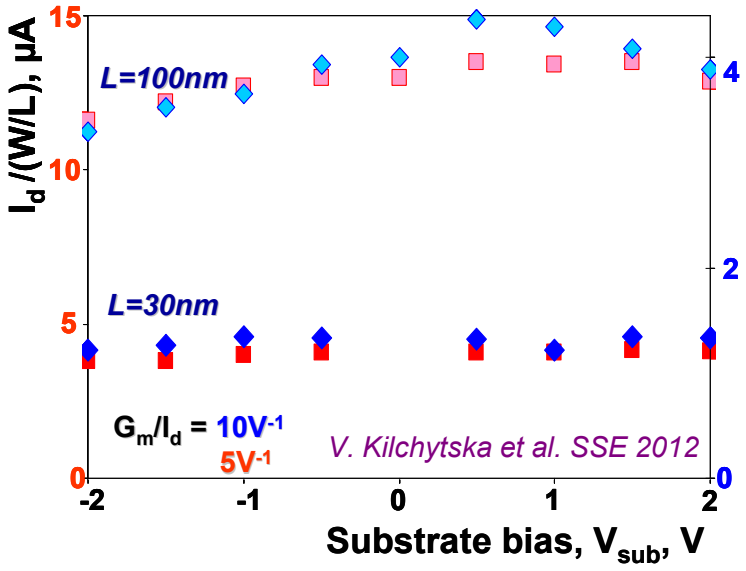
Examples

1) Effect of high-T



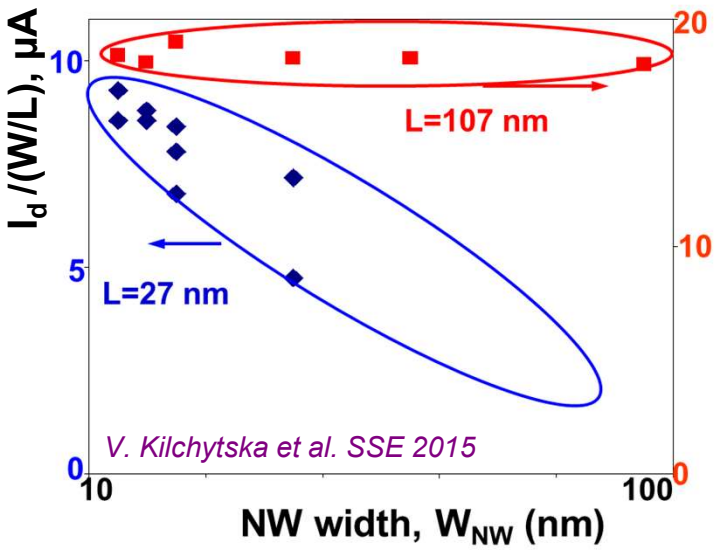
- limited $I_{d\ norm}$ reduction, 20-30% over 200°C
- related to µ and R_{sd} degradations

2) Effect of V_{SUB}



- **V_{sub} → positive**
  ⇨ $I_{d\ norm}$↑ of 5-10%
- Sign of beneficial effect of µ ↑

3) Effect of W_{NW}

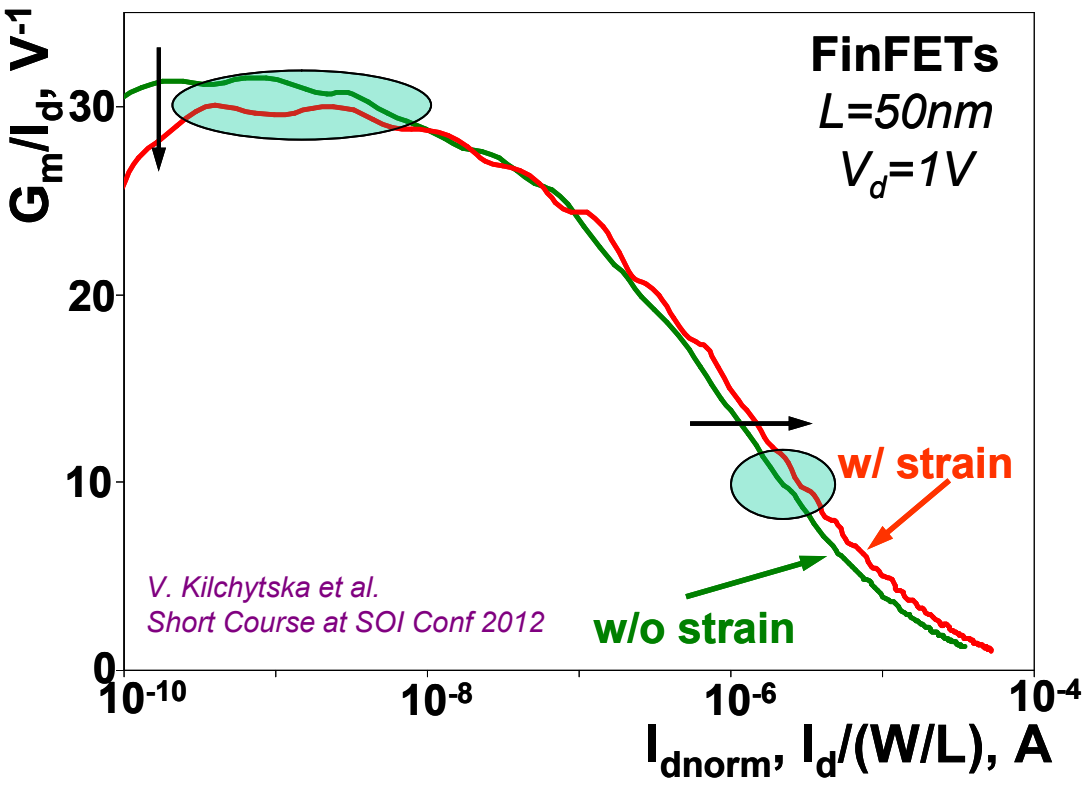


- **long-L:** $I_d/(W/L)$ is almost const
- **short-L:** $I_d/(W/L)$ is improved by W_{NW} scaling
- due to improved SCE control in narrow devices

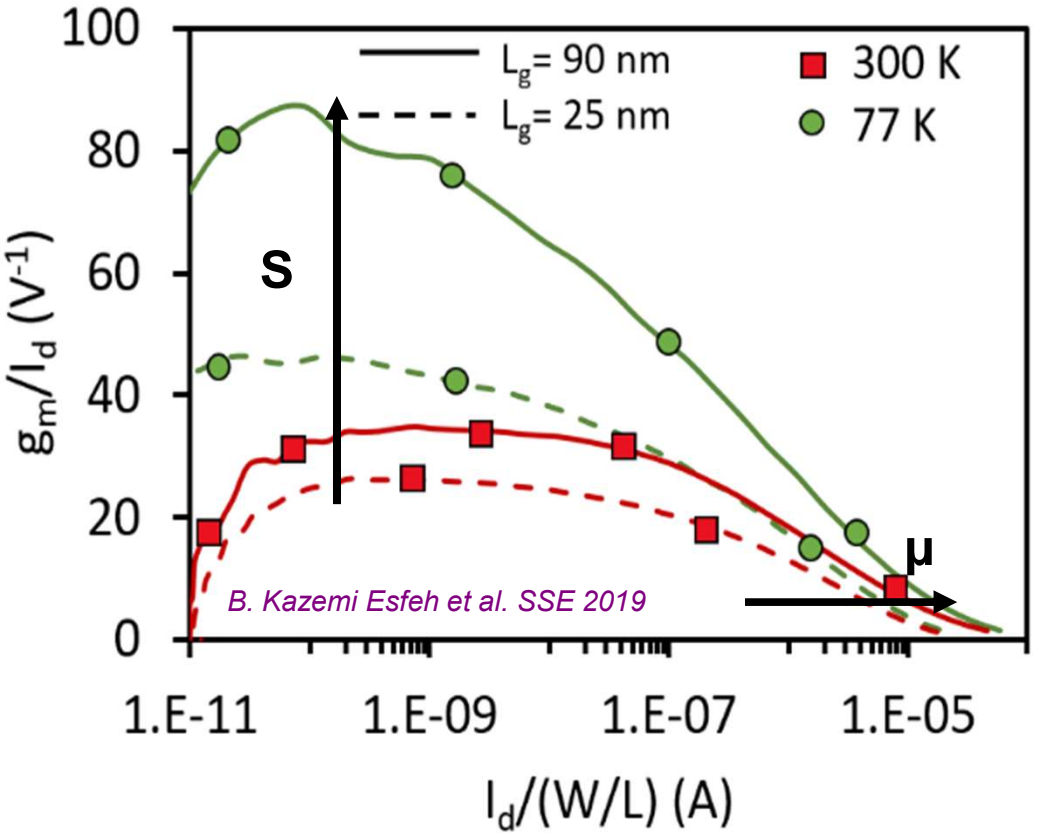
g_m/I_d Technique

Examples

4) strain introduction



5) Cryogenic temperatures

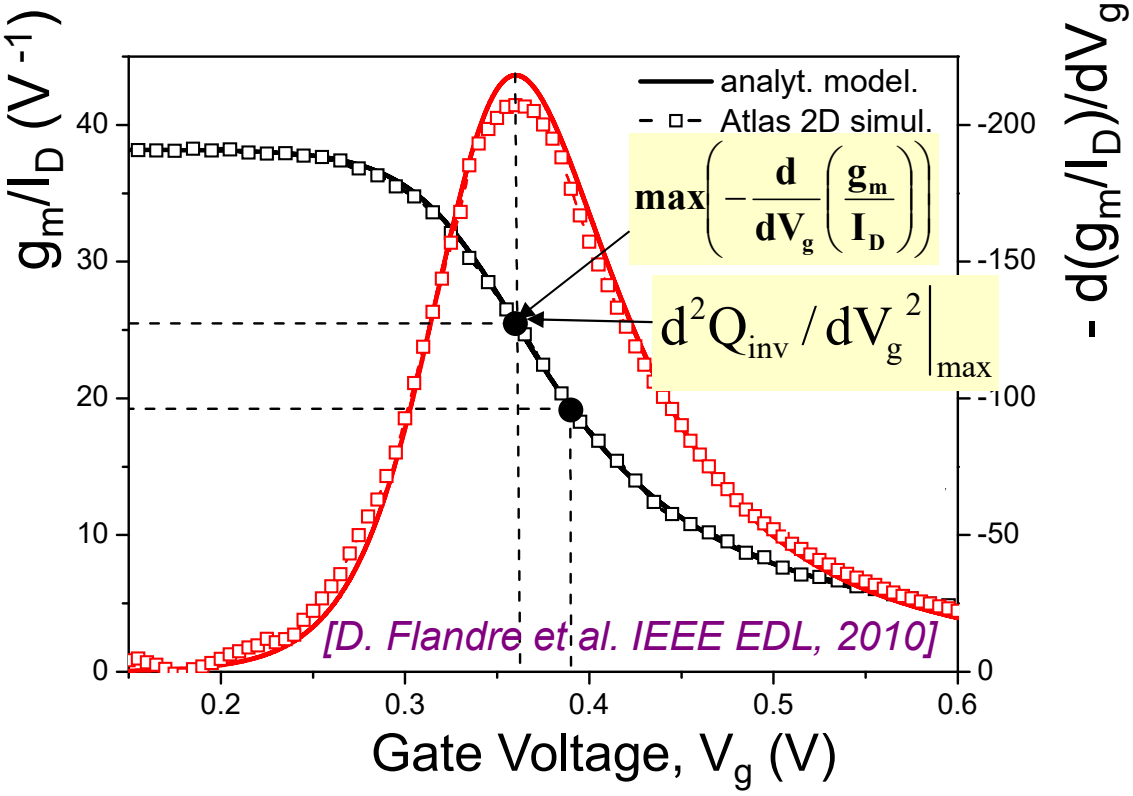


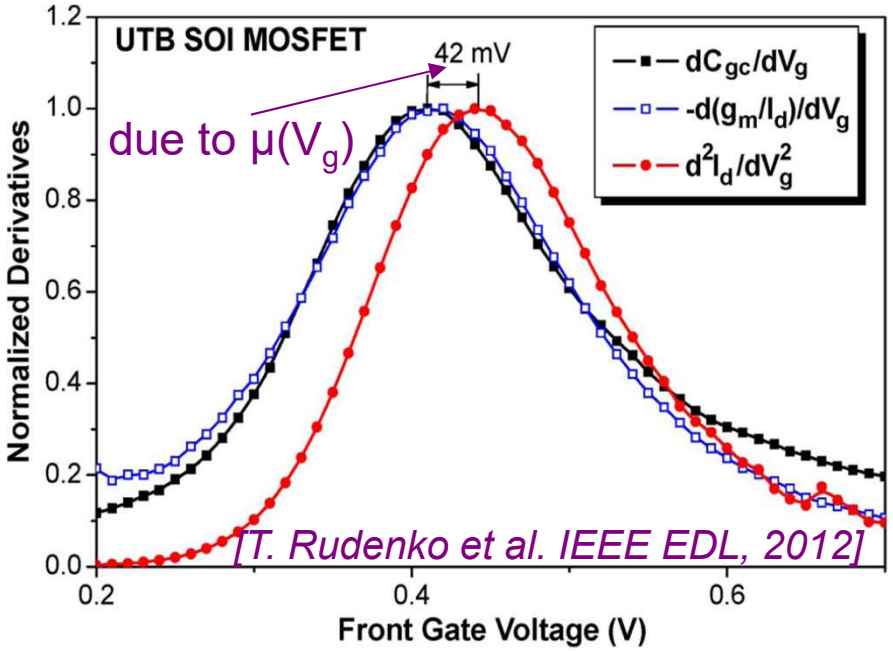
- *μ booster* ⇨ G_m ↑, I_d ↑
- *SCE control* ↓ ⇨ S ↑ *and DIBL* ↑ ⇨ V_{EA} ↓
- Tradeoff for Analog ???
- Depends on application / bias point of interest

- S ↓ *with* T ↓ *(~kT/q)*
- I_{d_norm} ↑ *with* T ↓ *due to μ* ↑

V_{Th} extraction

$d(g_m/I_d)/dV_g$





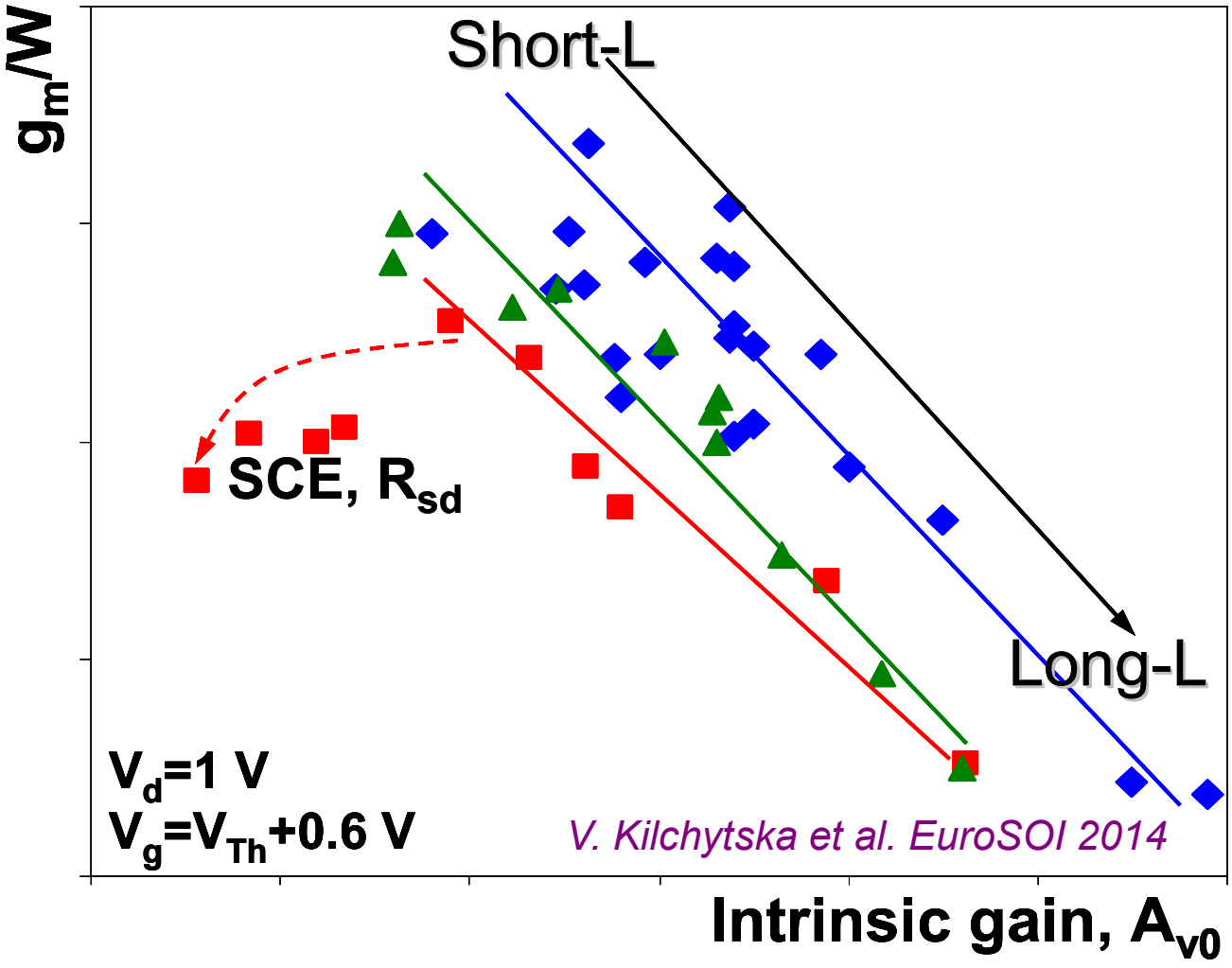
$$\frac{d}{dV_g}\left(\frac{g_m}{I_d}\right)=\frac{d^2(\ln I_D)}{dV_g^2}=\frac{q}{kT}\frac{d^2\varphi_s}{dV_g^2}$$

- Three methods allow assessing of $d^2Q_{inv}/dV_g^2|_{max}$ ($d^2\varphi_s/dV_g^2|_{min}$) criterion, namely dC_{gc}/dV_g, d^2I_d/dV_g^2, $d(g_m/I_d)/dV_g$
- dC_{gc}/dV_g is tricky for small-area
- $d(g_m/I_d)/dV_g$ is much less sensitive to the $\mu(V_g)$ and V_d than d^2I_d/dV_g^2

- Position of $d(g_m/I_D)/dV_g|_{min}$ coincides with that of $d^2Q_{inv}/dV_g^2|_{max}$

Methodology

g_m-A_v Analog Metric



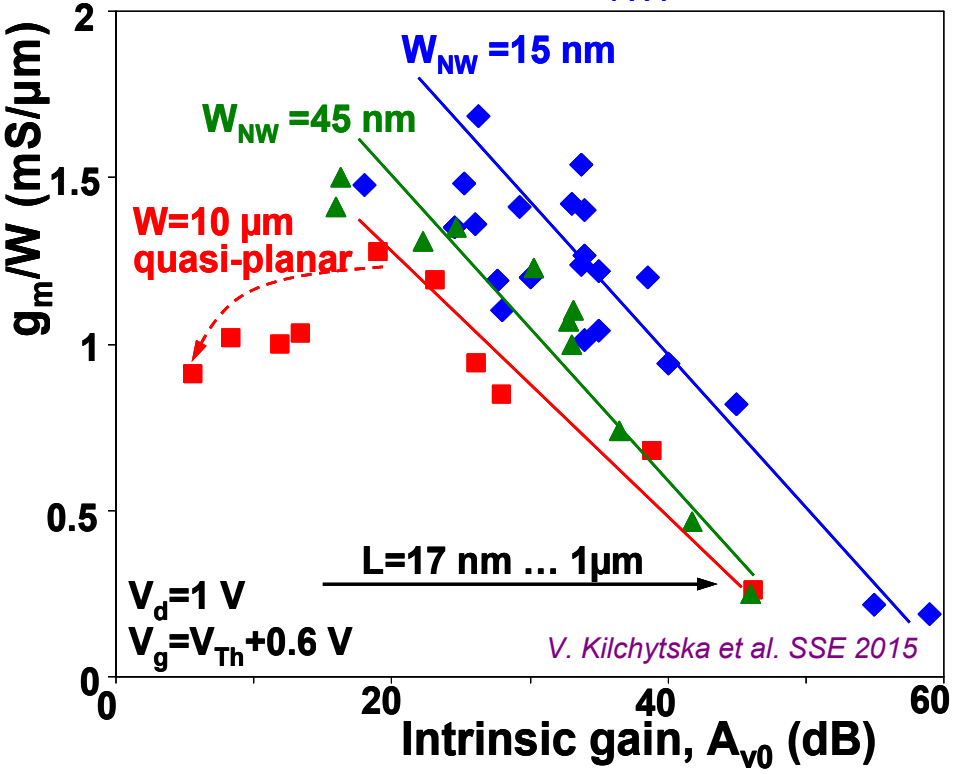
- analogue of I_{on}– I_{off} digital metric
- very visual
- for analog: both g_m and A_v are wanted to be high
- independent on V_T

Fair benchmarking of different fabrication processes, bias conditions, T

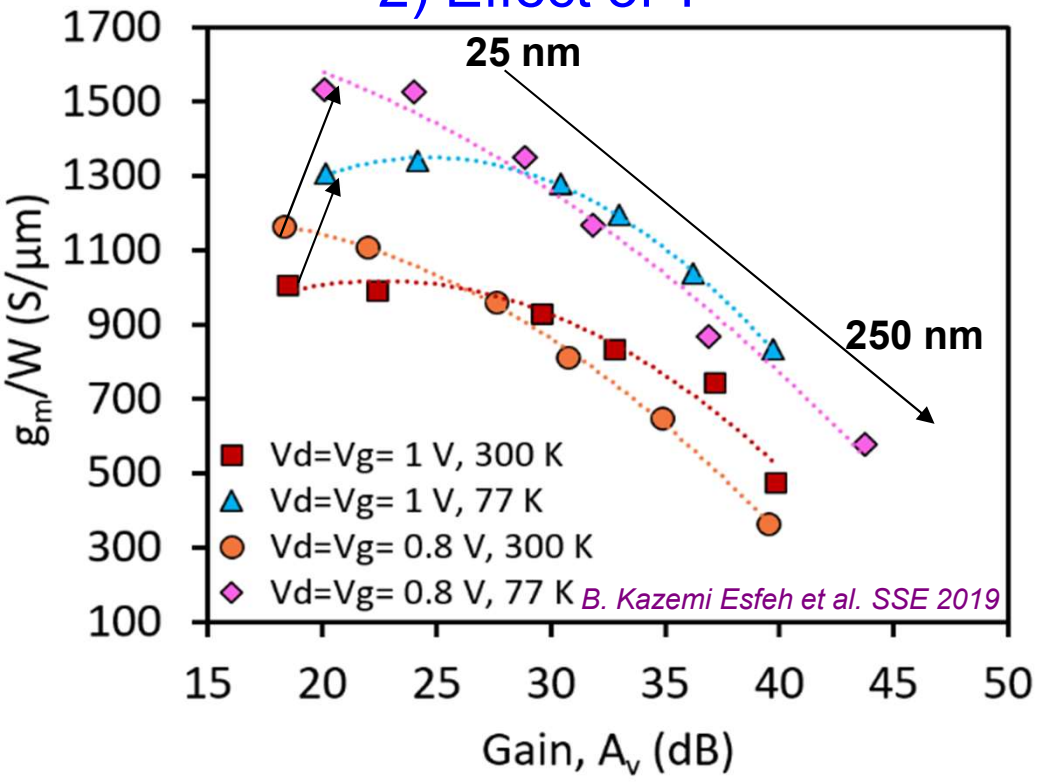
g_m-A_v Analog Metric

Examples

1) Effect of W_{NW}



2) Effect of T



❑ quasi volume inversion operation conditions + improved SCE control

⇒ I_d and g_m are improved

⇒ V_{EA} ↑ & A_v ↑

⇒ on the condition that $R_{sd,}$ interfaces, µ↓, etc. are well tolerated

❑ T reduction is beneficial for analog application as :

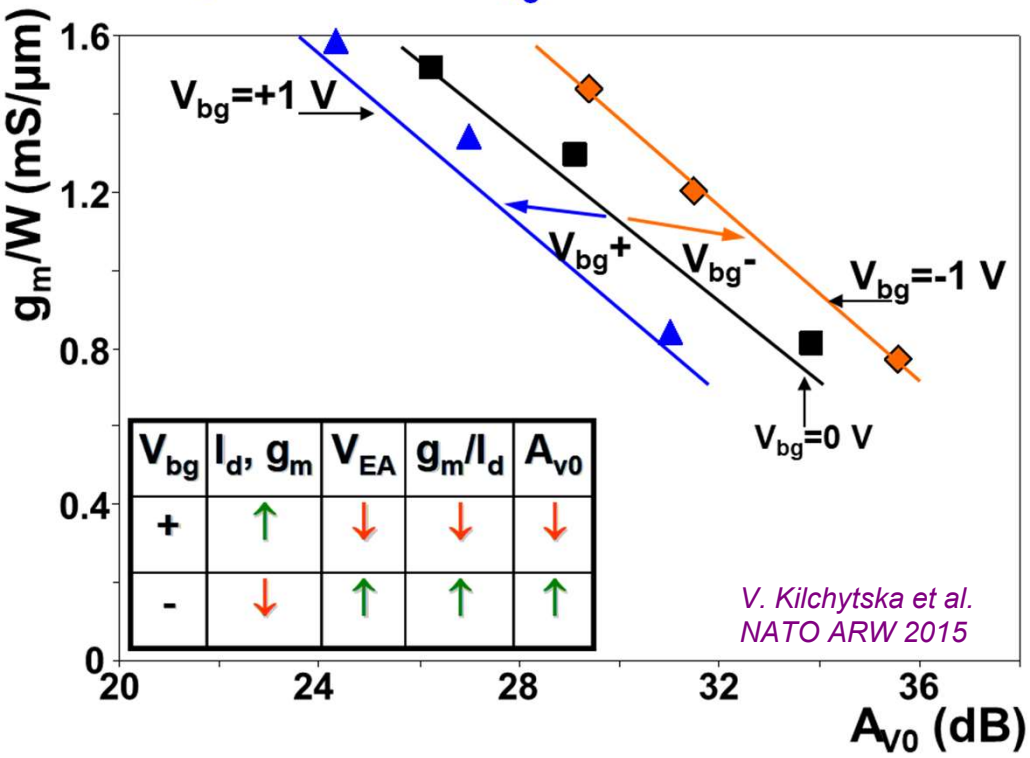
❑ Gain ↑

❑ g_m ↑

g_m-A_v Analog Metric

Examples

3) Effect of V_{bg} in UTBB FDSOI

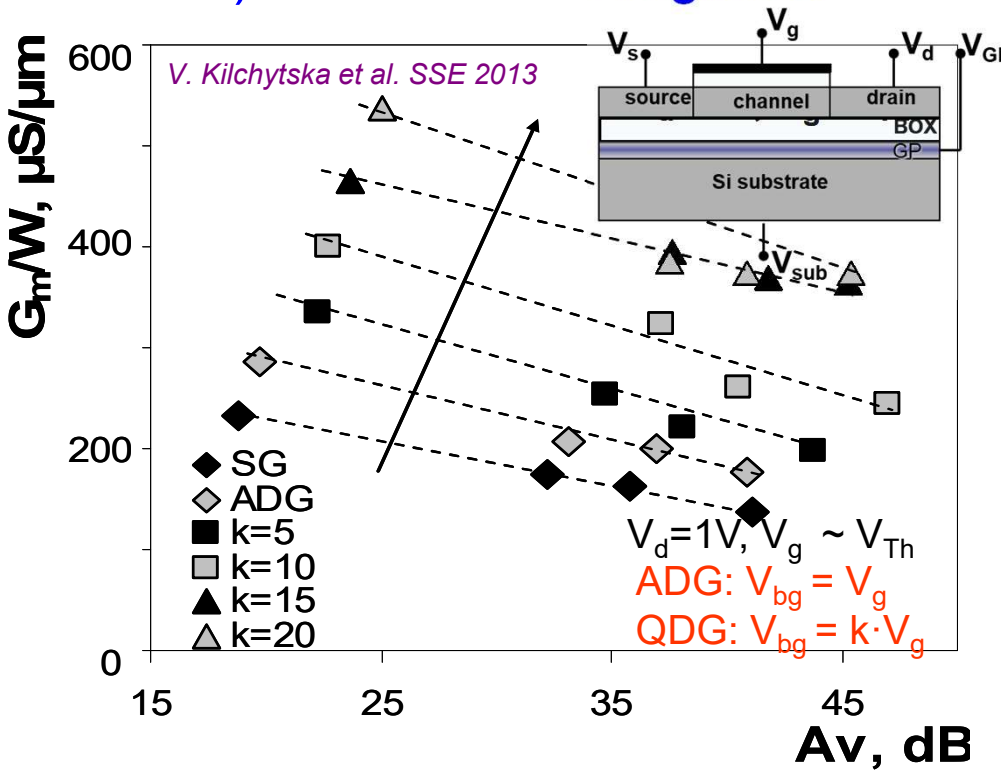


V_{bg}	I_d, g_m	V_{EA}	g_m/I_d	A_{v0}
+	↑	↓	↓	↓
-	↓	↑	↑	↑

- V_{sub} → "+" ⇨ g_m & $I_{d\ norm}$↑ of 5-10% (µ ↑)
- V_{sub} → "–" ⇨ V_{EA} ↑ (DIBL ↓) & G_m/I_d ↑↑ (V_T shift) ⇨ one can win ~ 5 dB in A_v max

⇒ Choice of V_{sub} "+" or "-" depends on targeted applications (either I_d ↑ or A_v ↑)

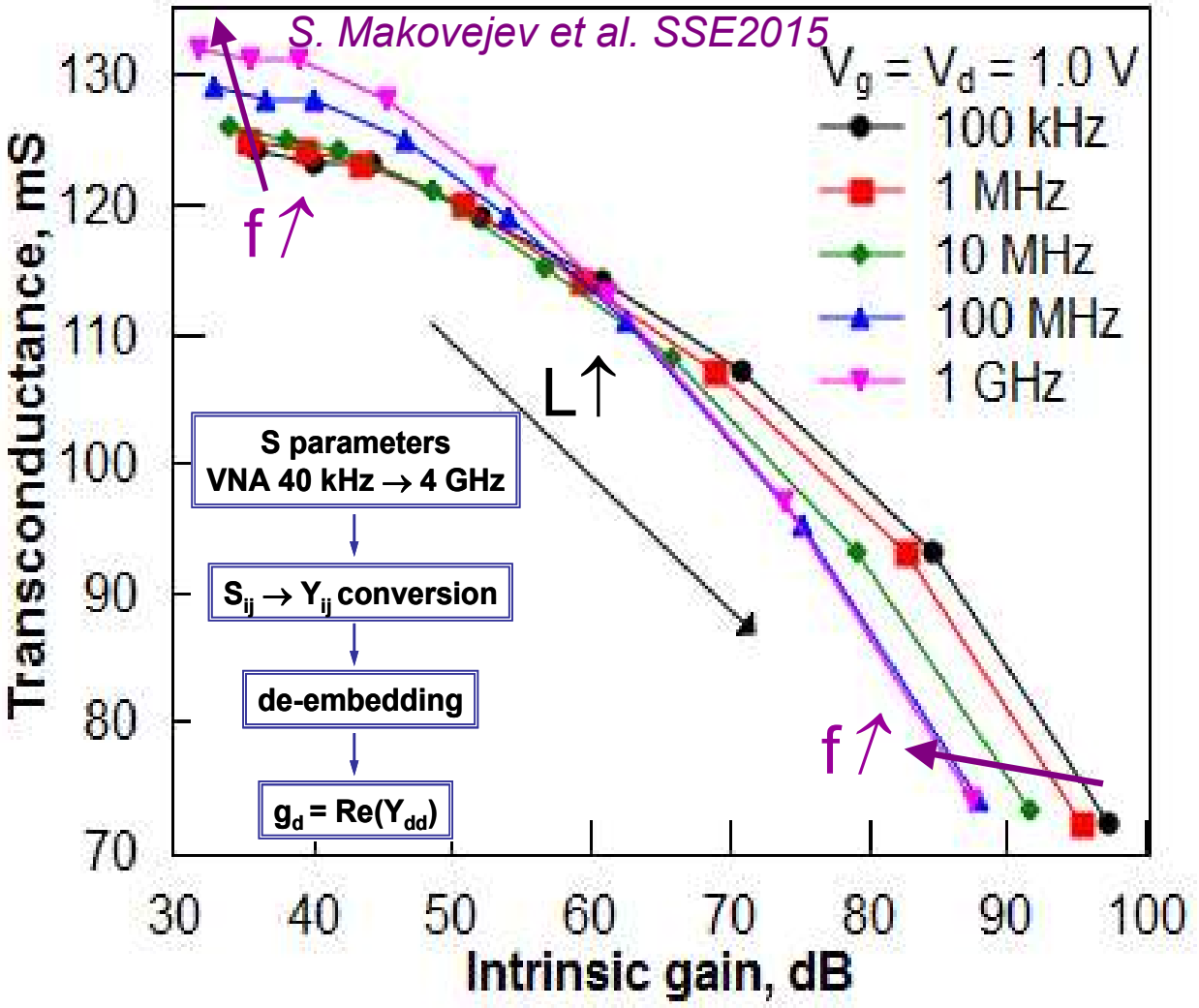
4) ADG or QDG regimes



- V_{Th} modulation in ADG & QDG mode is accompanied by S↓, DIBL ↓ and I_{off}=const *(Contrarily to the V_{sub} bias in SG mode)*
- I_d and G_m ↑↑ + DIBL↓ + A_v↑↑ can actually be exploited for analog applications
- impact of parasitics??? dynamic performance reduction ???

g_m-A_v Analog Metric

f-range



g_m – A_v analogue metric is strongly f-dependent

⇒ Performance prediction from DC data is insufficient

⇒ Frequency-dependent effects: *floating body, self-heating, substrate coupling, …*

$$g_d\,(f)\ \&\ g_m\,(f) \Rightarrow \ Gain\,(f)$$

⇒ Quest for wide-*f* characterization

g_m ↑, g_d ↑↑, A_v ↓ with f ↑

$$g_d(f) = g_{intr} + \Delta g_{d\_FB}(f) + \Delta g_{d\_SH}(f) + \Delta g_{d\_SUB}(f)$$

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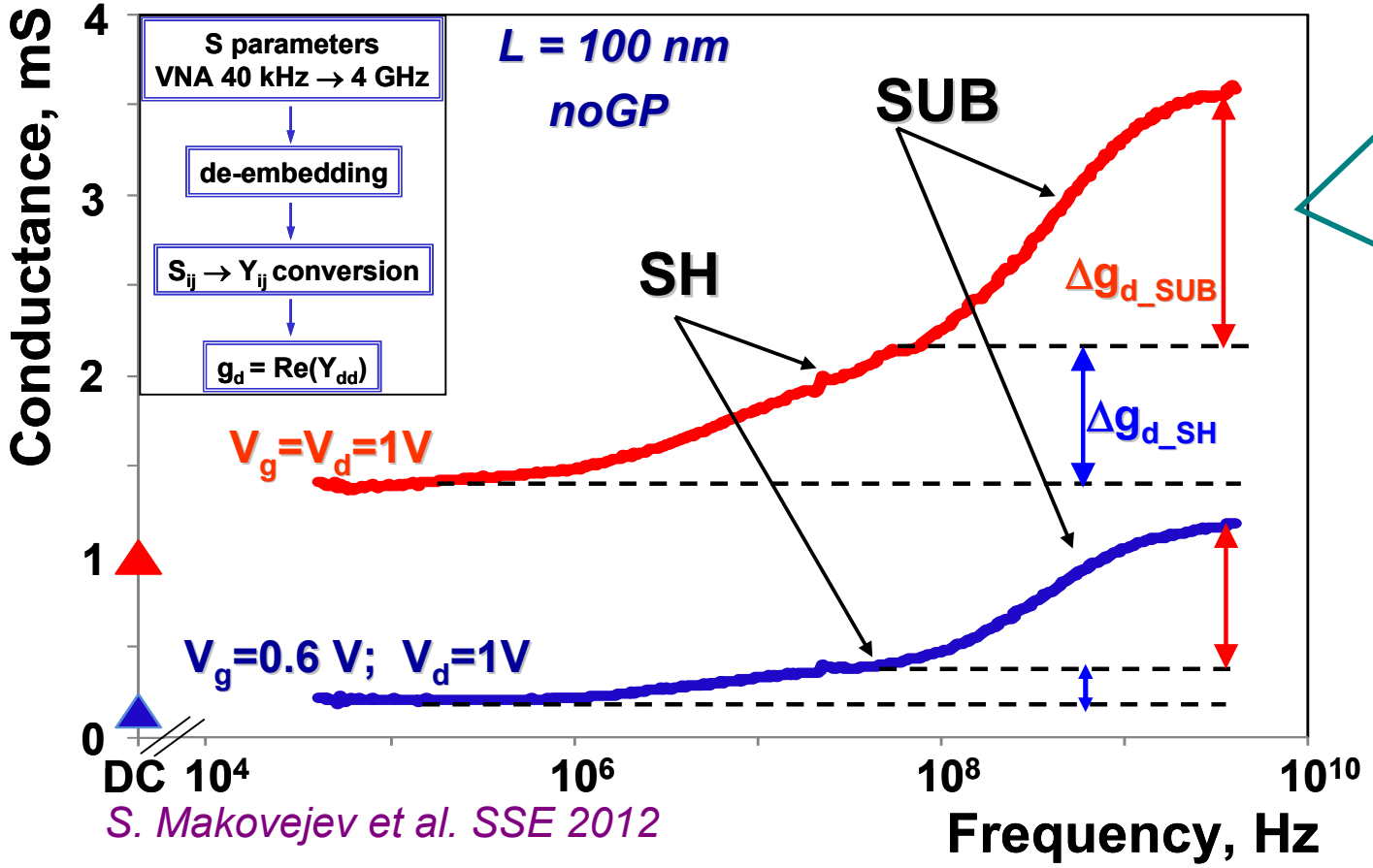
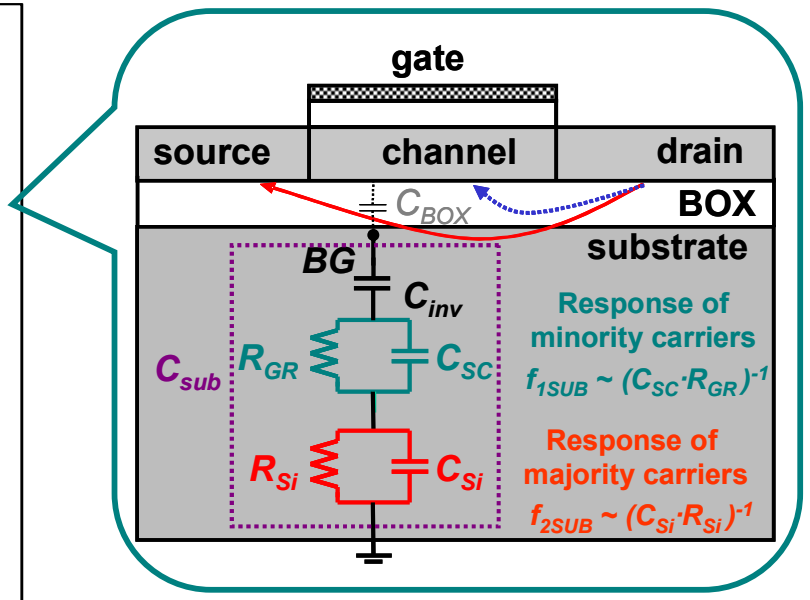
Methodology

Wide-f range approach

⇒ **Allows for distinguishing of different non-stationary effects**



S. Makovejev et al. SSE 2012



$$\Delta g_{d\_SUB} = (n-1) \cdot g_m \cdot \frac{v_{BGS}}{v_{DS}}$$

$$v_{BGS} \cong \frac{C_{BGD}}{C_{BGD} + C_{SBG} + C_{GBG} + C_{sub}} \cdot v_{DS}$$

V. Kilchytska et al. IEEE EDL 2003

⇒Two main reasons of $g_d(f)$ variation are: SH and SUB-related effects

$$g_d(f) = g_{intr} + \Delta g_{d\_FB}(f) + \Delta g_{d\_SH}(f) + \Delta g_{d\_SUB}(f)$$

Effect of technology downscaling on $g_d(f)$

- phonon boundary scattering ↑ (*when smaller than phonon mean free path 100-300 nm*)
- thermal capacitance C_{th} ↓
- use SOI-like architectures
- high J_{ds}

- S-to-D proximity
- Inversion in the substrate *(by V_d)* over the whole S-to-D distance

	SH	SUB
L ↓	↑	↑
T_{Si} ↓	↑	±
W_{fin} ↓	↑	↓
BOX ↓	↓	↑

- high J_{ds}
- interface proximities ⇒ interface effects ↑
- thermal conductivity ↓ ⇒ R_{th} ↑

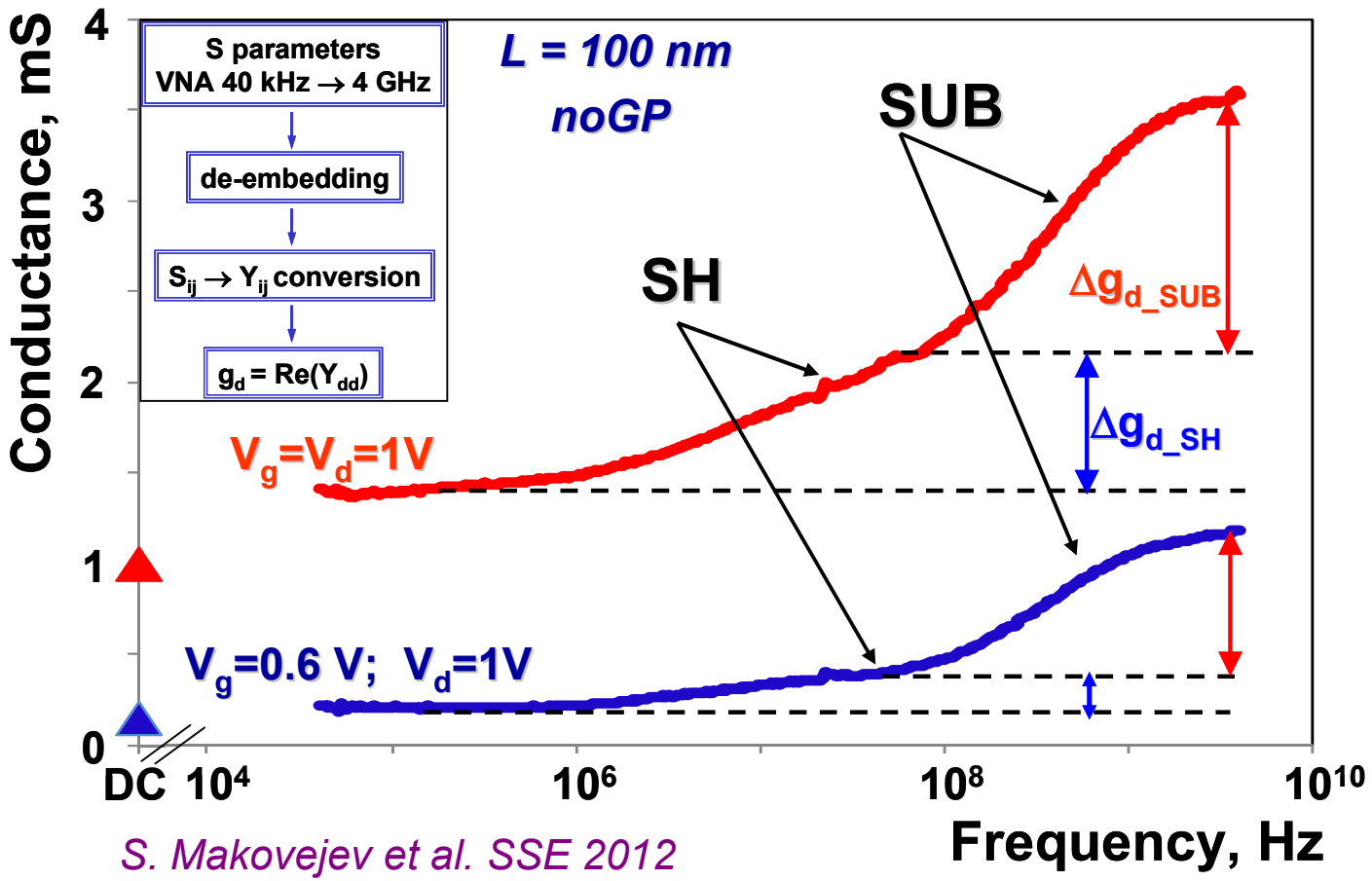
- coupling through the substrate reduces

- thinner thermal barrier

- stronger coupling through the substrate

Methodology

Wide-f range approach



S. Makovejev et al. SSE 2012

⇒ g_d degradation in f-range can be very strong (2-5 x of its DC value)

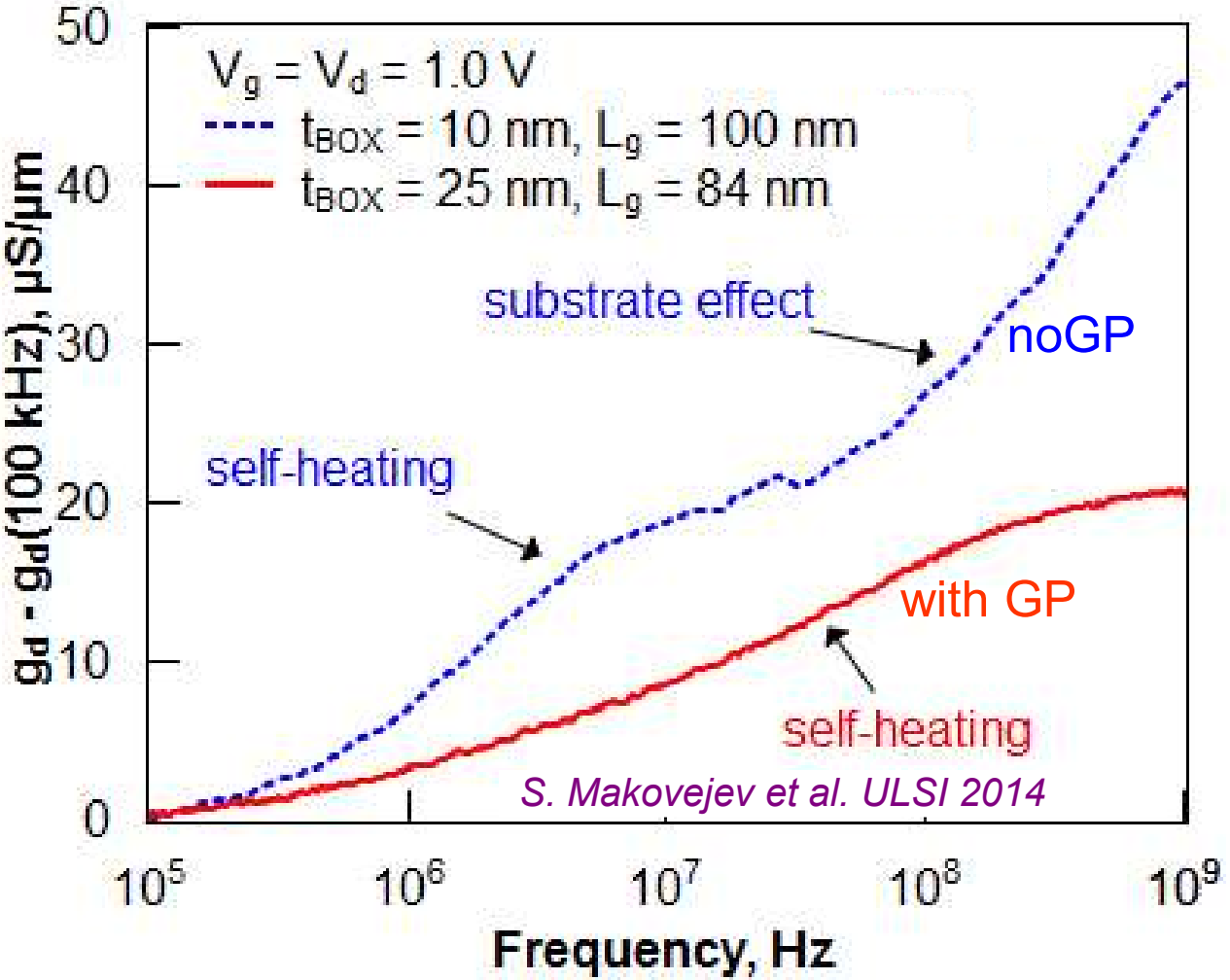
⇒Two main reasons of $g_d(f)$ variation are: SH and SUB-related effects

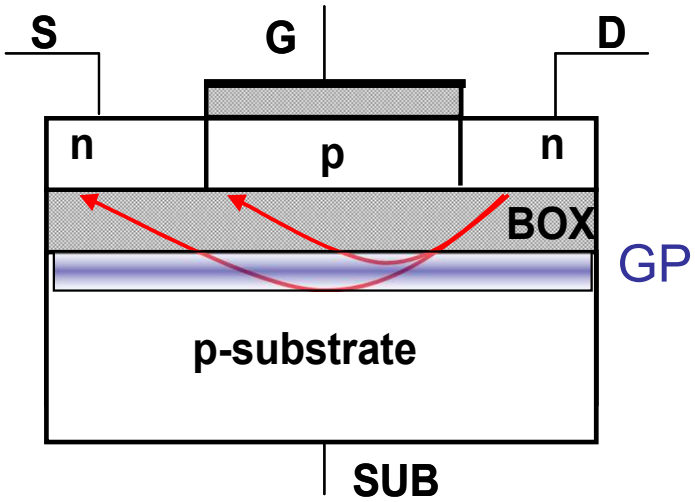
⇒ SUB-related degradation can be even stronger than SH-related one in UTBB devices without GP

Wide-f range

Examples

GP introduction





⇒ GP allows to suppress SUB-related g_d (f) variation

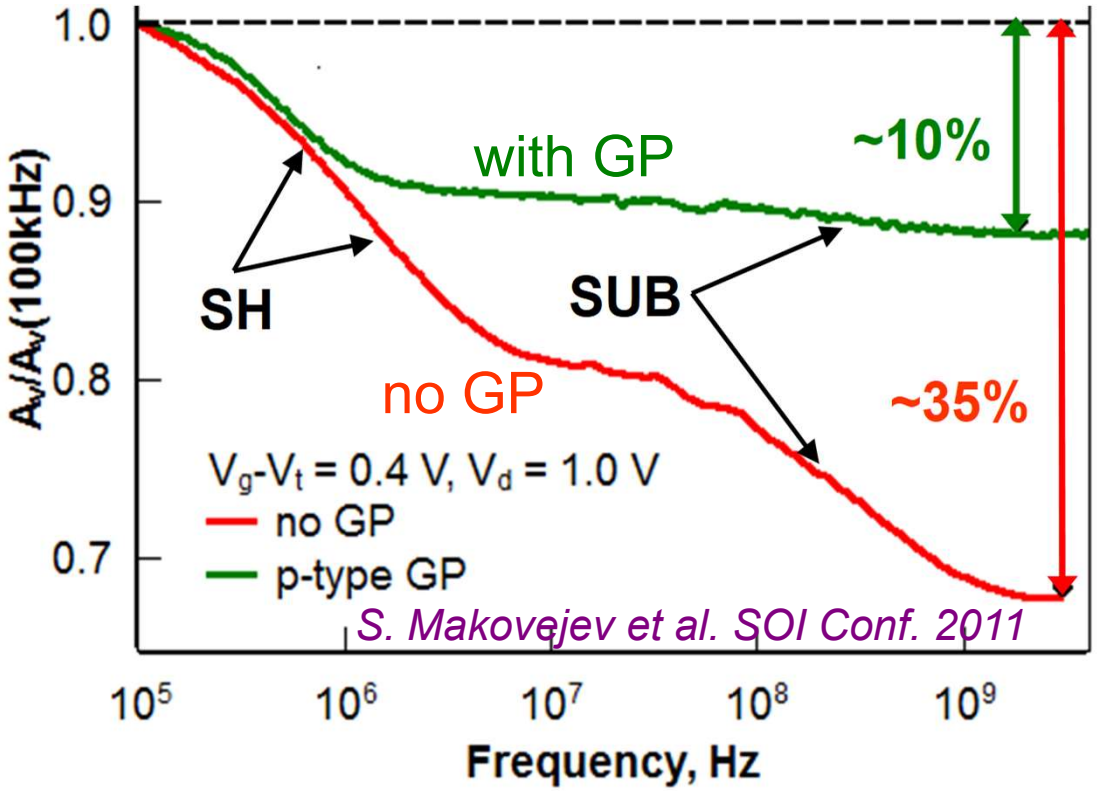
⇒ SH is the main reason of g_d(f) variation

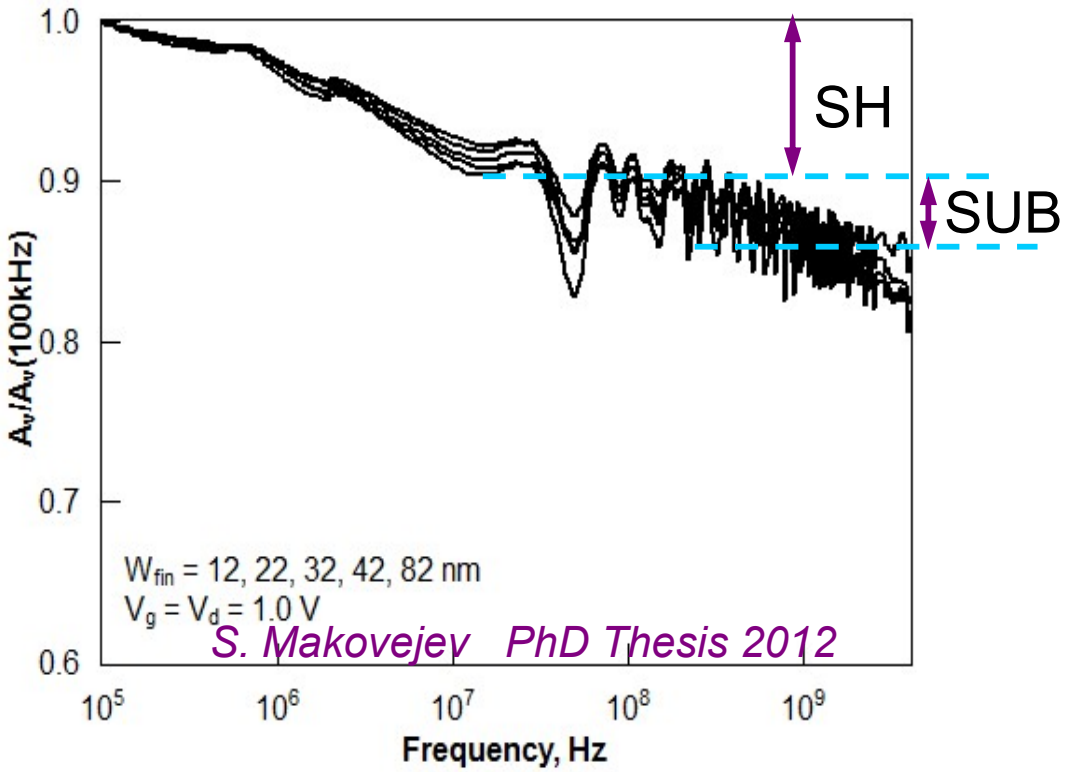
$$g_d(f) = g_{intr} + \Delta g_{d\_FB}(f) + \Delta g_{d\_SH}(f) + \Delta g_{d\_SUB}(f)$$

Wide-f range

Examples

UTBB versus FinFET





SH is the main reason of $g_d(f)$ variation
both in UTBB FDSOI and SOI-based FinFETs

Wide-f range

Examples

Different ways for SH reduction

⇒ Geometry optimization

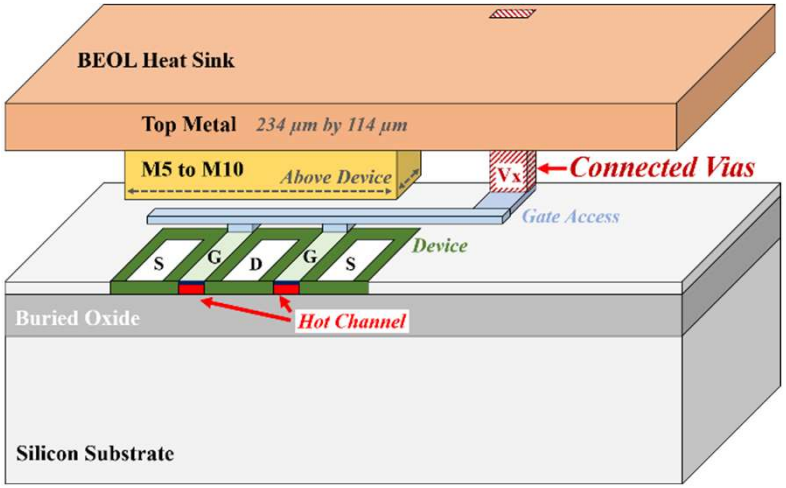
⇒ Lower bias

⇒ BOX thinning

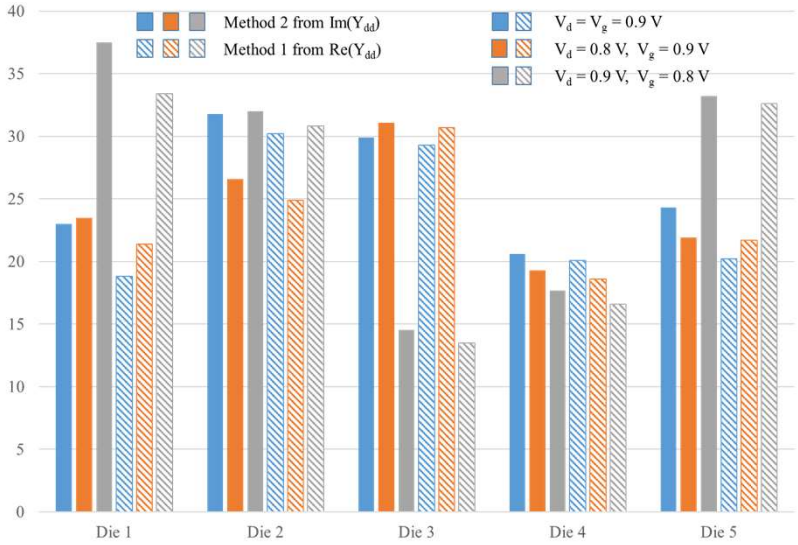
⇒ Use of high thermal conductivity materials

⇒ Heat sink implementation in the BEOL

⇒ ~20-30% of R_{th} reduction



R_{th} reduction, %



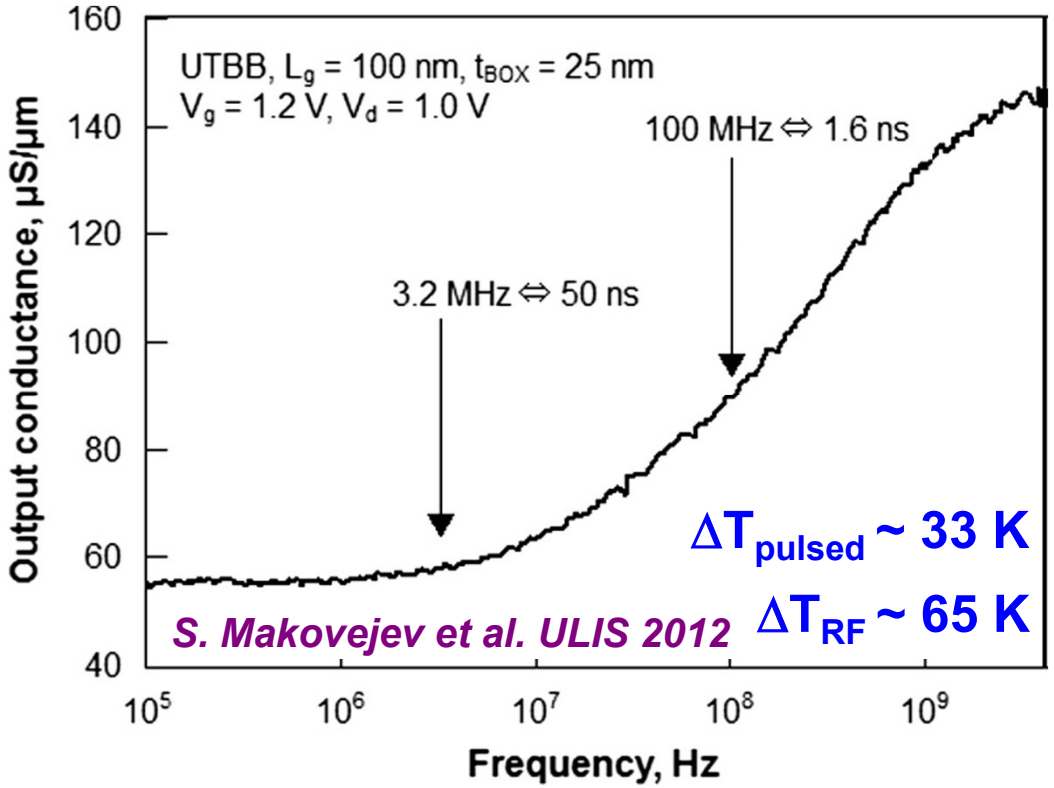
A. Halder et al, SSE 2021

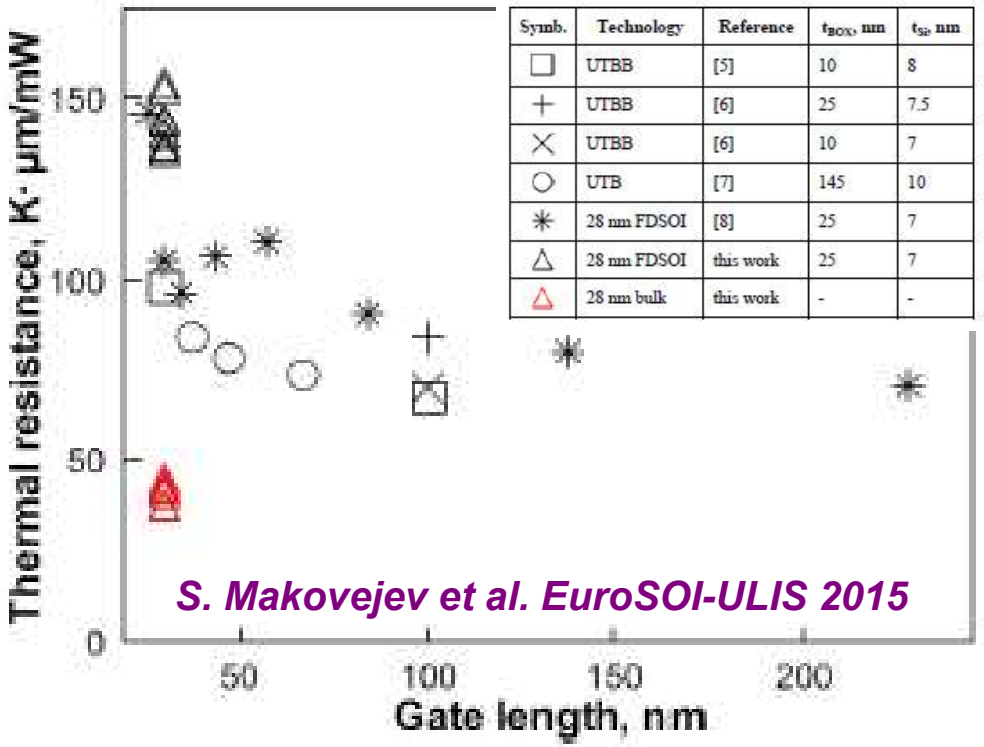
Wide-f range

Examples

SH features extraction using RF *(S-param)* method

$$R_{th} = \frac{\Delta g_{d\_SH}}{\left(I_d + g_{d\_LF} V_d\right) dI_d / dT_a} \Rightarrow \Delta T = R_{th} I_d V_d$$





Symb.	Technology	Reference	t_{BOX}, nm	t_{Si}, nm
□	UTBB	[5]	10	8
+	UTBB	[6]	25	7.5
×	UTBB	[6]	10	7
○	UTB	[7]	145	10
✳	28 nm FDSOI	[8]	25	7
△	28 nm FDSOI	this work	25	7
△	28 nm bulk	this work	-	-

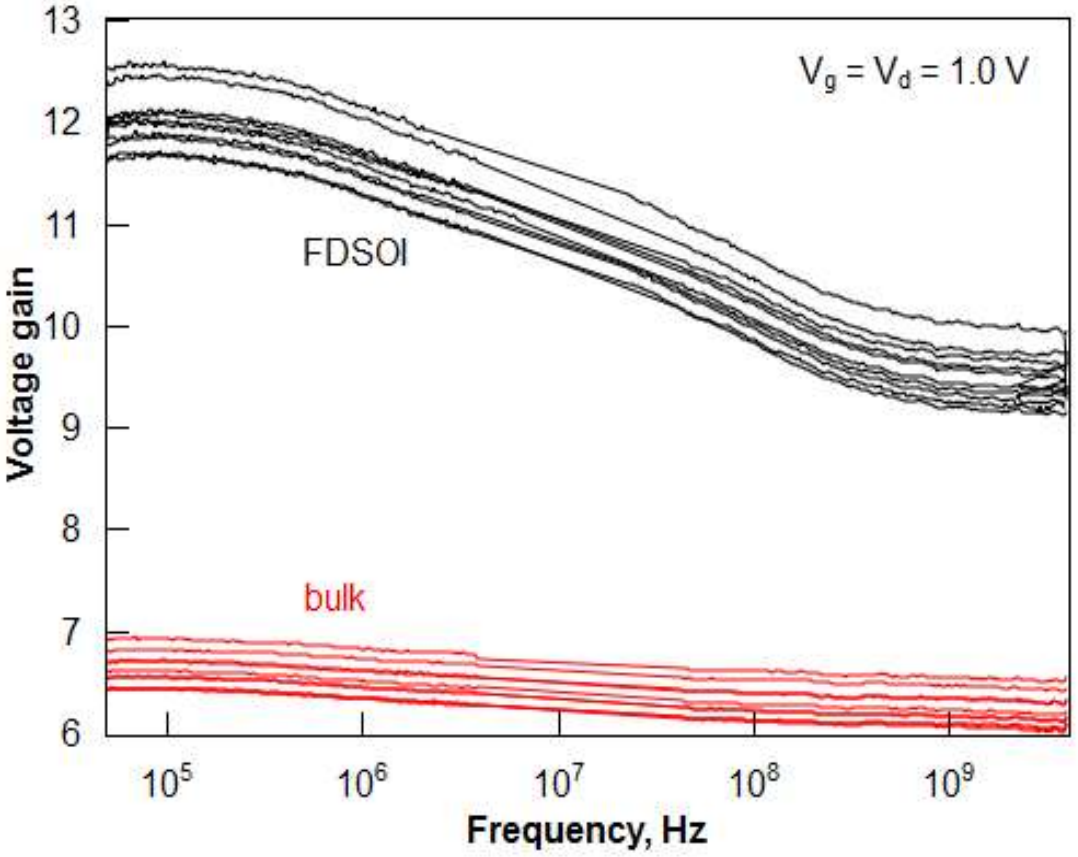
- Volume / surface is drastically decreasing
- R_{th} ~ 1/surface, C_{th} ~ volume
- $\tau_{th}=R_{th}\cdot C_{th}$ (nanoseconds → RF is needed)

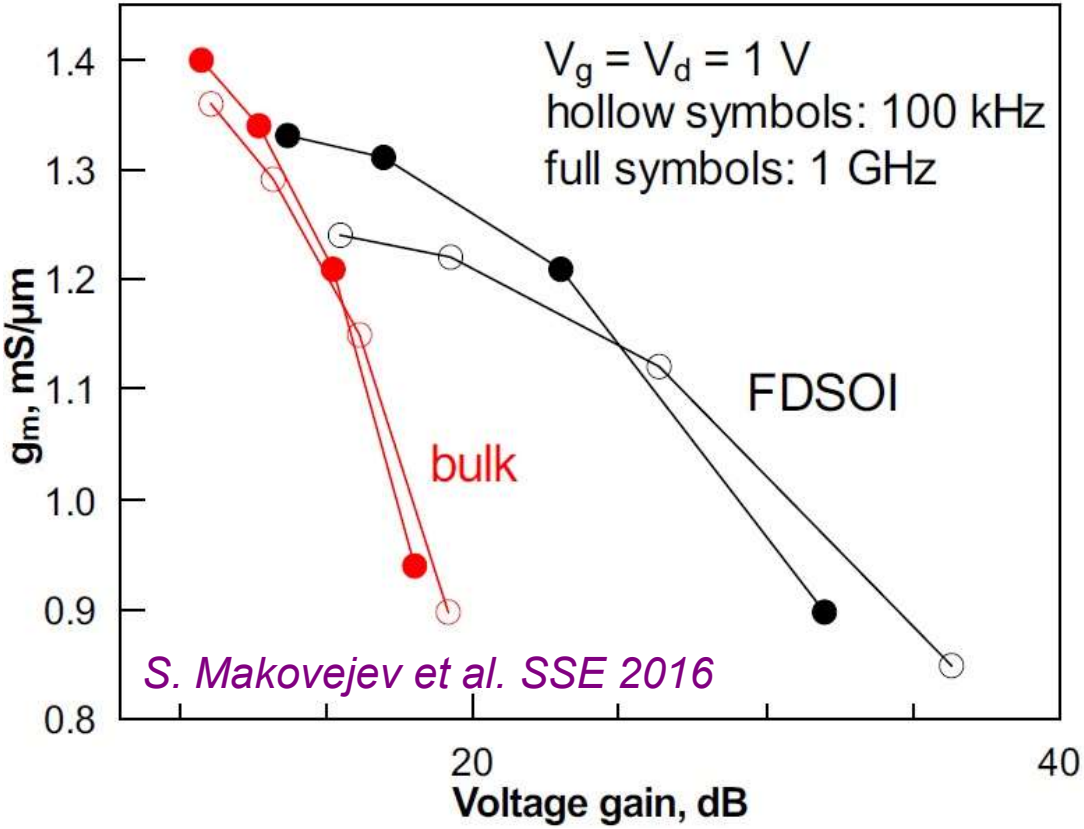
- R_{th} in bulk is lower than in any of benchmarked FDSOI
- C_{th} is higher in bulk than in FDSOI due to larger Si volume available for generated heat
- Temperature rise due to self-heating
  - ~32 K in bulk and ~87 K in FDSOI

Wide-f range

Examples

FDSOI versus Bulk



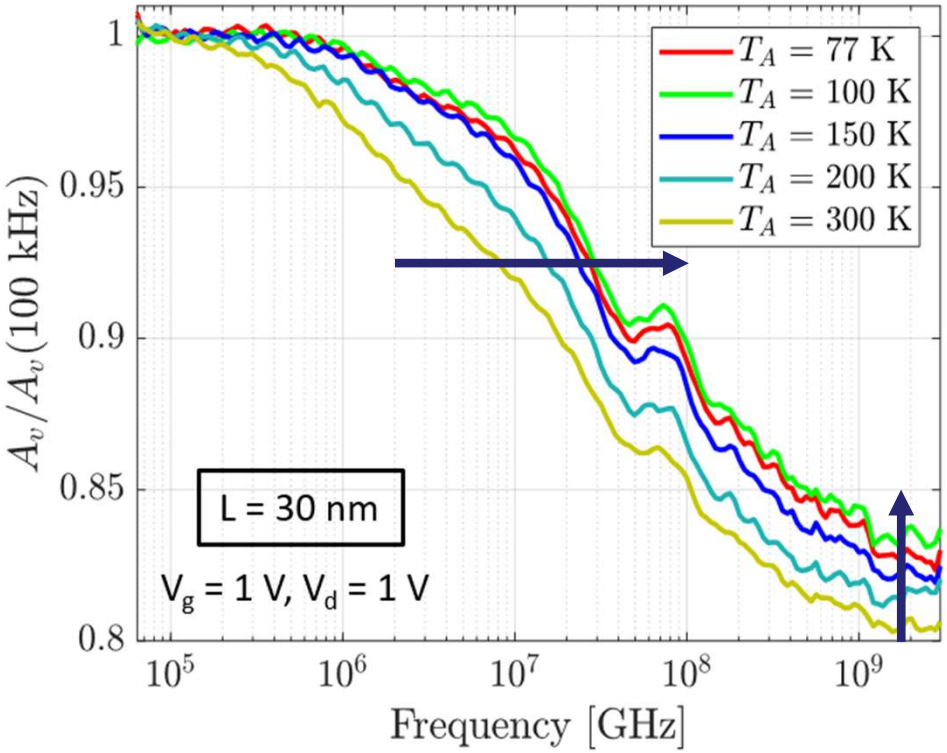


- In spite of stronger SH effect (*Temperature rise due to SH is ~32 K in bulk and ~87 K in FDSOI*), FDSOI outperform bulk in terms of Analog FoM in entire frequency range
- While thermal effects are stronger in FDSOI, their influence on device parameters is limited

Wide-f range

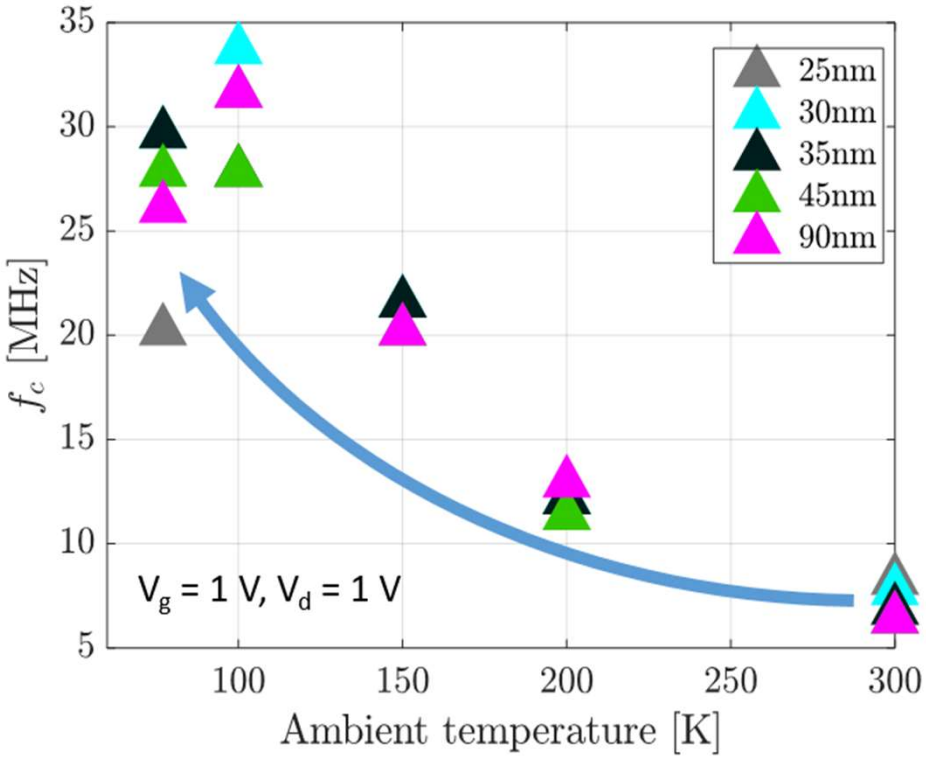
Examples

SH in cryogenic



ΔT_{77}~120K

ΔT_{300}~105K



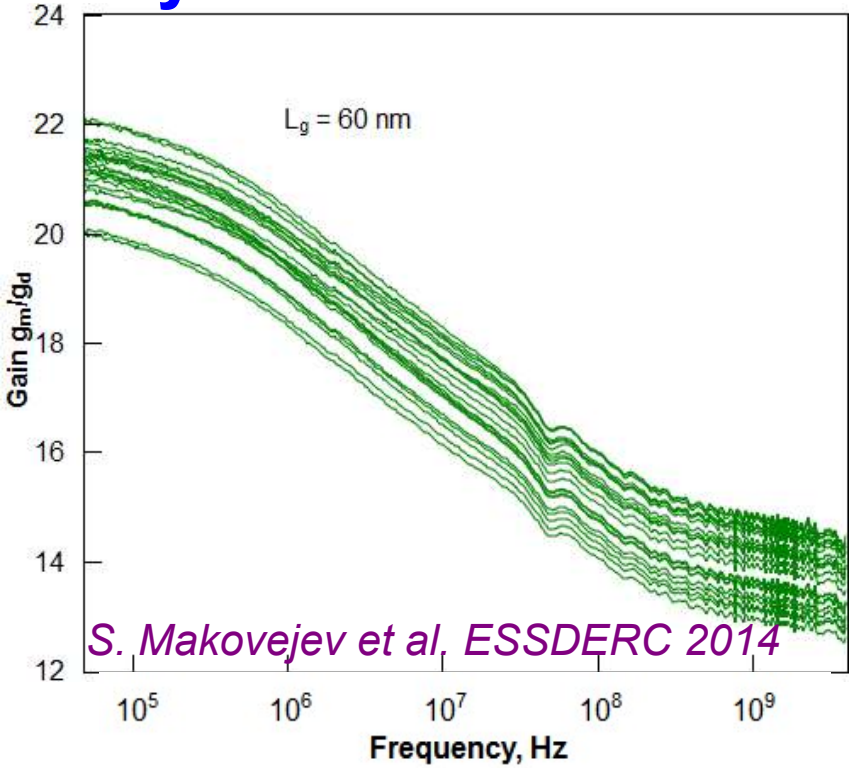
L. Nyssens et al. ESSDERC 2019

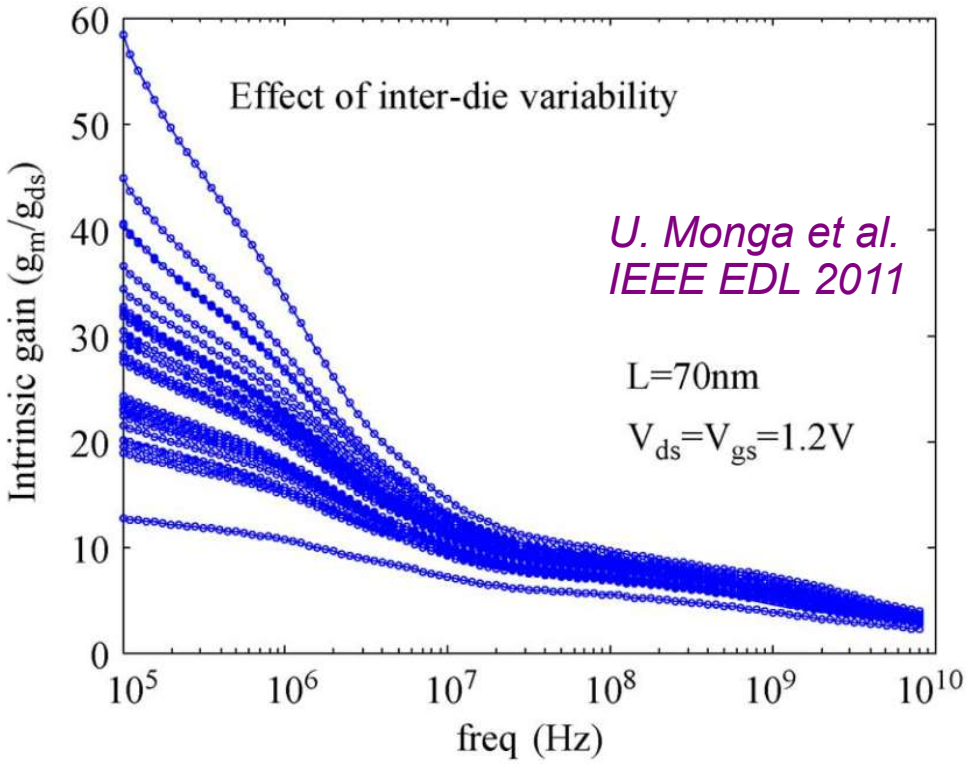
- SH-related degradation of Analog FoM is slightly reduced at cryogenic temperatures
- Thermal time constant is further reduced at cryo ⇒ RF technique is even more relevant
- Device temperature is particularly different from ambient at cryo ⇒ crucial for modelling

Wide-f range

Examples

Variability UTBB versus FinFET

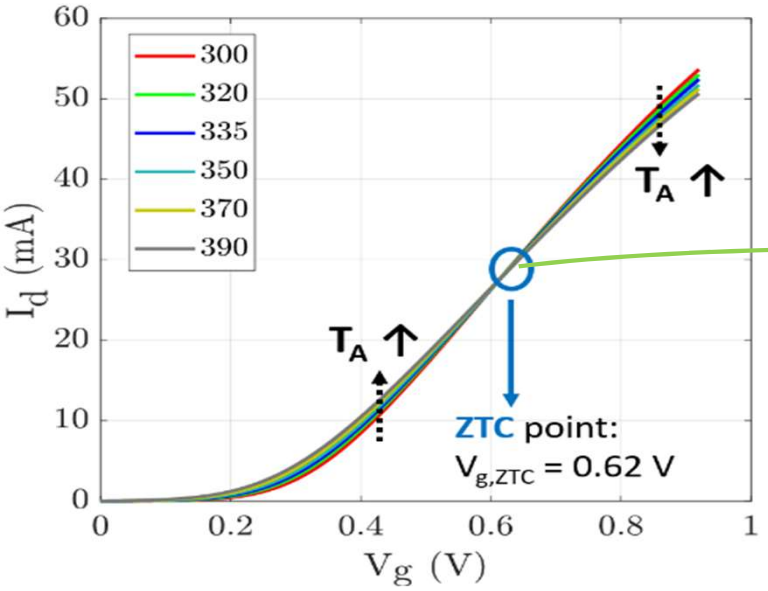


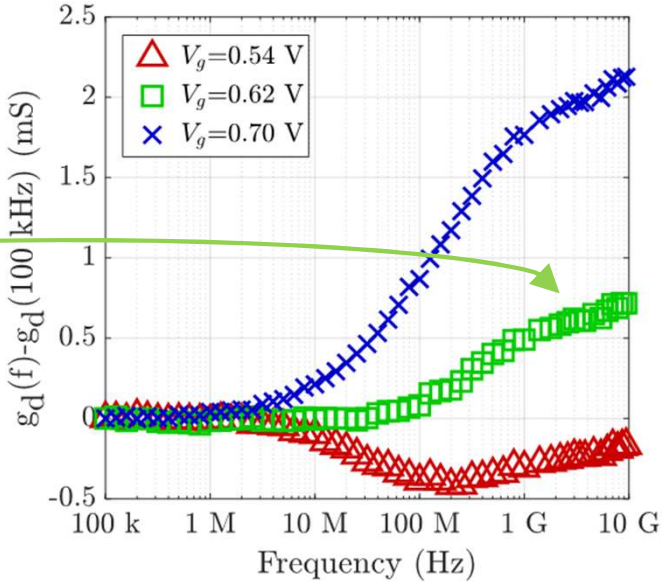


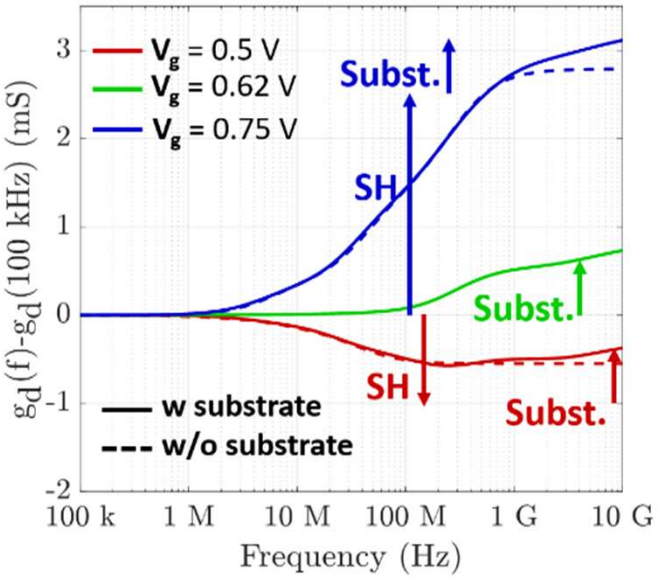
- Behavior in term of die-to-die variation is very different
  - FDSOI: small and almost f-independent
  - FinFETs: strong low-f inter-die variability and f-dependent (suggested SH)
- SH depends on device dimensions (T_{Si}, T_{BOX}, etc.) ⇒ subject to variability
- 3D architecture ⇒ control over the fin geometry is more challenging ⇒ SH-related variability is stronger *(dominates?)* in FinFETs

Wide-f range Separation of SHE and SE

Extraction at ZTC point allows for separate SHE and SE analysis







L. Nyssens et al. IEEE EDL 2021, VLSI 2021

⇒ **misestimation is ~5%, for large I_d**

⇒ **can reach ~50% for lower Id in M.I.**

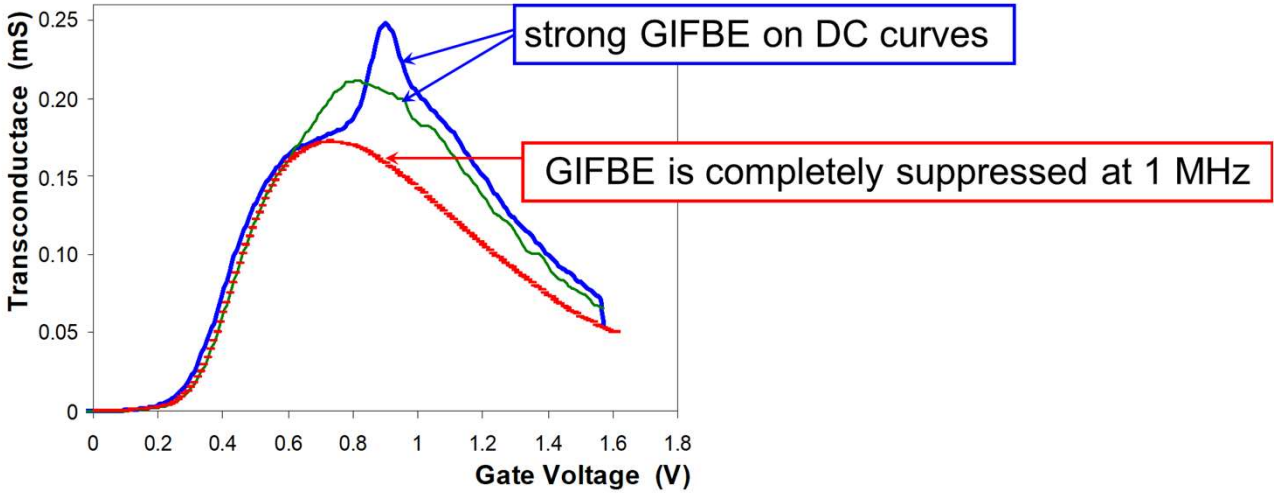
⇒ At ZTC point g_d (f) variation is SHE free

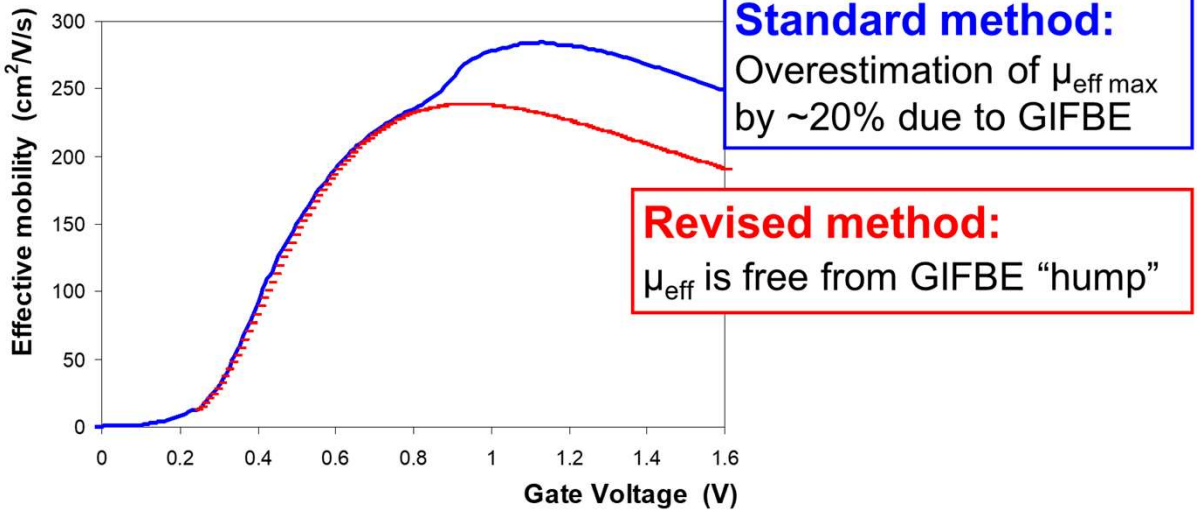
⇒ Allows for "clean" (SHE-free) extraction of Substrate/Back gate network

⇒ Substrate Effect-free extraction of SHE parameters

Examples

Mobility extraction using split C-V





V. Kilchytska et al. EDL 2005

Standard split C-V

$$\mu_{eff} = \frac{L^2 \cdot I_D}{V_D \cdot \int_{V_0}^{V_G} C_{GC}(V_G) dV_G}$$

Revised split C-V

$$\mu_{eff} = \frac{L^2}{V_D} \cdot \frac{\int_{V_0}^{V_G} G_m(V_G) dV_G + I_{D_0}}{\int_{V_0}^{V_G} C_{GC}(V_G) dV_G}$$

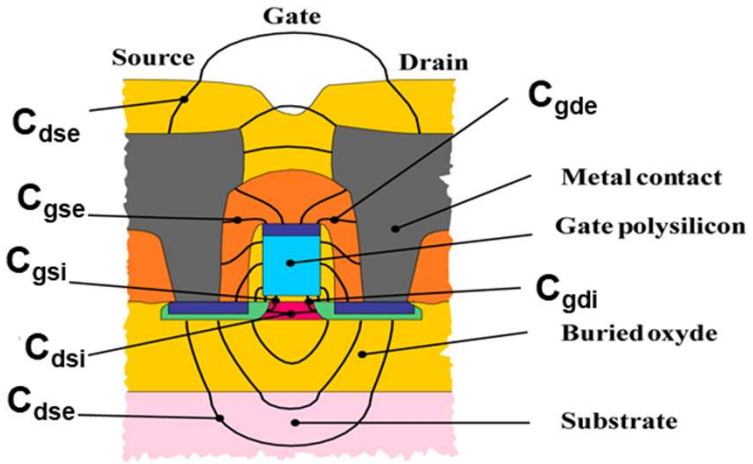
- an integral of high-frequency transconductance instead of the DC drain current to suppress influence of GIFBE on extracted μ_{eff}
- allows for extraction of non-stationary effects-free mobility

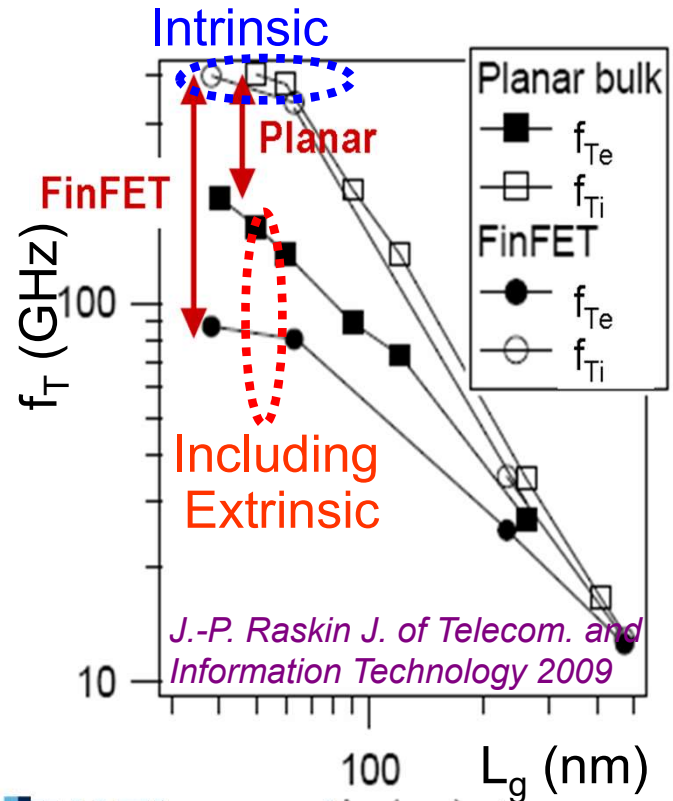
Outline

- ✓ Introduction
- ✓ Analog/RF Figures of Merit
- ✓ Methodology used for device assessment
  - ⇒ DC-based Techniques
  - ⇒ Wide frequency range measurements
  - ⇒ RF characterization methodology
- ✓ Conclusions

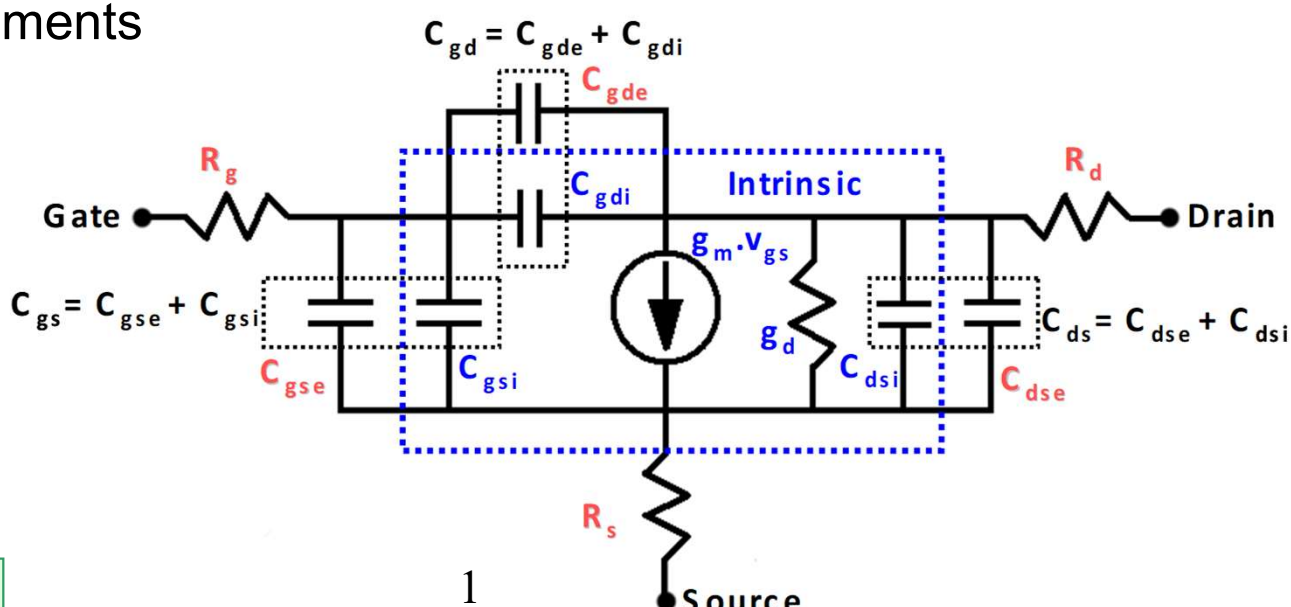
Methodology

RF Characterization





- With devices downscaling importance of extrinsic device parasitics enormously increases. They can even dominate.
- Particularly important for advanced architectures
- It is important to separate "intrinsic" and "extrinsic" elements



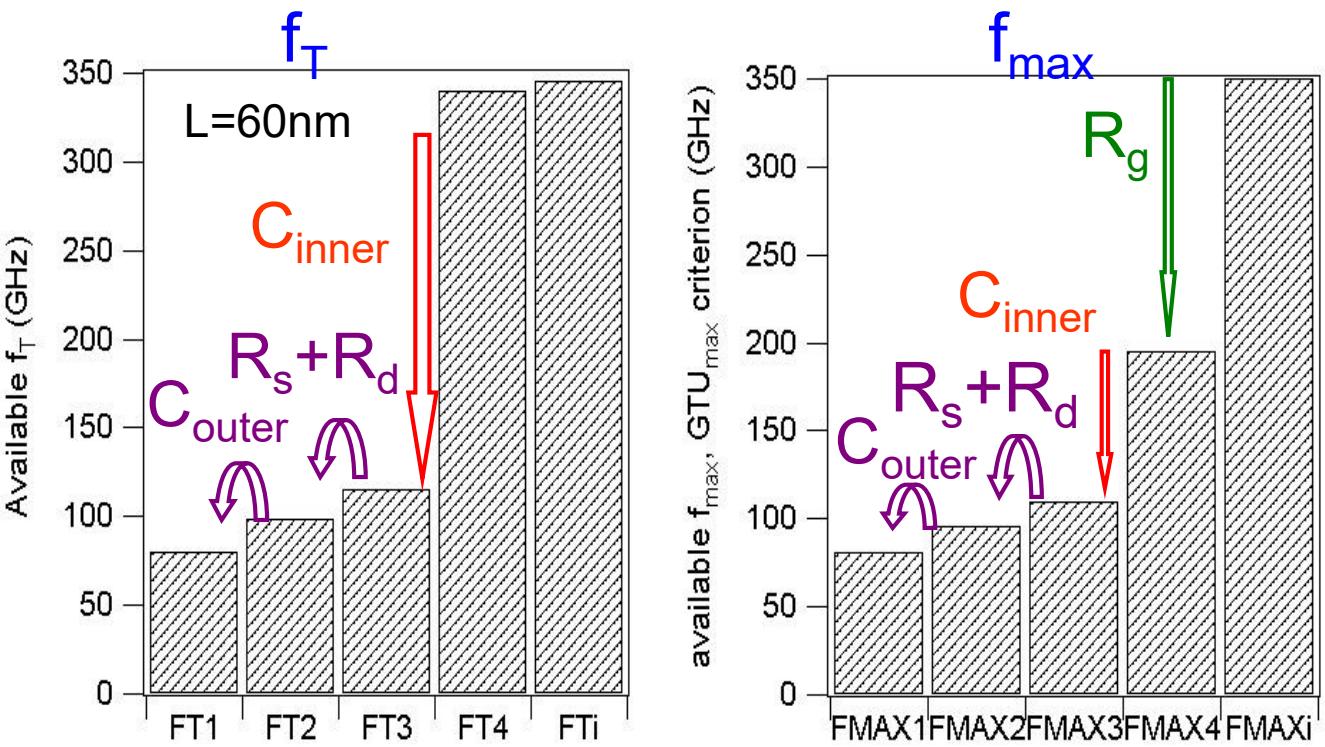
$$f_T \approx \frac{g_m}{2 \cdot \pi \cdot C_{gs}} \frac{1}{\left(1 + \frac{C_{gd}}{C_{gs}}\right) + (R_s + R_d) \cdot \left(\frac{C_{gd}}{C_{gs}} \cdot (g_m + g_d) + g_d\right)}$$

$$f_{max} \approx \frac{g_m}{4 \cdot \pi \cdot C_{gs}} \frac{1}{\left(1 + \frac{C_{gd}}{C_{gs}}\right) \sqrt{g_d \cdot (R_g + R_s) + \frac{1}{2} \cdot \frac{C_{gd}}{C_{gs}} \cdot \left(R_s \cdot g_m + \frac{C_{gd}}{C_{gs}}\right)}}$$

RF Methodology

Examples

FinFETs



J.-P. Raskin J. of Telecom. and Information Technology 2009

- ❑ 60% of f_T ↓ is due to C_{inner}
- ❑ 15% due to C_{outer} + $R_{S,D}$
- ❑ 40% of f_{max} ↓ is due to R_g
- ❑ 30% due to C_{inner}

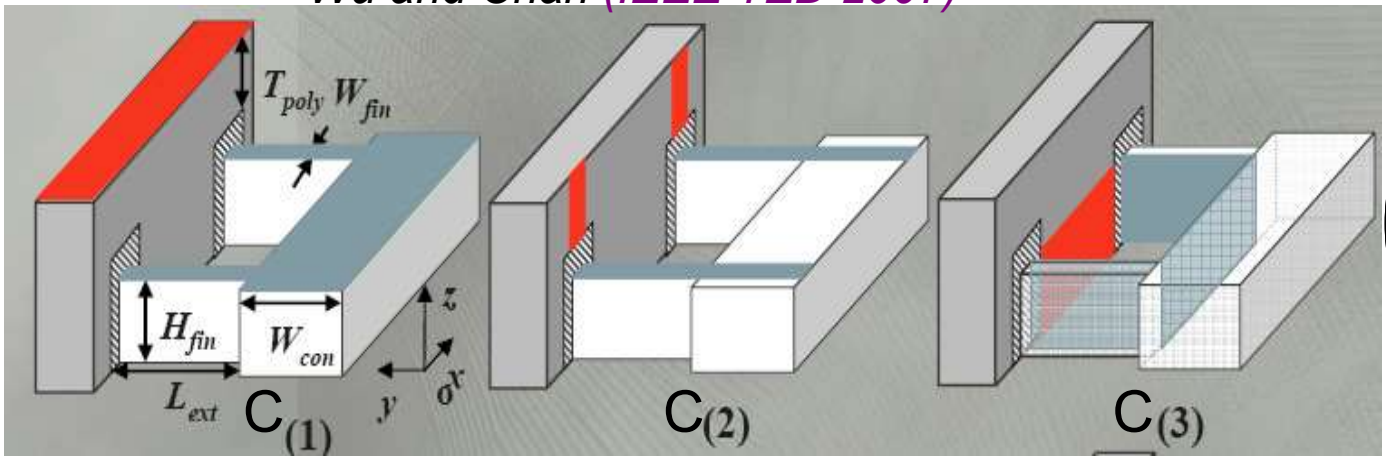
⇒ C_{inner} is a big bottleneck for FinFET's RF performance

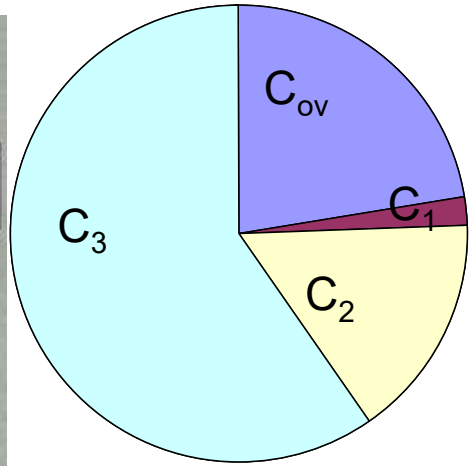
⇒ Specific for 3D

⇒ Largest effect is due to coupling between S/D side walls and G wrapping between the fins

⇒ C_{inner} is predicted to be re-duced by S_{fin}↓ or by H_{fin}/W_{fin} ↑

Wu and Chan (IEEE TED 2007)



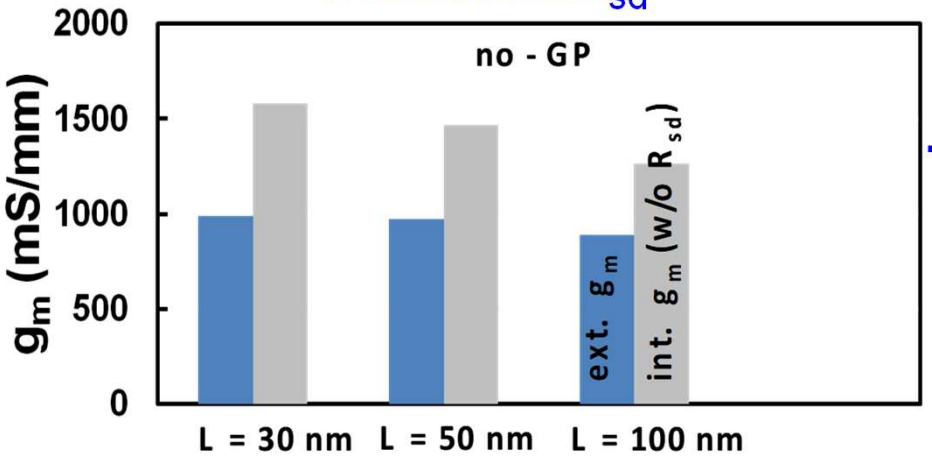


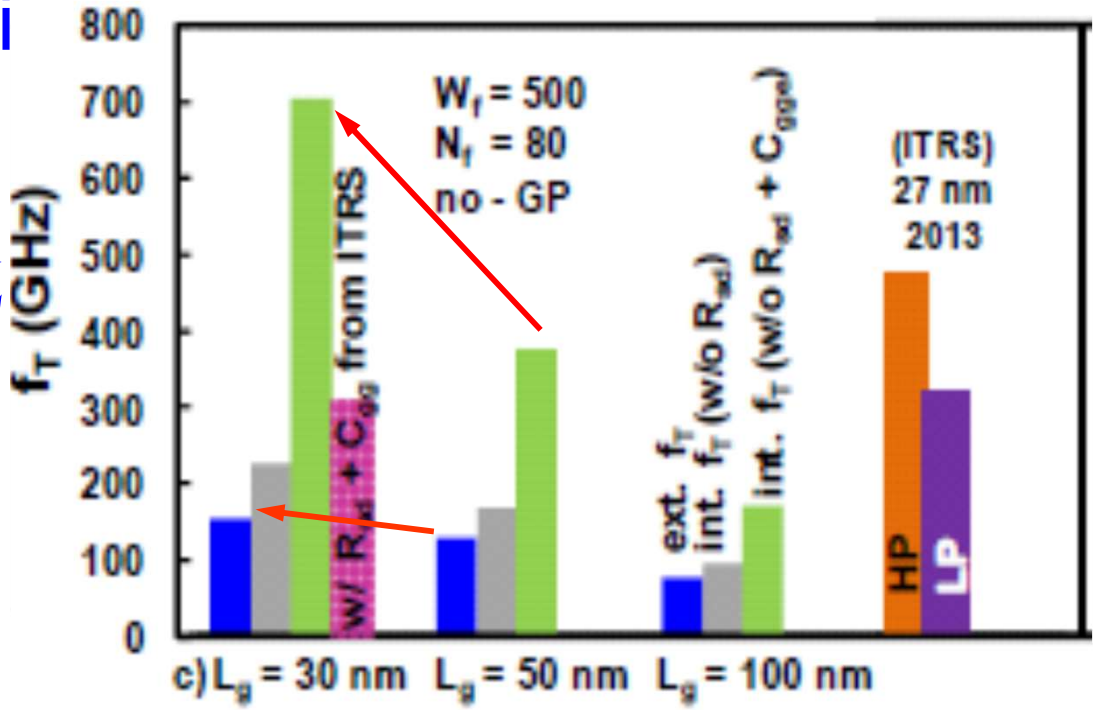
RF Methodology

Examples

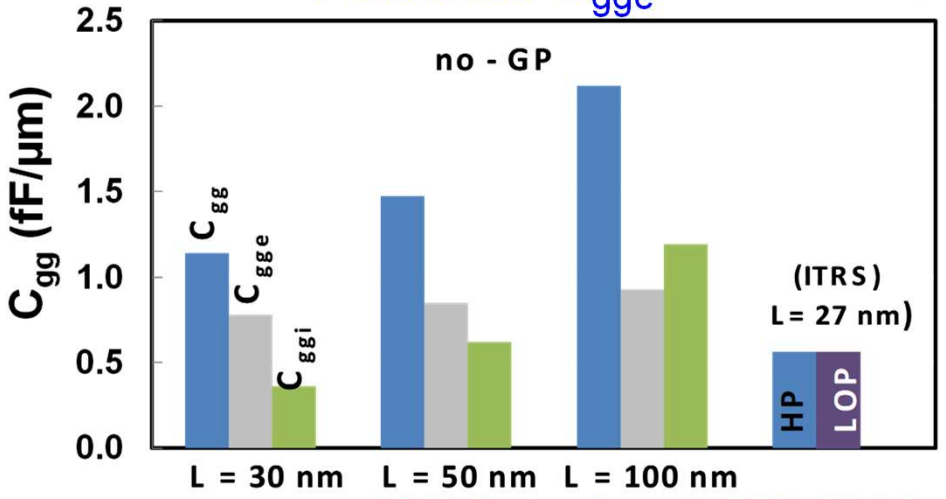
UTBB - Leti

Parasitic R_{sd}





Parasitic C_{gge}



M.K.Arshad et al, SSE 2014

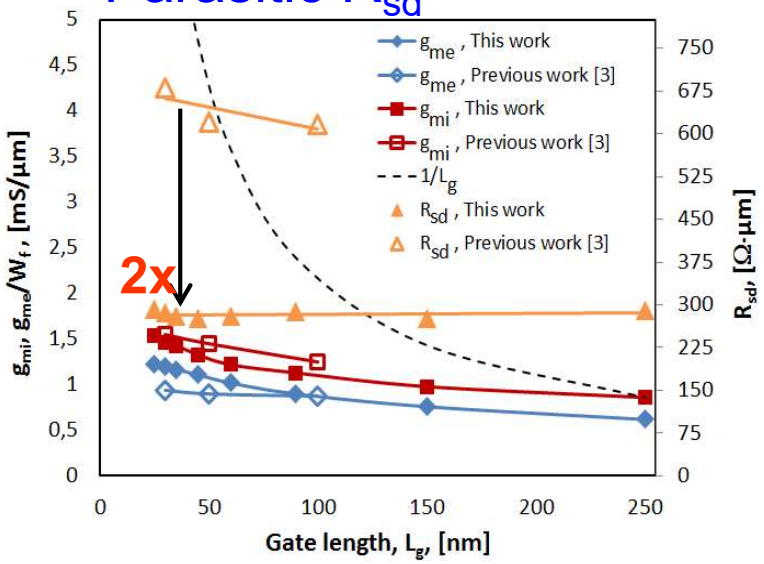
- Increased impact of R_{sd} and C_{gge} as L ↓
- particularly C_{gge}: $C_{ggi} > C_{gge}$ in 100 nm-long devices, but $C_{gge} > C_{ggi}$ in 30 nm-long ones
- Process was not optimized for RF
- f_T as high as requested by ITRS for LP applications is achievable if ITRS requirements for R_{sd} and C_{gg} are respected

RF Methodology

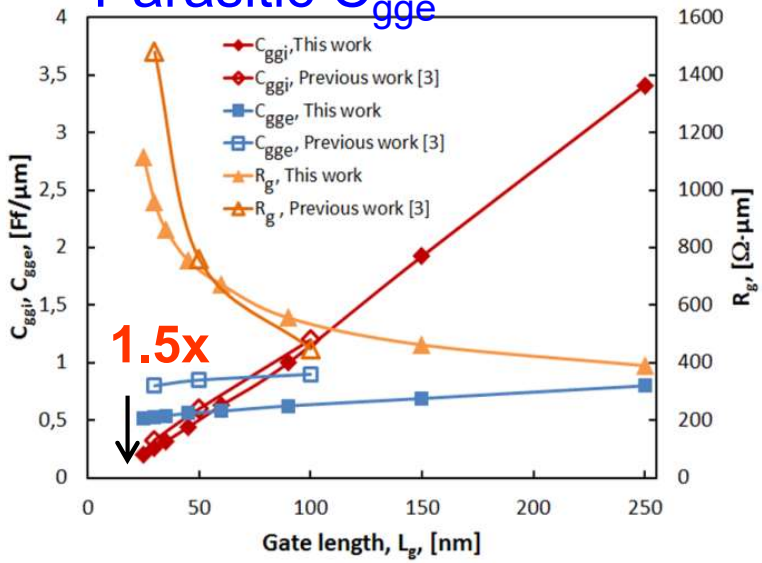
Examples

28FDSOI vs UTBB - Leti

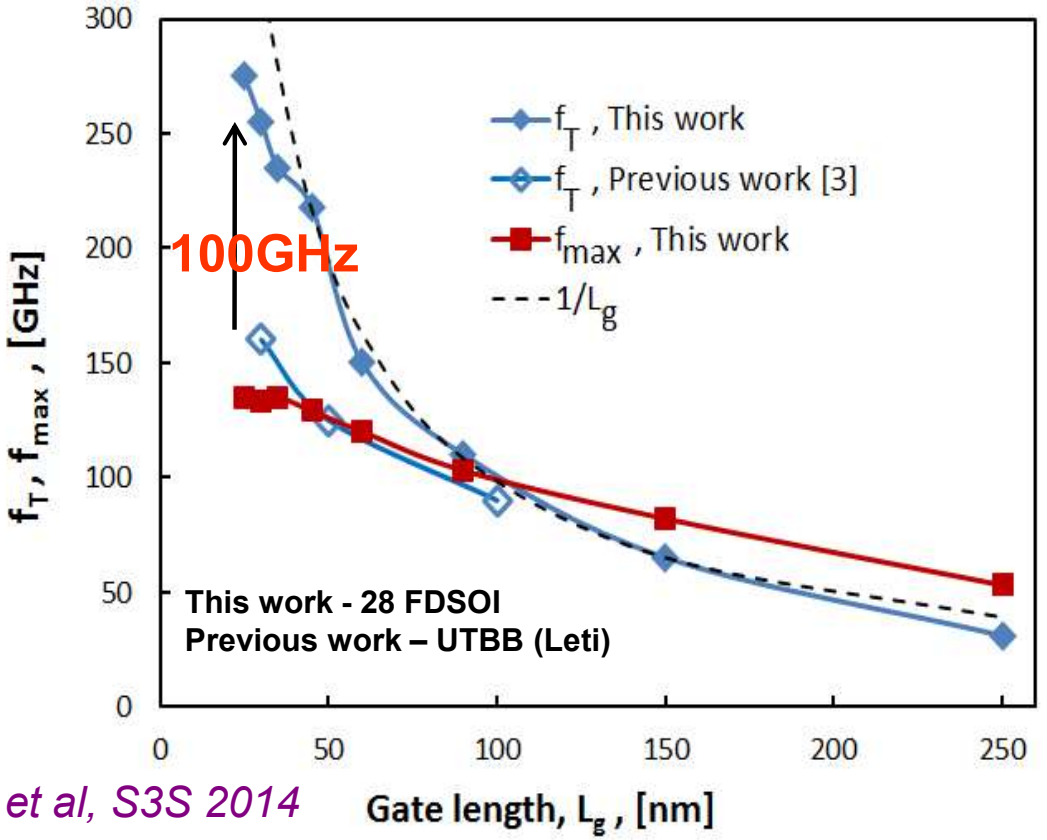
Parasitic R_{sd}



Parasitic C_{gge}



f_T



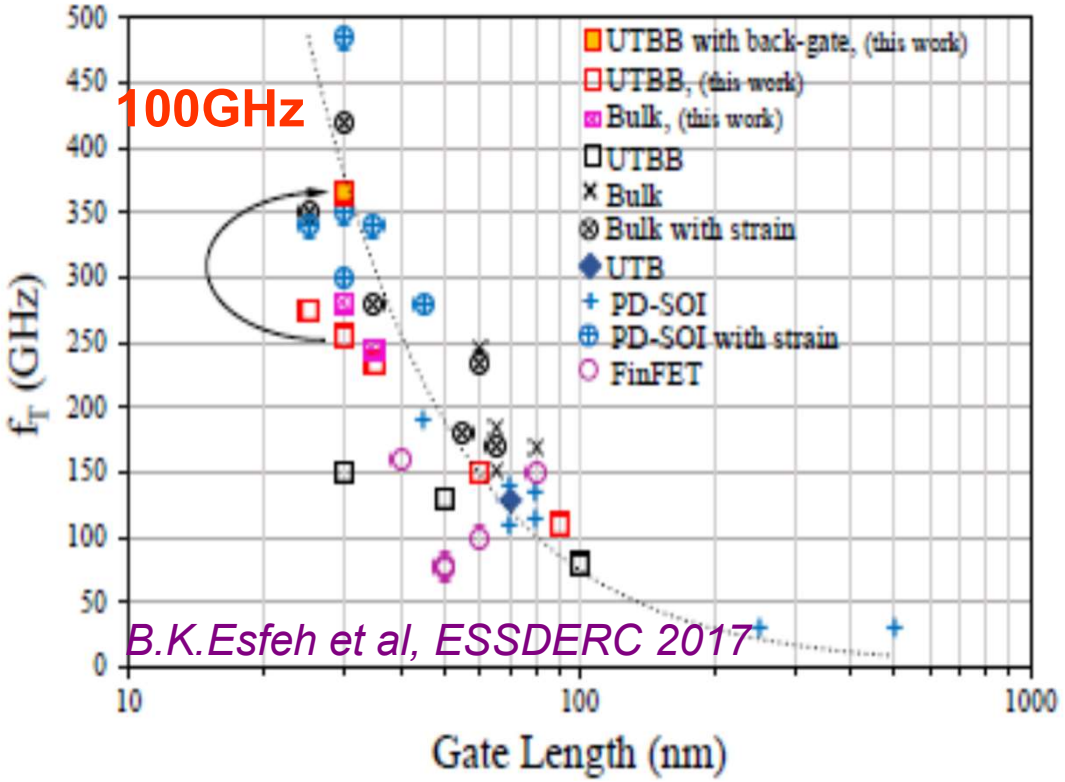
B.K.Esfeh et al, S3S 2014

28FDSOI to UTBB *(Leti)* **improvement of parasitics** ***(R_{sd}, R_g, C_{gg_ext}) ⇒ f_T ~ 280GHz and f_{MAX} ~ 250 GHz***

slightly lower than requested by ITRS ***(f_T=322 GHz , f_{max} = 284 GHz for L_g=24 nm) ⇒ further improvements?***

Examples

Newest 28FDSOI

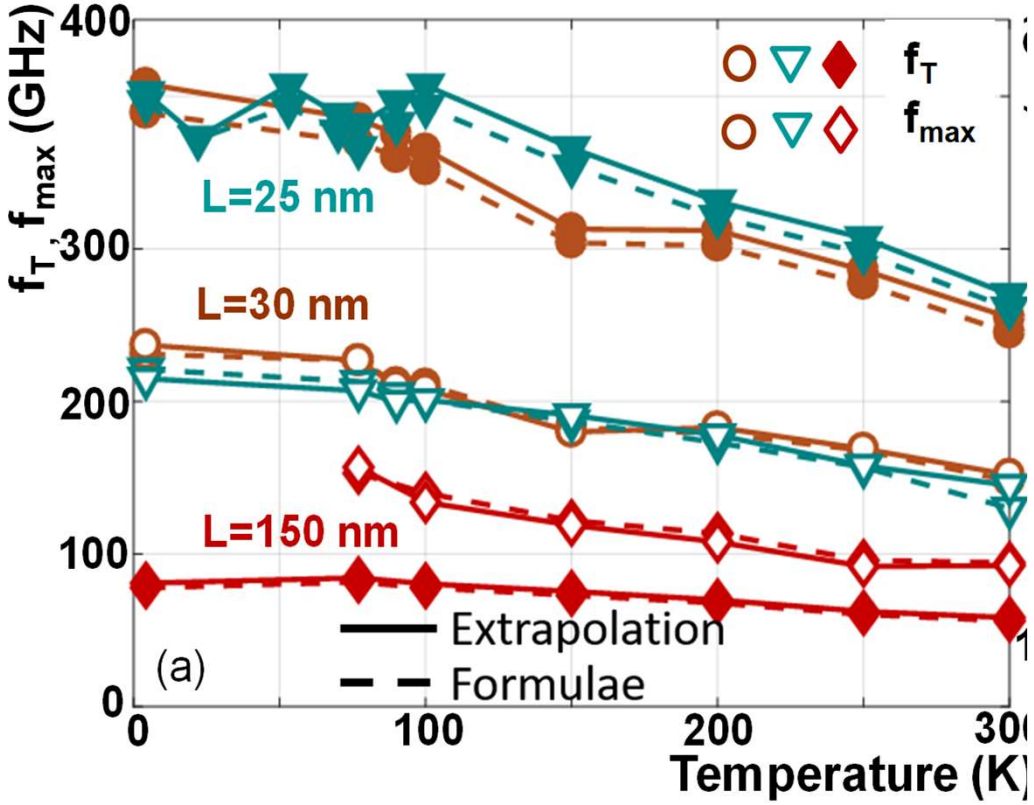


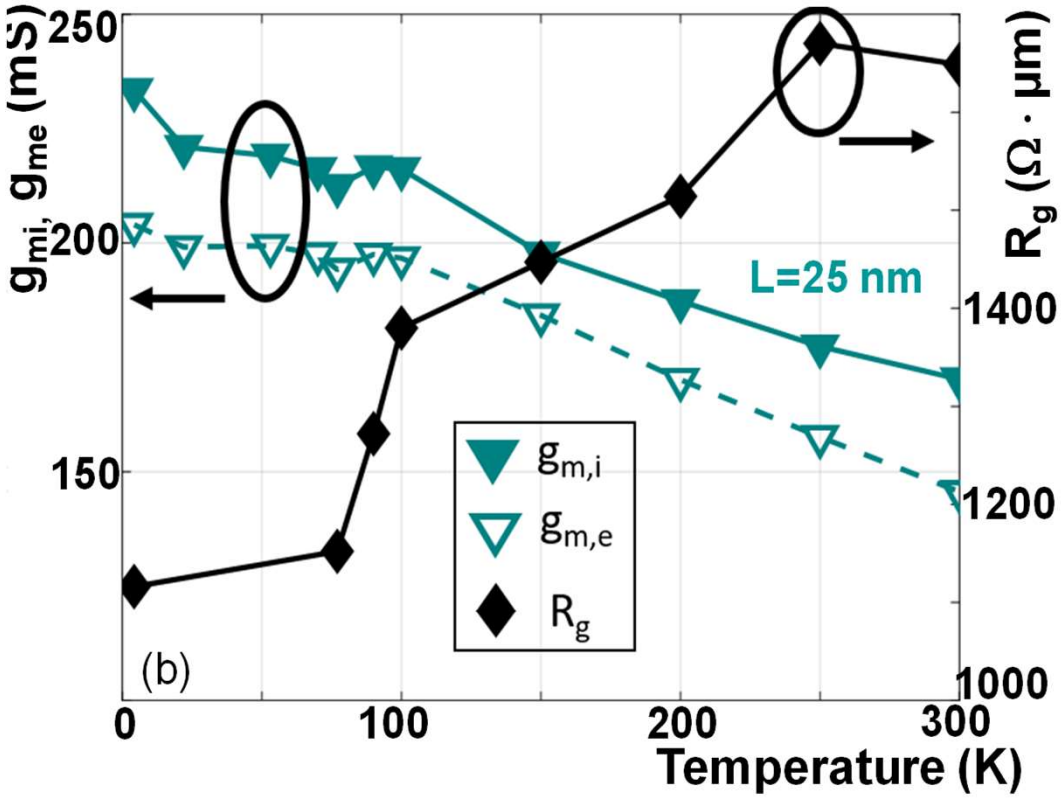
- g_m: about 10% increased
- C_{gg} : ~20% reduced
- ***f_T ~ 360GHz fits ITRS requirements***

RF Methodology

Examples

28FDSOI at cryo



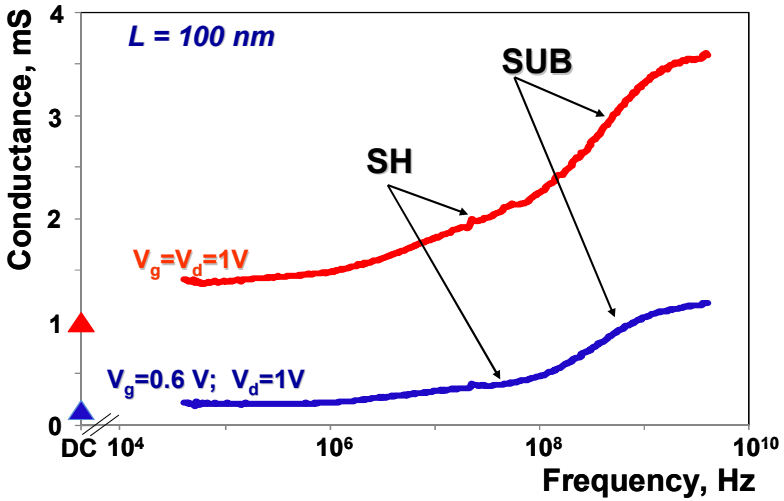


B. Kazemi Esfeh, IEEE JEDS 2019
L. Nyssens et al, IEEE JEDS 2020

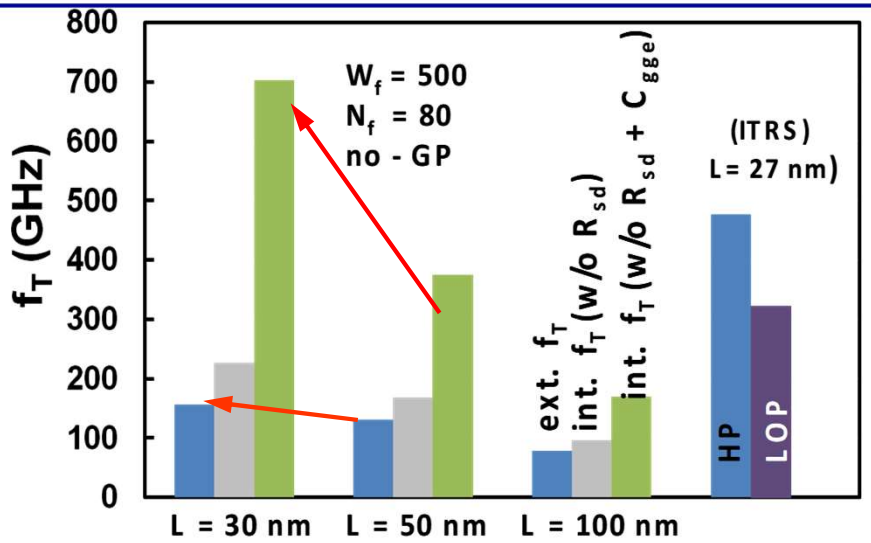
- **130 GHz increase of f_T and 75 GHz of f_{max}** for the shortest device (**30% increase**)
- Due to g_m increase (~40%) (related to μ) and Rg reduction (for f_{max})
- C_{gg} and R_{sd} are almost constant vs T

Conclusions

Take away



❑ Performance prediction based exclusively on DC data may be inaccurate (device benchmarking may be misleading)

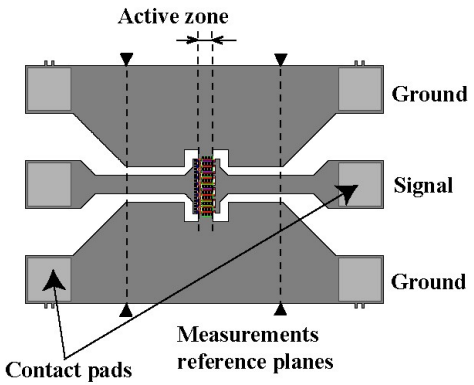


❑ Impact of parasitics on device FoM enormously increases with L↓

⟹ appropriate techniques allow for fair benchmarking linked to the device physics and operation conditions

⟹ wide-band analysis is required for the fair FoM assessment

⟹ separation of "intrinsic" and "extrinsic" elements related performance is mandatory



⟹ adequate structures (with RF access pads) to be included in the layout from the very beginning of the technology development

ACKNOWLEDGEMENTS

Many PhD students and colleagues M.K.Md. Arshad, D. Lederer, P. Simon, G. Pailloncy, D. Levaque, T. Rudenko, J. Alvarado, S. Burignat and many others actively participated in the characterization/simulation work as well as gathering and analyzing the results

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Research projects ….

Reaching 22

WELCOME Characterization Platform (ELEN/ICTEAM/UCL):