High-Resistivity Substrates with PN Interface Passivation in 22 nm FD-SOI

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***Abstract*—In this paper, GlobalFoundries' 22 nm FD-SOI process was run on standard and high-resistivity wafers evaluating a PN junction interface passivation solution to counter parasitic surface conduction (PSC) effects. Substrate quality was monitored in terms of losses, effective resistivity (ρ_{eff}) and generated harmonics through on-wafer measurements of coplanar waveguides (CPW), fabricated in either bottom metal or in top metal layers. The PN patterns demonstrate effective passivation of the PSC, enabling ρ_{eff} values in the kΩcm range. Patterns with bias contacts were fabricated, demonstrating substantial increase in ρ_{eff} when applying a reverse bias to widen the depletion regions. PN grid patterns also exhibit good RF performance results, and are attractive since they alleviate layout/PN pattern co-design.**

I. Introduction

Nowadays, advanced CMOS nodes are competitive for radio-frequency (RF) and mm-wave applications. In particular, FD-SOI devices boast f_t and f_{max} metrics in the range of 300 to 400 GHz [1], and support rich back-end-of-line options with up to 11 metal layers, including several thick layers supporting high-Q RF/mm-wave passives and interconnects.

The silicon substrate is part of the electromagnetic environment of such passives and devices, and can be responsible for significant amounts of losses, coupling and non-linear signal distortion [2] if the silicon resistivity is low.

Using high-resistivity (HR) silicon substrates (with nominal resistivity ρ_{nom} > 1 kΩcm) rather than standard doped silicon (ρ_{nom} = 10 to 20 Ωcm) brings an improvement to these effects, though the benefits are hindered by the *parasitic surface conduction* (PSC) effect. A PSC layer is induced by fixed positive charges at the Si/SiO_2 interface that attract significant amounts of free electrons, forming a thin channel-like layer that is highly conductive [3, 4]. PSC then degrades (lowers) the *effective resistivity* (ρ_{eff}) sensed by coplanar circuitry overlying the Si-substrate stack. For these reasons the ρ_{eff} of HR substrates is typically in the range of 30 to 150 Ωcm.

Interface passivation solutions have then been developed to counter the PSC layer, the most widespread of which is the *trap-rich* solution, that introduces a thin layer of polysilicon in between the SiO_2 and Si, that is rich in defects that trap free carriers and render the interface resistive [4]. Trap-rich SOI has seen strong industrial success in PD-SOI nodes. However, FD-SOI support below-BOX features (back-gate contacts, isolations wells, diodes, etc.) that are difficult to integrate within defect-rich poly-Si. Such compatibility issues motivate the development of alternative interface passivation schemes.

The *PN interface passivation* technique is then particularly of interest for FD-SOI. By utilizing alternating regions of P- and N-type doping, the conductive interface is interrupted locally by induced depletion junctions, whose chain-series combination results in a strong increase in overall substrate impedance (ρ_{eff}). This passivation scheme was first described in [5,6], though in those works the lithography resolution was limited by the university laboratory equipment to 1 µm. Still, the ρ_{eff} of measured CPW lines was shown to be increased from a few tens of Ωcm on a HR substrate (with PSC) to around 1 kΩcm when adding the PN passivation arrangement that induced an interface depletion junction density of 5% using that lithography. Those previous works describe that having the ability to pack a higher density of depletion junctions in series beneath the RF passive will further improve RF performance. This was tested in a short-loop process in [7].

In this paper, the PN interface passivation solution is applied within GlobalFoundries' 22FDX® line run on both the standard 10 Ωcm Si as well as on a split run using HR 985 Ωcm wafers provided by Soitec. Up to approximately 30% interfacial depletion junction density is achieved, enabled by the advanced lithography for below-BOX implants in the 22FDX® platform. On-wafer RF measurements of CPW test structures demonstrate strong increase in substrate ρ_{eff} lower substrate loss and reduced non-linearities.

II. Fabricated Structures

Two types of PN passivation patterns were designed below two types of CPW lines, drawn in different levels of the technology's back-end-of-line.

A. CPW Line Geometries

The first CPW structure is implemented in the last Cu layer "QB" (3 µm thick and approximately 10 µm from the Si substrate) and has a signal line width W of 35 µm, and a signal to ground spacing S of 25 µm. The second CPW structure is formed in stacked M1 and M2 (combined thickness of 0.17 µm, and approximately 130 nm from the Si substrate) using W=20 µm and S=20 µm. Lines of multiple lengths (760 µm and 2000 µm) were fabricated, along with dedicated Open and Thru structures, to enable a wideband mTRL calibration and extraction of the line's equivalent RLGC parameters [8].

B. PN Interface Passivation Pattern Geometries

Two types of PN passivation patterns are considered in this paper: (i) *PN-lines* and (ii) *PN-grid*. They are both represented in Figure 1, and serve to increase the impedance between the S and G lines of the CPW by impeding the E-field path between these with multiple highly-resistive depletion regions. The *PN-lines* pattern includes a DC biasing option through on-chip high-valued resistor elements. This allows for the reverse DC biasing of the PN junctions, to widen the depletion regions and further increase substrate impedance. Small sizings were used to define both patterns in compliance with the process design rules (Figure 1).

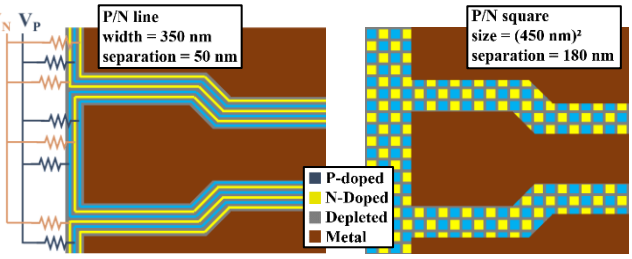

Fig. 1. Representation of the fabricated PN patterns below a CPW.

III. RF Performance Results

The CPW lines are measured under small- and large-signal conditions on-wafer using a pair of GSG probes (Infinity probes from FormFactor). From the S-parameter data, the line loss (α) and effective resistivity and permittivity parameters of the underlying material are extracted according to [8]. Single-tone large-signal measurements were performed by sweeping the power of a 900 MHz (f_0) input signal and analyzing the spectral contents at the output of a 2 mm CPW line. The substrate non-linearity induces signal distortion, and this is benchmarked using the harmonic output components H2 (at $2f_0$ of 1.8 GHz) and H3 (at $3f_0$ of 2.7 GHz) plotted relative to the H1 fundamental power.

A. CPW Performance in a Bottom Metal Layer

The RF performance results obtained from measured CPW lines in the stacked M1 and M2 layers are shown in Figure 2.

Moving from the standard resistivity substrate to the HR substrate demonstrates a 2.2 dB reduction in lineic loss at 5 GHz, justified by the increase of ρ_{eff} from 10 Ωcm to 70 Ωcm, along with a 30 to 40 dB reduction in substrate-induced second harmonic level.

These RF metrics are further improved when including the PN interface passivation solution, as the effective resistivity increases to 600 Ωcm at 5 GHz when the *PN-line* passivation is present without any applied junction voltage. When applying a 3 V reverse PN bias, ρ_{eff}(5 GHz) increases further to 2.2 kΩcm, and the H2 distortion level is 20 dB below the HR without passivation.

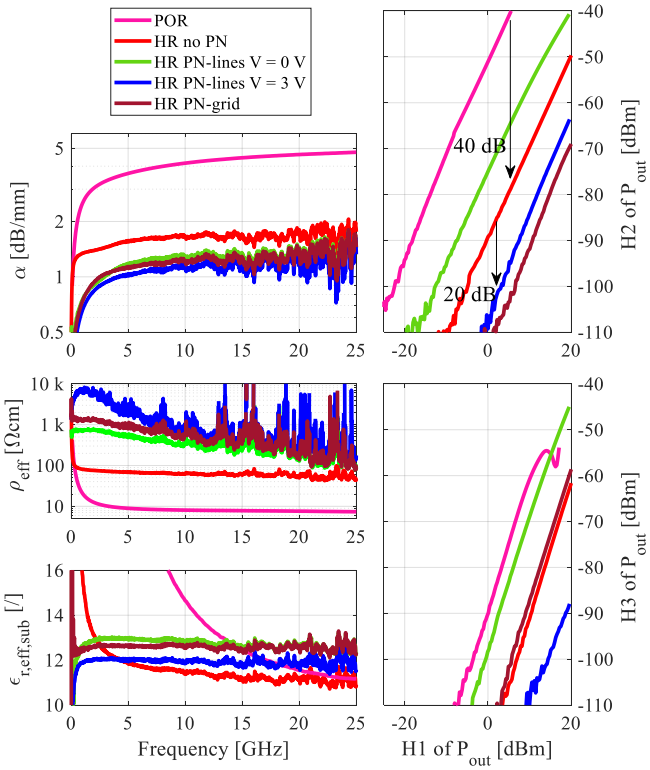

Fig. 2. RF substrate FoMs measured from M1M2 CPW lines. Small-signal data (α, ρ_{eff}, $\varepsilon_{r,eff,sub}$) extracted from mTRL of mumtiple CPWs. Large-signal data (H1, H2, H3) measured at 900 MHz fundamental on a 2 mm-long CPW.

The *PN-grid* passivation provides an effective resistivity value of 900 Ωcm at 5 GHz, and a similarly low H2 level. At f_0 of 900 MHz, these linearity results (-74 dBm) are close to those of a 2 mm-long line on trap-rich eSI70™ substrates [4].

All RF FoM data is recapped in Table I.

TABLE I. RF FoMs of CPW Lines on Different Substrate Options

CPW metal and substrate options		*α(5 GHz) [dB/mm]*	*ρ_{eff}(5 GHz) [Ωcm]*	*H2 at H1=15 dBm, (f_0 = 900 MHz) [dBm]*
M1M2	POR	3.7	10	-27
	HR	1.5	70	-59
	HR PN-lines 0 V	1.3	600	-48
	HR PN-lines 3 V	1.0	2200	-70
	HR PN-grid	1.2	900	-74
QB	POR	0.21	150	/
	HR	0.16	300	/
	HR PN-lines 0 V	0.06	1900	/
	HR PN-lines 3 V	0.05	4200	/

B. CPW Performance in a Top Metal Layer

Similar benchmarking was performed on CPWs implemented in the QB metal layer (*PN-grid* below QB-lines not implemented), and the results are given in Table I.

IV. Conclusion

In this paper, the PN passivation solution of HR interfaces has been integrated into an advanced industrial design flow, the 22FDX® node from GlobalFoundries.

Strong improvements in substrate-induced losses and non-linearities have been observed, with ρ_{eff} metrics above 1 kΩcm being achieved below 20 GHz (9 GHz) for CPW lines implemented in the QB (M1M2) layer. With PN passivation, RF performance roll-off over frequency is expected [5,6], though simulations [9] predict that a ρ_{eff} higher than 1 kΩcm is achievable up to 40 GHz by optimizing the P and N implant energies and doses and by using higher resistivity Si.

The idea of reverse biasing the PN junctions to increase the depletion region width and the substrate impedance was demonstrated to have the desired effect, enabling an increase of a factor 2x to 4x in ρ_{eff} by applying a 3 V bias, to attain ρ_{eff} values in the kΩcm-range.

The concept of a PN grid array was also demonstrated to function well. Though this solution does not achieve the best in-class RF results presented in this paper, they remain of decent quality, and, this PN pattern has the advantage of not requiring a co-design with the EM passive's layout, but can be patterned as a regular array beneath it, lightening the designer's work load and layout constraints.

Overall, the PN passivation offers quality RF substrate FoMs, and its compatibility with FD-SOI is validated.

Acknowledgment

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