Analysis, Modeling, and Design of a 2.45-GHz RF Energy Harvester for SWIPT IoT Smart Sensors

Pengcheng Xu, *Student Member, IEEE*, Denis Flandre, *Senior Member, IEEE*,
and David Bol, *Senior Member, IEEE*

***Abstract*—Simultaneous wireless information and power transfer (SWIPT) is a flexible and cheap way to supply Internet-of-Things (IoT) smart sensors avoiding battery replacement. In this paper, we analyze, model, and design a 2.45-GHz RF energy harvesting (RFEH) system based on a discrete-component matching network (MN), a custom 65-nm CMOS cross-coupled rectifier, and an off-the-shelf storage-charging power management unit (PMU), which regulates the rectifier output voltage with maximum power point tracking (MPPT). We propose a reverse global analysis to model the RFEH. It allows an accurate prediction of the power harvesting efficiency (PHE) to directly size the MN and select the RFEH MPPT regulation ratio, at different incident RF power levels. We perform parasitic-aware RFEH design to take advantage of printed circuit board (PCB)/package capacitive parasitics at the rectifier input for optimizing the π-MN with the help of the proposed RFEH modeling results. We show that this parasitic capacitance introduces a maximum bound on the real impedance at the rectifier input to ensure good impedance matching in practice. MPPT is used to help reach this target real impedance at given incident RF power, as the rectifier equivalent input impedance is a function of both its input and output voltages. Measurement results show a sensitivity as low as −17.1 dBm with a peak PHE of 48.3% at −3-dBm incident RF power. Global modeling, simulation, and measurement results demonstrate that the PHE is limited by PCB/package parasitic capacitance and that PCB/packaging technology improvement to reduce parasitic capacitance by 150 fF could boost the PHE up to 45% for a low incident RF power level of −10 dBm.**

***Index Terms*—Cross-coupled rectifier, impedance matching, maximum power point tracking (MPPT), power harvester efficiency (PHE), RF energy harvesting (RFEH), simultaneous wireless information and power transfer (SWIPT).**

I. Introduction

WIRELESS power transfer (WPT) is a flexible way to supply Internet-of-Things (IoT) smart sensors without battery replacement. This is usually done with sub-gigahertz WPT using a specific power transmitter added to the building infrastructure. As mainstream short-range low-power (LP) communications like WiFi or Bluetooth low-energy (BLE) uses 2.45-GHz band, sub-gigahertz WPT also requires a second specific antenna on the smart sensor for receiving the RF power. Therefore, WPT at 2.45 GHz is an interesting alternative for more compact and cheaper smart sensors. Going one step further, re-using BLE/WiFi infrastructure enables simultaneous wireless information and power transfer (SWIPT). As an example, such a 2.45-GHz SWIPT occupancy-detection smart sensor with RF energy harvesting (RFEH) system is demonstrated in [1] and [2].

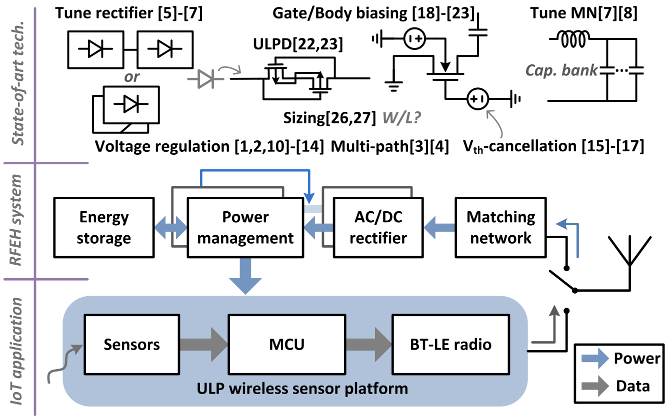

Fig. 1. SWIPT IoT smart sensor system and RFEH state-of-the-art techniques.

Fig. 1 shows the concept of RF-supplied IoT smart sensor for SWIPT. A single antenna would be used with an RF switch between BLE communications and RFEH. The RFEH system collects the ac electromagnetic power of the RF wireless link when BLE is mute and converts it into a dc electrical power to supply an ultra-LP (ULP) sensor platform. A typical RFEH system is composed of an impedance matching network (MN), an ac/dc rectifier, a power management unit (PMU), and a rechargeable energy storage (lithium-ion battery or supercapacitor). The MN matches the rectifier input impedance to the antenna impedance, typically 50 or 75 Ω, to avoid reflecting incident RF power. After ac/dc conversion by the rectifier, the PMU generates a stable voltage to supply the ULP platform regardless of the variable incident RF power while managing the storage element.

Because of strong path loss and limited maximum RF power emission due to regulations for human health problem, the system incident RF power is limited in a range from −25 to 0 dBm [1], [2]. Therefore, it is a key challenge for the SWIPT system to achieve good harvesting efficiency over this wide incident power range. As depicted in the upper part of Fig. 1, solutions in the literature include dual/multi-path

---

Manuscript received January 15, 2019; revised April 4, 2019; accepted April 21, 2019. This paper was approved by Guest Editor Hong-June Park. This work was supported by the Brussels Institute for Research and Innovation (INNOVIRIS) through the COPINE-IoT Project. *(Corresponding author: Pengcheng Xu.)*

The authors are with the Department of Electrical Engineering, ICTEAM Institute, Université catholique de Louvain (UCLouvain), 1348 Louvain-la-Neuve, Belgium (e-mail: pengcheng.xu@uclouvain.be; denis.flandre@uclouvain.be; david.bol@uclouvain.be).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JSSC.2019.2914581

rectifiers, which consist of a LP path using low-V_{th} transistors for high efficiency at low RF power and a high-power path using high-V_{th} transistors for high efficiency at high input power [3], [4]. Another solution is reconfigurable rectifiers based on multiple identical primary rectifying units connected in series or parallel depending on the input RF power level [5]–[7]. In order to compensate rectifier equivalent input impedance variation with input RF power, a tunable MN based on a capacitor bank was implemented in [7] and [8]. Similar to the photovoltaic (PV) energy harvesting system [9], maximum power point tracking (MPPT) is also introduced in [1], [2], and [10]–[14] to regulate rectifier output voltage for improving harvester performance. To decrease the rectifier forward ON-resistance and limit reverse leakage current, self-V_{th}-cancellation/compensation [15]–[17], gate/body biasing [18]–[23], and ULP diode (ULPD) [24], [25] were implemented in the rectifier circuit design. The rectifier transistor threshold voltage and sizes are optimized in [26] and [27] with gradient method sizing methodology to maximize the rectifier power conversion efficiency (PCE).

However, in several previously proposed solutions, the configuration switches introduce power losses due to their series resistance. Large switches can be selected for low series resistance. However, as we will study in this paper, any parasitic capacitance added (e.g., by these switches) at the rectifier input becomes critical for the MN design at 2.45 GHz. Consequently, a rectifier independently optimized for good PCE cannot guarantee a better power harvester efficiency (PHE) in the RFEH system due to impedance mismatch problem and power loss in the MN. In this paper extended from [10], we fully study the design of an RFEH system at 2.45 GHz without reconfiguration switches. We analyze and demonstrate the impact of the parasitic capacitance at the rectifier input and validate the interest of rectifier output voltage regulation with MPPT. On the strength of the proposed RFEH global modeling, we optimize a π-MN by using the parasitic capacitance as a contribution to implement the capacitor of the π-MN. The block schematic analysis, RFEH system global modeling, and parasitic-aware design measurement results are in excellent agreement. The proposed RFEH system is introduced in Section II with the analysis of the characteristics of cross-coupled rectifier operated at its MPPT and of the π-MN design. In Section III, we perform RFEH system modeling based on reverse global analysis to size the MN, accurately predict the PHE, and select the MPPT regulation ratio at different incident RF power levels, and the Appendix provides RFEH modeling mathematical derivation in detail. The parasitic-aware design and measurement of the proposed RFEH prototype are described and compared with the state of the art in Section IV.

II. RFEH SYSTEM AND SCHEMATIC ANALYSIS

A. Proposed RFEH System

The proposed 2.45-GHz RFEH system is depicted in Fig. 2. It is built around a custom cross-coupled rectifier designed in 65-nm CMOS. The rectifier architecture allows dynamic self-V_{th} cancellation but as its input is differential, it requires the addition of a Balun to the single-ended antenna. The MN is based on the π topology to help cancel the rectifier parasitic input capacitance coming from printed circuit board (PCB) and chip package, as presented in Sections II-C and IV-A. The rectifier output voltage is regulated by the storage-charging path inside the PMU, which performs MPPT to preserve good PCE in the rectifier and limits its equivalent input impedance variation over the incident RF power range as will be explained in Section II-B. The PMU we will use is able to regulate the rectifier output voltage to a specific MPPT ratio γ_{MPPT} at 50%, 70%, or 85% of its open-circuit voltage. It also boosts the rectifier output voltage to charge the storage element.

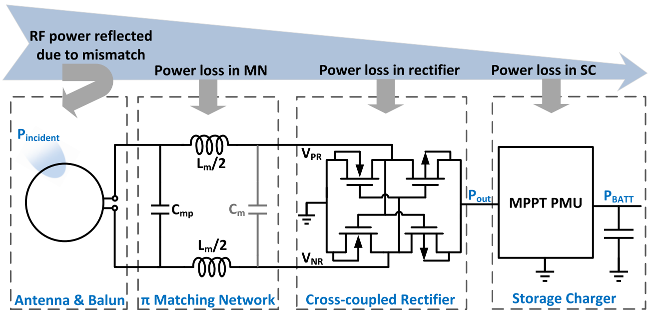

Fig. 2. Proposed RFEH system and its power loss classification. The MN element C_{m} in gray comes from the parasitic capacitors of both the chip package and the PCB. L_{m} and C_{mp} are parasitic-aware sized for impedance matching.

There are four main sources of RF power losses in the RFEH system: RF power reflected back over the air due to impedance mismatch, power loss in the matching network, power loss in the rectifier, and power loss in the PMU. The PHE of RFEH system is the ratio between the extracted dc output power P_{out} delivered to the load (here in Fig. 2 we consider the PMU as the load) and the RF incident electromagnetic power on the receiver antenna, which would be collected with a perfect impedance match, P_{incident} in short. As the similar RFEH performance metrics in [1], [2], and [12], PHE can be expressed as

$$\text{PHE} = P_{\text{out}}/P_{\text{incident}} = \text{PEE}_{\text{MN}} \times \text{PCE}_{\text{MN}} \times \text{PCE}_{\text{rec}} \quad (1)$$

where PEE_{MN}, PCE_{MN}, and PCE_{rec} are the MN power extraction efficiency $[=(P_{\text{incident}} - P_{\text{reflected}})/P_{\text{incident}}]$, MN PCE $[=P_{\text{in.rec}}/(P_{\text{incident}}-P_{\text{reflected}})]$, and rectifier PCE $(=P_{\text{out}}/P_{\text{in.rec}})$, respectively. They correspond to the first three of four main power losses sources as illustrated in Fig. 2. In the proposed RFEH system, we use an off-the-shelf storage-charging PMU (AEM30940 from e-peas). Therefore, we consider this PMU as the rectifier load without taking its efficiency into account, namely, the power loss in the storage charger (SC) shown in Fig. 2. This definition is fair with respect to RFEH performances comparison in Table I.

Because of the wide RF path loss range, preserving good PHE over the resulting incident RF power range is a challenge [1], [2]. Let us mention that the PCE metric defined as $\text{PCE} = P_{\text{out}}/P_{\text{absorbed}} = P_{\text{out}}/(P_{\text{incident}} - P_{\text{reflected}})$ in [28] and [29] is a limited metric for RFEH systems as it neglects

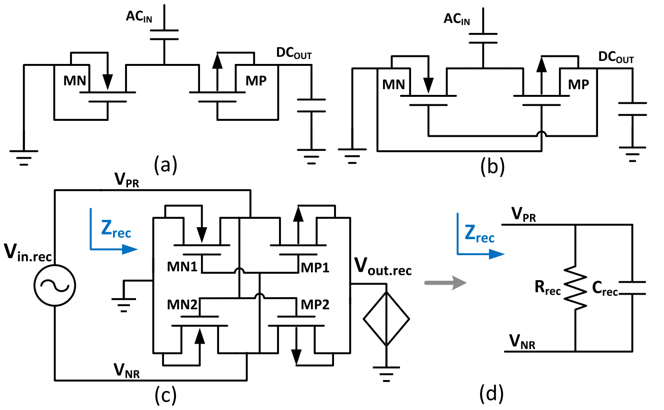

Fig. 3. Rectifier schematic. (a) Conventional Greinacher rectifier. (b) Static self-V_{th}-cancellation Greinacher rectifier. (c) Dynamic self-V_{th}-cancellation cross-coupled rectifier. (d) Rectifier equivalent input impedance model. The MPPT regulation effect on rectifier output voltage is treated as a voltage controlled voltage source. $V_{\text{out.rec}} = \gamma_{\text{MPPT.rec}} \times V_{\text{out.rec.OC}}$. Here, $V_{\text{out.rec.OC}}$ is the rectifier output voltage at open circuit.

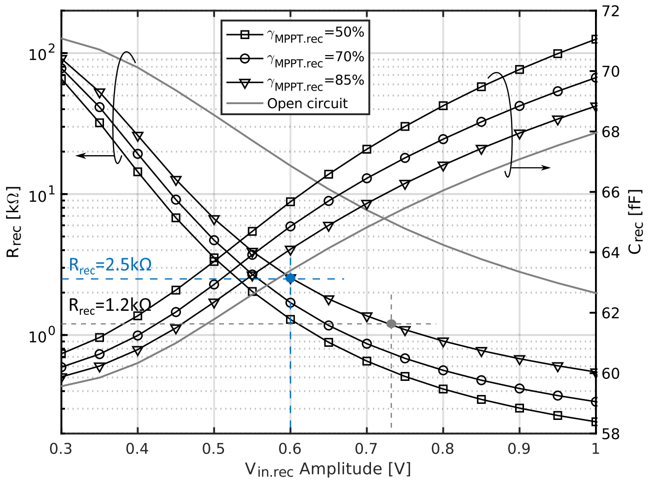

Fig. 4. Cross-coupled rectifier equivalent input impedance depending on rectifier input voltage with given MPPT regulation ratio at 2.45 GHz. The one-stage rectifier is four internal cross-coupled rectifier units in parallel with sizes nMOS 5 μm/60 nm and pMOS 10 μm/60 nm.

the reflected power due to impedance mismatch that can vary a lot with the incident RF power range. A high PCE is thus a required condition but not a sufficient condition for high performance of RFEH systems. This is why we use the PHE definition depicted in (1) as the RFEH performance metric in this paper.

B. Cross-Coupled Rectifier

The proposed RFEH uses a custom rectifier design in 65-nm LP CMOS with low-V_{th} (LVT) transistors. It is based on the dynamic self-V_{th}-cancellation cross-coupled topology [15], [16], which achieves a higher rectifier PCE than the conventional Greinacher rectifier in Fig. 3(a), especially at low input power conditions. In this differential scheme, as shown in Fig. 3(c), the gates of transistors are actively biased by dynamic differential-mode signals. On the one hand, when V_{PR} is negative, it corresponds to the forward bias condition for the MN1 diode, because the gate voltage of MN1, which is V_{NR}, is positively biased and effectively decreases the turn-on voltage of MN1, resulting in a small ON-resistance. On the other hand, when V_{PR} becomes positive, which corresponds to the reverse bias condition, the gate voltage rapidly decreases, which effectively reduces MN1 reverse leakage current. This is better than the static-V_{th}-cancellation Greinacher rectifier as depicted in Fig. 3(b), which increases reverse leakage current due to low V_{th}.

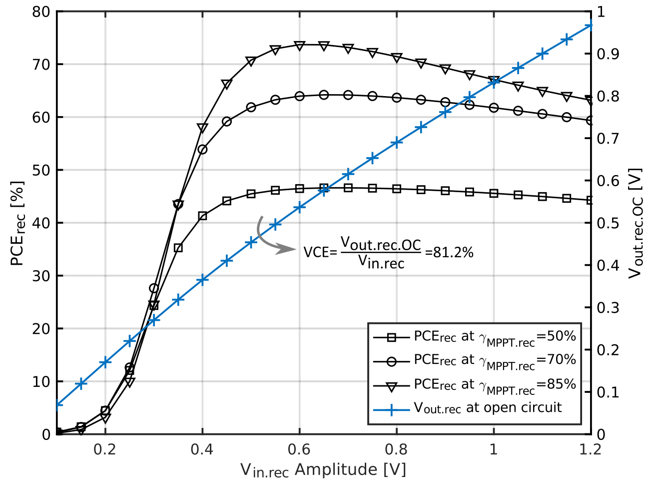

Fig. 5. Cross-coupled rectifier PCE and rectifier output voltage at open circuit depending on the rectifier input voltage.

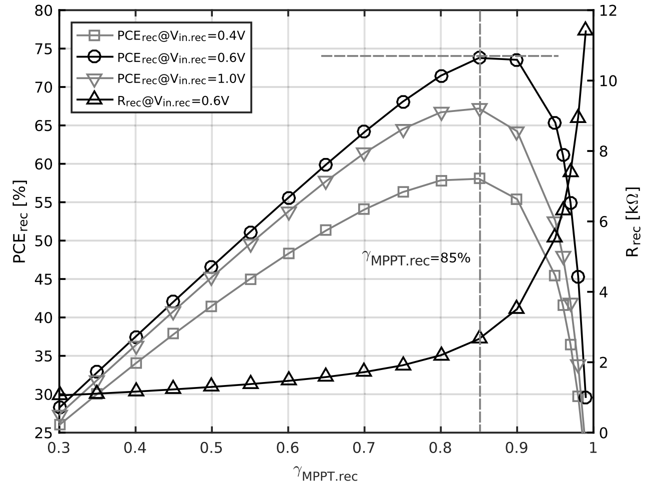

Fig. 6. Cross-coupled rectifier PCE and equivalent input resistance depending on the rectifier MPPT regulation ratio. For each $V_{\text{in.rec}}$, the optimum $\gamma_{\text{MPPT.rec}}$ for PCE_{rec} is around 85%.

As shown in Fig. 3(d), the rectifier equivalent input impedance Z_{rec} can be modeled as a resistor R_{rec} and capacitor C_{rec} in parallel for representing its real and imaginary parts. For a given sizing of the rectifier, Z_{rec} is a function of the rectifier input $V_{\text{rec.in}}$ and output $V_{\text{out.rec}}$ at given operational frequency (here, $f_0 = 2.45$ GHz). It can be expressed as

$$\begin{aligned} Z_{\text{rec}} &= \left.\frac{V_{\text{in.rec}}(\omega)}{I_{\text{in.rec}}(\omega)}\right|_{\omega=2\pi f_0} \\ &= R_{\text{rec}} || C_{\text{rec}} = f(V_{\text{in.rec}}, V_{\text{out.rec}}). \end{aligned} \tag{2}$$

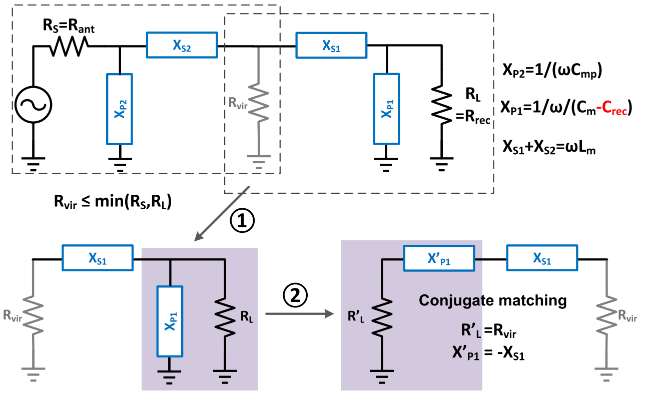

Fig. 7. Sizing π-MN elements. Step 1: divide π-MN into two L-MNs with a virtual resistor R_{vir} which is not real in the practical circuit. Step 2: convert X_{P1} and R_{rec} in parallel into X'_{P1} and R'_{rec} in series for conjugate matching. Then repeat Step 2 for right L-MN. At last, C_{rec} should be detracted from X_{P1} elements.

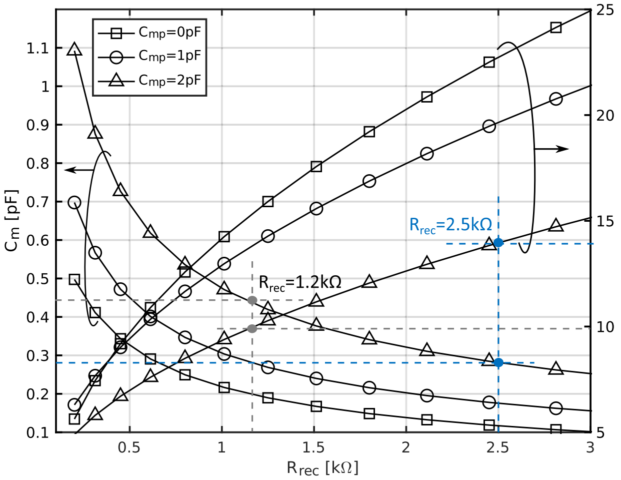

Fig. 8. Sizing results of the π-MN depending on R_{rec} at 2.45 GHz with 50-Ω antenna impedance (blue dashed line with $C_{\text{m}} = 0.29$ pF and gray dashed line with $C_{\text{m}} = 0.45$ pF). C_{rec} is taken into consideration as expressed in (7).

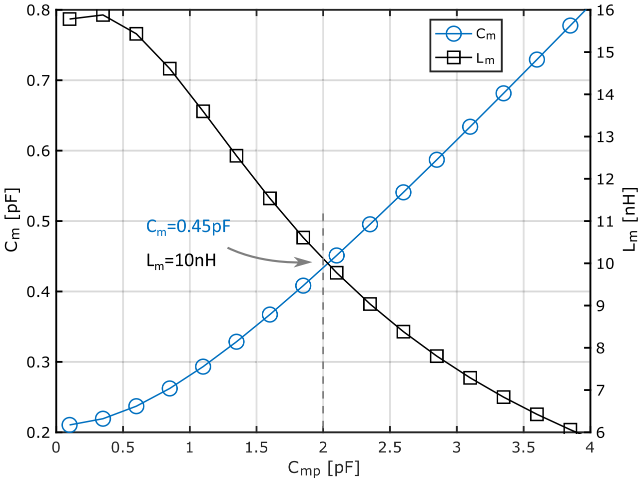

Fig. 9. π-MN sizing results depending on C_{mp} for $R_{\text{rec}} = 1.2$ kΩ and $C_{\text{rec}} = 65$ fF.

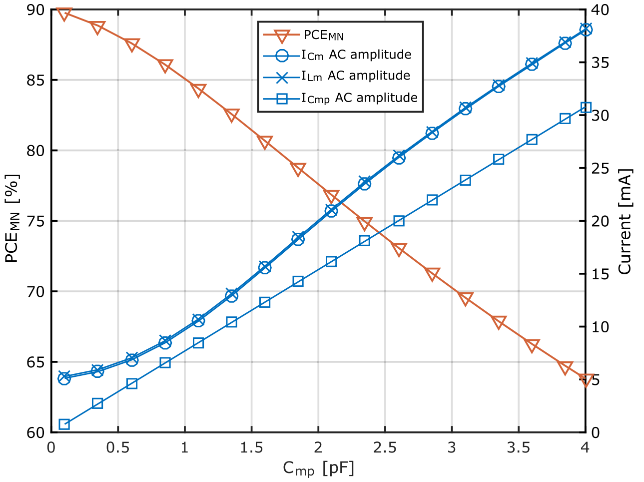

Fig. 10. Matching network elements ac current amplitude and PCE_{MN} depending on C_{mp} with $R_{\text{rec}} = 1.2$ kΩ, $C_{\text{rec}} = 56$ fF, and $V_{\text{in.rec}} = 0.5$ V ac amplitude (in fact, $\text{PCE}_{\text{MN}} = f(Z_{\text{MN}}, Z_{\text{rec}})$ is not relevant with the input voltage as expressed in (11) of Section III assuming both Z_{MN} and Z_{rec} are independent of $V_{\text{in.rec}}$). The element quality factors of L_{m}, C_{m}, and C_{mp} are correspondingly equal to 35, 200, and 200.

In Fig. 4, the post-layout simulations show that the rectifier input resistance R_{rec} increases greatly at low $V_{\text{rec.in}}$ as transistors enter the near-/sub-threshold region. For example, at 0.3 V corresponding to a −30-dBm incident RF power with an ideal MN and 50-Ω antenna impedance, R_{rec} is higher than 100 kΩ. At 0.75 V corresponding to an incident RF power of 0 dBm, R_{rec} is below 1 Ω. This illustrates the challenge of MN sizing and design for a wide incident RF power range. However, its capacitance C_{rec} remains around 65 fF as it is dominated by the bias-independent access and fringing capacitance of the transistor, while the bias-dependent gate-to-channel part is minimized, especially when the MOSFETs are driven in weak inversion at part of time even with high $V_{\text{in.rec}}$ ac amplitude. Fig. 5 shows the excellent PCE_{rec} performance of this cross-coupled rectifier. Thanks to its dynamic self-V_{th}-cancellation ability, the PCE_{rec} is above 50% at 0.4-V $V_{\text{in.rec}}$ ac amplitude. At open circuit, rectifier voltage conversion efficiency (VCE) is around 81.2%. Since rectifier equivalent input impedance is a function of its input and output voltages as shown in (2), rectifier performance is linked with its MPPT regulation ratio [13]. As depicted in Fig. 6, the best PCE_{rec} is achieved at $\gamma_{\text{MPPT.rec}} = 85\%$. However, a higher MPPT regulation ratio also increases R_{rec}, which will impact the impedance matching as we will discuss in Section II-C.

C. π *Matching Network*

To extract the maximum power from an RF source, the load impedance must be equal to the complex conjugate (i.e., identical real impedance with opposite reactance) of the source impedance. The antenna equivalent impedance R_{ant} is 50 Ω for the 1/4-wavelength printed monopole antenna in this design. In two-elements L-MN, the circuit quality factor is fixed when the source and load impedances are determined. In contrast, π-MN with three elements (L_{m}, C_{m}, and C_{mp}) as illustrated in Fig. 2 can be used for narrowband high-Q application [30].

As represented in Step 1 of Fig. 7, π-MN can be separated into two L networks with a virtual resistor R_{vir} whose resistance must be smaller than both the antenna impedance R_{S} and the load resistor R_{L} (here R_{L} is the equivalent input resistance R_{rec} of the rectifier operated at its MPPT) for sizing π-MN parameters.

C_{mp}, L_{m}, and C_{m} in π-MN are sized from a selected R_{vir} in [30]. However, here we prefer to decide C_{mp} first since it is a real component in π-MN and has effect on L_{m}, C_{m}, and PCE_{MN} as shown in Figs. 8–10. By reversing derivation from [30], the virtual resistor R_{vir} can be expressed in terms of C_{mp} as

$$R_{\text{vir}} = R_{\text{ant}}/[1 + (\omega R_{\text{ant}} C_{\text{mp}})^2]. \tag{3}$$

On the strength of (3), we update π-MN sizing based on selected R_{vir} to C_{mp}. The separated left and right L-MN circuits quality factors are, respectively, equal to

$$Q_L = \sqrt{(R_{\text{ant}}/R_{\text{vir}} - 1)} \tag{4}$$

$$Q_R = \sqrt{(R_{\text{rec}}/R_{\text{vir}} - 1)}. \tag{5}$$

As represented in Step 2 of Fig. 7 for parallel-to-series impedance transformation, it gives two independent equations for conjugate matching. Therefore, L_{m} and C_{m} can be, respectively, derived as

$$L_m = R_{\text{vir}}(Q_L + Q_R)/\omega \tag{6}$$

$$C_m = Q_R/(\omega R_{\text{rec}}) - C_{\text{rec}} \tag{7}$$

where $\omega = 2\pi f_0$. As expressed in (7), C_{rec} is taken into consideration at the final step by subtracting it from the primary $C_{\text{m}}(=Q_R/(\omega R_{\text{rec}}))$. Fig. 8 shows the required L_{m} and C_{m} values to achieve a perfect match as a function of the rectifier input resistance R_{rec} and the C_{mp} value. If $C_{\text{mp}} = 0$, the π-MN network is actually an L-MN and the values of its elements L_{m} and C_{m} follow the L-MN sizes. Let us mention again that R_{rec} varies with the incident RF power. This comes from the varying voltage ac amplitude at the rectifier input combined with the highly non-linear characteristics of the transistors at low gate voltage, as discussed in Section II-B. The sum of parasitic capacitance C_{pa} from chip package and PCB can contribute to the equivalent C_{m} as will be discussed in Section IV. $(C_{\text{m}} - C_{\text{pa}})$ is the capacitance that should be finally added in practical MN. Therefore, a higher resistance R_{rec} at low $V_{\text{in.rec}}$ requires less C_{m}, as depicted in Fig. 8, and decreases parasitic capacitance margin.

As depicted in Fig. 9, a larger C_{mp} helps to increase the target C_{m} and releases parasitic capacitance margin that contributes to equivalent C_{m}. For matching $R_{\text{rec}} = 1.2$ kΩ and $C_{\text{rec}} = 65$ fF rectifier equivalent input impedance, with $C_{\text{mp}} = 0$, C_{m} is only around 0.2 pF. It increases to 0.45 pF when $C_{\text{mp}} = 2$ pF. However, increasing C_{mp} to improve the parasitic capacitance margin is not a free gift. As shown in Fig. 10, it also enhances the ac current amplitude in π-MN and thus decreases PCE_{MN}, because all MN elements have parasitic resistors due to the finite-element quality factor. The power loss in MN is boosted by the square of ac current amplitude. Considering $Q = 35$ for the inductor (L_{m}) and $Q = 200$ for the capacitors (C_{mp} and C_{m}), PCE_{MN} goes down from 90% to 77% with C_{mp} increasing from 0 to 2 pF. This will also be verified by the modeling RFEH in Section III-B. Fig. 10 shows that L_{m} and C_{m} flow almost the same amount of ac current. This is because, as illustrated in Fig. 11, the current going through L_{m} is the sum of currents going through C_{m} and Z_{rec}. Since the impedance magnitude of L_{m} (ωL_m) is much less than the magnitude of Z_{rec}, L_{m} and C_{m} flow almost the same amount of ac current.

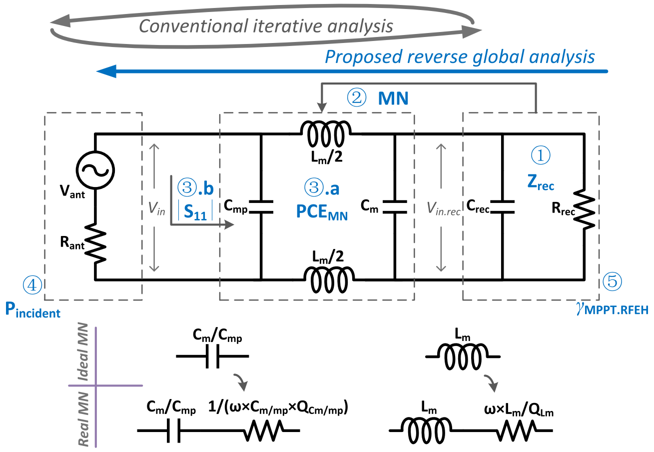

Fig. 11. Proposed RFEH system modeling on strength of reverse global analysis with ideal or real MN. Step 1: characterize rectifier as in Section II-B. Step 2: size π-MN parameters as in Section II-C. Step 3: compute power efficiency PCE_{MN} based on (11) and $|S_{11}|$ parameters based on (12). The global PHE is calculated by (1). Step 4: compute corresponding RFEH input incident RF power P_{incident}. Step 5: compute corresponding RFEH output MPPT regulation ratio $\gamma_{\text{MPPT.RFEH}}$.

III. PROPOSED RFEH MODELING METHOD WITH REVERSE GLOBAL ANALYSIS

As discussed in Section II-B, we characterize the rectifier by applying an ac voltage $V_{\text{in.rec}}$ across the rectifier input with MPPT regulation on its output. However, the incident RF power P_{incident} is injected from antenna and thus not directly at rectifier input nodes V_{PR} and V_{NR}, as illustrated in Fig. 2. Due to the nonlinear behavior of the rectifier as depicted in Fig. 4, it is challenging to deal with the interaction between the antenna, MN, rectifier, and MPPT regulator in the RFEH system. The relationship between the rectifier input $V_{\text{in.rec}}$ and the RFEH input P_{incident} is linked with the MN performance (both PEE_{MN} and PCE_{MN}). Different MNs generate different $V_{\text{in.rec}}$ even with the same input P_{incident}. In addition, $\gamma_{\text{MPPT.rec}}$ of the rectifier alone required to generate a given MPPT-regulated output voltage is not the same as $\gamma_{\text{MPPT.RFEH}}$ of the RFEH global system. Indeed, when simulating the rectifier alone, the rectifier input voltage $V_{\text{in.rec}}$ is forced at the fixed value, no matter its output is open circuit or regulated with MPPT. On the other hand, when considering the global RFEH system at fixed P_{incident}, $V_{\text{in.rec}}$ varies with the rectifier output voltages $V_{\text{out.rec}}$ due to the associated change in the impedance match because $V_{\text{out.rec}}$ has effect on rectifier equivalent input impedance Z_{rec} as shown in (2) and Fig. 4. Therefore, even with the same input P_{incident} and MN, different rectifier output conditions cause different $V_{\text{in.rec}}$. Therefore, in the conventional iterative analysis [31], [32], both corresponding incident RF power P_{incident} and output MPPT regulation ratio $\gamma_{\text{MPPT.RFEH}}$ are not known for a given rectifier with $V_{\text{in.rec}}$ and $\gamma_{\text{MPPT.rec}}$. Z_{rec} needs to be iteratively recomputed for the matched rectifier to fine-tune the MN parameters and $\gamma_{\text{MPPT.RFEH}}$. For optimizing MN at different P_{incident} or for MN elements with different qualify factors, the conventional iterative analysis only based on SPICE simulation will be more tedious and approximative.

In this section, we propose an RFEH system modeling method with the reverse global analysis for filling the gap between the rectifier characterized at ($V_{\text{in.rec}}$, $\gamma_{\text{MPPT.rec}}$) and corresponding RFEH with (P_{incident}, $\gamma_{\text{MPPT.RFEH}}$), as illustrated in Fig. 11. In addition, it predicts the optimized MN sizes and efficiency performances (PEE_{MN}, PCE_{MN}, PCE_{rec}, and PHE) at different P_{incident}. In other words, with a single SPICE simulation for rectifier characterization alone, the modeling computes efficiency performances for the whole RFEH system with optimized MNs at different incident RF powers.

A. Modeling With an Ideal Matching Network

With an ideal MN, all elements are assumed to have infinite quality factor (Q), namely, without any parasitic resistors in capacitors and inductors. Therefore, the PCE_{MN} is 100%. The MN extracting RF power $P_{\text{in}} = (V_{\text{in}}/\sqrt{2})^2/\text{real}(Z_{\text{in}})$ is exactly equal to the rectifier input power $P_{\text{in.rec}} = (V_{\text{in.rec}}/\sqrt{2})^2/R_{\text{rec}}$, where Z_{in} is the equivalent input impedance looking from MN V_{in} as depicted in Fig. 11. PEE_{MN} can also be up to 100% if the MN is sized from Z_{rec} as discussed in Section II-C and without mismatch caused by π-MN parasitic resistors, namely, $Z_{\text{in}} = R_{\text{ant}}$. As defined in (1), the global RFEH PHE is finally equal to rectifier PCE_{rec}. Therefore, we have $P_{\text{incident}} = P_{\text{in}} = P_{\text{in.rec}}$. V_{in} and P_{incident} can be, respectively, expressed as

$$V_{\text{in}} = V_{\text{in.rec}}/\sqrt{R_{\text{rec}}/R_{\text{ant}}} \tag{8}$$

$$P_{\text{incident}} = (V_{\text{in.rec}}/\sqrt{2})^2/R_{\text{rec}}. \tag{9}$$

From (8), the MN voltage gain that is defined as the ratio between $V_{\text{in.rec}}$ and V_{in} can be expressed as $\text{Gain}_{\text{MN}} = (R_{\text{rec}}/R_{\text{ant}})^{1/2}$. With (9), we can compute the optimum MN sizes and PHE ($=\text{PCE}_{\text{rec}}$) depending on P_{incident}, which are discussed in Section II and characterized in Step 1 but depending on $V_{\text{in.rec}}$. The expressions for the corresponding $\gamma_{\text{MPPT.RFEH}}$ are the same as derived in Section III-B.

B. Modeling With a Real Matching Network

In practice, as discussed in Section II-C, any inductor and capacitor component has a parasitic resistance. This is illustrated in Fig. 11 with the first-order model that is a pure inductor/capacitor in series with a resistance due to the finite quality factor. They are, respectively, expressed as $R_{\text{Cm}} = 1/(\omega C_{\text{m}} Q_{\text{Cm}})$, $R_{\text{Lm}} = \omega L_{\text{m}}/Q_{\text{Lm}}$, and $R_{\text{Cmp}} = 1/(\omega C_{\text{mp}} Q_{\text{Cmp}})$. There is, therefore, an inevitable power loss in the MN. These parasitic resistances also cause impedance mismatch. There is no possibility to achieve perfect conjugate matching by this single π-MN that is sized will ideal elements as illustrated in Fig. 7. Two or more L-MNs/π-MNs in series could be used to solve this problem. As in a Smith Chart, there are almost always more than one way to reach the center point where the reflection coefficient is zero from a given impedance [33]. For example, an inductor can be added in parallel for canceling parasitic capacitance by resonating instead of by increasing C_{mp} in π-MN as discussed in Section II-C. However, it greatly increases MN sizing complexity and design cost and also increases power loss in the MN. Therefore, this paper focuses on single π-MN sizing and design. In practice, $P_{\text{incident}} \neq P_{\text{in}} \neq P_{\text{in.rec}}$ since both PEE_{MN} and PCE_{MN} are less than 100%. More accurate modeling can be performed in five steps with a global reverse analysis from the rectifier to the incident power as depicted in Fig. 11. In Step 1, the rectifier equivalent input impedance Z_{rec} and PCE_{rec} depending on $V_{\text{in.rec}}$ for a given $\gamma_{\text{MPPT.rec}}$ are extracted, as explained in Section II-B. This is the only step that needs circuit SPICE simulation since the rectifier characteristic is non-linear and strongly dependent on the CMOS technology. All the following steps can be performed by analytical computation with the equations derived in the following. In Step 2, π-MN is sized depending on Z_{rec} as explained in Section II-C.

Once the rectifier equivalent input impedance Z_{rec} and π-MN are defined, the MN voltage gain Gain_{MN}, the MN power conversation efficiency PCE_{MN} in Step 3.a, the reflection coefficient S_{11} magnitude in Step 3.b, and the MN power extraction efficiency PEE_{MN} can be, respectively, expressed as [see the Appendix for the mathematical derivation in detail and (11) is shown at the bottom of this page]

$$\text{Gain}_{\text{MN}} = (1/Z_{\text{in}} - 1/Z_{\text{Cmp}}) \times (Z_{\text{Cm}}||Z_{\text{rec}}) \tag{10}$$

$$|S_{11}|(\text{dB}) = 20 \times log_{10}|(Z_{\text{in}} - R_{\text{ant}})/(Z_{\text{in}} + R_{\text{ant}})| \tag{12}$$

$$\text{PEE}_{\text{MN}} = 4R_{\text{ant}} \times \text{real}(Z_{\text{in}})/(Z_{\text{in}} + R_{\text{ant}})^2 \tag{13}$$

where $Z_{\text{in}} = Z_{\text{Cmp}}||(Z_{\text{Lm}} + Z_{\text{Cm}}||Z_{\text{rec}})$, $Z_{\text{Cmp}} = R_{\text{Cmp}} + 1/(j\omega C_{\text{mp}})$, $Z_{\text{Cm}} = R_{\text{Cm}} + 1/(j\omega C_{\text{m}})$, and $Z_{\text{Lm}} = R_{\text{Lm}} + j\omega L_{\text{m}}$. The rectifier input power is

$$P_{\text{in.rec}} = (V_{\text{in.rec}}/\sqrt{2})^2/R_{\text{rec}}. \tag{14}$$

Therefore, the corresponding incident RF power in Step 4 can be computed as

$$P_{\text{incident}} = P_{\text{in.rec}}/(\text{PCE}_{\text{MN}} \times \text{PEE}_{\text{MN}}). \tag{15}$$

Equation (15) expresses the relationship between $V_{\text{in.rec}}$ and P_{incident}. As a result, the π-MN sized from Z_{rec} at given $V_{\text{in.rec}}$ at Step 2 can be converted to its corresponding

$$\text{PCE}_{\text{MN}} = \frac{\text{Gain}_{\text{MN}}^2/R_{\text{rec}}}{\text{Gain}_{\text{MN}}^2/R_{\text{rec}} + R_{\text{Cm}}(\text{Gain}_{\text{MN}}/Z_{\text{Cm}})^2 + R_{\text{Cmp}}/Z_{\text{Cmp}}^2 + R_{\text{Lm}}(1/Z_{\text{in}} - 1/Z_{\text{Cmp}})^2} \tag{11}$$

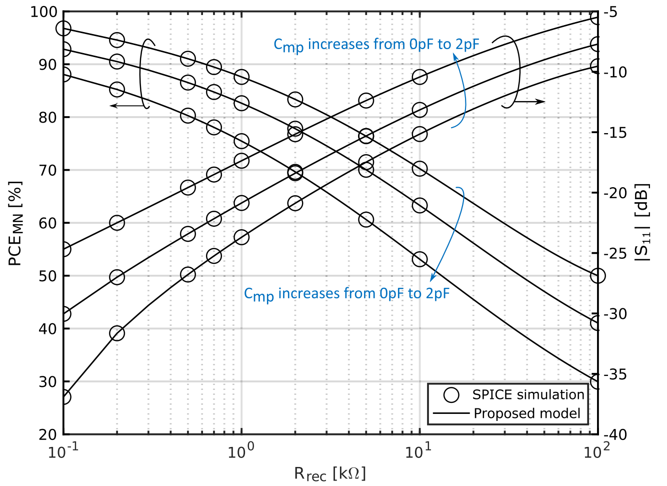

Fig. 12. Comparison between the full SPICE simulation and proposed modeling computation on PCE$_{\mathrm{MN}}$ and $|S_{11}|$. The π-MN is sized depending on R_{rec} as depicted in Fig. 8.

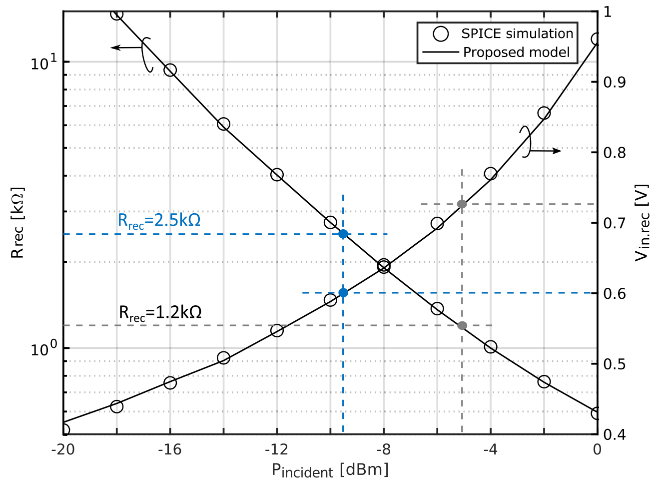

Fig. 13. Rectifier equivalent input resistor and input voltage depending on incident RF power with π-MN sized at $C_{\mathrm{mp}} = 2$ pF. $V_{\mathrm{in.rec}}$ increases about 25 mV with $C_{\mathrm{mp}} = 0$ pF and corresponding R_{rec} decreases as depicted in Fig. 4.

P_{incident}. Combining (11), (13), and PCE$_{\mathrm{rec}}$ extracted in Step 1, the global RFEH system PHE can be computed as expressed in (1).

In order to get the optimum $\gamma_{\mathrm{MPPT.RFEH}}$ at corresponding P_{incident}, the rectifier open-circuit output voltage in the RFEH system needs to be computed first, which is expressed as $V'_{\mathrm{out.rec.OC}}$. Let us emphasize here that $V'_{\mathrm{out.rec.OC}}$ is not corresponding to the previous given $V_{\mathrm{in.rec}}$, otherwise we could directly get $V'_{\mathrm{out.rec.OC}}$ from Fig. 5 since $V_{\mathrm{out.rec.OC}} = \mathrm{VCE} \times V_{\mathrm{in.rec}}$. Rectifier input voltage $V_{\mathrm{in.rec}}$ is changed to $V'_{\mathrm{in.rec}}$ due to actual matching conditions (both PEE$_{\mathrm{MN}}$ and PCE$_{\mathrm{MN}}$) changed at open circuit. Therefore, $V'_{\mathrm{out.rec.OC}}$ corresponds to $V'_{\mathrm{in.rec}}$. Assuming the rectifier equivalent input impedance is Z'_{rec} at the RFEH open circuit, we can combine (11), (13), and (14) to express $V'_{\mathrm{in.rec}}$ as

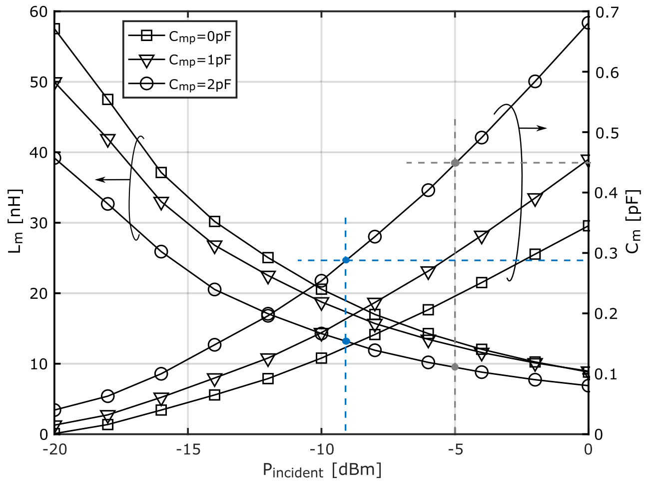

Fig. 14. Computed π-MN sizes depending on incident RF power.

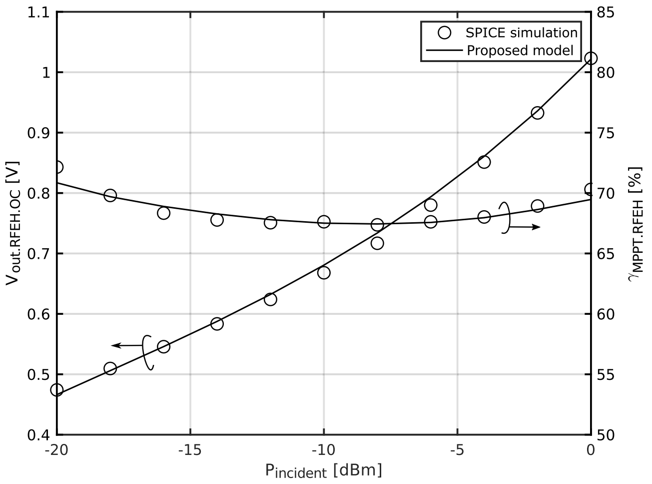

Fig. 15. RFEH open-circuit output voltage and corresponding MPPT regulation ratio depending on incident RF power with π-MN sized at $C_{\mathrm{mp}} = 0$ pF. $V_{\mathrm{out.RFEH.OC}}$ decreases about 35 mV with $C_{\mathrm{mp}} = 2$ pF and corresponding $\gamma_{\mathrm{MPPT.RFEH}}$ is also around 70%.

$$\begin{aligned} V'_{\mathrm{in.rec}} &= \sqrt{2P'_{\mathrm{in.rec}} \times \mathrm{real}(Z'_{\mathrm{rec}})} \\ &= \sqrt{\frac{2P_{\mathrm{incident}} \times \mathrm{real}(Z'_{\mathrm{rec}})}{\mathrm{PCE_{MN}}\big|_{Z'_{\mathrm{rec}}} \times \mathrm{PEE_{MN}}\big|_{Z'_{\mathrm{rec}}}}}. \end{aligned} \tag{16}$$

As depicted in Fig. 4 and expressed in (2), the monotonic relationship between rectifier Z_{rec} and $V_{\mathrm{in.rec}}$ at open circuit is the other constraint condition in addition to (16) and it be expressed as $Z'_{\mathrm{rec}} = f(V'_{\mathrm{in.rec}}, \mathrm{VCE} \times V'_{\mathrm{in.rec}})$. Z'_{rec} can be simplified to R'_{rec} in parallel with a constant 65-fF C'_{rec} since rectifier input capacitance variation with $V_{\mathrm{in.rec}}$ is very limited. The generic function of *polyxpoly* in MATLAB [34] can be used to find the above two independent functions, single intersection point expressed as $V'_{\mathrm{in.rec}} = V_{\mathrm{in.rec.OC}}$ and $Z'_{\mathrm{rec}} = Z_{\mathrm{rec.OC}}$. Therefore, $V'_{\mathrm{out.rec.OC}} = \mathrm{VCE} \times V_{\mathrm{in.rec.OC}} = V_{\mathrm{out.RFEH.OC}}$. Therefore, in Step 5, $\gamma_{\mathrm{MPPT.RFEH}}$ can be expressed as

$$\gamma_{\mathrm{MPPT.RFEH}} = \frac{\gamma_{\mathrm{MPPT.rec}} V_{\mathrm{out.rec.OC}}}{V_{\mathrm{out.RFEH.OC}}} = \frac{\gamma_{\mathrm{MPPT.rec}} V_{\mathrm{in.rec}}}{V_{\mathrm{in.rec.OC}}}. \tag{17}$$

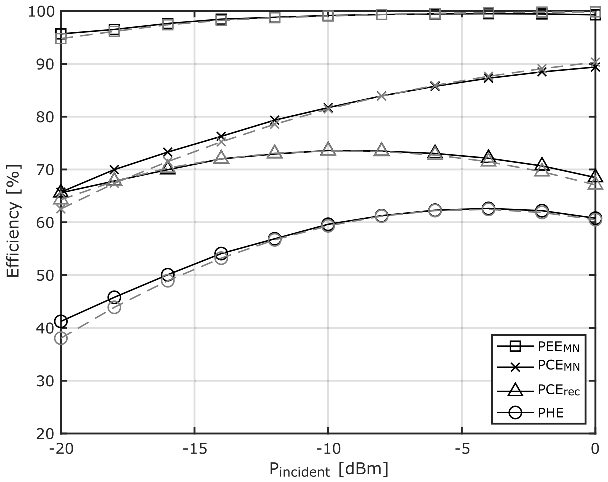

Fig. 16. RFEH blocks and global power efficiencies performance with π-MN sized at $C_{\mathrm{mp}} = 0$ pF and $\gamma_{\mathrm{MPPT.RFEH}} = 70\%$. Gray dash lines: proposed modeling computation results. Black lines: fully SPICE simulation results.

C. Modeling Results and Verification

All the following modeling results in this section are based on the rectifier characterized in Section II-B with $\gamma_{\mathrm{MPPT.rec}} = 85\%$ since this ratio maximizes $\mathrm{PCE}_{\mathrm{rec}}$ as shown in Fig. 6. As depicted in Fig. 12, the proposed modeling results obtained in Step 3 match the full SPICE simulation results on $\mathrm{PCE}_{\mathrm{MN}}$ and $|S_{11}|$. Using finite quality factors for the π-MN elements ($Q_{\mathrm{Cm}} = 200$, $Q_{\mathrm{Cmp}} = 200$, and $Q_{\mathrm{Lm}} = 35$), the increasing R_{rec} resistance decreases the $\mathrm{PCE}_{\mathrm{MN}}$ and increases $|S_{11}|$ (namely, decreases $\mathrm{PEE}_{\mathrm{MN}}$). This further shows the challenge to achieve good PHE at low incident RF power as mentioned in the Introduction. At given R_{rec}, the increasing C_{mp} degrades RFEH $\mathrm{PCE}_{\mathrm{MN}}$ and $|S_{11}|$ performance due to the higher ac current amplitude in π-MN, as depicted in Fig. 10, despite the fact that it can relax the parasitic capacitance margin on the equivalent C_{m}.

The relationship between P_{incident} and $V_{\mathrm{in.rec}}$ is shown in Fig. 13 as computed in Step 4. $R_{\mathrm{rec}} = 1.2$ kΩ characterized at $V_{\mathrm{in.rec}} = 0.72$ V corresponds to −5-dBm P_{incident}. A higher R_{rec} is with a lower P_{incident}. The computed π-MN sizes depending on P_{incident} are depicted in Fig. 14. Comparing Figs. 8 and 14 shows that the low P_{incident} causes high R_{rec} due to low $V_{\mathrm{in.rec}}$ at low P_{in} and vice versa. For example, at $P_{\mathrm{incident}} = -5$ dBm, the corresponding $R_{\mathrm{rec}} = 1.2$ kΩ with $C_{\mathrm{m}} = 0.45$ pF and $L_{\mathrm{m}} = 10$ nH at $C_{\mathrm{mp}} = 2$ pF. At $P_{\mathrm{incident}} = -9.5$ dBm, the corresponding R_{rec} is 2.5 kΩ with $C_{\mathrm{m}} = 0.29$ pF and $L_{\mathrm{m}} = 13.5$ nH at $C_{\mathrm{mp}} = 2$ pF.

As depicted in Fig. 15, the corresponding $\gamma_{\mathrm{MPPT.RFEH}}$ around 70% although the rectifier is characterized with $\gamma_{\mathrm{MPPT.rec}} = 85\%$ in Step 1. Fig. 16 shows the RFEH blocks and global system efficiency performances with the π-MN sizes optimized in Fig. 14 at $C_{\mathrm{mp}} = 0$ pF. Again, the results obtained with the proposed modeling match SPICE simulation results. The slight difference is mainly due to harmonics effect since the rectifier is non-linear, while during modeling and computation, it is modeled as a linear resistor and capacitor. The $\mathrm{PCE}_{\mathrm{rec}}$ remains high from 0 to −20 dBm. Since, as depicted in Fig. 5, with $\gamma_{\mathrm{MPPT.rec}} = 85\%$, the $\mathrm{PCE}_{\mathrm{rec}}$ is above 60% when $V_{\mathrm{in.rec}} > 0.5$ V. The PHE degradation at low P_{incident} is mainly caused by $\mathrm{PCE}_{\mathrm{MN}}$. Indeed, it shows that MN has a significant effect on RFEH performance.

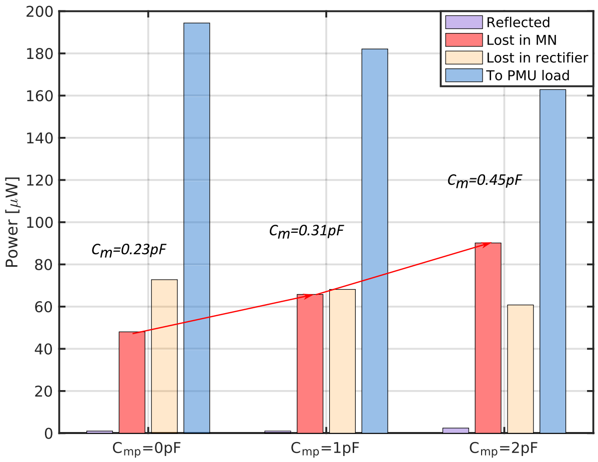

Fig. 17. RFEH power losses classification with π-MN sizes at different C_{mp} for target $P_{\mathrm{incident}} = -5$ dBm$(= 316.23\ \mu\mathrm{W})$.

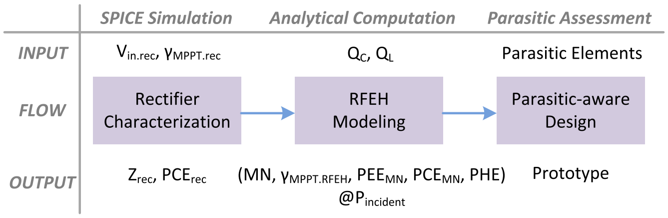

Fig. 18. Proposed RFEH prototype design flow with three successive tasks.

However, as depicted in Fig. 17, C_{m} is only about 0.23 pF at $P_{\mathrm{incident}} = -5$ dBm, which is less than what we estimated (as will be discussed in Section IV-A) for the package and PCB parasitic capacitors that can contribute to equivalent C_{m}. In line with what was depicted in Fig. 9, a larger C_{mp} relaxes the margin on parasitic capacitance. C_{m} is up to 0.45 pF with $C_{\mathrm{mp}} = 2$ pF. However, it causes power loss in MN increasing, finally, degrading the converted power to PMU load. As illustrated in Fig. 10, a larger C_{mp} enhances ac current amplitude in π-MN and increases power loss due to parasitic resistors.

IV. RFEH PROTOTYPE DESIGN AND MEASUREMENT RESULTS

As summarized in Fig. 18, the proposed RFEH prototype design flow is based on three successive tasks. First, a specified rectifier is characterized at different input voltages $V_{\mathrm{in.rec}}$ and output MPPT regulation ratios $\gamma_{\mathrm{MPPT.rec}}$ by the SPICE simulation, as depicted in Fig. 4. Second, rectifier characterization results Z_{rec} and $\mathrm{PCE}_{\mathrm{rec}}$ are included in the proposed RFEH model for sizing MN and computing $\mathrm{PEE}_{\mathrm{MN}}/\mathrm{PCE}_{\mathrm{MN}}/\mathrm{PHE}$ performance at corresponding input P_{incident} and output MPPT regulation ratio $\gamma_{\mathrm{MPPT.RFEH}}$ with given lumped elements quality factors as depicted in Fig. 11. Third, parasitic elements are taken into consideration for optimizing MN in practical

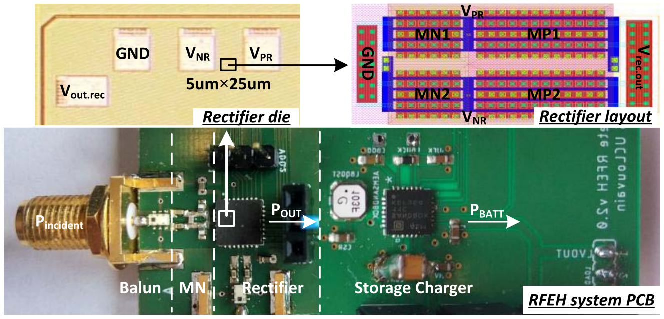

Fig. 19. Proposed RFEH system prototype implementation.

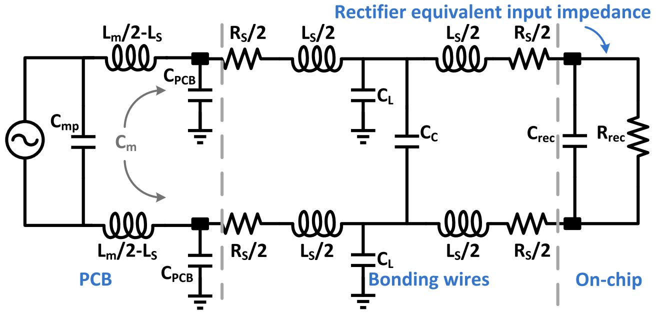

Fig. 20. Model of PCB/package parasitics (5×5 mm QFN32L with $R_S = 46$ mΩ, $L_S = 1.11$ nH, $C_L = 202$ fF, and $C_C = 39$ fF).

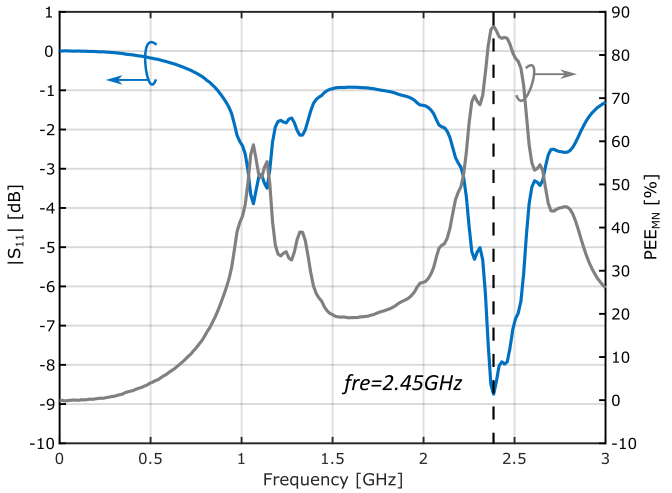

Fig. 21. Reflection coefficient $|S_{11}|$ and corresponding PEE_{MN} measurement results by sweeping the RF operational frequency.

design as illustrated in Figs. 19 and 20. If different rectifiers are characterized in the first task, this flow can also be used to size the rectifier by comparing their modeling results. In this paper, we focus on the specified rectifier already used in [10] and characterized in Section II-B.

A. RFEH Prototype Parasitic-Aware Design

The cross-coupled RF rectifier was designed and fabricated in a 65-nm LP CMOS process with 5 μm×25 μm area and assembled in a 5×5-mm open-cavity QFN32L package. As depicted in Fig. 19, the full RFEH system also includes a Balun, a discrete-component MN, and the AEM30940 PMU from e-peas semiconductors for storage charging with pseudo-MPPT [35]. It allows configuring the γ_{MPPT} ratio at 50%, 70%, or 85% (we used an internal prototype but the commercial product has selectable ratios of 50%, 65%, or 80%). The selected AEM30940 battery-charging PMU operates with pseudo-MPPT. Indeed, it periodically disconnects the rectifier output and senses its open-circuit voltage (in this design, $V_{\text{out.rec.OC}}$ is close to 81.2%×$V_{\text{in.rec}}$ ac amplitude, as illustrated in Fig. 5) and then regulates the rectifier output voltage by forcing $V_{\text{out.rec}}$ to a configurable ratio $\gamma_{\text{MPPT.RFEH}}$ of $V_{\text{out.rec.OC}}$.

At 2.45 GHz, PCB and package parasitics have a magnified impact compared to sub-gigahertz. The C_{m} capacitance in the π-MN has a minimum value coming from the combination of the PCB (C_{PCB}) and package (C_{L} and C_{C}) parasitics, as depicted in Fig. 20. From the datasheet of QFN package model, the total parasitic from two input RF bonding wires and PCB is around 0.30 pF ($=C_{\text{L}}/2+C_{\text{C}}+C_{\text{PCB}}/2$) if $C_{\text{PCB}} = 0.30$ pF [with a trace length (L) of 5.5 mm, width (W) of 0.7 mm, and height (H) of 0.5 mm in FR4 PCB and $C_{PCB} = \epsilon WL/H$. Here, ϵ is PCB permittivity]. As depicted in Fig. 8, the 0.30-pF C_{m} value requires an equivalent input resistance of the rectifier below 0.6 kΩ when C_{mp} is 0 pF (corresponding to an L-MN). This is a difficult target for sizing the rectifier at low incident RF power. Therefore, using $C_{\text{mp}} = 2$ pF, the R_{rec} requirement is relaxed to 2.3 kΩ. However, in real measurement, due to extra parasitic capacitor from PCB arbitrary soldering and extra bonding wire length for die position in package, which depends on fabrication technique and is variable case by case, the equivalent C_{m} is estimated at 0.45 pF from RF Vector Network Analyzers (VNA) measurement. The corresponding matched R_{rec} is close to 1.20 kΩ with $C_{\text{mp}} = 2$ pF and $L_{\text{m}} = 10$ nH as depicted in Fig. 14, which results in an explicit L_{m} of 7 nH in series with the parasitic inductance L_{S} of the bonding wires. This means that the best matching occurs when the incident RF power results in R_{rec} of 1.20 kΩ at $P_{\text{incident}} = -5$ dBm as predicted with modeling results shown in Figs. 13 and 14. Let us mention here that assuming sub-gigahertz WPT at 900 MHz, the same 0.45-pF C_{m} equivalent parasitic capacitance would require a target R_{rec} of 4 kΩ, which is much easier to obtain at low incident RF power, as depicted in Fig. 13.

B. RFEH Prototype Measurements Results

The measured $|S_{11}|$ parameter at the MN input for −5-dBm incident power with open load shows excellent matching at 2.45 GHz as depicted in Fig. 21. The PEE_{MN} curve is the vertical mirror of $|S_{11}|$ as explained in Section III-B because of $\text{PEE}_{\text{MN}} = 1 - |S_{11}|^2$ (here, $|S_{11}|$ is in linear units). Since this matching depends on R_{rec}, it is sensitive to $V_{\text{in.rec}}$ and $V_{\text{out.rec}}$. Fig. 22(a) shows that the optimum matching is reached for different $V_{\text{out.rec}}$ values. The best matching is at $P_{\text{incident}} = -5$ dBm, which is in agreement with modeling results and parasitic-aware design in Section IV-A. MPPT thus helps preserving a good matching from 0 to −10 dBm.

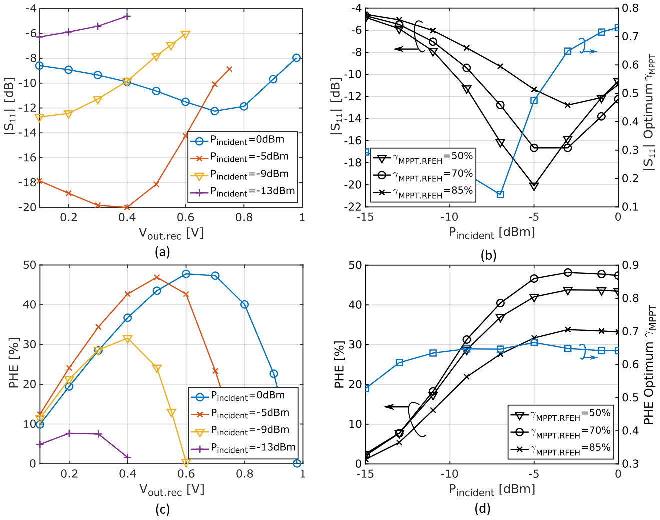

Fig. 22. RFEH measurement results depending on rectifier output voltage $V_{\text{out.rec}}$ and incident RF power P_{incident}. (a) $|S_{11}|$ versus $V_{\text{out.rec}}$ at different P_{incident}. (b) $|S_{11}|$ versus P_{incident} at different $\gamma_{\text{MPPT.RFEH}}$ and its optimum $\gamma_{\text{MPPT.RFEH}}$. (c) PHE versus $V_{\text{out.rec}}$ at different P_{incident}. (d) PHE versus P_{incident} at different $\gamma_{\text{MPPT.RFEH}}$ and its optimum $\gamma_{\text{MPPT.RFEH}}$.

However, below −10 dBm, the mismatch becomes serious as R_{rec} becomes significantly higher than the target 1.2 kΩ for which the π-MN was sized with 0.45-pF C_{m} contributed from parasitic capacitors. As depicted in Fig. 22(b), the optimum $\gamma_{\text{MPPT.RFEH}}$ for $|S_{11}|$ is reduced at low P_{incident}, because the low $V_{\text{out.rec}}$ helps to mitigate the R_{rec} increase due to low $V_{\text{in.rec}}$, as shown in Figs. 4 and 6. Fig. 22(c) clearly shows that the PHE is maximized for a $V_{\text{out.rec}}$ voltage that varies from 0.25 to 0.65 V as a function of the incident RF power. This really validates the need for rectifier output voltage MPPT regulation. The $\gamma_{\text{MPPT.RFEH}}$ ratio to select is analyzed in Fig. 22(d) with the PHE obtained for 50%, 70%, and 85% ratios. For the target $P_{\text{incident}} = -5$ dBm, the optimum $\gamma_{\text{MPPT.RFEH}}$ is close to 70% which agrees with the modeling results, as depicted in Fig. 15. At other P_{incident}, the best PHE is reached at $\gamma_{\text{MPPT.RFEH}}$ ratio of 70% as a trade-off between an optimum PCE_{rec} at higher ratio $\gamma_{\text{MPPT.RFEH}}$ (although $\gamma_{\text{MPPT.RFEH}} \neq \gamma_{\text{MPPT.rec}}$, they are positively correlated) and a better matching (thanks to lower R_{rec}) at lower $\gamma_{\text{MPPT.RFEH}}$.

Fig. 23 shows that PHE measurement results are in excellent agreement with the post-layout simulation results with all parasitic elements taken into account. The proposed RFEH has an excellent performance from 0 to −10 dBm, thanks to the parasitic-aware design on the strength of π-MN optimized sizes from the proposed RFEH global modeling results in Fig. 14 and the absence of reconfiguration switches. Below −10 dBm, the impedance mismatch shows up. The PHE suffers from both the reflected power loss and the associated $V_{\text{rec.in}}$ drop, which results in a low PCE_{rec} as shown in Fig. 5.

To demonstrate that the PHE of the proposed RFEH system is limited at low P_{incident} by the PCB/package parasitic capacitance, we simulated the RFEH assuming that this equivalent capacitance could be reduced to 0.30 pF. Results in Fig. 23 show that in this case, the PHE can be kept higher than 25% down to −16 dBm with sensitivity below −20 dBm. Furthermore, without considering the minimum parasitic capacitance, the theoretical RFEH roof performance keeps the PHE above 40% down to −20 dBm with the π-MN optimally sized for each target P_{incident}, as proposed in Fig. 14.

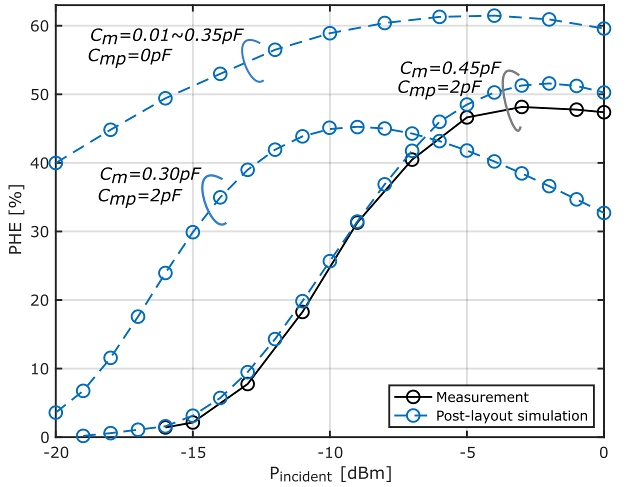

Fig. 23. RFEH PHE with $\gamma_{\text{MPPT.RFEH}} = 70\%$ measurement and post-layout simulation results. The curve with $C_{\text{m}} = 0.01$–0.35 pF label is theoretical PHE roof with π-MN sizes optimized for each target P_{incident} as shown in Fig. 14 with $C_{\text{mp}} = 0$ pF. The other curves have a fixed π-MN with $C_{\text{mp}} = 2$ pF.

As summarized in Table I, compared to the previous works, we use the proposed RFEH system modeling methodology and parasitic-aware design techniques beyond MPPT. No configuration switch is used. Not only it avoids parasitic capacitor and power loss but also it does not need additional/external power supply to drive the switch. With only one stage, the rectifier output voltage $V_{\text{out.rec}}$ at open circuit can be up to 400 mV at −17.1 dBm. Instead of boosting $V_{\text{out.rec}}$ by increasing the number of rectifier stages in [3], [6], and [7], the MPPT PMU that can start from 380 mV with an input voltage operation ranging from 50 mV to 5.5 V [35] internally boosts and regulates the rectifier output $V_{\text{out.rec}}$ to 1.8 V to power supply load as in [1]. Almost all peak PHE happens at high P_{incident} around 0 dBm because the rectifier equivalent input impedance Z_{rec} is low at high P_{incident}, as illustrated in Figs. 4 and 13. Compared to high Z_{rec}, a low Z_{rec} is easier to be matched by MN since it is closer to antenna impedance. This means that a smaller inductance L_{m} and capacitance C_{mp} are needed to compensate a certain C_{m} which is contributed by parasitic capacitors, as depicted in Figs. 8 and 20. The RFEHs in [21] and [26] achieve high PHE but they only concern rectifier efficiency alone by assuming an ideal matching without RF power been reflected and power loss on MN. Indeed, as illustrated in the measurement results shown in Fig. 22, these power losses significantly influence RFEH performance. The good PHE in [26] is also obtained, thanks to its low operational frequency with less rectifier switching losses and conduction losses which are another challenge at 2.45 GHz.

TABLE I

TECHNIQUE AND PERFORMANCE COMPARISON

	This work	[1] 2018 PATMOS	[3] 2017 TCAS-II	[6] 2016 ISCAS	[7] 2017 JSSC	[21] 2018 ISCAS	[26] 2016 JSSC
Rectifier Process	65nm	Discrete	65nm	0.18μm	0.18μm	0.13μm	0.25μm
Frequency	2.45GHz	2.45GHz	900MHz	2.40GHz	915MHz	915MHz	13.56MHz
Topology	Cross-coupled	Greinacher doubler	Cross-coupled	Greinacher doubler	Greinacher doubler	Cross-coupled	Cross-coupled
Techniques	MPPT, modeling and parasitic-aware design	MPPT	Dual-path	Tune rectifier	Tune MN and rectifier	V_{th} compensation	ULPD, gradient sizing
Config. Switch	No	No	Yes	Yes	Yes	No	No
No. Rectifier Stages	1	1	5	12	8	8	3
Rectifier Load	PMU	PMU	Resistor 147kΩ	Charged Capacitor	PMU	Resistor 0.5MΩ	Current sink 10μA
Sensitivity @$V_{out.rec.OC}$	-17.1dBm/ -22.7dBm† @400mV	-10.9dBm‡ @400mV	-17.7dBm @1V	-22dBm† @1.25V	-14.8dBm @1V	-30.5dBm†* @1V	N.A. N.A.
Peak PHE @$P_{incident}$	48.3%/ 45%† @-3dBm/ -10dBm	32.5% @0dBm	34.5% @-2dBm	38.4%† @0dBm	26% @0dBm	42.8%†* @-16dBm	72%* @1V_{PP}

† Post-layout simulation results. * Only concerning PCE_{rec} without PEE_{MN} and PCE_{MN}. ‡ Including sensor power consumption.

V. CONCLUSION

A full 2.45-GHz RFEH system with MPPT for SWIPT IoT smart sensors is presented in this paper. We model the RFEH system with a global reverse analysis to integrate the non-linear rectifier characteristics into the full system for predicting the efficiency and optimizing the MN design. The schematic simulation, global modeling, and prototype measurement results achieve an excellent match. Because of the high impact of capacitive parasitics, which are more critical at 2.45 GHz than below 1 GHz, the parasitic-aware RFEH design first estimates PCB/package parasitic capacitance and then takes it into account to size the explicit capacitance required for the π-MN. This sizing is enabled by the RFEH modeling results with the predicted corresponding input incident RF power and output MPPT regulation ratio.

RFEH prototype measurement results show an experimental sensitivity of −17.1 dBm and peak PHE of 48.3% at −3 dBm. The simulation shows that reducing the parasitic PCB/package capacitance by 150 fF would result in 45% PHE down to −10 dBm with a sensitivity as low as −22.7 dBm. Designing 2.45-GHz RFEHs with the help of the proposed modeling methodology thus shows great potential down to −20 dBm of incident RF power. Below −20 dBm, the parasitic capacitive margin vanishes, which is an open challenge for future work.

APPENDIX

RFEH MODELING MATHEMATIC DERIVATION

As depicted in Fig. 11, the real inductor and capacitor elements are first-order modeled as a parasitic resistor in series with their corresponding pure reactive elements. The resistors result in RF power losses in MN. However, as depicted in Fig. 10, loss-less capacitors and inductors influence ac current amplitude, which finally have an effect on resistive power losses since they are the products of resistances and the square of ac currents. Therefore, the power losses on practical C_{m}, C_{mp}, and L_{m} can be thus, respectively, expressed as

$$\begin{aligned} P_{\mathrm{Cm}} &= I_{\mathrm{Cm}}^2/2 \times R_{\mathrm{Cm}} \\ &= (V_{\mathrm{in.rec}}/Z_{\mathrm{Cm}})^2/2 \times R_{\mathrm{Cm}} \end{aligned} \tag{18}$$

$$\begin{aligned} P_{\mathrm{Cmp}} &= I_{\mathrm{Cmp}}^2/2 \times R_{\mathrm{Cmp}} \\ &= (V_{\mathrm{in}}/Z_{\mathrm{Cmp}})^2/2 \times R_{\mathrm{Cmp}} \end{aligned} \tag{19}$$

$$\begin{aligned} P_{\mathrm{Lm}} &= I_{\mathrm{Lm}}^2/2 \times R_{\mathrm{Lm}} \\ &= (I_{\mathrm{in}} - I_{\mathrm{Cmp}})^2/2 \times R_{\mathrm{Lm}} \\ &= [V_{\mathrm{in}} \times (1/Z_{\mathrm{in}} - 1/Z_{\mathrm{Cmp}})]^2/2 \times R_{\mathrm{Lm}} \end{aligned} \tag{20}$$

where both voltage and current here represent their ac amplitude values. By Ohm's law, the relationship between rectifier input $V_{\mathrm{in.rec}}$ and π-MN input V_{in} can be expressed as

$$\begin{aligned} V_{\mathrm{in.rec}} &= I_{\mathrm{Lm}} \times (Z_{\mathrm{Cm}}||Z_{\mathrm{rec}}) \\ &= (I_{\mathrm{in}} - I_{\mathrm{Cmp}}) \times (Z_{\mathrm{Cm}}||Z_{\mathrm{rec}}) \\ &= V_{\mathrm{in}} \times (1/Z_{\mathrm{in}} - 1/Z_{\mathrm{Cmp}}) \times (Z_{\mathrm{Cm}}||Z_{\mathrm{rec}}). \end{aligned} \tag{21}$$

From (21), the MN voltage gain $\mathrm{Gain}_{\mathrm{MN}} = V_{\mathrm{in.rec}}/V_{\mathrm{in}}$ can be expressed as (11), as shown at the bottom of the page 7.

The total power losses on π-MN P_{MN} are the sum of P_{Cm}, P_{Lm}, and P_{Cmp}. Combining (14) and (18) to (21), the $\mathrm{PCE}_{\mathrm{MN}} = P_{\mathrm{in.rec}}/(P_{\mathrm{MN}} + P_{\mathrm{in.rec}})$ can be further derived as (11), which is used in Step 3.a in Fig. 11.

Except for reflected RF power due to mismatch, the RF power extracted by MN system can be expressed as

$$\begin{aligned} P_{\mathrm{in}} &= I_{\mathrm{in}}^2/2 \times \mathrm{real}(Z_{\mathrm{in}}) \\ &= [V_{\mathrm{ant}}/(Z_{\mathrm{in}} + R_{\mathrm{ant}})]^2/2 \times \mathrm{real}(Z_{\mathrm{in}}). \end{aligned} \tag{22}$$

Let us emphasized here only real part of Z_{in} consuming electrical power. When $Z_{\mathrm{in}} = R_{\mathrm{ant}}$, the MN extracts the maximum RF power, thanks to the perfect conjugate matching in the π-MN. Therefore,

$$P_{\mathrm{in.max}} = P_{\mathrm{incident}} = V_{\mathrm{ant}}^2/(8 \times R_{\mathrm{ant}}). \tag{23}$$

Combining(22) and (23), the RFEH MN power extraction efficiency $\mathrm{PEE_{MN}}$ can be expressed as

$$\begin{aligned}\mathrm{PEE_{MN}} &= P_{\mathrm{in}}/P_{\mathrm{incident}}\\ &= \frac{4R_{\mathrm{ant}} \times \mathrm{real}(Z_{\mathrm{in}})}{(Z_{\mathrm{in}} + R_{\mathrm{ant}})^2}.\end{aligned} \tag{24}$$

From (12) and (13), we can also get directly the relationship between $|S_{11}|$ and $\mathrm{PEE_{MN}}$, which is $\mathrm{PEE_{MN}} = 1-|S_{11}|^2$ (here, $|S_{11}|$ is in linear units) as illustrated in Fig. 21.

As expressed in (11)–(14), once the MN impedance Z_{MN} and rectifier equivalent input impedance Z_{rec} are specified, $|S_{11}|$, $\mathrm{Gain_{MN}}$, $\mathrm{PEE_{MN}}$, and $\mathrm{PCE_{MN}}$ can be computed, respectively. The proposed RFEH modeling method is quite flexible. It can be easily applied on another operational frequency and both the rectifier and MN can be updated to another topology, supposing that the rectifier characterization in Step 1 and MN sizing in Step 2, as depicted in Fig. 11, are with this given frequency and topology. If a fixed MN is already specified, then Step 2 can be skipped. Equations (18)–(20) should be re-computed accordingly when a more complex lumped/distributed element model is used. If the rectifier load is a resistor or current sink but not MPPT PMU, then Step 5 can also be skipped. However, the rectifier should be characterized by the corresponding load in Step 1. More explicitly, the rectifier equivalent input impedance Z_{rec} is the rectifier with its load equivalent input impedance, but not rectifier alone.

ACKNOWLEDGMENT

The authors would like to thank P.-A. Haddad (ON Semi), P. Simon (UCLouvain Welcome), and S. Houtain (e-peas) for fruitful discussions about RF energy harvesting (RFEH) prototype design and measurement.

REFERENCES

[1] R. Dekimpe, P. Xu, M. Schramme, D. Flandre, and D. Bol, "A battery-less BLE IoT motion detector supplied by 2.45-GHz wireless power transfer," in *Proc. IEEE 28th Int. Symp. Power Timing Modeling, Optim. Simulation (PATMOS)*, Jul. 2018, pp. 68–75.

[2] R. Dekimpe, P. Xu, M. Schramme, P. Gérard, D. Flandre, and D. Bol, "A battery-less BLE smart sensor for room occupancy tracking supplied by 2.45-GHz wireless power transfer," *Integration*, vol. 67, pp. 8–18, Jul. 2019.

[3] Y. Lu *et al.*, "A wide input range dual-path CMOS rectifier for RF energy harvesting," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 64, no. 2, pp. 166–170, Feb. 2017.

[4] J.-H. Tsai, C.-Y. Kuo, S.-H. Lin, F.-T. Lin, and Y.-T. Liao, "A wirelessly powered CMOS electrochemical sensing interface with power-aware RF-DC power management," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 9, pp. 2810–2820, Sep. 2018.

[5] S. Scorcioni, A. Bertacchini, and L. Larcher, "A 868 MHz CMOS RF-DC power converter with −17 dBm input power sensitivity and efficiency higher than 40% over 14 dB input power range," in *Proc. IEEE ESSCIRC (ESSCIRC)*, Sep. 2012, pp. 109–112.

[6] Z. Zeng, X. Li, A. Bermak, C.-Y. Tsui, and W.-H. Ki, "A WLAN 2.4-GHz RF energy harvesting system with reconfigurable rectifier for wireless sensor network," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2016, pp. 2362–2365.

[7] M. A. Abouzied, K. Ravichandran, and E. Sánchez-Sinencio, "A fully integrated reconfigurable self-startup RF energy-harvesting system with storage capability," *IEEE J. Solid-State Circuits*, vol. 52, no. 3, pp. 704–719, Mar. 2017.

[8] M. Stoopman, S. Keyrouz, H. J. Visser, K. Philips, and W. A. Serdijn, "Co-design of a CMOS rectifier and small loop antenna for highly sensitive RF energy harvesters," *IEEE J. Solid-State Circuits*, vol. 49, no. 3, pp. 622–634, Mar. 2014.

[9] X. Liu and E. Sánchez-Sinencio, "An 86% efficiency 12 μW self-sustaining PV energy harvesting system with hysteresis regulation and time-domain MPPT for IOT smart nodes," *IEEE J. Solid-State Circuits*, vol. 50, no. 6, pp. 1424–1437, Jun. 2015.

[10] P. Xu, D. Flandre, and D. Bol, "Design of a 2.45-GHz RF energy harvester for SWIPT IoT smart sensors," in *Proc. IEEE Asian Solid-State Circuits Conf. (ASSCC)*, Nov. 2018, pp. 107–110.

[11] X. Hua and R. Harjani, "A 5μW-5 mW input power range, 0-3.5V output voltage range RF energy harvester with power-estimator-enhanced MPPT controller," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, May 2018, pp. 1–4.

[12] P.-H. Hsieh, C.-H. Chou, and T. Chiang, "An RF energy harvester with 44.1% PCE at input available power of −12 dBm," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 6, pp. 1528–1537, Jun. 2015.

[13] C.-H. Chou and P.-H. Hsieh, "A 100-MHz radio-frequency energy harvester for passively powered devices," in *Proc. IEEE Eur. Conf. Circuit Theory Design (ECCTD)*, Aug. 2015, pp. 1–4.

[14] J. Wang, Y. Jiang, J. Dijkhuis, G. Dolmans, H. Gao, and P. Baltus, "A 900 MHz RF energy harvesting system in 40 nm CMOS technology with efficiency peaking at 47% and higher than 30% over a 22 dB wide input power range," in *Proc. 43rd IEEE Eur. Solid State Circuits Conf. (ESSCIRC)*, Sep. 2017, pp. 299–302.

[15] K. Kotani and T. Ito, "High efficiency CMOS rectifier circuit with self-$\mathrm{V_{th}}$-cancellation and power regulation functions for UHF RFIDs," in *Proc. IEEE Asian Solid-State Circuits Conf. (ASSCC)*, Nov. 2007, pp. 119–122.

[16] K. Kotani, A. Sasaki, and T. Ito, "High-efficiency differential-drive CMOS rectifier for UHF RFIDs," *IEEE J. Solid-State Circuits*, vol. 44, no. 11, pp. 3011–3018, Nov. 2009.

[17] Z. Hameed and K. Moez, "A 3.2 V −15 dBm adaptive threshold-voltage compensated RF energy harvester in 130 nm CMOS," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 4, pp. 948–956, Apr. 2015.

[18] T. Umeda, H. Yoshida, S. Sekine, Y. Fujita, T. Suzuki, and S. Otaka, "A 950-MHz rectifier circuit for sensor network tags with 10-m distance," *IEEE J. Solid-State Circuits*, vol. 41, no. 1, pp. 35–41, Jan. 2006.

[19] H. Xu and M. Ortmanns, "A temperature and process compensated ultralow-voltage rectifier in standard threshold CMOS for energy-harvesting applications," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 58, no. 12, pp. 812–816, Dec. 2011.

[20] T. Le, K. Mayaram, and T. Fiez, "Efficient far-field radio frequency energy harvesting for passively powered sensor networks," *IEEE J. Solid-State Circuits*, vol. 43, no. 5, pp. 1287–1302, May 2008.

[21] S. M. Noghabaei, R. L. Radin, Y. Savaria, and M. Sawan, "A high-efficiency ultra-low-power CMOS rectifier for RF energy harvesting applications," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2018, pp. 1–4.

[22] J. Shin, I.-Y. Chung, Y. J. Park, and H. S. Min, "A new charge pump without degradation in threshold voltage due to body effect [memory applications]," *IEEE J. Solid-State Circuits*, vol. 35, no. 8, pp. 1227–1230, Aug. 2000.

[23] A. K. Moghaddam, J. H. Chuah, H. Ramiah, J. Ahmadian, P.-I. Mak, and R. P. Martins, "A 73.9%-efficiency CMOS rectifier using a lower DC feeding (LDCF) self-body-biasing technique for far-field RF energy-harvesting systems," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 4, pp. 992–1002, Apr. 2017.

[24] G. Gosset, B. Rue, and D. Flandre, "Very high efficiency 13.56 MHz RFID input stage voltage multipliers based on ultra low power MOS diodes," in *Proc. IEEE Int. Conf. RFID*, Apr. 2008, pp. 134–140.

[25] D. Levacq, C. Liber, V. Dessard, and D. Flandre, "Composite ULP diode fabrication, modelling and applications in multi-V_{th} FD SOI CMOS technology," *Solid-State Electron.*, vol. 48, no. 6, pp. 1017–1025, 2004.

[26] P.-A. Haddad, G. Gosset, J.-P. Raskin, and D. Flandre, "Automated design of a 13.56 MHz 19 μW passive rectifier with 72% efficiency under 10 μA load," *IEEE J. Solid-State Circuits*, vol. 51, no. 5, pp. 1290–1301, May 2016.

[27] P.-A. Haddad, J.-P. Raskin, and D. Flandre, "Automated design of a 13.56 MHz corner-robust efficient differential drive rectifier for 10 μA load," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2016, pp. 1822–1825.

[28] T. Soyata, L. Copeland, and W. Heinzelman, "RF energy harvesting for embedded systems: A survey of tradeoffs and methodology," *IEEE Circuits Syst. Mag.*, vol. 16, no. 1, pp. 22–57, 1st Quart., 2016.

[29] C. R. Valenta and G. D. Durgin, "Harvesting wireless power: Survey of energy-harvester conversion efficiency in far-field, wireless power transfer systems," *IEEE Microw. Mag.*, vol. 15, no. 4, pp. 108–120, Jun. 2014.

[30] C. Bowick, J. Blyler, and C. Ajluni, *RF Circuit Design*, 2nd ed. New York, NY, USA: Nownos, 2001.

[31] P.-A. Haddad, J.-P. Raskin, and D. Flandre, "Efficient passive energy harvesters at 950 MHz and 2.45 GHz for 100 μW applications in 65 nm CMOS," in *Proc. IEEE Int. Conf. Electron., Circuits Syst. (ICECS)*, Dec. 2016, pp. 508–511.

[32] P.-A. Haddad, "Optimization of passive rectifiers from silicon CMOS technologies to graphene," Ph.D. dissertation, UCLouvain Univ. Catholique de Louvain, Ottignies-Louvain-la-Neuve, Belgium, 2017.

[33] K. Chang, *Radio Frequency Circuit Design*. New York, NY, USA: Wiley, 2006.

[34] MathWorks. (2019). *Polyxpoly: Intersection Points for Lines or Polygon Edges*. [Online]. Available: https://nl.mathworks.com/help/map/ref/polyxpoly.html

[35] *AEM30940—Highly-Efficient Regulated Dual-Output, Ambient Energy Manager for DC or AC Sources or High-Frequency RF Input With Optional Primary Battery*, e-peas, Mont-Saint-Guibert, Belgium, 2018.

Pengcheng Xu (S'13) received the bachelor's degree (Hons.) in physics from Shanghai Normal University, Shanghai, China, in 2013, and the master's degree (Hons.) in integrated circuit engineering from Tongji University, Shanghai, in 2016. He is currently pursuing the Ph.D. degree with the Université catholique de Louvain (UCLouvain), Louvain-la-Neuve, Belgium.

In 2015, he was an Exchange Student with the University of Erlangen–Nuremberg, Erlangen, Germany. Since 2017, he has been a Research Assistant in electronic engineering with UCLouvain. He was the Holder of the National Scholarship for three times. He has authored or coauthored six technical papers, including 2019 Integration, 2019 JSSC, 2019 ISSCC, 2018 ASSCC, 2018 PATMOS, and 2017 S3S. His research area includes analog and mixed-signal integrated circuit design.

Mr. Xu is a Student Member of SSCS. He was a recipient of the Shanghai Outstanding Graduates Student Award and the Meritorious Winner in the 2013 Mathematical Contest in Modeling of America (MCM).

Denis Flandre (M'85–SM'03) received the M.S. degree in electrical engineering, the Ph.D. and the Research Habilitation degrees from the Université catholique de Louvain (UCLouvain), Louvain-la-Neuve, Belgium, in 1986, 1990, and 1999, respectively. His Ph.D. research was on the modeling of silicon-on-insulator (SOI) MOS devices for characterization and circuit simulation. His Ph.D. thesis was on a systematic and automated synthesis methodology for MOS analog circuits.

Since 2001, he has been a Full-Time Professor with UCLouvain. He is the Co-Founder of CISSOID, a spin-off company of UCLouvain focusing on SOI and high-reliability integrated circuit design and products. He is also a Scientific Advisor of two other UCLouvain start-ups: INCIZE (semiconductor characterization and modeling for design of digital, analog/RF, and harsh environment applications) and e-peas [energy harvesting and processing solutions for longer battery life and increased robustness in all Internet of Things (IoT) applications]. He is involved in the research and development of SOI MOS devices, digital and analog circuits, as well as sensors, MEMS and solar cells, for special applications, more specifically ultralow-voltage low-power (LP), microwave, biomedical, radiation-hardened and high-temperature electronics, and microsystems. He has authored or coauthored more than 900 technical papers or conference contributions. He has co-invented 12 patents. He has organized or lectured many short courses on SOI technology, devices and circuits in universities, industrial companies, and conferences. He has participated or coordinated numerous research projects funded by regional and European institutions.

Dr. Flandre has been a member of several EU Networks of Excellence on High-Temperature Electronics, SOI Technology, and Nanoelectronics and Micro-nanotechnology and is an Active Member of the SOI Industry Consortium and the EUROSOI Network. He was a recipient of several scientific prizes and best paper awards.

David Bol (S'07–M'09–SM'18) received the M.Sc. degree in electromechanical engineering and the Ph.D. degree in engineering science from the Université catholique de Louvain (UCLouvain), Louvain-la-Neuve, Belgium, in 2004 and 2008, respectively.

In 2005, he was a Visiting Ph.D. Student with the CNM National Centre for Microelectronics, Seville, Spain, in advanced logic design. In 2009, he was a Post-Doctoral Researcher with intoPIX, Louvain-la-Neuve, in a low-power (LP) design for JPEG2000 image processing. In 2010, he was a Visiting Post-Doctoral Researcher with the Laboratory for Manufacturing and Sustainability, University of California at Berkeley, Berkeley, CA, USA, in the life-cycle assessment of the semiconductor environmental impact. In 2015, he participated to the creation of e-peas semiconductors, Louvain-la-Neuve. He leads the Electronic Circuits and Systems (ECS) Research Group, UCLouvain, with Prof. D. Flandre focused on ultra-LP design of integrated circuits for the Internet of Things (IoT) including computing, power management, sensing, and RF communications with a focus on technology/circuit interaction in nanometer CMOS nodes, variability mitigation, mixed-signal SoC architecture, and implementation. He is currently an Assistant Professor with UCLouvain. He lectures four M.Sc. courses in electrical engineering at UCLouvain on digital, analog, and mixed-signal integrated circuits and systems as well as sensors. He has authored or coauthored more than 100 technical papers and conference contributions. He holds three delivered patents.

Dr. Bol was a recipient of the three Best Paper/Poster/Design Awards in the IEEE Conferences (ICCD 2008, SOI Conference 2008, and FTFC 2014). He also serves as an Editor for the *Journal of Low-Power Electronics and Applications* (MDPI), a TPC Member for the IEEE S3S Conference, and a Reviewer for various journals and conferences, such as the IEEE JOURNAL OF SOLID-STATE CIRCUITS, the IEEE TRANSACTIONS ON VLSI SYSTEM, and the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEM I/II. Since 2008, he has been presenting several invited papers, keynotes, and tutorials in international conferences including a forum presentation at the IEEE ISSCC 2018 and a tutorial at ESSCIRC 2018.