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Investigation and optimization of traps properties in Al_2O_3/SiO_2 dielectric stacks using conductance method

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ABSTRACT

In this work, the properties of the interface traps between various Al_2O_3/SiO_2 dielectric stacks and Si substrate are investigated by the conductance method. The trap state density and energy level distribution in the silicon bandgap are extracted for four stacks fabricated by different processes. Our results indicate that the trap state density can be optimized so that Al_2O_3/SiO_2 can be advantageous for nano-scale transistors and resistive switching memory.

1. Introduction

Al_2O_3 metal oxide has been introduced in many applications, including gate dielectric in metal–oxidesemiconductor field-effect transistors (MOSFETs) [1], surface passivation in photodetectors and photovoltaics, bipolar resistive random access memory (RRAM) [2] and radio frequency switches [3]. As the quality of the silicon interface critically influences the performance of such devices, a thin interfacial SiO_2 layer is usually grown between metal oxide and silicon. In order to understand the physical origin of the interface traps and optimize the deposition technique of the stacks, we further investigate the properties of the interface traps between thin dielectric Al_2O_3/SiO_2 stacks on silicon substrate in the present work. With the conductance method, we extract the trap density, their energy level distribution in the Si bandgap and thus optimize the stack quality.

2. Experiment details

Fig. 1 is the schematic cross-section of a MOS capacitor with the Al_2O_3/SiO_2 stack. The equivalent circuit of the MOS capacitor is inset in the figure. We use a non-destructive 907 μm-diameter Hg probe as gate contact. Here, R_s is the series resistance of the Si substrate. C_{ox} is the capacitance of the dielectric stack. G_p and C_p are the parallel equivalent conductance and capacitance, respectively, corresponding to the Si top interface.

The preparation of the MOS capacitors is as follows: 3-inch Si wafers ($\langle 1\,0\,0\rangle$, *p*-type, 10 Ω·cm, single-side polished) were cleaned by Piranha solution (H_2SO_4/H_2O_2 3:1) at 110 °C for 20 min. After the Piranha cleaning, all the wafers were dipped by HF/deionized water (1:50) solution for removing the native oxide on the Si surfaces. Then the Si wafers were immediately put into Koyo thermal system for forming thermal SiO_2 or Fiji F200 ALD machine for depositing SiO_2 and Al_2O_3. The thicknesses of the various dielectric layers were mapped by Ellipsometer over whole the wafers. By using E-gun evaporation, 300-nm-thick Al was deposited on the backside of the Si wafers as the back electrode of the MOS capacitor. Finally, all the wafers were annealed in forming gas (N_2/H_2 9:1) at 432 °C for 30 min. We prepared four kinds of gate dielectric stacks in this work. Table 1 lists the compositions of four stacks and the related thicknesses of different dielectric layers.

Mercury Probe Station was used as the front electrode of the MOS capacitor. The electrical measurements were carried out under dark by LCR 4284 m with the frequency range from 1 kHz to 1 MHz.

3. Results and discussion

Fig. 2a shows the measured C-V curves with for frequencies from 1 kHz to 1 MHz for sample 1 (sample 2 features similar response). Large and weaker frequency dispersion are observed, respectively, in accumulation and in depletion region. Moreover, a "bump" appears in the lower-frequency C-V curves ($f < 100$ kHz). Besides, one can see the frequency-dependent flatband shift, which prevents the correct flatband voltage (V_{fb}) extraction. Using the model proposed in [4], corrected

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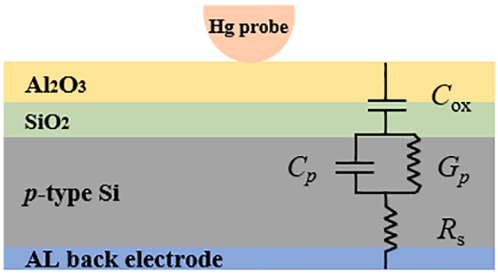

Fig. 1. Schematic cross-section of MOS capacitor with the Al_2O_3/SiO_2 stack. The inset shows the equivalent circuit of the MOS capacitor.

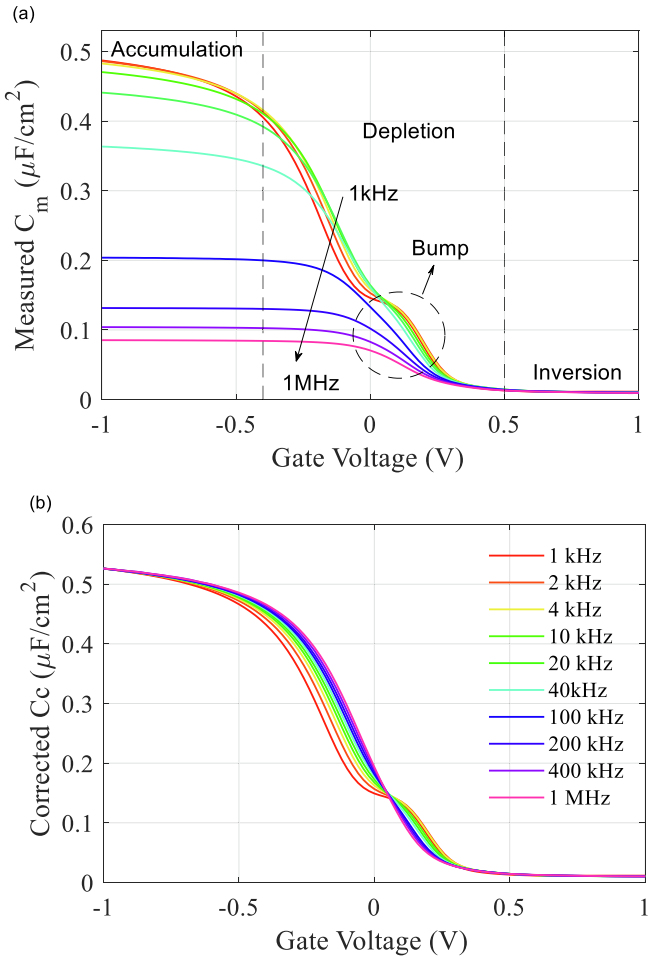

Fig. 2. (a) Measured capacitance versus gate voltage from 1 kHz to 1 MHz for sample 1 and (b) Corrected capacitance versus gate voltage after removing series resistance for the same sample.

capacitance and conductance, C_c and G_c, can be calculated in order to withdraw the effect of series resistance (R_s in Fig. 1). The corrected C-V curves are plotted in Fig. 2b. In Table 1, V_{fb} is then calculated by the second derivative technique [5], summarized in Table 1. In the accumulation region, the frequency dispersion caused by R_s is eliminated. However, the "bump" and frequency-dependent flatband shift still exist. The "bump" is a sign of the interface trap presence. The frequency-dependent flatband shift is related to high interface trap density (D_{it}), which results in the Fermi-level pinning [6] when $qD_{it} \approx C_{ox}$ (the capacitance of the dielectric stack in Fig. 1). In other words, when $qD_{it} > C_{ox}$, the flatband voltage shifts with frequency. To make a comparison with C_{ox}, we calculate D_{it} in the following discussion.

Fig. 3a shows the G_c/ω (V) curves, where G_c is the corrected

Table 1
Summary of interface trap densities for Four gate dielectric stacks, including compositions, Target, Measured, and Equivalent Oxide Thicknesses.

Sample number	Dielectric stack	Target thickness (nm)	Measured thickness (nm) *	EOT (nm)**	V_{fb} (V)	D_{it} ($cm^{-2}eV^{-1}$)
1	PE-ALD Al_2O_3/PE-ALD SiO_2	3.5/2	3.7 ± 0.2/ 2.5	4.1	− 0.06	6.37×10^{11}
2	T-ALD Al_2O_3/PE-ALD SiO_2	3.5/2	3.5 ± 0.2/ 2.5	4.0	+ 0.31	5.87×10^{11}
3	PE-ALD Al_2O_3/ thermal SiO_2	3.5/2	2.8 ± 0.1/ 2.5	3.7	+ 0.61	5.20×10^{10}
4	T-ALD Al_2O_3/ thermal SiO_2	3.5/2	3.2 ± 0.2/ 2.5	3.9	+ 0.69	6.21×10^{10}

*Measured thickness is the average value of 16 points on one sample.
**By using the measured thickness of each layer and theoretical permittivity, Equivalent Oxide Thickness (EOT) is calculated by: $t_{EOT} = t_{SiO_2} + (k_{SiO_2}/k_{Al_2O_3})t_{Al_2O_3}$.

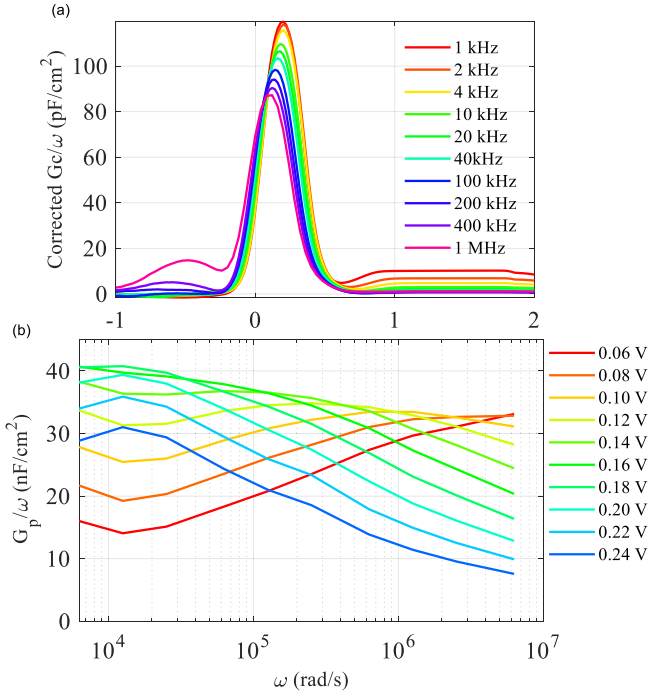

Fig. 3. (a) Corrected G_c/ω (V) curves after withdrawing series resistance from 1 kHz to 1 MHz for sample 1. (b) Parallel equivalent conductance (G_p/ω) as a function of angular frequency (ω) at different response gate voltages in depletion region for sample 1.

conductance of the MOS capacitor after removing R_s. The peak positions of the G_c/ω (V) curves shift to low voltage values with increasing frequency due to the presence of interface trap states. Moreover, the peak amplitude decreases with increasing frequency. Therefore, we obtain the interface trap response for a gate voltage range from 0.06 to 0.24 V, under the related frequencies of Fig. 3a. In order to accurately estimate the interface trap density and calculate the correct time constant [7], we further withdraw the capacitance of the dielectric stack (C_{ox}). Fig. 3b presents the G_p/ω (ω) curves, where ω is the angular frequency ($2\pi f$) and G_p is the parallel equivalent conductance in Fig. 1. The full width at half

maximum (FWHM) of G_p/ω (ω) curves are broader than that of Gaussian function with single level trap state. This implies that a large dispersion exists in the time constant of the interface trap and the interface trap states distribute at different energy levels in the Si bandgap. The quantitative relationship between G_p/ω and D_{it} is given by Eq. (1) [8], where τ is the time constant of the interface trap and q is electron charge.

$$\frac{G_p}{\omega} = \frac{qD_{it}}{2\omega\tau} ln\left(1 + (\omega\tau)^2\right) \quad (1)$$

For a given response gate voltage, G_p/ω reaches the maximum value when $\omega\tau = 1.98$. Therefore, the interface trap density (D_{it}) can be approximately calculated through Eq. (2) [9]:

$$D_{it} \approx \frac{2.49}{q}\left(\frac{G_p}{\omega}\right)_{max} \quad (2)$$

We extract the maximum D_{it} from the green curve in Fig. 3b, where $(G_p/\omega)_{max} = 40.7$ nF/cm^2, $V = 0.18$ V and f ($\omega/2\pi$) $= 2$ kHz. The calculated qD_{it} of 1.02×10^{-7}F/cm^2 has the same order of magnitude as C_{ox} (5.25×10^{-7}F/cm^2). This results in the weak Fermi-level pinning and therefore, the frequency-dependent shifts appearing in sample 1.

According to the Shockley-Read-Hall statistics of the capture and emission rate [10], the time constant of the interface trap (τ) depends on the energy difference ($\Delta E = E_T - E_v$) between the trap energy level (E_T) and the top of the Si valence band (E_v) in p-type Si as below [11]:

$$\tau = \frac{1}{\omega} = \frac{exp(\Delta E/kT)}{\sigma v_t N_V} \quad (3)$$

where σ is the capture cross section of the trap 2.84×10^{-15} cm^{-2}, v_t is the average thermal velocity of majority carriers, N_V is the effective density of state in valence band, k is Boltzman constant and T is room temperature. For an angular frequency ω responding to $(G_p/\omega)_{max}$ in Fig. 3b, a ΔE can be calculated through Eq. (3). By combining Eqs. (2) and (3), we obtain the D_{it} ($\Delta E = E_T - E_v$) profile that is plotted in Fig. 4. It can be found that at room temperature, the trap energy states distribute in the band from 0.315 to 0.352 eV above the top of the Si valence band. Moreover, the maximal trap densities of 6.37×10^{11} cm^{-2}eV^{-1} and 4.09×10^{11} cm^{-2}eV^{-1} for sample 1 and 2, respectively, appear at the energy level of 0.339 eV and 0.334 eV.

High interface trap density leads to the decrease of the carrier mobility in the transistors' channel [4] and rapture of the conductive filament in the resistive switching memory [11]. In order to reduce the interface trap density, the difference of the interface trap properties at the interface between gate stack Al_2O_3/SiO_2 and Si according to the fabrication methods was compared. In the case of Al_2O_3 directly deposited on Si, the lattice mismatch causes the interface traps, and thus an interfacial SiO_2 capable of reducing the mismatch and improve interface characteristics. We compared two kinds of technologies for forming ultrathin SiO_2 layer sandwiched Al_2O_3 and the Si substrate. One is thermal oxidation and the other is the plasma enhanced atomic layer deposition (PE-ALD). For sample 3 and 4 in Table 1, the Si wafers were put into Koyo thermal system for forming thermal SiO_2 layer of 2 nm at 900 °C in an ultra-dry oxygen atmosphere. Fig. 5 demonstrates the measured C-V curves for sample 3 (sample 4 presents the similar C-V curves). It is obvious that in the depletion region, the "bump" does not appear and the frequency dispersion is strongly reduced. These are attributed to low D_{it} value. Indeed, in Table 1, samples 3 and 4 have the D_{it} values of about 5×10^{10} cm^{-2}eV^{-1} which are an order of magnitude lower than that of samples 1 and 2. The results are consistent with earlier research [4]. They suggest that in the case of PE-ALD SiO_2 (as in the samples 1, 2) the surfaces of the Si wafers may be damaged by the plasma in the pretreat step of PE-ALD. Contrarily, in the case of thermal SiO_2 (as in samples 3 and 4), D_{it} value is low thanks to good bonding properties of the thermal SiO_2 formed by oxidizing the Si substrate. A positive V_{fb} value can now be extracted corresponding to a negative value of oxide charges in Al_2O_3 films [12]. This could make possible the reduction of doping in nMOSFETs while maintaining the threshold voltage [1].

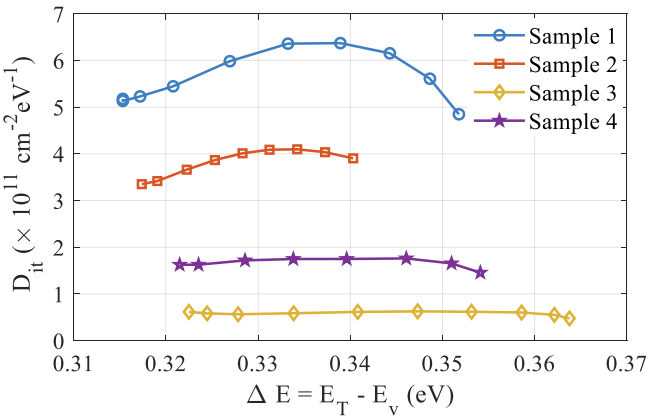

Fig. 4. D_{it} ($\Delta E = E_T$-E_v) profile of sample 1 and 2 calculated by combining Eqs. (2) and (3) in the text, showing D_{it} distributes in the energy band of the Si.

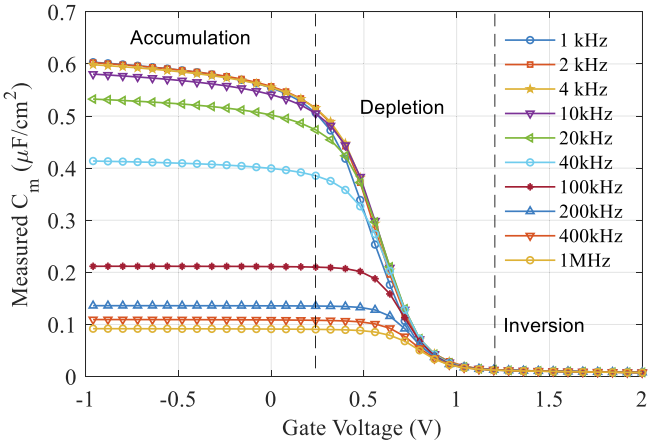

Fig. 5. Measured capacitance versus gate voltage from 1 kHz to 1 MHz for sample 3, without the "bump" and significant frequency dispersion in depletion region.

4. Conclusions

Summarizing, the high quality SiO_2 layer plays an important role in the thin Al_2O_3/SiO_2 stacks on Si substrates. Using conductance method, we accurately extract the interface traps for four thin Al_2O_3/SiO_2 stacks fabricated using different fabrication processes. Our results reveal that the optimized synthesis technology of the SiO_2 layer allows to reduce the interface trap density for an order of magnitude. This could improve the final performance of nano-scaled transistors and resistive switching memory, such as increasing the carrier mobility, decreasing the gate current leakage and the nonlinearity of resistive switching characteristics [13].

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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