Characterization of LPCVD Polycrystalline Silicon Trap-Rich Based Substrates for RF Applications

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A category of engineered Silicon-on-Insulator (SOI) substrates suitable for radio-frequency (RF) applications relies on the introduction of a trap-rich (TR) polycrystalline silicon (polySi) layer to prevent the formation of a parasitic surface conduction (PSC) sheet beneath the buried oxide (BOX), detrimental for RF performances (Figure 1) [1], [2]. Figures of merit (FoM) for such applications are insertion loss, linearity and crosstalk. The substrate's contribution to those FoM can be related to the effective resistivity ρ_{eff} [3] and the second harmonic power H2 [4] measured on coplanar waveguide (CPW) line structures (inset of Figure 2(a)). Though this measurement provides a way to assess the substrate suitability for RF applications, it does not give direct information about introduced traps; whose properties are difficult to characterize due to the combination of high resistivity and large trap density. In the TR layer Fermi-level pinning occurs, preventing the use of capacitive measurement techniques.

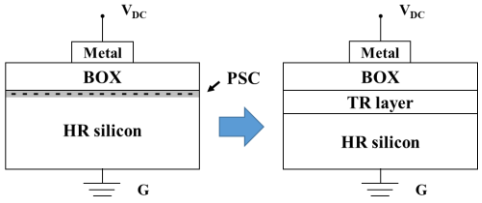

Figure 1 – Impact of the TR layer on the RF substrate for the suppression of the PSC layer, detrimental for RF applications. In that case, the PSC is represented by a conductive layer of electrons. But it can be made of holes instead depending on V_{DC}, the fixed oxide charges and so on. For each structure, the metal depicts the circuit fabricated on the engineered SOI wafer. The base substrate is a high resistivity (HR) silicon ($\rho > 1$ kΩ.cm).

For this study, we associated both RF and trap characterization. Because of the mentioned difficulties, deep level transient spectroscopy (DLTS) [5] is not suitable to characterize such substrates. Instead, we used a variant of this technique called photo-induced current transient spectroscopy (PICTS) [6]. In this method, free carriers are provided by sample illumination. A transient current, due to thermal de-trapping after light extinction, was measured between t_0 and T_w. The time t_0 is the cut-off time of the first part of the transient while T_w is the period in which the transient is measured. The signal was then processed to obtain, over a temperature range, a spectrum depending on the trap energy levels and capture cross-sections. Three RF substrates (called structures A, B and C) were fabricated to study both the impact of the introduction of a TR layer and the impact of the substrate anneal. Structure A is a high-resistivity (HR) silicon wafer. For structures B and C, 1.65 µm of undoped polySi was deposited by low-pressure chemical vapor deposition (LPCVD) of silane, on HR substrates. For each structure, the HR silicon is p-type and has a resistivity of 3-8 kΩ.cm. Finally, structure C undergoes an anneal of 900°C during 2 hours in N_2 ambient. For RF measurement, a 400 nm-thick SiO_2 film was deposited by plasma-enhanced chemical vapor deposition (PECVD), using tetraethoxysilane (TEOS) as a precursor, to provide electrical insulation between the studied structure and the deposited CPW lines. Concerning PICTS measurements, Schottky barrier

diodes were fabricated by the evaporation of semi-transparent Ti metal on the top of the studied structures (inset of Figure 2(b)).

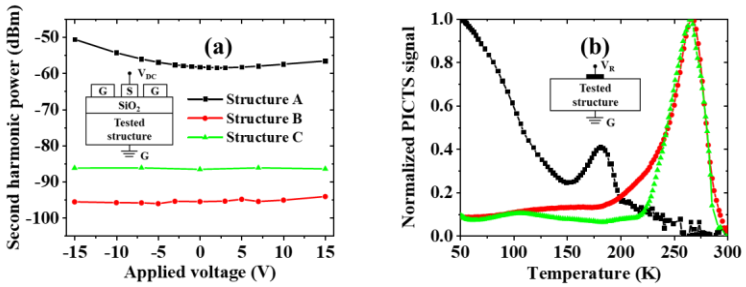

Figure 2 – Measured second harmonic power H2 as a function of V_{DC} (a) on structures A, B and C (described in the text). Measured PICTS spectra (b) on structures A, B and C for λ = 940 nm, V_R = 10 V, t_0 = 5 ms and T_w = 100 ms. Each spectrum was measured for saturation conditions. For clarity, the PICTS signal was normalized to its maximum value. Tested structured for each measurement was depicted in the inset of each figure.

H2 measurements as a function of applied bias V_{DC} were performed on structures A, B and C. Obtained results are shown in Figure 2(a). It can be noticed that the presence of the TR layer allows a reduction of the second harmonic power by 35 dB while the substrate anneal increases it by 10 dB. Level of harmonics for structure A is higher because of the formation of the PSC layer, making the semiconductor surface highly conductive. In the case of structures B and C, it can be noticed that H2 is nearly independent on applied voltage V_{DC}. This is due to Fermi level pinning preventing band curvature at the surface of the semiconductor and formation of the PSC layer (see Figure 1). PICTS spectra, measured at saturation conditions on structures A, B and C, are shown in Figure 2(b) for an illumination wavelength λ of 940 nm and a reverse voltage V_R of 10 V. For structure A (HR substrate), the signal decreases as a function of T and a peak is located at 180 K. Concerning structures B and C, the dominant part of the spectrum is present near ambient temperature with a peak lying at 270 K. The effect of the anneal was the reduction of the normalized PICTS signal intensity between 100 and 225 K. By studying the PICTS spectrum under several conditions, such as the illumination wavelength λ or the filling pulse t_p, we were able to see that the signal detected in structure A originates from the surface, likely interface states between the deposited metal and the semiconductor. Concerning the peak observed in structure B and C, its variation with λ shows us that it is present in the volume, has an activation energy of 0.45 eV and captures preferentially electrons. We associated it with the presence of the polySi layer. Moreover, by performing complementary secondary ion mass spectroscopy (SIMS) and scanning resistance profiling (SRP) measurement we were able to highlight the presence of boron contamination inside polySi for structure C, partly responsible for the 10 dB increase of H2.

To conclude, we highlight two important parameters for the understanding of TR RF properties: information on introduced traps (density and signature) and contamination level. PICTS allows us to bring information about the first one. However, for a more complete comprehension of the TR layer, it has to be associated with techniques giving complementary information about introduced contamination (SIMS, SRP, …).

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