



UNIVERSITÉ CATHOLIQUE DE LOUVAIN
ECOLE POLYTECHNIQUE DE LOUVAIN
ICTEAM INSTITUTE

High-Performance Ultra-Low-Voltage Digital and RF Circuits based on Adaptive Forward Back Biasing in 28nm FDSOI CMOS

Guerric de Streel

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Dissertation committee:

Prof. David Bol (ICTEAM Institute, UCL), advisor
Prof. Denis Flandre (ICTEAM Institute, UCL),
Prof. Catherine Dehollain (EPFL, Lausanne),
Dr. HDR Andreia Cathelin (STMicroelectronics, Crolles),
Dr. Jan Craninckx (Imec, Heverlee),
Prof. Christophe De Vleeschouwer (ICTEAM Institute, UCL), President

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HIGH-PERFORMANCE ULTRA-LOW-VOLTAGE DIGITAL AND RF CIRCUITS BASED ON ADAPTIVE FORWARD BACK BIASING IN 28NM FDSOI CMOS

Guerric de Streef
Ecole Polytechnique de Louvain
ICTEAM Institute



Université catholique de Louvain
Louvain-la-Neuve (Belgium)

À mes parents

CONTENTS

Acknowledgments	xi
Abstract	xiii
Acronyms	xvii
List of notations	xix
Author's publication list	xxiii
1 Introduction	1
1.1 Dealing with the IoT sustainability challenges: a circuit design point-of-view	4
1.2 Dealing with the IoT sustainability challenges: a technology scaling and FDSOI point-of-view	5
1.3 Thesis objectives	6
1.4 Thesis outline	7
2 Back biasing potential in 28nm FDSOI for pushing ULV logic circuits in the high-performance domain	11
2.1 Introduction	13
2.2 Back biasing analysis at device level	16
2.3 Back biasing analysis at gate level	19
2.3.1 Scaling and back biasing impact on frequency and energy efficiency	20
2.3.2 Delay equalization and back biasing compensation schemes	25
2.3.3 Impact of back biasing compensation schemes on minimum energy point	30
2.3.4 Impact of back biasing compensation schemes on robustness	33
2.4 Back biasing analysis at standard cell library level	36
2.5 Back biasing analysis at IP level	38
	vii

2.6	Discussion	41
2.7	Conclusion	42
3	Back biasing potential in 28nm FDSOI for pushing wideband analog/RF circuits in the ULV domain	49
3.1	Introduction	51
3.2	Moderate inversion biased devices for RF	53
3.2.1	Impact of voltage scaling	53
3.2.2	Impact of technology scaling	55
3.2.3	Impact of FBB	58
3.3	Efficient sizing methodology for noise-cancelling Low Noise Amplifiers	60
3.4	Impact on wideband noise-cancelling LNA design	64
3.4.1	Impact of technology scaling	64
3.4.2	Impact of voltage scaling	66
3.4.3	Impact of back biasing	66
3.5	Discussion & Conclusions	67
4	SleepTalker: an ULV UWB TX SoC featuring adaptive-FBB-based channel selection	77
4.1	Introduction	79
4.2	Architecture of the duty-cycled PLL-free TX system	81
4.3	Design and implementation of the TX	83
4.3.1	Duty-cycled frequency synthesis	83
4.3.2	Pulse Shaping Power Amplifier	88
4.3.3	ULV High-Speed Digital Implementation	93
4.4	SoC integration	96
4.4.1	DC/DC Converter	96
4.4.2	+1.8V/−1.8V On-Chip Generation	98
4.4.3	Forward Back Biasing Generator	99
4.4.4	Physical Implementation	100
4.5	Experimental Validation	101
4.5.1	Experimental Setup	103
4.5.2	Back-Biasing Generation	104
4.5.3	Carrier Frequency Tuning with Adaptive FBB	106
4.5.4	TX Performances	106
4.5.5	Comparison to the State-of-the-Art	109
4.6	Conclusion	110

Conclusions and perspectives	115
O.6.1 How does FDSOI with its back biasing capability influence the energy/speed tradeoff in ULV digital circuits?	115
O.6.2 How does FDSOI with its back biasing capability influence the power/performances in analog/RF circuits?	117
O.6.3 How can the back biasing capability be used to design ULV radios while meeting the specifications of communication standard	118
Appendix A: Wideband LNA small signal model	121

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ABSTRACT

The deployment of the Internet-of-Things ubiquitous sensing paradigm is constrained by the development of the four functions usually embedded in a wireless sensor node:

- **Power management**, targeting efficient energy harvesting from the environment, conversion and storage.
- **Sensing**, with an emphasis on versatility, energy efficiency and accuracy depending on the targeted application.
- **Data processing**, such as feature extraction or compression, to limit the amount of data to communicate wirelessly.
- **RF communication**, to transmit sensed and processed data to the cloud with high data-rate and low energy per bit.

In this work, we explore the design of high-performance ultra-low-voltage (ULV) circuits for both the data processing and the RF communication function with a common objective: the improvement of the energy/performance trade-off. To improve this tradeoff, we rely on innovative digital and analog/RF circuits and systems design as well as on the exploitation of 28nm FDSOI CMOS process. In the last few years, FDSOI technology has emerged as an industrially-proven solution to overcome the limitations of bulk technologies and continue the trend of Moore's law. In addition to a lower cost compared to FinFet solutions, FDSOI can provide both high-speed or low-leakage solution and is thus an interesting candidate for the implementation of highly-efficient ultra-low-power circuits. Its performances rely on a better electrostatic control of the channel, lower variability, lower parasitic capacitances, lower leakage, steeper subthreshold slope and wide back-biasing range compared to the body-bias range in bulk technology. Among these characteristics, the capability to apply an overdrive back bias voltage above the supply voltage is a key feature of this dissertation. We intend to look at the usefulness of forward back biasing in the design of high performance circuits related to the data processing and RF functionalities of a typical wireless sensor node by looking at three questions:

- How does FDSOI with its back biasing capability influence the energy/speed tradeoff in ULV digital circuits?
- How does FDSOI with its back biasing capability influence the power/performances in analog/RF circuits?
- How can the back biasing capability be used to design ULV radios while meeting the specifications of communication standard?

As a first step, we study of the impact of back biasing on ultra-low-voltage logic by looking at the evolution of the minimum energy point for several innovative back biasing schemes from gate level to IP level. We show that overdrive forward back biasing helps to extend the design space to higher frequency of operation while keeping minimum energy. Asymmetric adaptive back biasing is presented as a way to mitigate the effect of systematic NMOS/PMOS mismatch on minimum energy point and robustness. At IP level, we prove that mixing two or three overdrive back biasing voltages can be used to reduce the energy per cycle of microcontroller cores over a wide range of frequency of operation.

As a second step, we study the performances of 28nm FDSOI with its back biasing capability for analog/RF circuits. A reduction of the supply voltage of RF analog circuits, to ensure compatibility with digital parts or to improve the power consumption, strongly challenges the analog/RF design in nanometer CMOS technologies due to the limited voltage headroom. We show that reducing the supply voltage pushes devices from strong inversion to moderate inversion. Forward back biasing can be used to mitigate this trend and increase the design space. We further show the impact of technology scaling on important RF figure of merits to highlight the ability of 28nm FDSOI to trade speed for power. Then, we illustrate this ability at circuit level with one objective: optimizing a wideband low noise amplifier for the hot topic of software-defined radios. We analyze a wideband LNA to show that technology scaling and forward back biasing shift the minimum supply voltage limitation from the bandwidth constraint to the noise constraint.

Finally, we demonstrate the potential of back-biasing in 28nm FDSOI to push digital RF circuits in the ULV domain with a silicon demonstrator: SleepTalker. This chip is an IEEE 802.15.4a ultra-wideband transmitter SoC designed for ultra-low-voltage in 28nm FDSOI CMOS. Operated at 0.55V, it achieves a record energy efficiency of 14pJ/bit with embedded power management, highly duty-cycled digital baseband and programmable pulse shaping for compliance with regulation. A wide-range on-chip adaptive forward back biasing is used for threshold voltage reduction allowing 3.5 to 4.5GHz operation at 0.55V thereby showing that back-biasing can act as an enabler for ultra-low-voltage RF circuits. The forward back biasing is also used for PVT compensation and tuning of both

the carrier frequency and the output power which shows how it can be used as a control knob for RF functionality.

ACRONYMS

ADFBB	Adaptive Differential forward back-biasing
BB	Body- or back-biasing
BBCO	Back-bias-controlled oscillator
BOX	Buried oxide
CG	Common gate
CS	Common source
CMOS	Complementary metal-oxide semiconductor
DFBB	Differential forward back-biasing
DFVS	Dynamic frequency/voltage scaling
DIBL	Drain-induced barrier lowering
DoF	Degree of freedom
FBB	Forward body- or back- bias
FD	Fully depleted
FO	Fan out
FOM	Factor of merit
GL	Gate length
GP	General purpose
IADFBB	Inverse Adaptive Differential forward back-biasing
IC	Inversion Coefficient
IoT	Internet-of-Things
LNA	Low noise amplifier
LO	Local oscillator
LP	Low power
LVT	Low Threshold Voltage
MEP	Minimum energy point
MOSFET	Metal-oxide semiconductor field effect transistor
NM	Noise margin

NMOS	N-type MOSFET
PA	Power amplifier
PG	Power gating
PMOS	P-type MOSFET
PVT	Process voltage temperature
RBB	Reverse body- or back- bias
RDF	Random dopant fluctuation
RVT	Regular Threshold Voltage
SDR	Software defined radio
SNM	Static noise margin
SoC	System-on-chip
SOI	Silicon on insulator
TSPC	True single phase clock
TX	Transmitter
ULP	Ultra low power
UTBB	Ultra thin body and box
UWB	Ultra-wideband
WSN	Wireless sensor node

LIST OF NOTATIONS

Device-level symbols

γ	Linearized body-effect coefficient	$[mV/V]$
η	Drain-induced-barrier-lowering coefficient	$[mV/V]$
μ_0	Zero-bias mobility	$[m^2/(V.s)]$
σ_{V_t}	Threshold-voltage standard deviation	$[mV]$
C_g	Intrinsic gate capacitance	$[fF/\mu m]$
C_{ox}	Gate-oxide capacitance	$[fF/\mu m^2]$
I_0	Subthreshold reference current	$[A/\mu m]$
I_{gate}	Gate leakage current	$[A/\mu m]$
I_{off}	Off-state drain current	$[A/\mu m]$
I_{on}	On-state drain current	$[A/\mu m]$
I_{sub}	Subthreshold drain current	$[A/\mu m]$
L_{eff}	Effective channel length	$[nm]$
L_g	Gate length (printed unless otherwise specified)	$[nm]$
n	Body-effect factor	$[-]$
S	Subthreshold swing	$[mV/dec]$
U_{th}	Thermal voltage	$[mV]$
V_{bs}	Body-to-source (bulk) or Back-gate-to-source (FDSOI) voltage	$[V]$
V_{ds}	Drain-to-source voltage	$[V]$
V_{gs}	Gate-to-source voltage	$[V]$
V_T	Threshold voltage	$[V]$
V_{T0}	Zero-bias threshold voltage	$[V]$
W	Channel width	$[nm]$

I_{eff}	Effective current	[A]
$\beta_{I_{eff}}$	NMOS/PMOS effective current ratio	[—]
IC	Inversion Coefficient	[—]
g_m	Small-signal transconductance	[S]
g_d	Output conductance	[S]
f_T	Transition frequency	[Hz]
G_n	Channel noise transconductance	[S]
g_m	Device transconductance	[S]

Circuit-level symbols

β_{del}	Rise/fall inverter delay ratio	[—]
C_L	Load capacitance	[fF]
E_{dyn}	Dynamic energy per operation	[J]
E_{cycle}	Energy per operation	[J]
E_{leak}	Leakage energy per operation	[J]
f_{clk}	Clock frequency	[Hz]
F_{SNM}	Static-noise-margin factor	[—]
I_{leak}	Circuit leakage current	[A]
P_{dyn}	Dynamic power consumption	[W]
P_{leak}	Static power consumption	[W]
T_{del}	Critical-path delay	[s]
V_{BB}	Back-bias voltage	[V]
V_{FBB}	Forward back-bias voltage	[V]
V_{RBB}	Reverse back-bias voltage	[V]
V_{dd}	Supply voltage	[V]
E_{MEP}	Minimum energy per operation	[J]
f_{MEP}	Clock frequency of minimum-energy point	[Hz]
V_{MEP}	Supply voltage of minimum-energy point	[V]

η_{gate}	Gate yield	$[-]$
η_{die}	Die yield	$[-]$
F	Noise figure	$[-]$
NF	Noise factor	$[-]$
G_M	Circuit/block transconductance	$[S]$

AUTHOR'S PUBLICATION LIST

Related journal papers

- JP1. G. de Streel and D. Bol, "Study of back biasing schemes for ULV logic from the gate level to the IP level", in *Journal of Low Power Electronics and Applications*, vol. 4, no. 3, pp. 168-187, Jul. 2014.
- JP2. G. de Streel, C. Dehollain and D. Bol, "Improving Efficiency of Wideband Noise-Cancelling LNAs through Technology Scaling and Moderate Inversion for ULV RF circuits", in *IEEE Transactions on Circuits and Systems II (TCASII)*, in review, 5p.
- JP3. G. de Streel, F. Stas, T. Gurne, F. Durant, C. Frenkel and D. Bol, "SleepTalker: a 28nm FDSOI ULV 802.15.4a IR-UWB Transmitter SoC achieving 14pJ/bit at 27Mb/s with Adaptive-FBB-Based Channel Selection and Programmable Pulse Shape", in *IEEE Journal of Solid State Circuits (JSSC)*, in review, 12p.

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- CP1. G. de Streel and D. Bol, "Impact of back gate biasing schemes on energy and robustness of ULV logic in 28nm UTBB FDSOI technology", in *IEEE International Symposium on Low Power Electronics and Devices (ISLPED)*, pp. 255-260, 2013.
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- CP3. G. de Streel, D. Flandre, C. Dehollain and D. Bolt, "Towards Ultra-Low-Voltage Wideband Noise-Cancelling LNAs in 28nm FDSOI", in *IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference*, pp. 1-2, 2015.

- CP4. G. de Streel, F. Stas, T. Gurne, F. Durant, C. Frenkel and D. Bol, "SleepTalker: a 28nm FDSOI ULV 802.15.4a IR-UWB Transmitter SoC achieving 14pJ/bit at 27Mb/s with Adaptive-FBB-based Channel Selection and Programmable Pulse Shape", in *IEEE International Symposium on Very Large Scale Integration (VLSI)*, pp. 1-2, 2016.

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- ICK1. D. Bol, J. De Vos, F. Botman, G. de Streel, S. Bernard, D. Flandre and J.-D. Legat, "Green SoCs for a sustainable Internet-of-Things", in *IEEE Faible Tension Faible Consommation (FTFC)*, pp. 1-4, 2013.
- ICK2. D. Bol, G. de Streel and D. Flandre, "Can we connect trillions of IoT sensors in a sustainable way? A technology/circuit perspective", in *IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference*, pp. 1-3, 2015.

Unrelated journal papers

- UJP1. N. Couniot, G. de Streel, F. Botman, A. Kuti Lusala, D. Flandre and D. Bol, "A 65-nm 0.5-V DPS CMOS Image Sensor with 17-pJ/frame.pixel and 42-dB Dynamic Range for Ultra-Low-Power SoCs", in *IEEE Journal of Solid State Circuits (JSSC)*, vol. 50, pp. 2419-2429, 2015.
- UJP2. A.S.N. Pereira, G. de Streel, N. Planes, M. Haond, R. Giacomini, D. Flandre and V. Kilchytska, "An in-depth Analysis of Temperature Effect on DIBL in UTBB FD SOI MOSFETs Based on Experimental Data, Numerical Simulations and Analytical Models", in *Solid State Electronics*, in review, 15p.

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- UCP1. G. de Streel, D. Bol and J.-D. Legat, "Multi-VT ultra-low-power FPGA implementation in 65nm CMOS technology", in *IEEE Faible Tension Faible Consommation (FTFC)*, pp. 1-4, 2012.
- UCP2. G. de Streel, J. De Vos, D. Flandre and D. Bol, "A 65nm 1V to 0.5V linear regulator with ultra-low quiescent current for mixed-signal ULV SoCs", in *IEEE Faible Tension Faible Consommation (FTFC)*, pp. 1-4, 2014. Awarded "Best Student IC Design Paper".
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- achieving 40-dB dynamic range”, in *IEEE International Symposium on Very Large Scale Integration (VLSI)*, 2p., 2014.
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- UCP6. A.S.N. Pereira, G. de Streel, N. Planes, M. Haond, R. Giacomini, D. Flandre and V. Kilchytska, “Analysis and Modelling of Temperature Effect on DIBL in UTBB FD SOI MOSFETs”, in *Joint International EUROSIOI Workshop and International Conference on Ultimate Integration on Silicon*, 2p., 2016.
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- UCP8. F. Stas, G. de Streel and D. Bol, “Sizing and Layout Integrated Methodology for 28nm Analog Circuits Using Digital PnR Tools”, in *IEEE Northeast Workshop on Circuits and Systems (NEWCAS)*, 4p., 2016.
- UCP9. T. Haine, F. Stas, G. de Streel, C. Gimeno Gasca, D. Flandre and D. Bol, “CAMEL: An Ultra-Low-Power VGA CMOS Imager based on a Time-Based DPS Array”, in *ACM International Conference on Distributed Smart Cameras*, 6p, 2016.
- UCP10. C. Gimeno Gasca, F. Stas, G. de Streel, D. Bol and D. Flandre, “A Wide-band Inductorless LNA Topology with Improved Noise and Linearity for 10-GHz Software-Defined Radios”, in *IEEE Transactions on Circuits and Systems I (TCASI)*, in review, 5p.

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- WP1. G. de Streel and D. Bol, “Study of Back Biasing Schemes for ULV Logic from Gate Level to IP Level”, in *Workshop on Energy Efficient Electronics and Applications*, Lausanne, 2013.
- WP2. G. de Streel and D. Bol, “Opportunities of 28nm FDSOI for ultra-low-voltage SoCs towards a sustainable Internet-of-Things”, in *LetiWorkshop FDSOICE*, Grenoble, 2015.

There is more to life than increasing its speed.

Mahatma Gandhi

CHAPTER 1

INTRODUCTION

INTRODUCTION

In the past decade, driven by the market's ever-growing demand for smartphones and tablets, the number of connected devices exploded to reach a startling number of 7.9 billions according to Cisco [1]. Following this growth, the global mobile data traffic increased by $4000\times$ in the past 10 years featuring a record cumulative aggregated growth rate of 74% in 2015 [1]. One of the key driver behind this trend is the sensor ubiquity in the mobile market popularizing the access to microphones, accelerometers or gyroscopes for example. These same sensors are predicted to be at the root of the next mobile device expansion with the emergence of sensor-based smart systems that join sensing, computing and communication capabilities [2]. This Internet-of-Things (IoT) vision is indeed aiming at embedding these functionalities inside delocalized physical objects connected to the Internet.

The IoT paradigm has become a hot topic in research during the last few years appearing as a promising solution for several high-profile and global issues such as food-, energy- and water-shortage, increasing cost of healthcare or climate change. Aside from these strong motivations, the IoT also benefits from large and economically-viable market segments such as [2]: smart-cities, -environment, -water, -energy distribution, -logistics, -agriculture, -domotic, -health, ... The rise of the IoT is expected to reach a trillion of Wireless Sensor Nodes (WSNs) distributed in the environment [2] adding to the forecasted 12 billions mobile devices predicted to be connected by 2020 [1]. This expansion is predicted to generate a tremendous pressure on mobile communication infrastructures that will have to sustain a predicted cumulative aggregated growth rate of Machine-to-Machine (M2M) communications as high as 38% up until 2020 [1]. This envisioned rate is even higher than the one of smartphones and phablets which dominates today's mobile communication [1].

But the rise of M2M mobile communications is not the only challenge to be faced in order to enable the pervasiveness of the IoT paradigm. Sustainability in all life-cycle phases is required from economical, societal and environmental points of view.

- **Sustainable maintenance** imposes extremely-low to zero maintenance operation for the WSNs in order to handle the trillions of WSNs.
- **Sustainable operation** implies reducing the overall electrical power consumption including both the nodes and their communication infrastructures (basestations and datacenters).
- **Sustainable production and end-of-life** by achieving low production cost and carbon footprint as well as low eco-toxicity.

An IoT WSN usually embeds four functionalities described in Fig. 1.1 [3].

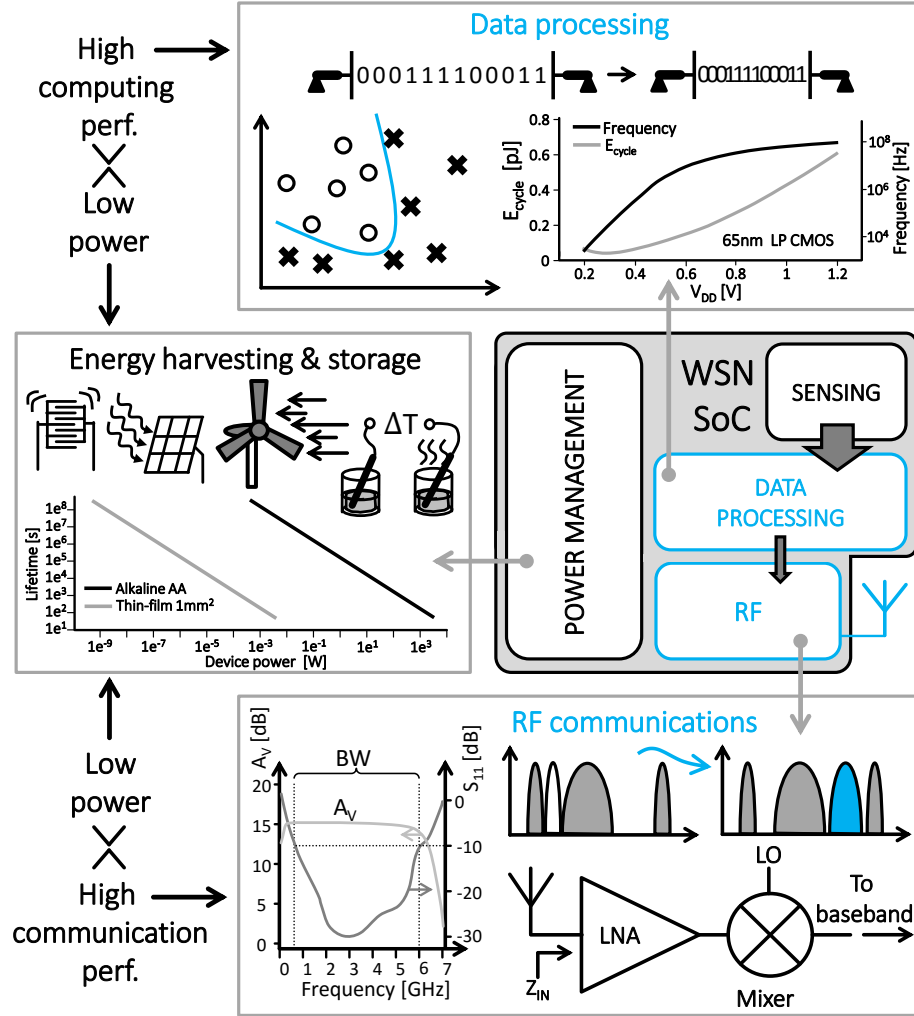


Fig. 1.1. Typical IoT wireless sensor node architecture with highlighted challenges and trade-offs.

On the power management side, sustainability calls for efficient energy-harvesting, conversion and storage in order to avoid the prohibitive maintenance cost of battery replacement with the associated eco-toxicity. Low off-chip component count is also required to limit the production carbon footprint. The typical power density level generated by an energy-harvesting source is around $15\text{mW}/\text{cm}^2$ for outdoor solar cells, $200\mu\text{W}/\text{cm}^3$ for piezoelectric or vibration

harvesters and even below $50\mu W/cm^3$ for thermoelectric [17]. Therefore, energy-harvesting operation imposes an extremely-low power budget, which puts heavy requirements on the sensing, data processing and RF communication functionalities (Fig. 1.1). On the data processing side, embedding high data processing abilities in WSNs to perform data compression, feature extraction or compressive sensing helps reducing the amount of data to communicate wirelessly as illustrated in Fig. 1.1. This is important to control the M2M communication growth and the cost of datacenters and basestations. On the RF communication side, high data-rate, energy-efficiency and connectivity are key targets to help transmitting sensed data to the cloud efficiently. The low-to-zero off-chip component count is also of importance to reduce the bill-of-material and the carbon footprint [5]. The M2M communications growth will lead to spectrum crowding that needs to be dealt with through spectrum agility or cognitive radios [3] as illustrated in Fig. 1.1.

In this work, we focus on the data processing and RF communication functions with the target to achieve high-performances in digital and analog/RF circuits at extremely-low power. In this general introduction, we briefly introduce the key challenges faced and results obtained based on innovations at circuit level and by leveraging the advantages of highly-scaled CMOS technology. We then define the objectives and give the outline of the text.

1.1 DEALING WITH THE IOT SUSTAINABILITY CHALLENGES: A CIRCUIT DESIGN POINT-OF-VIEW

As illustrated in Fig. 1.1, both RF communication and data processing functionalities are bound by strong constraints on power consumption. Circuit design for Ultra-Low-Power (ULP) applications received a strong interest from the research community over the last few years. Near- or subthreshold operation is one of the main research directions showing many interesting results for efficiency improvement through silicon demonstrator packing more and more functionalities every year [18] [22].

It has been proven that the energy-optimal operation of a digital circuit is achieved when the supply voltage is scaled to operate at Ultra-Low-Voltage (ULV) [11] where contributions from static and dynamic power are balanced to reach a minimum energy point and achieve energy savings of up to $10\times$ [15]. Fig. 1.1 illustrates the tradeoff opposing high frequency of operation to low energy per operation.

Analog circuits do not benefit from voltage scaling as evidently as digital ones. Supply voltage reduction has a negative impact on voltage swing, linearity and Signal to Noise Ratio (SNR) [12]. Furthermore, scaling the V_{DD} pushes devices in moderate or weak inversion reducing the f_T . Unfortunately, the designer may

be forced to reduce the supply voltage of analog/RF integrated blocks to keep up with technology-induced V_{DD} scaling, compliance with other digital blocks or to improve the energy-harvesting efficiency by reducing the requirement on output voltage. Threshold voltage is not scaling as fast as V_{DD} in order to maintain the leakage current manageable and this induces strong design constraints due to the shrinking voltage headroom. To alleviate these scaling-related issues, circuit design techniques such as body-input for differential pair, forward body-biasing or topology without device stacking has been proven useful to maintain performances with reduced V_{DD} such as bandwidth, gain or noise [16] as illustrated in Fig. 1.1.

Voltage scaling is a strong focus of this work. In both analog/RF and digital, we leverage the potential of advanced CMOS technology and circuit design techniques to improve the performance versus energy tradeoff critical for the targeted application.

1.2 DEALING WITH THE IOT SUSTAINABILITY CHALLENGES: A TECHNOLOGY SCALING AND FDSOI POINT-OF-VIEW

Technology scaling from the first Texas Instrument Germanium based integrated circuit [6] to Intel's 14nm FinFet CMOS [7] is certainly one of the most impactful industrial trend ever encountered. Moore's law captures the technology scaling impact on the semiconductor industry growth through a famous projection equation stating that the number of transistors per chip roughly doubles every two years [4]. Scaling down the features of classical bulk CMOS strongly impacts several key figures-of-merit from a digital as well as from an analog point-of-view.

Low-power digital circuits benefit from device feature scaling through the gate-length reduction enabling higher clock frequency [8]. Unfortunately, at ULV, the scaling comes at a cost in term of energy required to perform operations [19]. Indeed, channel length reduction increases several drawbacks such as short channel effects, random dopant fluctuation or reduced gate control over the channel leading to higher Drain Induced Barrier Lowering (DIBL) and lower subthreshold slope eventually harming circuit level performances at ULV [21] [20] [19].

Regarding analog/RF figures-of-merit at device level, technology scaling has brought a steady increase in transition frequency f_T at the expense of an intrinsic gain g_m/g_d reduction due to an output conductance increase [9]. The high f_T is an interesting feature for a designer as it can be traded for bias current to achieve the same bandwidth at lower power. Unfortunately, intrinsic gain reduction may force the designer to increase the devices gate length to compensate for short-channel effects and causes a f_T reduction alleviating the very interest of technology scaling [13]. This effect combined with higher device mismatch from random dopant fluctuation due to reduced area, voltage swing reduction and

the increased difficulty to stack devices with the supply voltage scaling renders difficult to confirm the overall advantage of technology scaling for analog/RF circuits.

To counteract these detrimental effects of technology scaling, the semiconductor industry is exploring two new device structures to limit the short-channel effects impact on device factors-of-merit through enhanced electrostatic control of the channel: FinFets and Fully-Depleted Silicon on Insulator (FDSOI) devices. Both of them are already commercially available and are predicted to represent over 50% of the foundry market by 2020 [10]. This work is centred on FDSOI devices and especially on the 28nm CMOS technology from STMicroelectronics which is, to this date, the most advanced commercially available FDSOI technology. This choice is based on the extensive SOI expertise present at UCL as well as the potentially higher performance in terms of leakage mitigation, minimum energy point level and higher speed at ULV that makes FDSOI the better fit for low-cost and ultra-low-power applications (for now and not due to intrinsic structural advantages over FinFet).

The FDSOI technology is based on bulk MOSFET technology keeping the same planar aspect to the opposite of 3D-structures such as FinFet. The devices are manufactured over a thin buried oxide (BOX) isolating it from the substrate with raised source and drain. Ultra-Thin-Body and Box (UTBB) 28nm FDSOI features 8nm of channel thickness which is undoped and hence is fully depleted. This topology presents several advantages: reduced junction capacitance between source or drain and bulk, better electrostatic control of the channel and reduced random dopant fluctuation thanks to the undoped channel. The enhanced electrostatic control of the channel leads to short-channel effect mitigation improving the subthreshold slope and the DIBL. In addition to a lower cost compared to FinFet solutions, FDSOI offers a wide Back-Biasing (BB) range compared to the body bias range in bulk technologies allowing to dynamically modulate the threshold voltage of the transistors.

These advantages may thus be used for implementing high-performance digital and analog/RF circuits.

1.3 THESIS OBJECTIVES

In this work, we explore the design of ultra-low-voltage circuits for both the data processing and RF communication functions of the IoT WSNs with a common objective: the improvement of the energy/performance trade-off. To improve this tradeoff, we rely on innovative digital and analog/RF circuits and systems design as well as on the exploitation of technology scaling as well as FDSOI device structure.

Among these innovations, we make an extensive use of the capability to apply an overdrive back bias voltage in FDSOI above the supply voltage. We specifically raise three research questions:

- How does FDSOI with its back biasing capability influence the energy/speed tradeoff in ULV digital circuits? As already mentioned in Section 1.2, pushing ULV logic toward deeply scaled CMOS technologies comes at the price of an energy penalty that we intend to circumvent in order to achieve high-performance ULV logic. We especially leverage the ultra-wide range of FBB available on FDSOI and quantify the energy saving and robustness improvement that we can achieve through optimal FBB selection and implementation.
- How does FDSOI with its back biasing capability influence the power/performances in analog/RF circuits? Scaling the supply voltage on analog/RF circuits is challenging the ability to operate the devices in strong inversion and thus to fulfil the RF specifications in term of bandwidth, gain or noise. We prove that technology scaling can help achieving high-performance analog/RF circuits at lower supply voltage thanks to an f_T improvement. We also analyze how the designer can trade this improved f_T for power and we propose a concrete case study by designing and optimizing a wideband LNA meeting the specifications of SDR applications.
- How can the back biasing capability be used to design ULV radios while meeting the specifications of communication standard? To demonstrate the findings resulting from the answers of the first question, we chose to design a digital ultra-wideband transmitter compliant with the relevant industrial standard. We push this design in ULV to achieve ultra-low-power and we demonstrate how an extensive use of the FBB is helpful to realize the first fully functional prototype of ULV RF transmitter.

1.4 THESIS OUTLINE

Each chapter of this work targets one of the questions stated in the previous section. Amongst them, Chapter 4 has a special status as it further serves as a general demonstrator of the back biasing potential for ULV design at high speed by covering functionality tuning and PVT compensation.

Chapter 2

We first present a study the impact of back biasing on ultra-low-voltage logic by looking at the evolution of the minimum energy point for several innovative

back biasing schemes from gate level to IP level. We show that forward back biasing can help extending the design space to higher frequency of operation while keeping minimum energy. Asymmetric adaptive back biasing is presented as a way to mitigate the effect of systematic mismatch on minimum energy point and robustness. At IP level, we show that mixing two or three overdrive back biasing voltages can be used to reduce the energy per cycle of microcontroller cores over a wide range of frequency of operation.

Chapter 3

Software-defined and reconfigurable radio design is a hot topic in RF research because of its potential to act as an enabler for cognitive communications but requires wideband RF front-end. To tackle the design of a wideband receiver for the IoT, we target two concurrent objectives: low noise figure and low power consumption. We show that reducing the supply voltage pushes devices from strong inversion to moderate inversion. Forward back biasing can be used to mitigate this trend and increase the design space. We also study the impact of technology scaling on important RF figures of merit to highlight the ability of 28nm FDSOI to trade speed for power. Then, we illustrate this ability at circuit level by looking at the optimum sizing of an ultra-low-voltage noise-cancelling wideband LNA. For this LNA, we show that technology scaling and forward back biasing shift the minimum supply voltage limitation from the bandwidth constraint to the noise constraint. Furthermore, we prove that moderate forward back biasing helps improving the power consumption under the noise and bandwidth constraints.

Chapter 4

In the last chapter of this dissertation, we demonstrate the potential of back biasing to push digital RF circuits in the ULV domain with a silicon demonstrator: SleepTalker. This chip is an IEEE 802.15.4a ultra-wideband transmitter SoC designed for ultra-low-voltage operation in 28nm FDSOI CMOS. Operated at 0.55V, it achieves a record energy efficiency of 14pJ/bit with embedded power management, highly duty-cycled digital baseband and programmable pulse shaping for compliance with regulation. A wide-range on-chip adaptive overdrive back biasing is used for threshold voltage reduction allowing 3.5 to 4.5GHz operations at 0.55V thereby showing that back-biasing can act as an enabler for the ultra-low-voltage RF circuit. The forward back biasing is also used for PVT compensation and tuning of both the carrier frequency and the output power which shows how it can be used as a control knob for RF functionality.

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CHAPTER 2

BACK BIASING POTENTIAL IN 28NM FDSOI FOR PUSHING ULV LOGIC CIRCUITS IN THE HIGH-PERFORMANCE DOMAIN

Abstract

Minimum energy per operation is typically achieved at Ultra-Low Voltage (ULV) where low speed and low robustness are two challenging issues. This chapter studies the impact of Back Biasing (BB) schemes on these features for FDSOI technology at three levels of abstraction: gate, library and IP. We show that Forward BB (FBB) can help cover a wider design space while operating in Ultra-Low-Voltage (ULV) in terms of optimal frequency of operation while maintaining the energy per operation at a minimum point. Asymmetric BB between NMOS and PMOS can mitigate the effect of systematic mismatch on Minimum Energy Point (MEP) and robustness. With optimal asymmetric BB, we achieve either a MEP reduction of up to 18% or a $36\times$ speed-up at the MEP. At IP level, we confirm the MEP reconfigurability through BB with synthesis results of microcontrollers at $0.35V$. We show that the use of a mix of overdrive FBB voltages further improves the energy efficiency. Compared to bulk $65nm$ CMOS, we are able to reduce the energy per cycle by 64% or increase the frequency of operation by $7\times$ while maintaining energy per operation below $3\mu W/MHz$ over a wide frequency range.

Contents

2.1	Introduction	13
2.2	Back biasing analysis at device level	16
2.3	Back biasing analysis at gate level	19
2.4	Back biasing analysis at standard cell library level	36
2.5	Back biasing analysis at IP level	38
2.6	Discussion	41
2.7	Conclusion	42

2.1 INTRODUCTION

The need for consequent embedded data processing abilities inside compact battery-less wireless sensor nodes is getting stronger [26]. In these systems, energy sobriety supersedes the traditional hunt for speed performances and the Ultra-Low-Voltage (ULV) operation region has become a hot topic in low-power research. Since 2002 and the first subthreshold CMOS logic demonstrator [11], ULV has proven to be an ideal candidate for WNS design and more generally for low-performance and high energy-efficiency applications. As introduced in [1] and modeled in [4], a Minimum Energy Point (MEP) due to the tradeoff between leakage energy (E_{leak}) and switching energy (E_{sw}) is achieved at ULV as shown in Fig. 2.1. Operating with aggressively scaled supply voltage (V_{DD}) near or below the threshold voltage (V_T) can lead to energy savings of up to $10\times$ [23].

Several key publications since [1] studied how the scaling of the supply voltage influences the energy-efficiency. Wang *et al.* in 2002 [1], Calhoun *et al.* in 2005 [4] [12] and Bol *et al.* in 2008 [15] made significant contributions to the pursue of optimal energy consumption. Wang *et al.* first analyzed the energy and delay curve of a ring oscillator taking into account the activity factor to prove the existence of an optimal energy point for given supply and threshold voltages. Calhoun *et al.* extended this work with a deeper understanding of the subthreshold energy consumption and gave an analytical expression for the optimal supply and threshold voltages. They were the first to rigorously express the energy consumption of digital logic as the sum of leakage and dynamic energy and to give analytical expressions for both. They also proved through measurements of a silicon demonstrator [12] that the optimal supply to reach the Minimum Energy Point (MEP) is sensitive to technology, temperature, duty cycle and workload. Bol *et al.* followed up this work by studying the impact of technology scaling and the unavoidable parasitic increase that comes with nanometer CMOS on the energy optimization. They showed that high DIBL and short channel effects reduces the incentive to use deeply-scaled CMOS technologies for ULV logic. In [18], they proved that taking into account DIBL and random dopant fluctuation, pushes the optimal gate length to use from 32nm to around 40nm in 32nm CMOS. They also studied through simulation how FDSOI technologies can influence the scaling potential of ULV logic. Since then, subthreshold FDSOI circuits are emerging, as shown in [25], and can lead to very high energy efficiency.

The supply voltage scaling down to ULV is limited by two constraints as illustrated in 2.1:

- **Target frequency constraint:** in order to meet the target frequency of the application, the V_{DD} may need to be raised above the optimal energy point.

- **Robustness constraint:** operating below the threshold voltage, the I_{ON}/I_{OFF} ratio of MOSFET is exponentially exacerbating the sensitivity to random variations and increasing functional failure probability [6]. The robustness limit is obtained by gradually reducing the supply voltage until the 3σ worst-case Signal to Noise Margins (SNM) fall below a threshold [15].

A thorough examination of the design techniques that can be used at ULV to mitigate such constraints can be found in [26].

Along with these constraints, the designer also faces a high number of degrees of freedom challenging the achievement of minimum energy through classical design methods. Several works such as [2] further extended in 2009 with silicon demonstrator in [7] present design methodologies for energy-performance optimization. The idea is to optimally choose both supply and threshold voltages as well as sizing in order to equalize the sensitivity of energy and performance to these parameters.

The subthreshold drain current exponential dependence on V_T renders ULV logic designs strongly sensitive to global variations leading to large design margins needed to ensure timing closure and thus to a strong reduction of the incentive to operate at ULV. The development of ULV is thus strongly linked to the apparition of adaptive schemes for global variation compensation such as adaptive supply voltage (AVS) or adaptive body biasing (ABB)[11]. [17] demonstrated the interest of body biasing in bulk for frequency and leakage compensation of super-threshold operated microprocessor. They proved that, even with rough adaptation of the V_T through body-biasing, the σ of the frequency distribution of the microprocessor can be reduced by $7\times$. [11] used the same body-biasing adaptation on ULV logic coupled with an adaptation scheme on the supply voltage in order to reduce the power consumption. They mentioned, as early as 2002, that dual-gate SOI should be an interesting lead to pursue for ULV logic in order to boost the efficiency of adaptive body-biasing schemes thus paving the way to this work.

FDSOI technology extends the adaptive V_T degree of freedom through its ultra-wide range of back-biasing thanks to the absence of source- and drain-to-substrate parasitic diode. It has already been proven that static or dynamic back-biasing on FDSOI logic circuits can lead to PVT compensation at ULV [14] and to power optimisation [32] But, to the author's knowledge, there are no previous study of the impact of back biasing on ULV logic design.

In this chapter, we explore the potential of back-biasing techniques in FDSOI technology to alleviate both constraints. BB voltage controls the V_T through the back gate and can be used to dynamically adapt V_T in operation. The impact of back gate voltage biasing on V_T is detailed in Section 2.2. As the minimum energy point and the operating frequency of the MEP (f_{MEP}) are linked to the threshold voltage [8], dynamic V_T can help keeping a circuit with varying

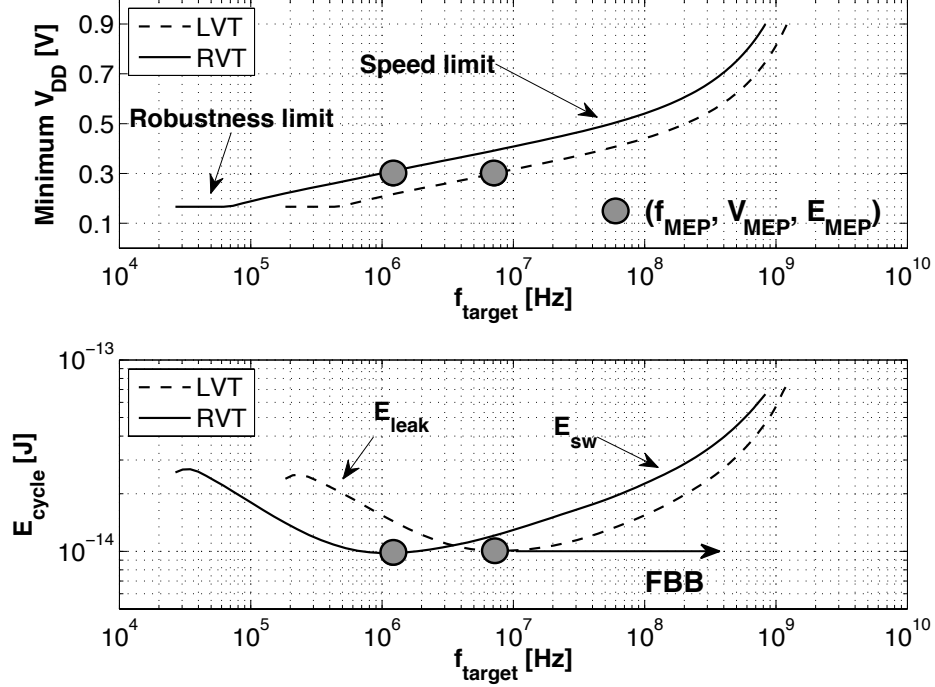


Fig. 2.1. Optimal E_{cycle} and minimal V_{DD} to achieve a target clock frequency in 28nm FDSOI RVT and LVT devices from Fig. 2.2 obtained through SPICE simulation of an 8-bit multiplier in 28nm FDSOI CMOS. We estimated the 3σ worst-case delay obtained through 1k Monte-Carlo (MC) simulations and the robustness limit is extracted from 80k MC simulations following the framework detailed in [5].

computational workload near an energetic optimum. Fig. 2.1 shows how the MEP is shifted toward higher operating frequencies between Regular V_T (RVT) and Low V_T (LVT) devices in a 28nm FDSOI high- κ /metal-gate CMOS technology [22]. These simulations results as all simulations conducted in this chapter were completed using the ELDO simulator from Mentor with 0.13 μ m bulk to 28nm FDSOI CMOS models from STMicroelectronics.

We study the impact of V_T modulation through BB at three abstraction levels:

- **At gate level**, we evaluate the impact of back gate biasing and of several schemes of NMOS/PMOS back gate biasing on key factors of merit of a testbench circuit simulated in SPICE at gate level. Technology scaling of bulk CMOS leads to increased variability, Drain Induced Barrier Lowering (DIBL) and gate leakage that contribute to raise the minimum energy level [8]. Scaling of the minimum energy level (E_{MEP}) with technology scaling is

limited by short channel effects in advanced bulk nodes calling for FDSOI technologies to keep reducing MEP while improving the corresponding f_{MEP} . In this work, the 28nm FDSOI technology MEP is compared to 0.13 μm , 90nm, 45nm and to 28nm bulk technologies MEP to quantify the high potential of FDSOI for Ultra-Low-Power (ULP) and ultra-low voltage design as anticipated in [27] [18] [33]. Section 2.3.1 illustrates the effect of scaling and back biasing in the ULV domain.

In addition to its use for trading performance for energy efficiency, body biasing has already been proposed on bulk technology to mitigate random V_T mismatch under Process Variation (PV) in [9]. In [10], the authors proposed an analytical framework to analyze the PMOS/NMOS ratio variation with supply voltage and an adaptive scheme to optimize this ratio while compensating Process Variations (PV). In this work, we use BB to control systematic PMOS/NMOS mismatch over the V_{DD} range without resorting to sizing modifications thus allowing the use of standard cell libraries sized at nominal voltage. Systematic mismatch cancellation results in both energy and robustness improvements. We show that such adaptive BB can save up to 18% of energy per cycle at MEP and improve gate count for 95% functional die yield by a factor of 6. Mismatch compensation schemes are described in Section 2.3.2 and energy efficiency and robustness results are provided in Sections 2.3.3 and 2.3.4.

- **At library level**, we recharacterize a standard cell library when applying different BB voltages and investigate the obtained performances as shown in Section 2.4.
- **At IP level**, we study the scaling perspective of ULV microcontrollers cores towards 28nm implementation by using the recharacterized libraries. We validate the conclusions made at gate and library level based on synthesis results of two microcontroller cores at 0.35V in 28nm FDSOI, as compared to the latest best-in-class results in 65nm CMOS bulk [23]. Energy efficiency results depending on the BB used during synthesis or during the operation of the microcontroller is discussed in Section 2.5.

This chapter consists of the collection of previously published results on FBB impact at gate level [29] and at IP level [30] synthesized in [31]. Sections 2.2 and 2.4 contain results from which we are able to extract a coherent view of BB in FDSOI circuits from device to synthesized IP.

2.2 BACK BIASING ANALYSIS AT DEVICE LEVEL

The V_T modulation through back gate biasing can be modelled as follows [12]:

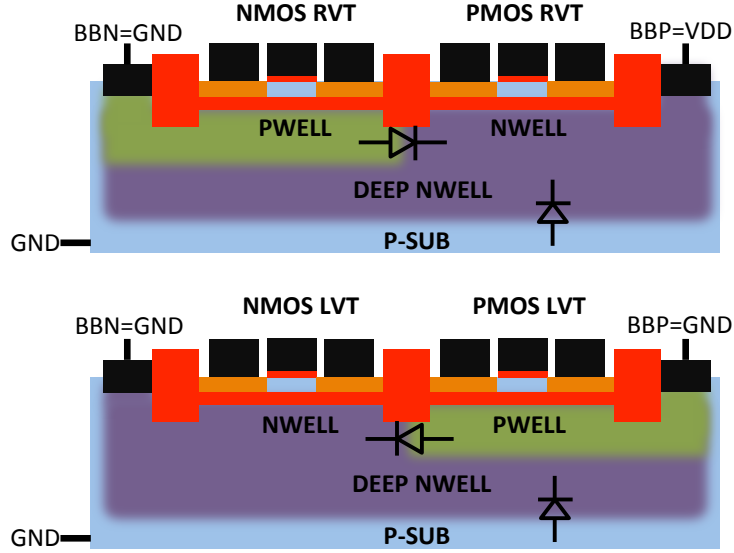


Fig. 2.2. Cross-section view of RVT and LVT devices in 28nm UTBB FDSOI technology from STMicroelectronics. Back Biasing voltages for: up - RVT devices similar to bulk technologies. Down - LVT devices implemented with flipped well.

$$V_T = V_{T0} - \gamma \times V_{BS} \quad (2.1)$$

with γ , the back gate effect taking into account the electrostatic control of the back gate over the channel, V_{BS} , the back gate biasing voltage and V_{T0} , the threshold voltage at $V_{BS} = 0V$.

A cross section of the two type of devices available in the 28nm FDSOI technology is shown in Fig. 2.2 featuring the Regular- V_T and the Low- V_T (LVT) device implemented using flipped well structures. Fig. 2.2 also illustrates the nominal BB connections to GND on the NMOS and V_{DD} on the PMOS for the RVT device and to GND on both NMOS and PMOS for the LVT device. The unusual PMOS BB connection for the LVT device is a recommendation from STMicroelectronics in order to compensate the ON current mismatch between the NMOS and PMOS as the LVT PMOS is significantly weaker compared to the LVT NMOS.

Fig. 2.3 shows the absolute value of V_T for NMOS and PMOS LVT devices. The V_T value drops with the forward BB down to 0.2V at $FBB = 3V$. Increasing the device's gate length (L) increases the V_T for all FBB voltages due to DIBL mitigation at long channel length.

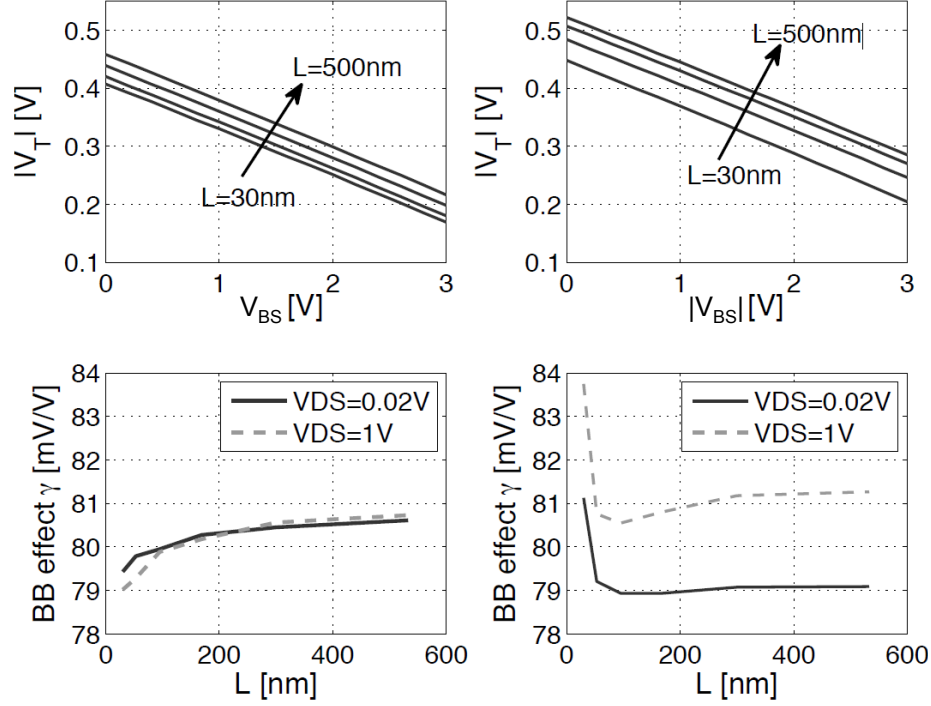


Fig. 2.3. Impact of BB on V_T for gate lengths from 30nm to 500nm and for $V_{DS} = 20\text{mV}$ unless otherwise indicated. The threshold voltage is extracted as the maximum of the second order derivative of the I_D current and γ is extracted as the slope of V_T for varying BB. Left: NMOS LVT device. V_{BB} represents the positive voltage with respect to the source voltage applied to the back-gate. Right: PMOS LVT device. V_{BB} represents the negative voltage with respect to the source voltage applied to the back-gate.

The γ parameter evolution with gate length is also featured in Fig. 2.3. For NMOS, γ is mostly independent of L but PMOS devices show higher variation with L and with V_{DS} , especially at short gate lengths. We can reduce the V_T and improve γ for the PMOS by using a minimum gate length devices. Lower V_T is interesting for high-speed ULV circuits in order to improve the I_{ON} current as shown in Section 2.3.2, while higher γ improves the efficiency of all the back biasing schemes for performance tuning presented in Section 2.3.2. In particular, short channel PMOS present lower systematic V_T mismatch than the NMOS, hence improving speed and robustness as shown in Sections 2.3.3 and 2.3.4.

Fig. 2.4 shows that the V_T is maximum at $V_{DS} = 0.1\text{V}$. In ULV circuits with V_{DD} down to $\approx 0.3\text{V}$, the high- V_T results in lower I_{ON} . The γ coefficient variation with V_{DS} is higher for the PMOS due to higher DIBL effect.

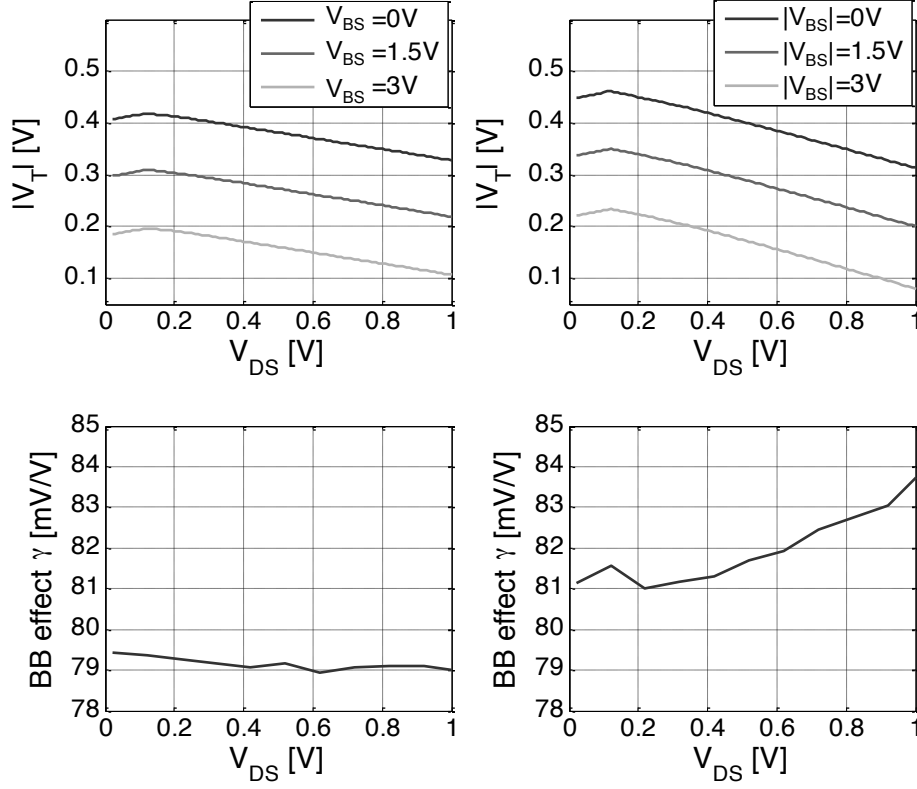


Fig. 2.4. V_T and γ coefficients for FBB=0V, 1.5V and 3V as a function of on V_{DS} and for $L = 30nm$ devices. Left: NMOS LVT device. Right: PMOS LVT device.

2.3 BACK BIASING ANALYSIS AT GATE LEVEL

Before analysing the impact of the back-biasing voltage at gate level, we first have to define the simulation setup used to apply back-biasing on logic cells. Fig. 2.5 features a cross-section of inverters implemented with the two devices flavor offered in 28nm UTBB FDSOI: LVT and RVT. In bulk technology, the range to apply body-biasing is limited by the drain- and source-to-bulk parasitic diode. In UTBB FDSOI, this diode is not present thanks to BOX isolation and the range to apply back-biasing is limited by the NMOS/PMOS back-gate diode illustrated in Fig. 2.5. For RVT devices, the range is limited for forward back-biasing and for LVT devices, the range is limited for reverse back-biasing.

Fig. 2.5 also illustrates the full V_T range achievable with RVT and LVT devices. Using RVT with reverse back-biasing leads to a V_T of 630mV at $V_{BB} = -3V$

and forward back-biasing on LVT can reduce the V_T up to around 150mV. The impact of forward and reverse back-biasing on the drain current at $V_{GS} = 0V$ is also shown in Fig. 2.5.

Until this point, all simulations are conducted with a maximum back-biasing voltage of 3V to highlight the full range of V_T modulation. However, STMicroelectronics guarantees reliability for a maximum voltage of 3V across the UTBB BOX. For a nominal supply voltage of $V_{DD} = 1V$ and in order to guarantee reliability for all V_{DD} up to the nominal voltage, we limit the FBB range to 2V for the rest of this work.

With the objective to achieve high-performance through forward overdrive back-biasing, we limit our investigation to LVT devices even if RVT without reverse back-biasing are sometimes used as baseline for comparison purpose.

All simulations are conducted with the latest version of the Design Kit available at the time which is the 2.4 version. Regardless of the quantitative precision obtained on the device characteristics and IdVg curves, the main trends and conclusions that are presented in this work remain relevant.

2.3.1 Scaling and back biasing impact on frequency and energy efficiency

To study the evolution of relevant figures of merit (FoMs) for circuit design with scaling, we simulate in SPICE an 8-bit benchmark multiplier ([15] appendix B) from $0.13\mu m$ to $28nm$. All simulations are conducted at $0.35V$ in order to be in the speed-limited region of the ULV domain and well above the robustness limit as illustrated in Fig. 2.1 and more precisely analyzed in Fig. 2.7. In $65/45nm$ bulk, we used upsized gate length to improve energy efficiency and functional robustness [8] [5].

Figs. 2.6 and 2.7 show SPICE simulations of an 8-bit benchmark multiplier at $0.35V$ in $0.13\mu m$, $90nm$, $65nm$, $45nm$ bulk with a GP CMOS process (Silicon-based/polysilicon oxide/gate stack) and in $28nm$ technology with an LP CMOS process (High- κ /metal oxide/gate stack), as offered by the foundry in both bulk and FDSOI technologies following the framework used in [5] [8]. $65nm$ and $45nm$ devices were upsized by $20nm$ and by $10nm$ respectively to compensate for DIBL effect. Signal-to-Noise Margins (SNMs) were simulated as proposed in [6] based on 80k-run Monte-Carlo simulations of cross-coupled NAND2-NOR2 gates and the V_{LIMIT} is defined as the minimum V_{DD} allowing a 0.1% negative noise margin.

As shown on Fig. 2.6(a), the maximum frequency increases between $0.13\mu m$ and $65nm$ as a result of the reduction of parasitic capacitances and V_T value. As predicted in [21], the $45nm$ node is slower than the $65nm$ one. There are three factors at play causing this speed reduction: a saturation of the typical subthreshold I_{ON} current, a significant increase of the I_{ON} variability and an NMOS/PMOS I_{ON} systematic mismatch. These three factors induce a 3σ worst case delay increase observed in Fig. 2.6(a).

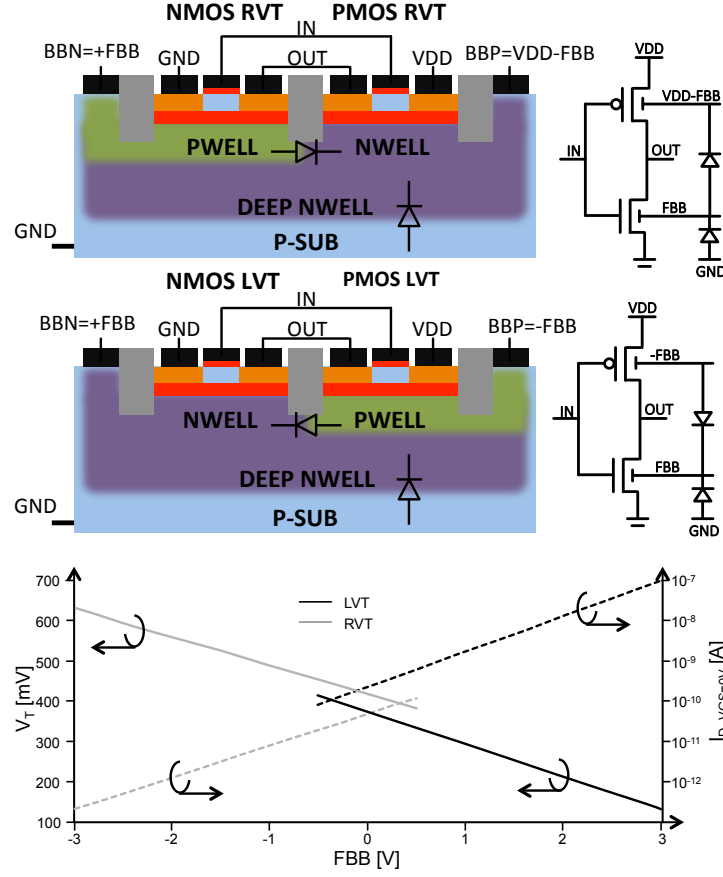


Fig. 2.5. Up: RVT and LVT inverter cross section and schematic featuring the back-gate to substrate diode and the NMOS/PMOS back-gate diode. Down: V_T and drain current at $V_{GS} = 0V$ for NMOS LVT and RVT with varying back-gate voltage.

The 28nm bulk implementation is slower than any other bulk nodes due to the LP CMOS process which features a higher V_T . Using FBB on the FDSOI implementation to reduce the threshold voltage can provide a speed-up as high as $17\times$ between a 0V bias and a 2V bias. Fig. 2.6(b) shows the same trend for the leakage power from both drain and gate leakages. The leakage of the 28nm bulk is reduced by a factor of $35\times$ compared to 45nm thanks to the LP CMOS process and the high- κ /metal gate. The FBB on FDSOI greatly increases the

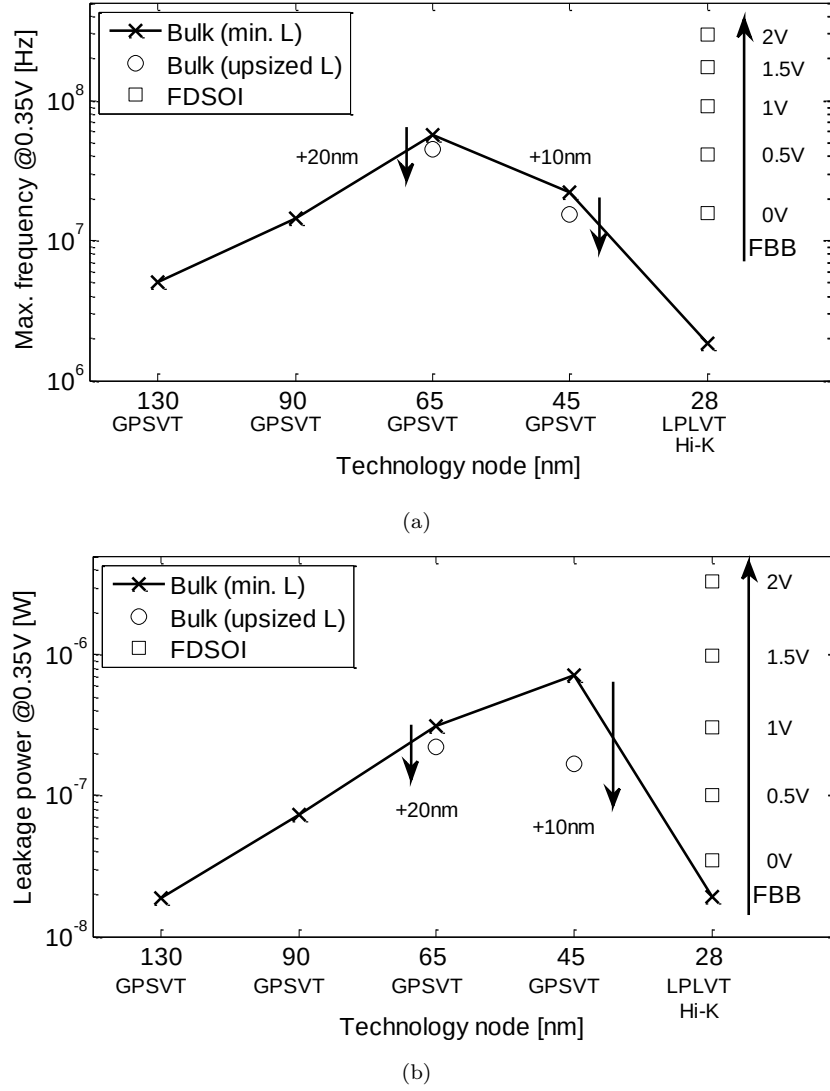
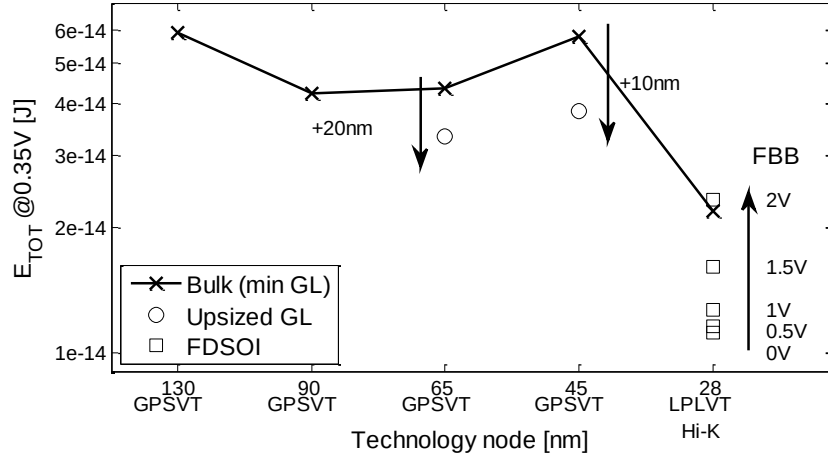
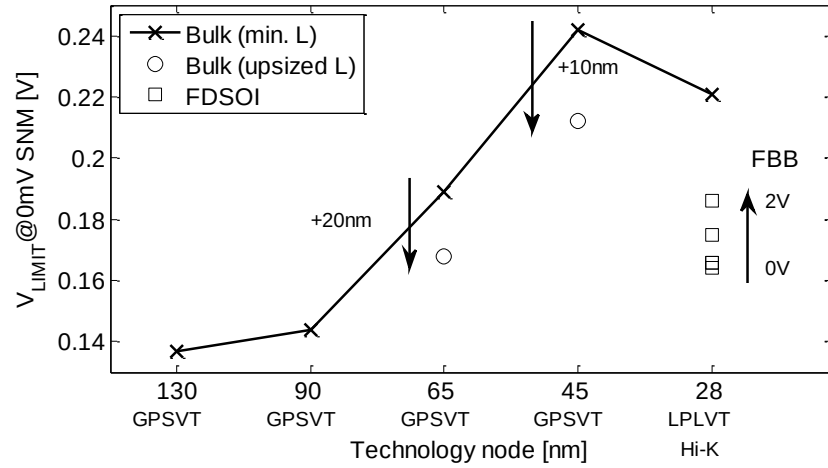


Fig. 2.6. Evolution of maximum frequency of operation and leakage power consumption with scaling in the ULV domain. The results were obtained through simulation based on the framework from [15] Appendix B.

leakage through the V_T reduction. The total E_{CYCLE} shown in Fig. 2.7(a) is degraded from 90nm to 45nm, illustrating the energy overhead of short channel effects, variability and gate leakage [8]. Upsized-gate-length at 65/45nm improves the total energy per cycle E_{CYCLE} at the expense of a 25/45% speed penalty.



(a)



(b)

Fig. 2.7. Evolution of energy per operation and robustness with scaling in the ULV domain. The results were obtained through simulation based on the framework from [15] Appendix B.

The 28nm technology shows outstanding results in E_{CYCLE} especially in FDSOI thanks to high- κ /metal gate and to lower short channel effects and thus reduced DIBL. Fig. 2.7(b) further illustrates the degradation of functional robustness at ULV through the evolution of the minimum V_{DD} to maintain noise margins V_{LIMIT} with scaling. As expected, the low variability due to undoped channel

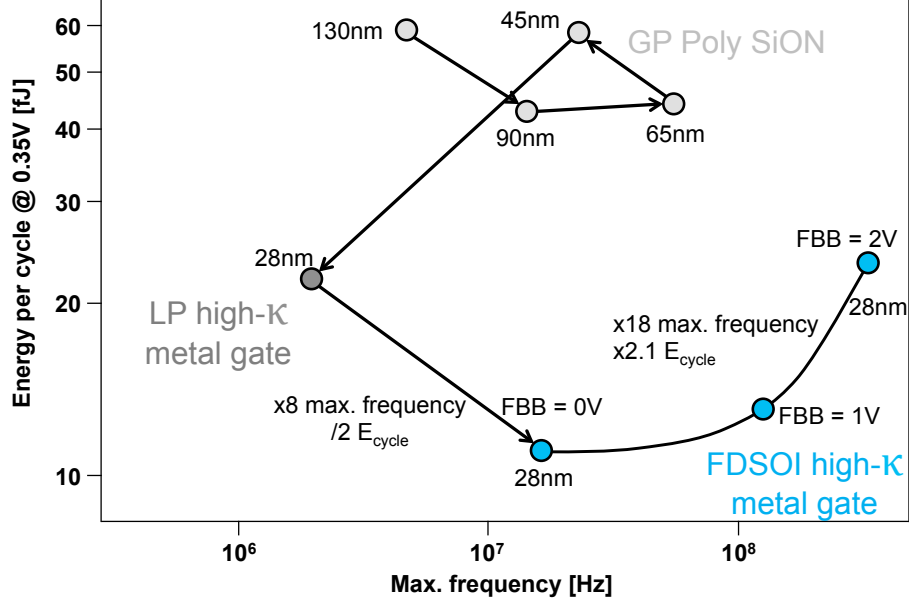


Fig. 2.8. Impact of technology scaling and FBB on the energy per cycle and on the frequency of operation.

and low short-channel effects of FDSOI restores functional robustness at 28nm by improving V_{LIMIT} .

Based on these results, we can discard the 28nm bulk technology as it will be too slow to implement ULV circuits in the MHz range and as it features a robustness limit close to the targeted supply voltage range. Contrary to 28nm bulk, FDSOI technology allows high-speed operation and high robustness at 0.35V.

To summarize, Fig. 2.8 shows the evolution of the energy per cycle depending on the technology node selected. Two key messages are highlighted:

- the short-channel effect-induced penalty on the energy observed in mainstream GP bulk technologies can be mitigated by taking advantage of innovations at the technology level introduced at the 28nm node such as high- κ /metal gate and FDSOI structures.
- FBB offers a wide frequency tuning range compared to the impact of technology scaling. This continuous range, illustrated by the line between the FBB=0V and FBB=2V points in Fig. 2.8 shows how the energy-per-cycle will evolve depending on the frequency imposed by the application in practical scenario. On this line, applying a moderate overdrive of $FBB = 1V$ leads to an interesting tradeoff between energy and speed and should be

used if the application is not setting a target frequency. Section 2.5 validates the potential of moderate FBB at IP level to reach similar conclusions.

2.3.2 Delay equalization and back biasing compensation schemes

Body biasing has already been proposed in bulk technology to mitigate random V_T mismatch under PV in [9]. In [10], the authors proposed an analytical framework to analyze PMOS/NMOS ratio variation with supply voltage and an adaptive scheme to optimize this ratio while compensating PV. In this work, we use BB to control systematic PMOS/NMOS I_{ON} mismatch over the V_{DD} range without resorting to sizing modifications, allowing the use of standard cell libraries sized at nominal voltage. We show that such adaptive BB can save 18% of energy per cycle at MEP and improve gate count for 95% functional die yield by a factor of 6.

To examine the impact of PMOS/NMOS ratio variation on the relevant FoMs, we model the subthreshold delay and leakage power. In subthreshold regime, the drain current can be expressed as in [12]:

$$I_{D,sub} = I_0 \times 10^{\frac{V_{GS} - \eta V_{DS}}{S}} \times (1 - e^{-\frac{V_{DS}}{U_{th}}}) \quad (2.2)$$

with U_{th} , the thermal voltage, S , the subthreshold swing and η modeling the DIBL effect. I_0 regroups the threshold voltage variation due to back gate voltage V_{BS} and bias-independent factors, particularly the body factor n and the zero-bias threshold voltage V_{T0} :

$$I_0 = \mu_0 C_{ox} \frac{W_{eff}}{L_{eff}} (n - 1) U_{th}^2 10^{\frac{-V_{T0} + \gamma V_{BS}}{S}} \quad (2.3)$$

The NMOS and PMOS I_{ON} are matched at nominal $V_{DD} = 1V$ by upsizing the PMOS width but a mismatch appears in the subthreshold domain and for varying BB as the drive current becomes exponentially dependent on the threshold voltage. Fig. 2.9 shows a divergence between NMOS and PMOS I_{ON} below 0.4V.

There are several ways to model the gate delay based on IdVd simulations. We compare four models expressed in Eq. 2.4 to Eq. 2.7.

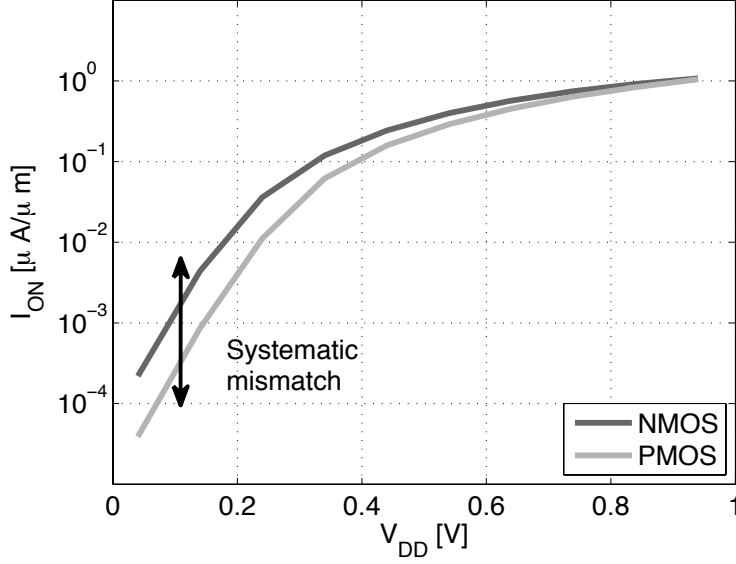


Fig. 2.9. NMOS and PMOS I_{ON} evolution with V_{DD} for LVT MOSFET with $FBB = 2V$ ($W_p = 160nm$, $W_n = 80nm$, $L_p = L_n = 30nm$ and $V_{DS} = V_{GS} = V_{DD}$, $V_{BS} = GND$). The PMOS BB is connected to GND. The results are obtained through SPICE simulations in 28nm CMOS FDSOI.

$$T_{del,inv} \propto \frac{CV_{DD}}{\text{mean}(I_{ON,N}, I_{ON,P})} \quad (2.4)$$

$$T_{del,inv} \propto \frac{CV_{DD}}{\text{mean}(I_{eff,N}, I_{eff,P})} \quad (2.5)$$

$$T_{del,inv} \propto \frac{CV_{DD}^2}{\text{mean}(\int_0^{V_{DD}} I_{D,N@V_{GS}=V_{DD}} dV_{DS}, \int_0^{V_{DD}} I_{D,P@V_{GS}=V_{DD}} dV_{DS})} \quad (2.6)$$

$$T_{del,inv} \propto \frac{CV_{DD}}{\text{mean}(\alpha_N, \alpha_P)} \quad (2.7)$$

$$\text{with } \alpha = \frac{1}{2} \int_0^{V_{DD}} I_{D@V_{GS}=V_{DD}} dV_{DS} + \frac{1}{2} \int_0^{V_{DD}} I_{D@V_{GS}=V_{DD}/2} dV_{DS}$$

Eq. 2.4 is based on the ON current and Eq. 2.5 is based on the effective current first defined in [11] as:

$$I_{eff} = \frac{1}{2} \{I_D(V_G = V_{DD}/2; V_D = V_{DD}) + I_D(V_G = V_{DD}; V_D = V_{DD}/2)\} \quad (2.8)$$

Eq. 2.6 and 2.7 are based on the integration of the $I_D V_D$ curve at $V_G = V_{DD}$ or at $V_G = V_{DD}/2$. Fig. 2.10 shows the modelling error compared to the simulated

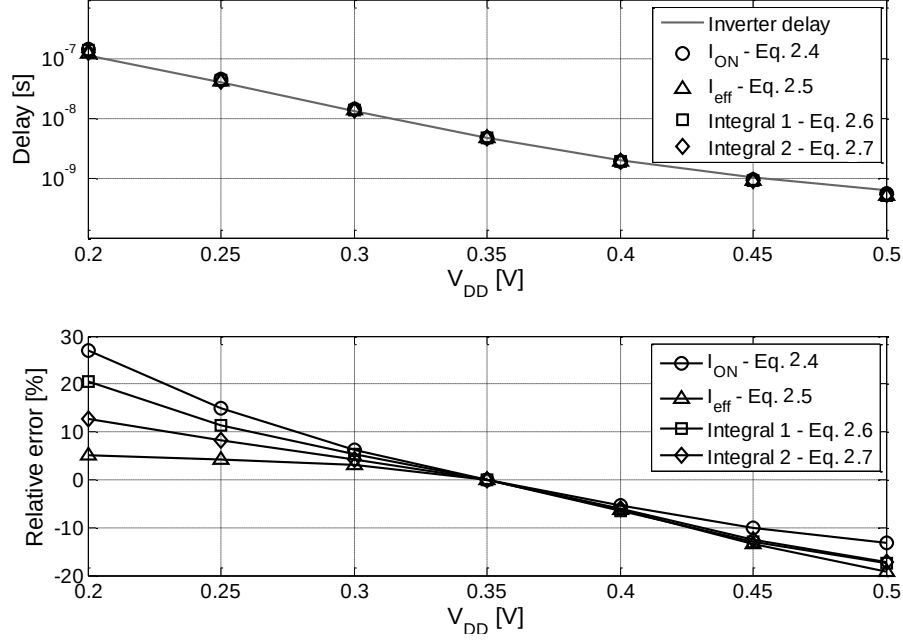


Fig. 2.10. Comparison between delay models from Eqs. 2.4 to 2.7 for an equivalent switching capacitance fitted at 0.35V and the simulated delay of a FO1 inverter chain.

delay of an FO1 inverter chain depending on V_{DD} . The modelling based on the effective current yields good matching at ULV and thus is chosen to study the impact of systematic mismatch on energy efficiency.

The subthreshold leakage power can be expressed as:

$$P_{leak} = I_0 10^{\frac{\eta V_{DD}}{S}} \times V_{DD} \quad (2.9)$$

Based on the models in subthreshold regime, we can study the impact of effective current mismatch on leakage energy. For an N-inverter chain, the total delay can be predicted as the product between the load capacitance C_{load} and the mean effective current:

$$T_{del} \propto \frac{2 \times N \times C_{load} \times V_{DD}}{(I_{eff,sub,NMOS} + I_{eff,sub,PMOS})} \quad (2.10)$$

The total leakage current can be written as the arithmetic mean between the two devices leakage currents:

$$P_{leak} = \frac{N}{2} (I_{0,N} 10^{\frac{\eta_N V_{DD}}{S_N}} + I_{0,P} 10^{\frac{\eta_P V_{DD}}{S_P}}) \times V_{DD} \quad (2.11)$$

If the systematic mismatch ratio between NMOS and PMOS effective current $\beta_{I_{eff}} = I_{eff,N}/I_{eff,P}$ is large, the delay can be, at best, divided by 2 compared to a unitary ratio situation. The leakage current of the faster device will be increased while the slower device leakage will be kept constant. The total leakage current will then increase by a factor $N/2 \times \beta_{I_{leak}}$, with $\beta_{I_{leak}} = I_{leak,N}/I_{leak,P}$, the leakage current ratio between NMOS and PMOS. The leakage energy:

$$E_{leak} = T_{del} \times I_{leak} \quad (2.12)$$

will be increased by a factor $N/4 \times \beta_{I_{leak}}$ that represents the E_{leak} loss caused by device mismatch as $\beta_{I_{leak}}$ is greater than one.

PMOS and NMOS devices feature different I_0 , subthreshold swings and DIBL factors which lead to larger than one $\beta_{I_{eff}} = I_{eff,N}/I_{eff,P}$, which is commonly corrected through an upsizing of the PMOS devices targeting equal rising and falling inverter delays. Implementing subthreshold circuits with standard library cells implies the use of cells balanced at nominal V_{DD} . Unfortunately, as the subthreshold I_{ON} divergence shown in Fig. 2.9 suggests, the $\beta_{I_{eff}}$ ratio will diverge from its value at nominal V_{DD} when the supply voltage is shrunk, leading to performance degradation. Fig. 2.11 illustrates the validation of this theoretical trend by simulations and shows the $\beta_{I_{eff}}$ spreading in the subthreshold domain that will cause an E_{leak} increase.

Based on these conclusions, we developed rise/fall delay mismatch compensation techniques by using the wide range of BB as a new degree of freedom offered by FDSOI technologies. By adapting the relative biasing between NMOS and PMOS devices, we can use the back gate to modify the $I_{0,NMOS}/I_{0,PMOS}$ ratio through the parameter γ in Eq. 2.3 and control the effective current mismatch.

In order to study the back biasing potential in subthreshold domain, we selected five levels of forward back biasing to be applied on LVT device (from 0V up to 2V).

Three FBB schemes are investigated, as represented in Fig. 2.12:

- **DFBBVDD**: this is the baseline FBB scheme used in Section 2.3.1 where the NMOS back gate BBN is biased at an FBB level and the PMOS back gate BBP is biased at -FBB to compensate in the first order the NMOS/PMOS systematic mismatch by boosting PMOS transistors. This scheme is a simple extrapolation of this rule where the supply voltage of a super-threshold standard cell based design is scaled down and no other modifications are made.
- **ADFBB**: as shown in Fig. 2.11, the PMOS I_{eff} boost with DFBBVDD is not strong enough at low V_{DD} . Furthermore, $\beta_{I_{eff}}$ diverges from its value in the super-threshold domain where standard cells are designed. In this scheme, an Adaptive Delta Forward Back Bias (ADFBB) is applied to the

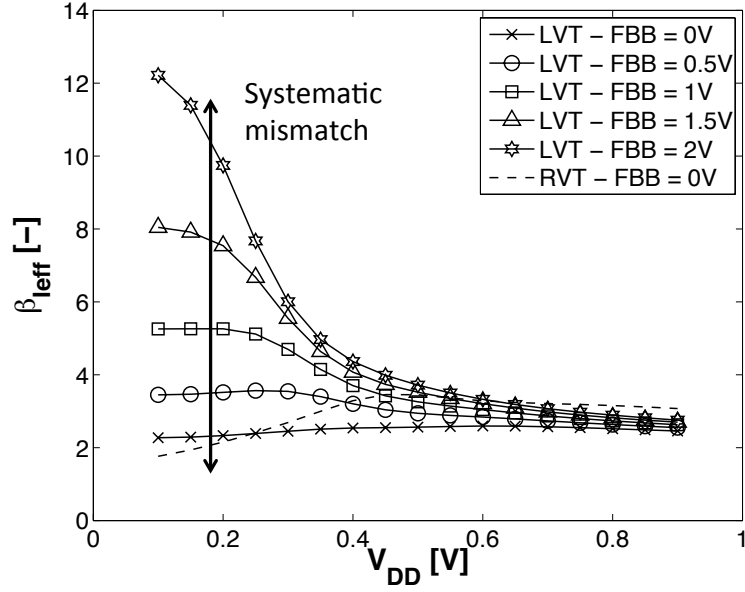


Fig. 2.11. NMOS-PMOS I_{eff} ratio evolution with V_{DD} for RVT MOSFETs and LVT MOSFETs with different FBB voltages ($W_p = W_n = 80nm$, $L_p = L_n = 30nm$). The PMOS BB is connected to GND-FBB. SPICE simulation results obtained in 28nm FDSOI CMOS.

PMOS devices to equalize rising and falling delays for an inverter at each V_{DD} .

- **IADFBB:** the goal of this scheme is to achieve the same delay equalization as with ADFBB by reducing the NMOS back bias instead of increasing the PMOS back bias.

Fig. 2.13 presents the rise-fall delay ratio $\beta_{del} = T_{fall}/T_{rise}$ for each scheme. We can see that the two adaptive asymmetric schemes lead to a very stable rise-fall delay ratio over V_{DD} . At high FBB, the DFBBVDD scheme cannot compensate the I_{eff} drift between NMOS and PMOS. We then expect the most spectacular energy savings between (I)ADFBB and DFBBVDD to be seen for high-speed devices.

For the ADFBB scheme, we can see that optimal DFBB is equal to V_{DD} plus a constant over every supply voltage. The same conclusion can be drawn for the IADFBB scheme keeping in mind that Fig. 2.13 only features the DFBB applied to the NMOS, which is the constant contribution, and an FBB equal to V_{DD} is simultaneously applied on the PMOS. This suggests that the systematic mismatch on I_0 , S and η between NMOS and PMOS is roughly constant over V_{DD} .

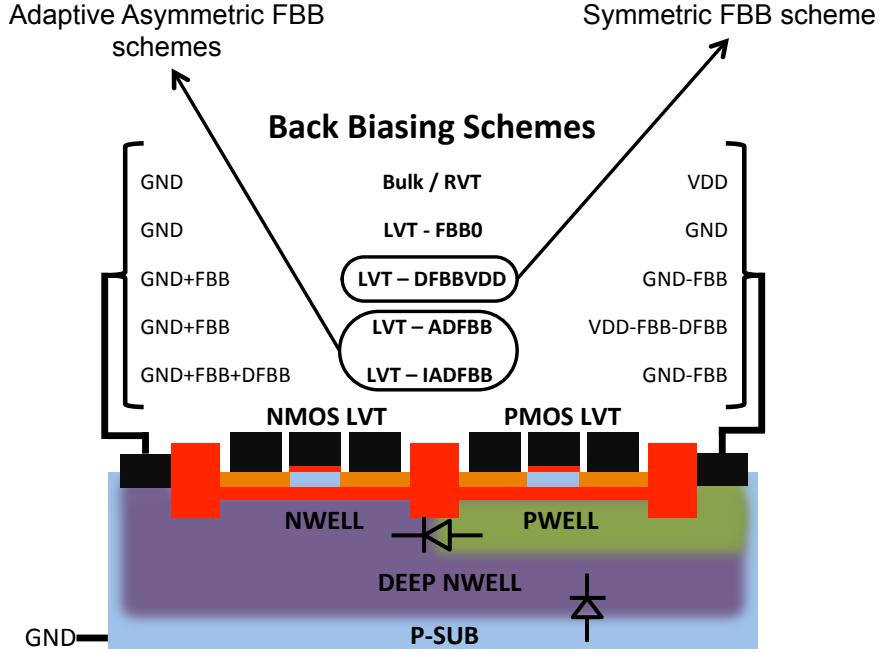


Fig. 2.12. Schematic view of an LVT device in 28nm UTBB FDSOI technology with description of symmetric and asymmetric back biasing schemes.

The constant contribution of the optimal DFBB increasing with FBB and the $\beta_{I_{eff}}$ increase at high FBB suggest that systematic mismatch is stronger for lower threshold voltages.

The granularity in the optimal DFBB for $V_{DD} > 0.5V$ can be explained by the limited sensitivity of the inverter delay with respect to V_T . When the inverter is not operated in the subthreshold region, this low derivative causes the optimal DFBB extraction method to reach the precision limit of the simulation.

2.3.3 Impact of back biasing compensation schemes on minimum energy point

To study the evolution of the MEP with FBB and DFBB schemes, we simulated an 8-bit multiplier with RVT devices and LVT- $FBB = 0V$ devices as baselines following a framework described in [15] Appendix B. We then applied, on the LVT implementation, an increasing FBB from 0V to 2V with the three DFBB schemes described in Section 2.3. The multiplier delay was extracted by fitting a lognormal distribution over the Monte-Carlo simulations and taking the mean

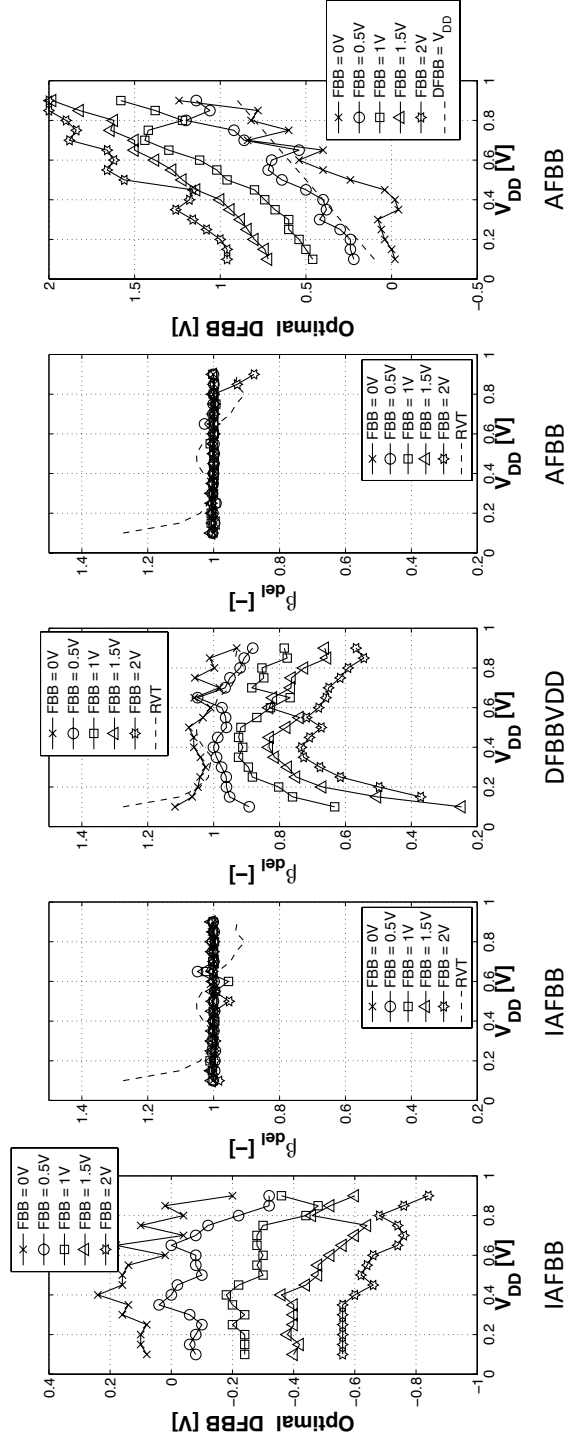


Fig. 2.13. Impact of ADFBB and IADFBB schemes as defined on Fig. 2.12 on inverter rise-fall delay ratio. From left to right: IADFBB optimal DFBF applied on NMOS, IADFBB rise-fall delay ratio, DFBBVDD rise-fall delay ratio, ADFBB rise-fall delay ratio, ADFBB optimal DFBF applied on PMOS ($W_p = 140nm$, $W_n = 80nm$, $L_p = L_n = 30nm$).

value plus 3σ as a worst-case value. Multiplier leakage power was estimated by the arithmetic mean over Monte-Carlo simulations.

Fig. 2.14 shows the E_{MEP} and the V_{DD} at which this energy is attained (V_{MEP}). For the (I)ADFBB schemes, the optimal DFBB at $V_{DD} = V_{MEP}$ from Fig. 2.13 was used. We can see that E_{MEP} is increasing as the FBB voltage is increased. As V_T is reduced, the MOSFETs enter the near-threshold regime which results in higher E_{leak} [12].

Different results were obtained by [8] on the same simulation framework for 45nm bulk technology. In bulk nodes, E_{MEP} improvement for low- V_T devices is linked to different phenomena compared to FDSOI. The V_T reduction in bulk technologies is done by lowering channel doping which narrows the channel depletion region, improves the subthreshold slope, reduces the gate leakage contribution but increases the DIBL effect. Therefore, in bulk process, an optimal V_T exists resulting from the tradeoff between DIBL mitigation, gate leakage reduction and subthreshold current improvement [8]. In FDSOI process, V_T variation is obtained by varying the Back Plane (BP) doping below the buried oxide [14] as shown in Fig. 2.12 leaving the channel undoped and V_T variations will not modify the depletion of the channel. As shown by measurements conducted on an analog FDSOI process in [19], both S and η are increased with FBB. Thus, increasing the V_T on FDSOI technologies will not lead to an E_{MEP} reduction.

Fig. 2.15 shows the evolution of E_{MEP} and f_{MEP} with FBB. Having access to a continuous V_T design space gives the possibility to shift the MEP depending on computational workload. Traditional subthreshold circuits try to approach the MEP by scaling down V_{DD} but are forced to move away from it if a higher throughput is needed. Dynamically adaptive FBB could help keeping the circuit near the MEP under a varying target frequency.

For small FBB, using ADFBB leads to degraded E_{MEP} levels. At high FBB, E_{MEP} with ADFBB is below E_{MEP} with DFBBVDD through a higher allowed f_{MEP} . This result is coherent with observations made from Fig. 2.11 and Fig. 2.13 that the DFBBVDD scheme is not adequate at high FBB. As ADFBB consists in boosting PMOS devices, the f_{MEP} increases. On the contrary, IADFBB slows down NMOS devices to match PMOS delay, leading to a reduced f_{MEP} . As shown in Fig. 2.14, IADFBB can offer an E_{MEP} level reduction of 11% at $FBB = 0V$ and up to 18% at $FBB = 0.5V$.

To objectively compare the interest of ADFBB and IADFBB schemes, we represented in Fig. 2.15 the position of the MEP as a function of the frequency at which this energy optimum is attained. Results indicate that IADFBB always leads to lower E_{MEP} value but at the cost of lower f_{MEP} . IADFBB can reduce by 18% the MEP level compared to DFBBVDD. On the contrary, ADFBB allows higher f_{MEP} at the cost of E_{MEP} degradation at low FBB but with E_{MEP} improvement at high FBB. Fig. 2.15 also shows that $FBB = 2V$ with

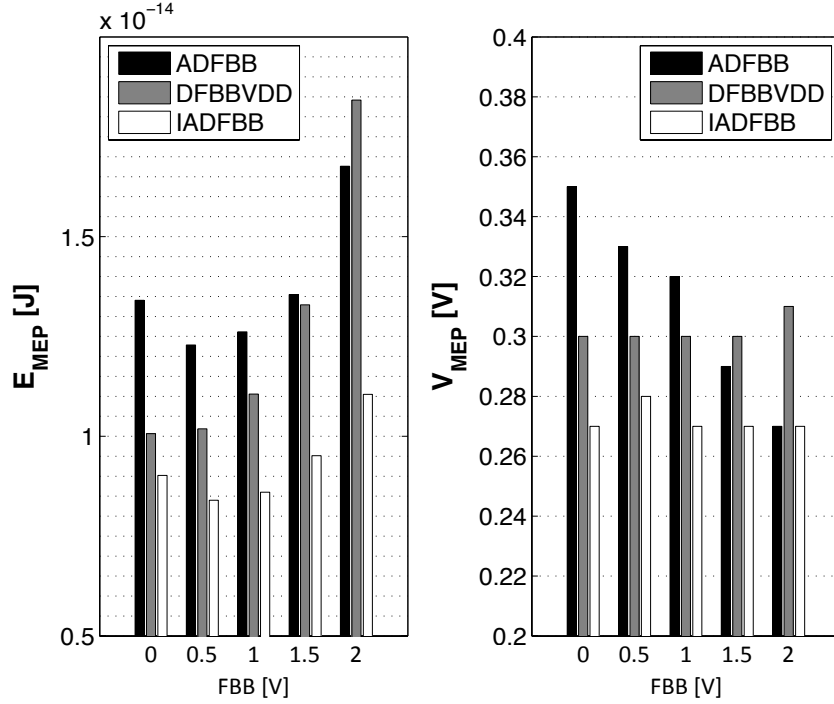


Fig. 2.14. Left: minimal E_{Cycle} for 0V to 2V FBB voltages and for all three DFBB schemes. Right: V_{DD} at MEP for 0V to 2V FBB voltages and for all three DFBB schemes.

ADFBB can improve the MEP frequency by $36\times$ compared to $FBB = 0V$ with DFBBVDD.

The Pwell/Nwell and Nwell/Psub diodes were not simulated. For positive value of FBB and with the DFBB values shown on Fig. 2.11, these diodes are reverse-biased. To ensure that their leakage current is negligible, we estimated the diodes area and perimeter for the 8-bit multiplier implemented with standard cells. In the worst case, for high FBB value and for the three DFBB schemes, the total leakage power is below $30fW$ at $25^\circ C$ and below $70pW$ at $125^\circ C$. This confirms that the leakage power of well diodes is negligible compared to the power of the multiplier.

2.3.4 Impact of back biasing compensation schemes on robustness

Resiliency to device variability is a critical feature to ULV circuits as they feature a magnified sensitivity due to reduced voltage levels [20]. We extract the robustness limit by analyzing the functional failure rate due to variability-induced bad logic levels as first described in [6]. The method used in this work is based on a

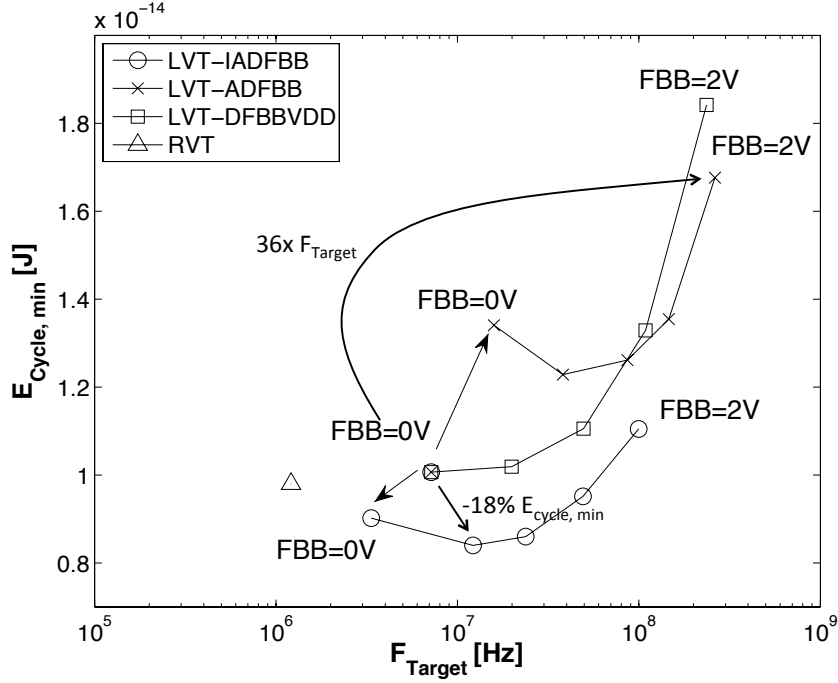


Fig. 2.15. MEP position in the target frequency design space for 0V to 3V FBB voltages and for all three DFBB schemes.

statistical estimation of the static noise margins (SNM) through Monte-Carlo simulations as used in the framework of [15].

Along with its impact on minimum energy, systematic mismatch between NMOS and PMOS currents leads to reduced robustness of logic levels against crosstalk, radiations or random variability. In the subthreshold domain, where the I_{ON}/I_{OFF} ratio is small, these phenomena, together with within-die V_T variability, can lead to insufficient low and high noise margins (NM_L and NM_H) and to functional failure. At first order and without DIBL effect, we can reduce Eq. 2.2 and express ON-state and OFF-state currents as:

$$I_{ON} = I_0 \times 10^{\frac{V_{DD}}{S}} \quad , \quad I_{OFF} = I_0 \quad (2.13)$$

We consider $I_{ON,N}/I_{OFF,P}$ and $I_{ON,P}/I_{OFF,N}$ ratios as figures of merit of robustness, which is a variation of the equivalent resistance model developed in [16]. We then discuss the theoretical impact of I_0 , S and η mismatches on these ratios:

I_0 : as the two ratios depend linearly on $I_{0,N}/I_{0,P}$ and $I_{0,P}/I_{0,N}$, having $I_{0,N} \neq I_{0,P}$ will a noise margin favoured over the other and lead to reduced global noise margin. Indeed, the gate noise margin is defined as $\min[NM_L, NM_H]$.

S : if $S_N > S_P$, the $I_{ON,N}/I_{OFF,P}$ ratio will be reduced as it can be written as:

$$10^{(-V_{T0} + \gamma V_{BS})/S_N} \times 10^{V_{DD}/S_N} \times 10^{(V_{T0} - \gamma V_{BS})/S_P} \quad (2.14)$$

A subthreshold swing mismatch will then lead to favor one noise margin over the other.

η : in the subthreshold domain, the DIBL effect increases both NMOS and PMOS currents in the same proportions. If the DIBL effect between the two devices is different, one drive current will be increased but when the high-DIBL device does not drive, the high-leakage and low-drive device will lead to reduced robustness.

In each case, maximizing $I_{ON,N}/I_{OFF,P}$ and $I_{ON,P}/I_{OFF,N}$ ratios is done with balanced devices.

In order to evaluate the impact of ADFBB and IADFBB on yield, we estimate the noise margins as proposed in [6] based on 80k Monte-Carlo simulations of a NAND2 gate cross-coupled with a NOR2 gate. As the NOR2 gate features a stacked pull-up network, it has the most stringent constraint on the low input noise margin V_{IL} and similarly, the NAND2 gate has the most stringent noise margin constraint on the low output level V_{OL} . Without precise information about the circuit paths, the considered benchmark can give an interesting figure of merit of functional failure probability at gate level.

To obtain an image of functional die yield based on this gate SNM extraction technique, we used a framework developed in [5] where the authors extrapolate die yield η_{die} as follows:

$$\eta_{die} = \eta_{gate}^{N_{gates}/2} \quad (2.15)$$

where η_{gate} is the gate yield computed with the Monte-Carlo simulations.

To consider the impact of noise and crosstalk, gate functional failure was defined as NOR2-NAND2 SNM below two thresholds: 30mV and 40mV. Using this model, we can compare the die yield depending on gate count using or not the (I)ADFBB compensation as plotted in Fig. 2.16.

Results indicate that having a 95% die yield with RVT devices limits the gate count to 80k gates for 40mV minimum SNM while using LVT devices can bring this limit to 320k gates. As predicted, balancing the I_0 between NMOS and PMOS has a positive impact on die yield. Fig. 2.16 shows that, at 30mV minimum SNM, we can improve by a factor of 6 the number of gates at 95% die

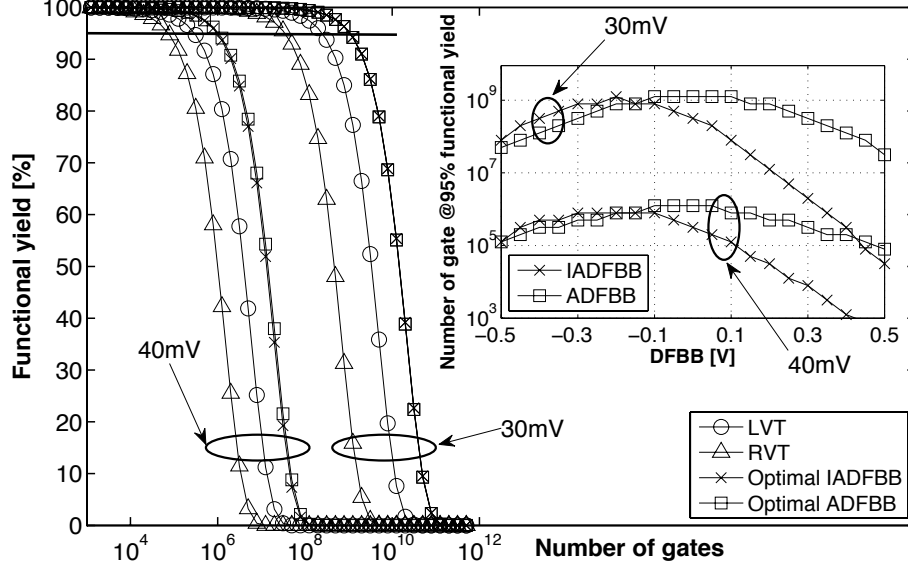


Fig. 2.16. Functional yield computed with the model described by Eq. 2.15 for an 8-bit multiplier @ $V_{DD} = 0.3V$ implemented with RVT and LVT devices ($FBB = 0V$). Gate noise margins were considered with two thresholds: 30mV and 40mV. Inset: maximum number of gates to maintain a 95% die yield with ADFBB and IADFBB schemes.

yield. At 40mV minimum SNM, the improvement factor between baseline LVT and LVT with (I)ADFBB is higher than $4\times$.

The inset in Fig. 2.16 indicates that a similar maximum number of gates at 95% die yield can be achieved with IADFBB and with ADFBB, which is coherent with the idea that these two techniques are two equivalent ways to balance $I_{eff,N}$ and $I_{eff,P}$. The inset in Fig. 2.16 also shows the optimal value of DFBB to be applied in order to maximize robustness. The two maxima appears at different DFBB values because they are applied differently in IADFBB and in ADFBB, as shown on Fig. 2.12. We can also see that the optimum DFBB values in each case for robustness are close to the optimum DFBB values found in Section 2.3.3 for energy minimization.

2.4 BACK BIASING ANALYSIS AT STANDARD CELL LIBRARY LEVEL

For 28nm FDSOI, we recharacterized the 12-tracks LVT standard-cell libraries from STMicroelectronics at 0.35V using Liberate tool from Cadence and ELDO simulator from Mentor. Three versions of the library are computed at FBB = 0V, 1V and 2V with DFBBVDD scheme. In order to characterize the impact of

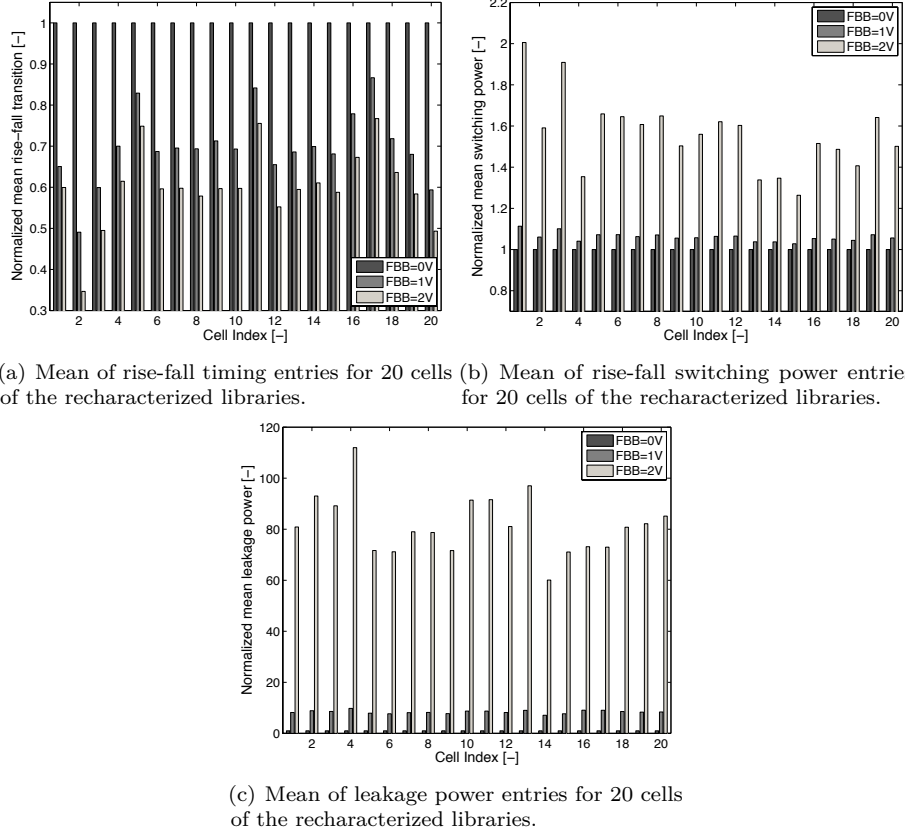


Fig. 2.17. Timing, switching power and leakage power factors of merit for the three recharacterized libraries for the 20 most used cells in the synthesized microcontrollers core from Section 2.5.

FBB on the library, we examine the 20 most used cells in the two microcontroller cores synthesized and presented in Section 2.5. Fig. 2.17(a) shows a mean rise-fall transition time drop of 20 to 40% from $FBB = 0V$ to $FBB = 1V$ and a 30 to 50% delay reduction between $FBB = 0V$ and $FBB = 2V$, depending on the cells.

Fig. 2.17(c) shows that the mean leakage increase between $FBB = 0V$ and $FBB = 1V$ is around $10\times$ and as high as $100\times$ between $FBB = 0V$ and $FBB = 2V$ due to the I_{OFF} exponential dependance on V_T .

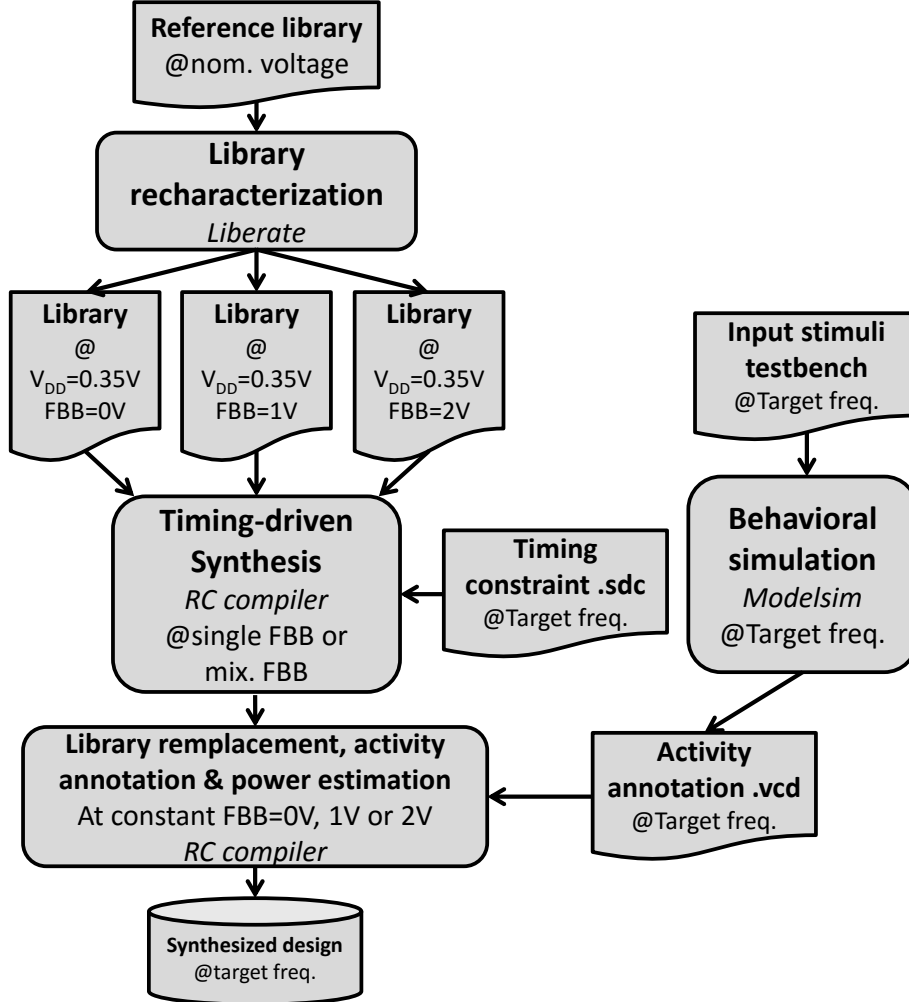


Fig. 2.18. Framework of the library recharacterization and IP synthesis to output core power consumption at $V_{DD} = 0.35V$ depending on the FBB schemes used.

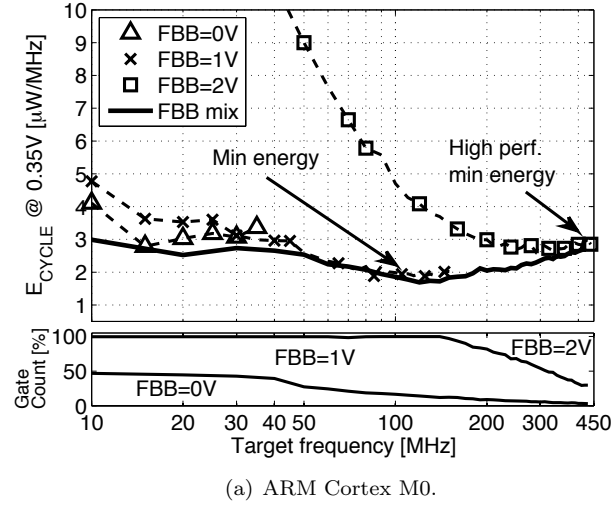
2.5 BACK BIASING ANALYSIS AT IP LEVEL

To assess the impact of FBB at the block level for ULV SoCs with high computing capabilities, let us consider two benchmark circuits: a 16-bit MSP430-compatible core from [36] as modified at UCL in the SleepWalker SoC swMSP430 [23] (including its instruction cache memory *I\$* and some peripherals) and the commercially-available ARM Cortex-M0 DesignStart 32-bit core. We run synthesis of these

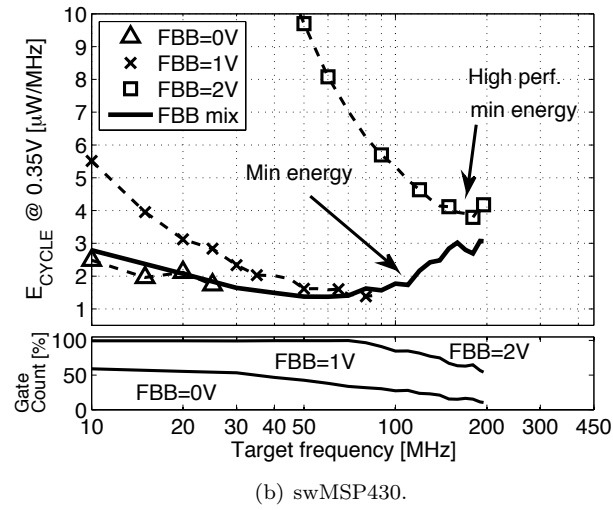
two cores both in 65nm bulk CMOS and in 28nm FDSOI at 0.35V with the recharacterized libraries presented in Section 2.4. For 65nm, standard-cell libraries with 20nm upsized gate length from [23] are considered. Synthesis is conducted for each of these versions separately and with a mix of the three versions as described in Fig. 2.18. First a recharacterization of the standard-cell library is completed at 0.35V and for FBB from 0V to 3V. Several synthesis are then conducted for increasing frequency and by using either only one FBB library or a mix of the three FBB libraries. Finally, to evaluate the performances of the synthesized design, the static and dynamic power is extracted either with the libraries used during synthesis or, if only one FBB library was used, after replacement of the cells with the cells characterized at a different FBB.

Figs. 2.19(a) and 2.19(b) show that synthesis with high FBB can achieve timing closure at high frequencies. The Cortex-M0 can be clocked at 440MHz in 28nm FDSOI with FBB=2V, achieving a speed-up of 8.8× compared to 65nm. However, as the core leaves the subthreshold region (V_T becomes lower than V_{DD} , resulting in a higher leakage energy), E_{CYCLE} is higher compared to the energy achieved at lower FBB. At low frequency, high FBB implementations suffer from energy overhead due to the integration of the high leakage power over a long cycle time. By allowing the synthesis tool to use a mix between the three FBB library versions, we manage to keep the energy per cycle below 3μW/MHz through the whole frequency design space. The evolution of the gate count breakdown between the three FBB library versions with frequency shows that faster gates are introduced in the design when the timing closure cannot be achieved with the previous FBB. Two key results are identified: first, the strict minimum energy point which is reached in the frequency range using mainly gates with 0V and 1V FBB voltages. Second, using 2V FBB gates allows to reach the high-speed minimum energy point. Fig. 2.20(a) illustrates the speed-up and energy saving between 65nm bulk and 28nm FDSOI implementations. We achieve on the Cortex-M0 a 42% E_{CYCLE} reduction and a 7× speed up if we target high performance or a 64% E_{CYCLE} reduction and a 2.4× speed up if we target energy minimization compared to the 65nm baseline. The difference between the E_{CYCLE} reductions of the two cores comes from different contributions of leakage and switching energy to E_{CYCLE} .

In practical applications, it is interesting to know how the FBB used for the synthesis influences the energy efficiency in operation. For a given target frequency, the designer has the choice to synthesize the IP with a low- or high-FBB library. A slow synthesized core can then be speed-up by applying a higher FBB during operation. Conversely, the core synthesized with a high-speed library can be slowed down with lower FBB in operation. Fig. 2.20(b) shows the energy per cycle for the ARM Cortex-M0 synthesized and operated with the three FBB libraries. The results are obtained with the framework illustrated in Fig. 2.18 by



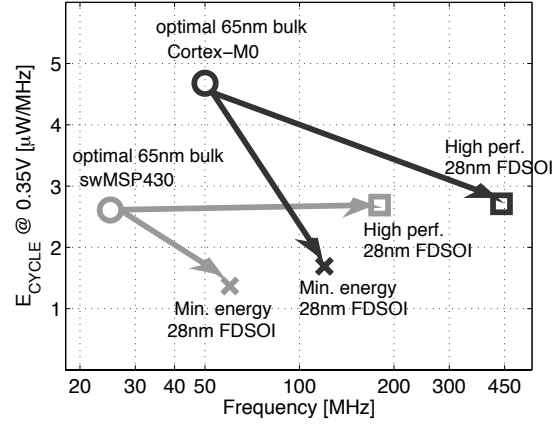
(a) ARM Cortex M0.



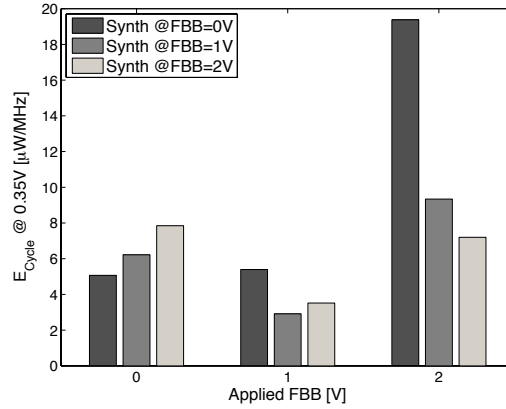
(b) swMSP430.

Fig. 2.19. Energy per cycle vs. the synthesis frequency for the Cortex-M0 and for the swMSP430 with each FBB library version and with the mix of all three versions.

changing the library FBB after synthesis. The core synthesized at FBB=0V is energy-inefficient for high FBB, high-speed operations and the core synthesized at FBB=2V maintains good energy efficiency over the entire range of FBB. In conclusion, in order to take advantage of the electrical control over the frequency of operation offered by the forward back biasing and still maintain good energy



(a) Evolution of the two energy minima @0.35V for swMSP430 and Cortex-M0 between 65nm baseline and 28nm FDSOI-optimized implementation.



(b) Energy per cycle for the Cortex-M0 synthesized using $FBB = 0V$, 1V or 2V @30MHz and running at different speeds depending on the applied FBB.

Fig. 2.20. Energy per cycle of synthesized cores depending on the frequency or depending on the FBB at synthesis.

efficiency, the synthesis operation should be conducted with a library characterized at high FBB.

2.6 DISCUSSION

The results presented in this chapter explored the potential energy savings that could be gained with an ideal FBB distribution down to each single gate. The analysis was stopped after the synthesis step and does not take into account the place and route step performance degradation. In practical implementations, the overhead of distributing one or several FBBs over the whole core area through multiple BB rails can be significant depending on the implementation choices and is outside the scope of this study. The designer should then use the framework and design guidelines presented in this chapter to evaluate the potential energy savings for a given design and draw a specification on the power consumption of the FBB generation and distribution circuit. This overhead can also be mitigated by using a larger distribution granularity and by operating, for example, at the block level of a complex digital SoC.

Chapter 4 presents a ULV silicon demonstrator which makes extensive use of FBB for functionality tuning and for V_T reduction. In this demonstrator, the BB generator circuitry was implemented along with the BB distribution over the design successfully proving the interest of FBB for ULV digital design.

PVT variations are not taken into account in this work as they can be compensated with adaptive schemes such as AVS [28] as opposed to local variability as analyzed in this chapter. Alternatively, adaptive FBB could be used for PVT compensation as illustrated in Chapter 4 through a silicon demonstrator. The asymmetric FBB schemes proposed in this chapter can also be used for example for compensating crossed process corners such as slow NMOS and fast PMOS corner or vice-versa.

Finally, all conclusions presented in this chapter are drawn from simulations based on the latest model cards from STMicroelectronics for technologies from $0.13\mu\text{m}$ bulk to 28nm UTBB FDSOI CMOS. The absolute value of the results presented in this chapter are subsequently linked to the accuracy of these models. We thus based all major contribution conclusions on trends and evolutions observed through simulations to free them from potential model inaccuracies.

2.7 CONCLUSION

The development of ultra-low power embedded devices such as wireless sensor nodes for the Internet-of-things calls for both very low energy per operation and high optimal frequency. The increasing impact of short-channel effects and variability on advanced bulk nodes degrades the minimum energy level at ULV in sub-90nm CMOS nodes. At gate level, we showed that 28nm UTBB FDSOI with smaller impact of short-channel effects and reduced variability can reduce the MEP level by $5.5\times$ compared to 45nm bulk node. We proposed to use the FBB to shift the MEP toward higher operating frequencies with limited energy penalty. Dynamic FBB modifications can thus be used to dynamically adapt the

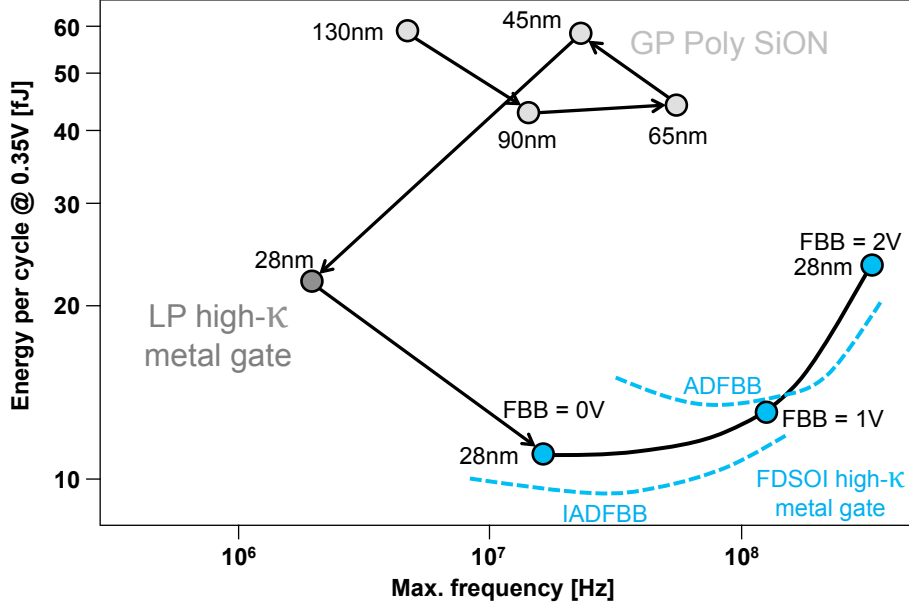


Fig. 2.21. Impact of technology scaling and FBB adaptive schemes on the energy per cycle and on the frequency of operation.

clock frequency to the fluctuating computational workload. We also provide a new method for systematic mismatch cancellation between NMOS and PMOS subthreshold currents for different FBB voltages. Adaptive and inverse adaptive FBB further extend the range of frequencies that leads to an energy minimum. Such adaptive schemes that are used to modify the speed/energy tradeoff can reduce the MEP value by 18% and increase the speed by $36\times$. Fig. 2.21 illustrates the design space gain offered by adaptive FBB schemes compared to the impact of technology scaling and non-differential FBB.

With the development of complex subthreshold circuits, keeping a reasonable functional yield becomes more challenging. The ADFBB and IADFBB schemes can provide a gate count improvement up to a factor of 6 while maintaining a 95% yield.

At IP level, we showed that UTBB FDSOI can provide either leakage reduction at low-speed or high-speed operations while maintaining E_{CYCLE} below the E_{CYCLE} achieved in 65nm and improve robustness at ULV. Compared to 65nm bulk, synthesis results show that the speed of ULV microcontrollers in 28nm FDSOI can be boosted by a factor of 7 in 28nm FDSOI and the E_{CYCLE} can be reduced by 64% with a mix of overdrive FBB voltages. We also showed that

mixing FBB during synthesis can lead to energy-efficient implementations for a wide range of frequencies of operation and that a microcontroller core synthesized at high speed can be kept energy-efficient even at low speed when a lower FBB is applied in operation.

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CHAPTER 3

BACK BIASING POTENTIAL IN 28NM FDSOI FOR PUSHING WIDEBAND ANALOG/RF CIRCUITS IN THE ULV DOMAIN

Abstract

Efficient wireless communication between Wireless Sensor Nodes (WSNs) and the cloud is a key enabler to a pervasive Internet-of-Things (IoT). The ability to deal with M2M communication growth and with the resulting crowded spectrum is driving the development of software-defined radios to bring versatility in the future of IoT communications. These radios impose heavy requirements on the Low-Noise Amplifier (LNA) over a wide frequency range. In order to be integrated in complex Systems-on-a-Chip (SoCs), such LNAs should also be implemented in advanced CMOS technologies to follow SoC development trends while benefiting from the high f_T available with technology scaling. In this chapter, we study the impact of technology scaling down to 28nm FDSOI and moderate inversion design to improve performances and reduce power for ultra-low-power RF designs. We first analyze the evolution of RF figures of merit at device level before expanding the work at circuit level to a noise-cancelling wideband LNA. Fair comparison between technologies is conducted thanks to an automatic sizing framework combining extensive design space exploration and small signal modelling. We first show that technology scaling causes the dominant constraint on minimum power to shift from bandwidth to noise. In this context, we demonstrate that moderate forward back biasing in 28nm FDSOI enables the operation at ULV with sub-mW power consumption for 6GHz operation with decent 3.8dB noise figure.

Contents

3.1	Introduction	51
3.2	Moderate inversion biased devices for RF	53
3.3	Efficient sizing methodology for noise-cancelling Low Noise Amplifiers	60
3.4	Impact on wideband noise-cancelling LNA design	64
3.5	Discussion & Conclusions	67

3.1 INTRODUCTION

As expressed in Chapter 1, efficient communication between WSNs and the cloud is a key enabler to a pervasive IoT. As such WSNs need to operate on energy-harvesting sources to limit the economical and environmental cost of battery replacement [1], there are stringent constraints on the energy consumption of the RF functionality to be embedded.

Along with the obvious energy challenge, the increasing number of connected nodes and wireless communication standards is causing a congestion of the RF spectrum. Software-Defined and reconfigurable Radio (SDR) design is a hot topic in RF research because of its potential to act as an enabler to cognitive radio, spectrum agility and seamless connectivity. Unifying SDR with the strongly-constrained power budget of IoT application is challenging as dedicated optimized radios feature higher performances for the same power consumption. Nevertheless, maximizing the hardware reuse between Wi-Fi, Bluetooth, GPS, cellular or even less industrialized communication schemes such as Ultra-Wideband (UWB) or mmWave will also help reducing the area cost in the WSN budget and increase the interoperability between sensor nodes or sensor networks. SDR might also be combined with wake-up radios for duty-cycled RX operation thus mitigating the power penalty conceded to achieve higher connectivity.

Power restrictions due to the targeted application as well as frequency performances and blocker resiliency requirements linked to the wideband nature of SDR renders such front-end challenging to design [33].

Using advanced CMOS technologies can help to meet these heavy requirements thanks to a high f_T [18]. However technology scaling has also led to a supply voltage reduction to maintain device reliability [14]. The simultaneous threshold voltage reduction is not as fast in order to keep the leakage current acceptable. This leads to a reduction of device's achievable transconductance that limits the dynamic range and pushes the operating point of the devices from strong inversion to moderate inversion [10].

Based on this application, we fix a case study described in Fig. 3.1: designing an inductorless wideband LNA with specifications aligned with the state-of-the-art of SDR or wideband LNAs described in Table 3.3 without using large and costly on-chip inductors. We target a 50Ω input impedance for compliance with existing antennas and a 15dB voltage gain on a 6GHz bandwidth. The bandwidth is defined as the frequency band in which the S_{11} parameter is lower than -10dB or the voltage gain has not dropped by more than 3dB. We also target an IIP2 over 20dBm and an IIP3 over 0dBm. The IIP2 and IIP3 are defined at 3GHz and with a two-tone analysis featuring a frequency spacing of 20MHz. Finally, we target a noise figure below 5dB and a total power below 1mW. The required specifications are summarized in Table 3.1.

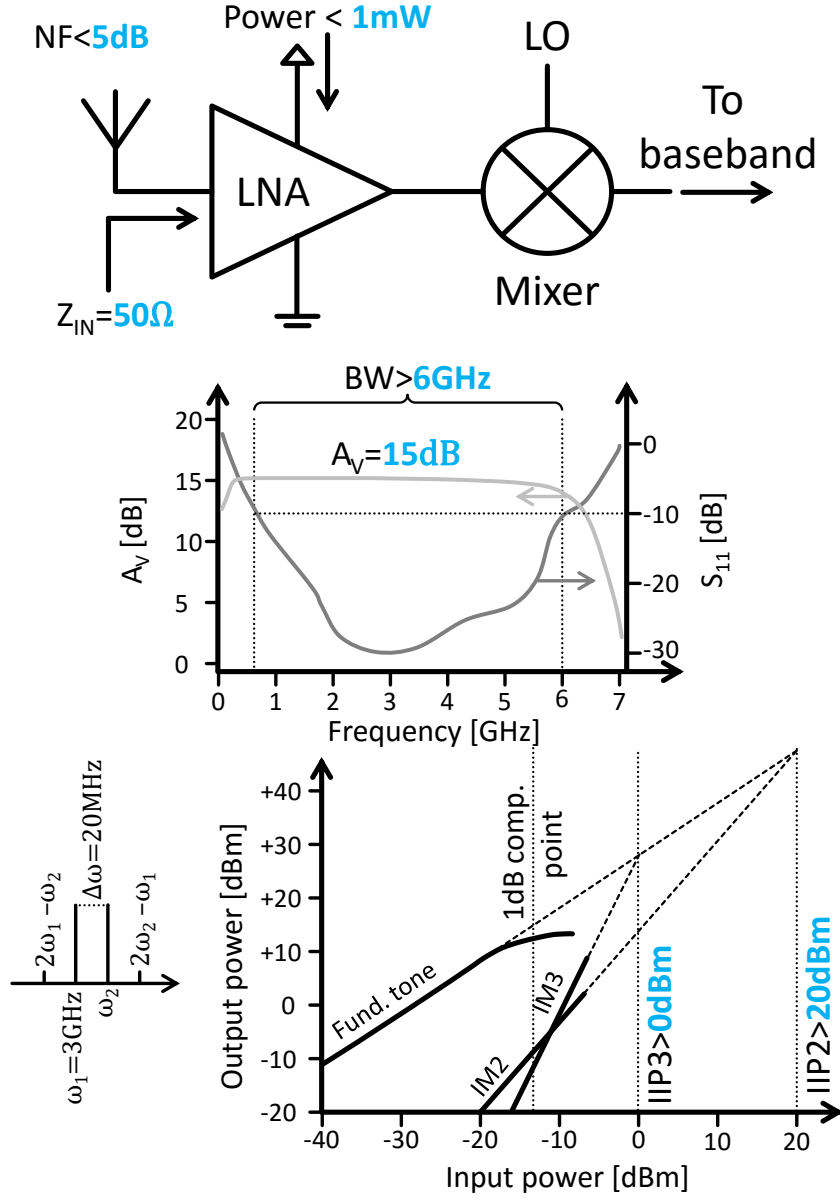


Fig. 3.1. Basic block diagram of the wideband receiver first two stages.

In this chapter, we study how technology scaling down to 28nm FDSOI and moderate inversion design can improve efficiency of LNAs for wideband applications through a 2-steps analysis:

Table 3.1. Targeted LNA specifications and performance requirements

Specification	
Z_{IN}	45-55 Ω
A_V	15dB
NF	< 5dB
IIP2	> 20dBm
IIP3	> 0dBm
Bandwidth	0-6GHz
Power	< 1mW
Inductor	NO

- At device level, we look at the impact of technology scaling and inversion level on RF-related Figures of Merit (FoM) such as f_T , thermal excess noise factor and transconductance.
- At circuit level, we use an efficient sizing framework to assess the impact of technology scaling and inversion level on a noise-cancelling wideband LNA.

We then show how a noise-cancelling architecture carefully sized in 28nm FDSOI can:

- circumvent the traditional inflexible tradeoff between NF, gain and input matching of wideband common-gate or resistive-feedback LNA architecture
- achieve sub-mW power at ultra-low-voltage thanks to moderate forward back biasing while maintaining good NF and bandwidth.

This chapter is organized as follows. Section 3.2 is centred on the impact of technology scaling on devices biased in moderate inversion through the analysis of RF figures of merit. Section 3.3 presents the LNA design methodology used to assess the impact of moderate inversion and technology scaling at block level. Section 3.4 presents and discusses the performances of a noise-cancelling LNA with technology and voltage scaling.

3.2 MODERATE INVERSION BIASED DEVICES FOR RF

3.2.1 Impact of voltage scaling

In modern mixed-signal RF SoCs, there are several incentives to scale down the supply voltage:

- The V_{DD} is scaling with technology for reliability reasons [14].
- Recent wideband receivers for SDR integrate several digital blocks in their RF front-end such as local oscillator generation or passive mixers and tend to move the analog-to-digital conversion closer to the RF input [15]. As digital logic energy efficiency is higher when scaling down the V_{DD} [17], the RF front-end is pushed to lower V_{DD} for voltage compatibility.
- Low V_{DD} allows operating on energy harvesting sources with reduced conversion losses or even without using a charge pump in the power management unit to obtain a higher voltage dedicated to the RF functionality [13].

This voltage scaling is moving the operating point of the devices from strong to moderate and even weak inversion. To illustrate this phenomenon, we look at 2 single device configurations: Common Gate (CG) and Common Source (CS) depicted in Fig. 3.2 that composed the LNA topology analysed in Section 3.3. The inversion level of each devices is measured through the Inversion Coefficient (IC) defined as in [16] and is based on the EKV modelling [12]:

$$IC = \frac{I_{DS}}{\frac{\mu C_{OX}}{2n} \frac{W}{L} (2nU_T)^2} \quad (3.1)$$

where n represents the slope factor and U_{th} , the thermal voltage.

We compute the minimum V_{DD} of the 2 configurations depending on the IC with the same method as in [10]. We suppose a typical signal amplitude of $V_{PP} = 2 \times U_{th}$ as well as a voltage drop of one $V_{DS,SAT}$ per biasing current source. The equations to obtain the minimum V_{DD} are for the CS configuration :

$$V_{DD} \geq 2 \times V_{DS,SAT} \quad (3.2)$$

$$V_{DD} \geq V_{PP} + V_{GS} \quad (3.3)$$

and for the CG configuration:

$$V_{DD} \geq V_{PP} + 3 \times V_{DS,SAT} \quad (3.4)$$

$$V_{DD} \geq V_{PP} + V_{GS} + V_{DS,SAT} \quad (3.5)$$

Fig. 3.2 presents simulation results in 28nm FDSOI of the minimum V_{DD} allowed in these conditions in function of the IC. We can observe that reducing the V_{DD} pushes the devices from Strong Inversion (SI) to Weak Inversion (WI) and that the CG configuration with a higher voltage headroom requirement is pushed faster in WI. Forward back biasing can be used to recover part of the design space lost when scaling down V_{DD} by reducing the threshold voltage and is thus an interesting tool to push RF devices at Ultra-Low Voltage (ULV).

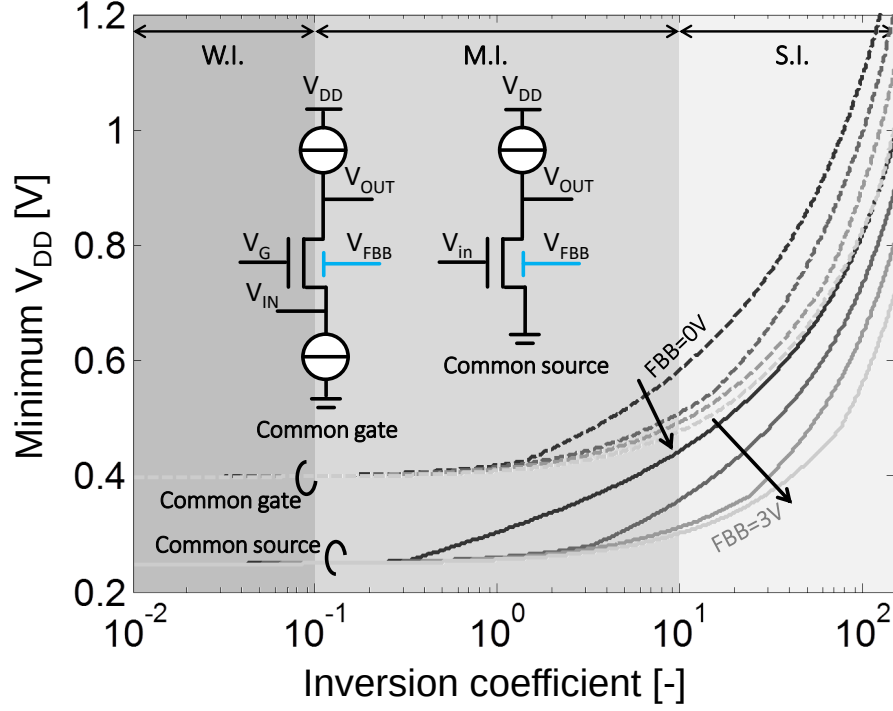


Fig. 3.2. SPICE simulations of the minimum V_{DD} depending on the IC for several V_{FBB} values in 28nm FDSOI and for 2 single-device amplifier configurations.

3.2.2 Impact of technology scaling

Shrinking device dimensions along with structure and material innovations has brought a tremendous increase in device transition frequency f_T . Fig. 3.3 depicts the f_T increase from $0.13\mu\text{m}$ to 28nm FDSOI showing a $25\times$ improvement that is kept approximately constant when varying the IC. This speed increase gives the designer the opportunity to trade f_T for power by reducing the IC value of the devices as will be shown in Section 3.3 and 3.4.

To look at the noise performances at device level, we use the thermal noise excess factor Γ based on the transconductance as defined in [9]. This excess factor is defined as the ratio between the thermal noise conductance and the transconductance:

$$\Gamma = \frac{G_n}{g_m} \quad (3.6)$$

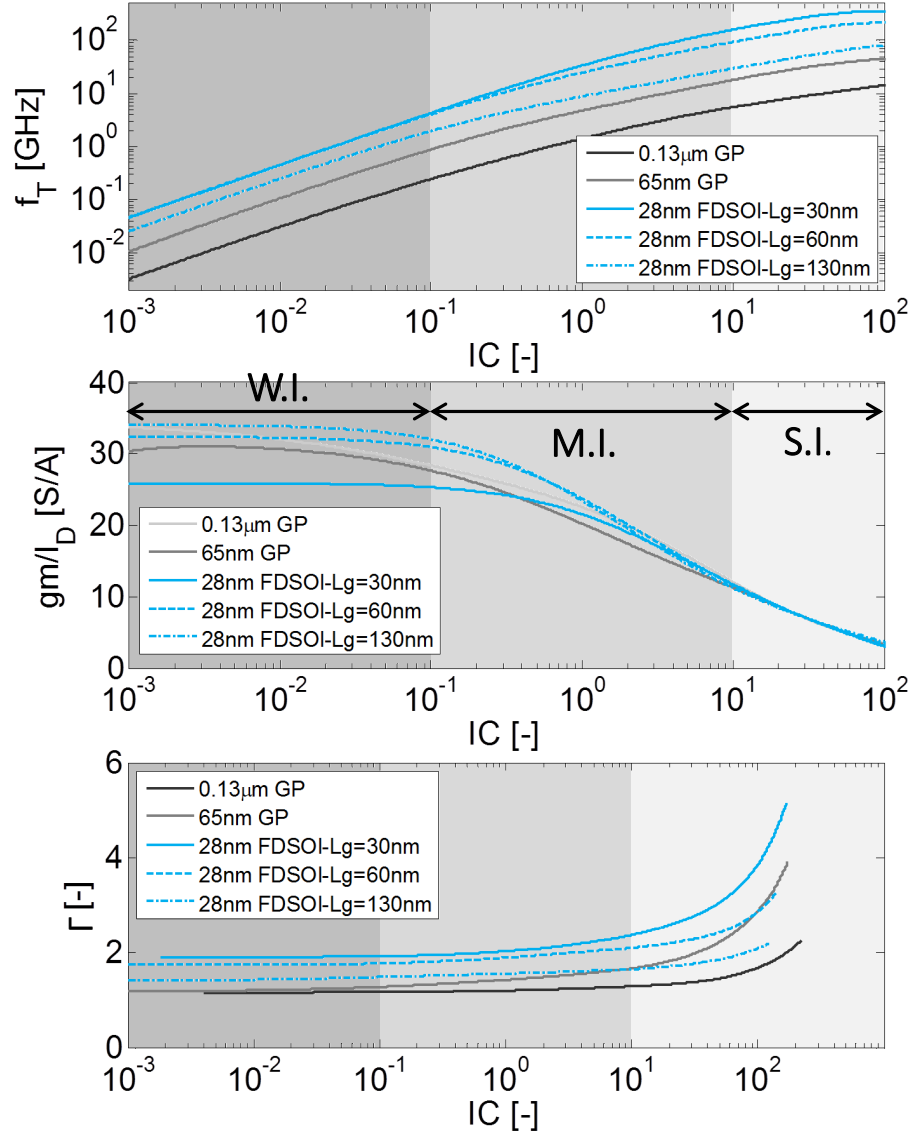


Fig. 3.3. SPICE simulations of f_T , gm/I_D r depending on IC for technology scaling from 130nm to 28nm FDSOI. In 28nm FDSOI, two different gate lengths ($L_g=30$ nm and $L_g=60$ nm) are compared.

where G_n is the thermal noise conductance and g_m the gate transconductance. This definition of excess noise is more relevant for circuit design than the more

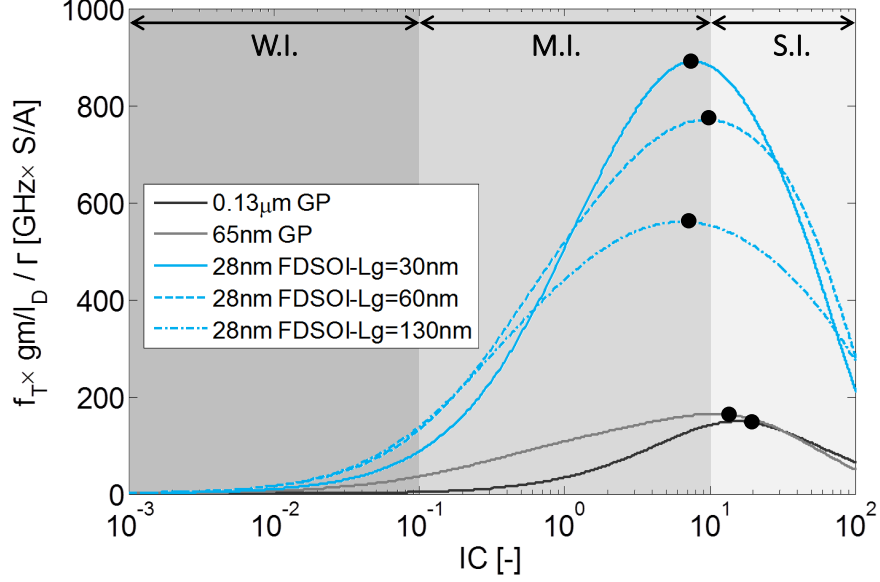


Fig. 3.4. Evolution of RF FoM_{dev} with technology scaling and IC. The increase from 65nm to 28nm FDSOI is more than 4× even when using an upsized gate length of 60nm to match the gate length of 65nm devices.

widespread excess factor defined with respect to the output conductance widely used in device modelling [8]. Indeed, Γ represents the cost in noise to generate a given transconductance. As shown in Fig. 3.3, the Γ is increasing in strong inversion as predicted by [11] and is degraded by technology scaling by short-channel effects and access resistances noise as modelled in [8].

Finally, to look at how technology scaling is globally influencing RF performances, we analyze three key device level FoMs: the f_T for speed, the Γ for noise and the g_m/I_D for DC gain and current efficiency. Wideband LNAs require high f_T , low noise and low-power leading to a challenging tradeoff to be found. To give some insight at device level, we group these three performances in a RF FoM_{dev} defined as:

$$FoM_{dev} = \frac{f_t \times g_m/I_D}{\Gamma} [GHz \times S/A]. \quad (3.7)$$

As shown in Fig. 3.4, this FoM_{dev} peaks at an optimum IC. This optimum operating point is slightly moving from strong inversion to moderate inversion with technology scaling. We can also observe that in order to achieve the same FoM_{dev} level in 28nm FDSOI compared to 65nm, we can reduce the IC by a factor 100 and thus reduce the bias current for the same device dimensions. The

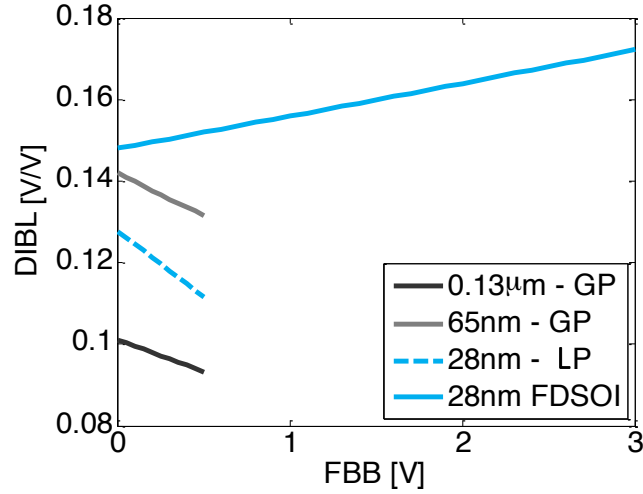


Fig. 3.5. Evolution of DIBL with FBB voltage on bulk technologies from $0.13\mu\text{m}$ to 28nm and on 28nm FDSOI with wide-FBB-voltage range.

linear dependence of FoM_{dev} favours minimum-length device because of the strong impact of gate length on f_T .

3.2.3 Impact of FBB

In addition to its impact on the V_T described in depth in Chap. 2, FBB has also an impact on drain control on the channel. The effect of drain voltage on the channel reduces the V_T (DIBL) but is also responsible for drain conductance degradation. In bulk technologies, FBB reduces the Drain-Induced Barrier Lowering (DIBL) by decreasing the size of the depletion region and have thus a positive impact as shown in Fig. 3.5. In Ultra Thin Body and Box (UTBB) FDSOI, as the channel is undoped, increasing the FBB does not influence the depletion regions size. However, it modifies the vertical position of the channel inside the Si body [6]. Fig. 3.6 illustrate the impact of FBB on mean channel position. Fig. 3.5 indicates that the DIBL is degraded by FBB in UTBB FDSOI and this phenomenon can be intuitively understood as the result of a reduction of the gate control over the channel.

In bulk technology, the reduction of the depletion region size leads to an improvement of the output conductance g_d and thus an increase of the device intrinsic gain g_m/g_d for a given IC as shown in Fig. 3.7. Indeed, for a fixed IC, the g_m variation with FBB is negligible as the device will keep the same inversion level. In FDSOI, the g_d and intrinsic gain of the device is degraded by the FBB due to the deeper channel position (Fig. 3.7). Applying FBB is thus no longer

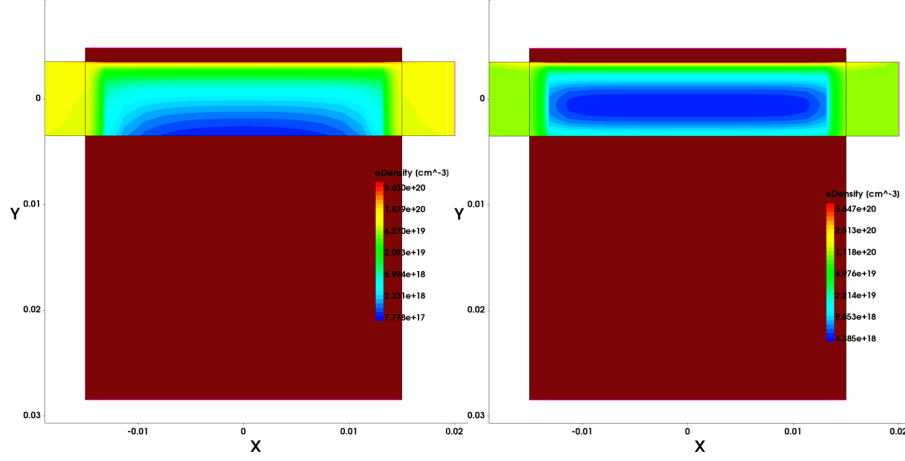


Fig. 3.6. TCAD simulation of the channel position in UTBB FDSOI device for 0V FBB (left) and 3V FBB (right).

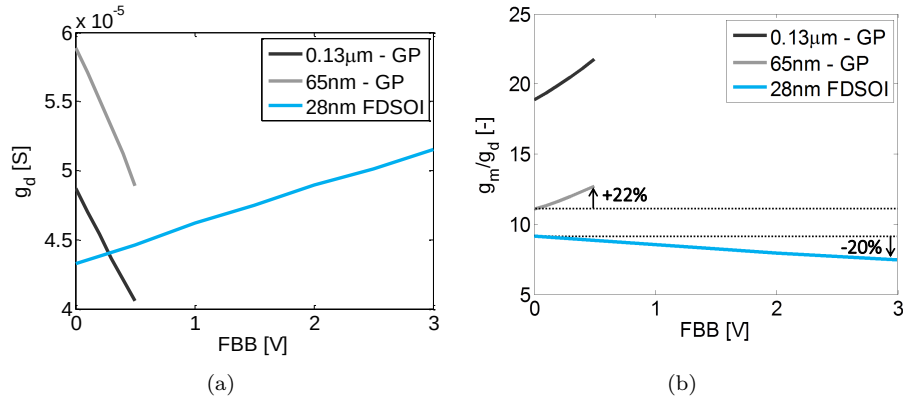


Fig. 3.7. Evolution of the output conductance g_d (a) and intrinsic device gain g_m/g_d (b) with FBB voltage. The degradation of the output conductance with FBB in FDSOI is directly linked to a reduction of the intrinsic device gain.

a cost-free operation regarding the analog performances and the 20% intrinsic gain degradation between FBB=0V and FBB=3V need to be taken into account when we study the usefulness of FBB for analog/RF applications. Indeed, there will be a tradeoff between the ability to reduce the V_{DD} at iso-performances and the intrinsic gain reduction with higher FBB.

3.3 EFFICIENT SIZING METHODOLOGY FOR NOISE-CANCELLING LOW NOISE AMPLIFIERS

To evaluate the impact of technology scaling and supply voltage reduction on RF performances at circuit level, we select a conventional wideband balun-LNA [2] based on the noise-cancelling topology from [3] shown in Fig. 3.8 along with the illustration of the noise-cancelling principle. This topology is well suited for wideband applications due to the separation between the common-gate stage setting the input matching and the common-source stage setting the voltage gain taking advantage of the wideband matching of the CG stage without its poor noise performances. Moreover, balun-LNAs offer lower second-order distortion, higher supply noise rejection and direct compatibility with the following mixer thanks to their differential output.

In the considered topology, the noise current of M_1 ($\overline{i_{M1}^2}$) generates a noise voltage at the input node of the amplifier as well as on the CG output node V_{OP} as shown in Fig. 3.8. The input noise voltage is amplified by the CS stage and is found at the CS output node V_{OM} in phase compared to the CG output node voltage noise. If the CS and CG voltage gain are equal, the noise contribution of M_1 is cancelled out while the signal contributions of both branches are in phase opposition. The same principle eliminates the distortion of M_1 as well.

To avoid the use of large on-chip inductors, the biasing of the CG stage uses a resistor R_B at the expense of some voltage headroom. The Degrees of Freedom (DoFs) of the LNA are the value and bias of all resistors and transistors as well as some general parameters: the transistors gate length (Lg), the forward back bias voltages in 28nm FDSOI and the supply voltage V_{DD} . The design objectives are summarized in Table 3.1 targetting a minimization of the Noise Figure (NF) and the power while restricting the input impedance matching to 50Ω , the voltage gain to $15dB$ and maximizing the 3^{rd} order intercept point (IIP3) as well as the bandwidth (BW). To compare the RF performances of wideband LNAs, we introduce two Figure of Merit (FoM_{LNA}) defined as:

$$FoM_{LNA,1} = \frac{Gain \times BW}{(F - 1) \times P_{TOT}} [GHz/mW]. \quad (3.8)$$

and,

$$FoM_{LNA,2} = \frac{Gain \times BW \times IIP3}{(F - 1) \times P_{TOT}} [GHz]. \quad (3.9)$$

A fair comparison on the impact of voltage and technology scaling on noise, bandwidth and power performances requires a uniform sizing framework. Such framework will also allow us to asses the impact of the global parameters such as transistor gate length (L) and forward back biasing in 28nm FDSOI. Even if some sizing tradeoffs have been studied in [2], [4] or [5], no global and efficient sizing method has been reported due to the high interaction level between all

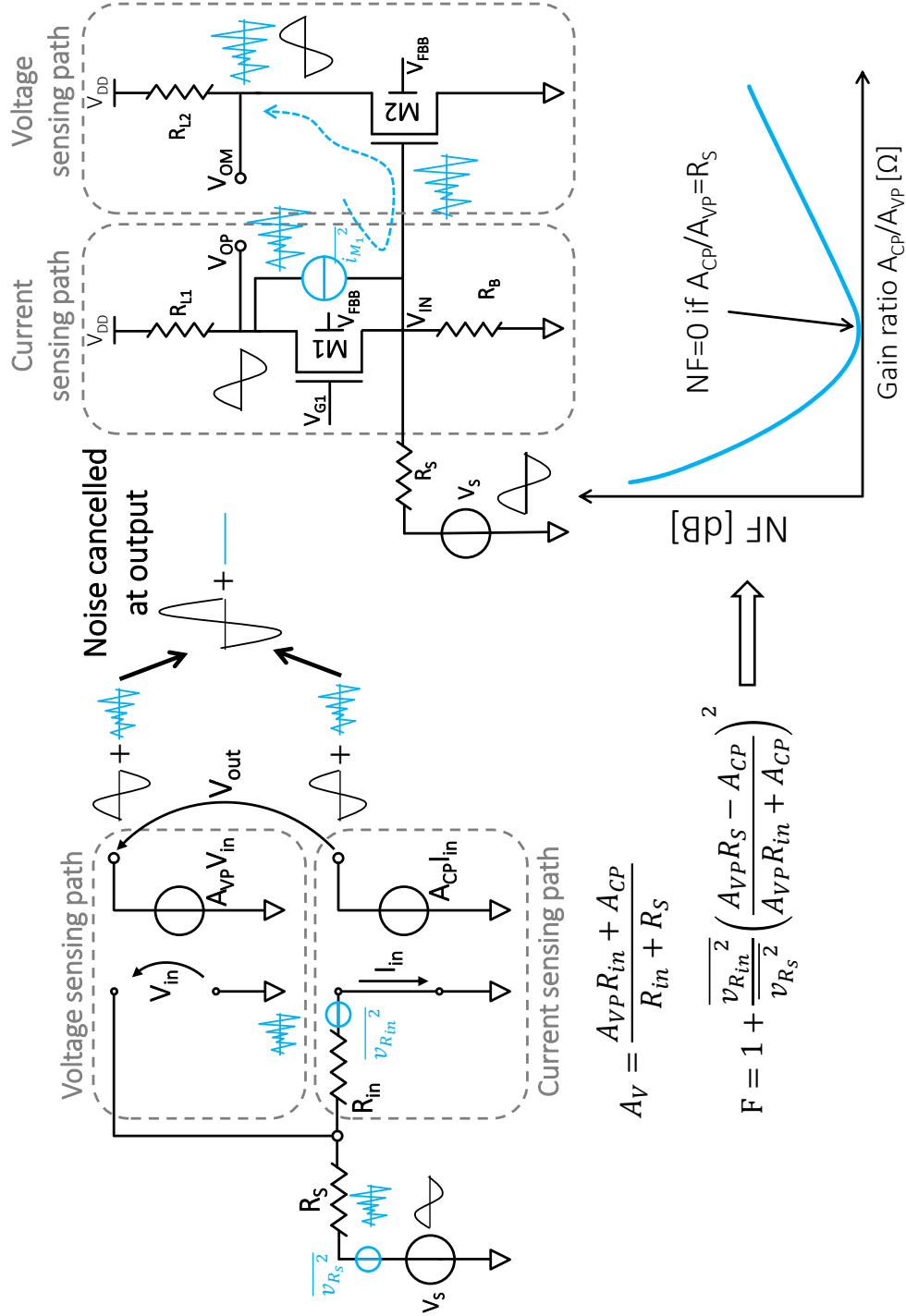


Fig. 3.8. Illustration of the noise cancelling principle. Right: schematic of the wideband balun LNA using a common gate (reps. common source) device to implement the current (resp. voltage) sensing path.

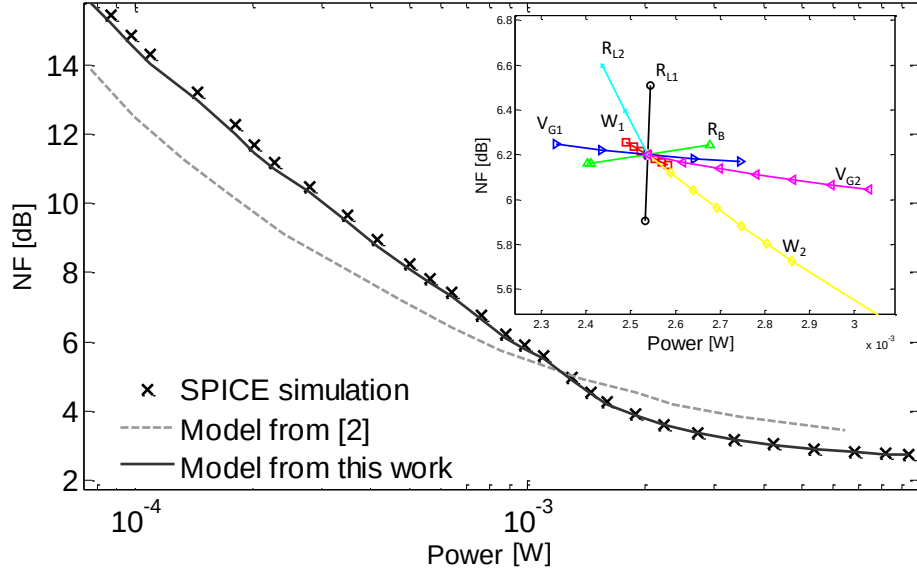


Fig. 3.9. Pareto curve of the optimal NF depending on the total power. The developed small signal model presents a good fit with SPICE simulations compared to the model proposed in [2]. Insert: evolution of NF with all 7 DoFs.

DoF and the FoMs. In advanced CMOS technologies, the approximations usually made when developing first-order small-signal analytical models lead to large errors compared to SPICE simulations, as shown in Fig. 3.9 for the NF for the model from [2]. Therefore, we developed an improved analytical AC model by taking into account the finite MOS output resistance, non ideal input matching and accurate sub-100nm CMOS noise model based on [8], which shows in Fig. 3.9 an excellent agreement with SPICE. The implementation details about the small-signal model can be found in Appendix A.

Nevertheless, analytical sizing guidelines are difficult to extract from this complete model. The insert in Fig. 3.9 shows the effect of all DoFs on NF illustrating the high level of interaction between them. In order to study the impact of the global DoF on FoMs, we developed a time-efficient sizing framework first presented in [7] and illustrated in Fig. 3.10 that minimize NF for varying power under the constraint of input matching and 15dB gain. A preselection of design points meeting these 2 constraints is first conducted using fast DC SPICE simulations. Following that, a reduced number of time-consuming noise simulations are performed for each preselected points and the NF, gain and BW are predicted using the developed analytical model. A total of 10^{10} design

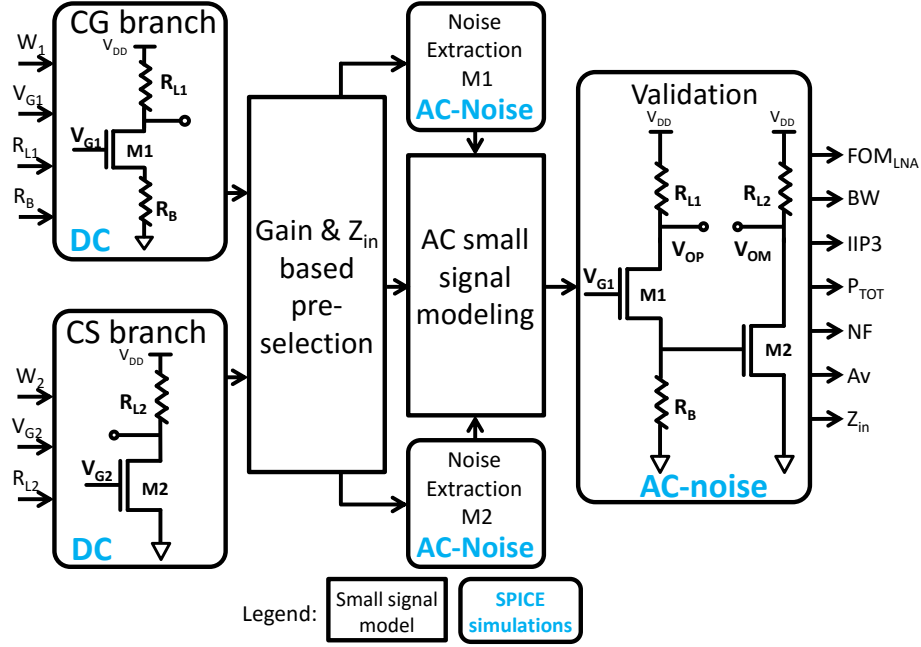


Fig. 3.10. Proposed automatic sizing framework. There are 7 DoFs distributed in 2 independent branches: the width and V_G of M_1 and M_2 and the value of R_{L1} , R_{L2} and R_B . The length and back bias of M_1 and M_2 as well as the supply voltage are considered as global parameters.

combinations are tested and only 4498 points on average are selected based on the gain and input impedance pre-selection process. On these pre-selected points, an average of 870 design combinations are selected based on the output of the small-signal model depending on the global variables such as V_{DD} , L_g and FBB. This allows us to validate through time-consuming noise simulations an average number of 0.09ppm of design combinations compared to brute force. We achieved an average speed-up of $120\times$ on an Intel Xeon 18-core CPU at 2GHz compared to brute force sizing.

The Pareto curve of NF vs. power regrouping the optimal points is selected as shown in Fig. 3.9 and validated through AC-noise SPICE simulations.

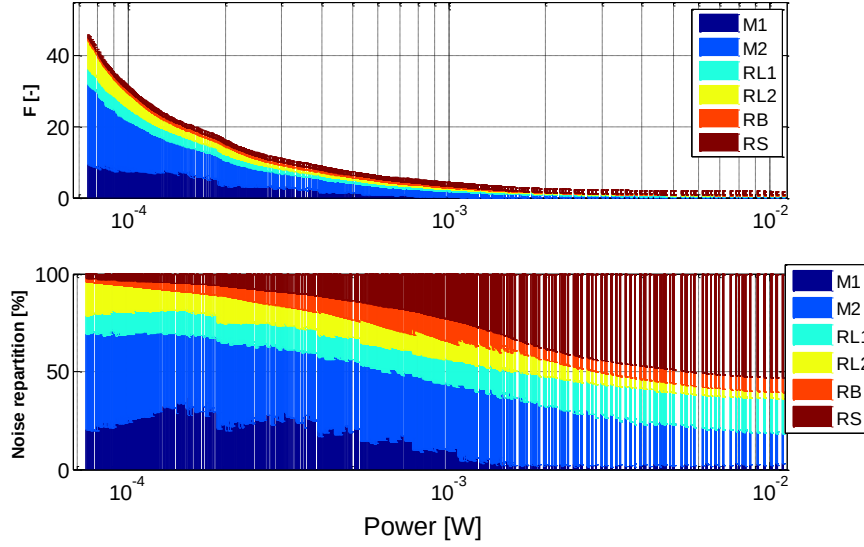


Fig. 3.11. Noise repartition between the passive and active elements of the LNA. M_2 noise is dominating over M_1 due to the noise cancelling effect. The noise of M_1 is more efficiently cancelled at high total power.

3.4 IMPACT ON WIDEBAND NOISE-CANCELLING LNA DESIGN

Fig. 3.11 shows the noise repartition between resistors and transistors. M_2 noise dominates all the contributions and M_1 noise is completely cancelled when the power targeted is over 1mW.

3.4.1 Impact of technology scaling

To study the impact of technology scaling on the LNA performances, we first look at the evolution of $FoM_{LNA,1}$ as shown in Fig. 3.12. The improvement of the peak $FoM_{LNA,1}$ between 28nm FDSOI and 65nm is almost $2\times$ as a direct result of the larger bandwidth for the same bias current as also illustrated in Fig. 3.12. The improvement of $FoM_{LNA,1}$ between $0.13\mu m$ and 65nm is less significant due to the limited bandwidth improvement and the slightly higher noise in 65nm alleviating the benefits of scaling between 65nm and $0.13\mu m$. We can also observe that, at high power, the $FoM_{LNA,1}$ is not improving with power due to bandwidth and power limitations.

Finally, Fig. 3.12 presents the mean IC of the 2 devices after sizing by the framework and depending on the power. We can see that, as anticipated at device level in Section 3.2, the two transistors are pushed toward moderate inversion

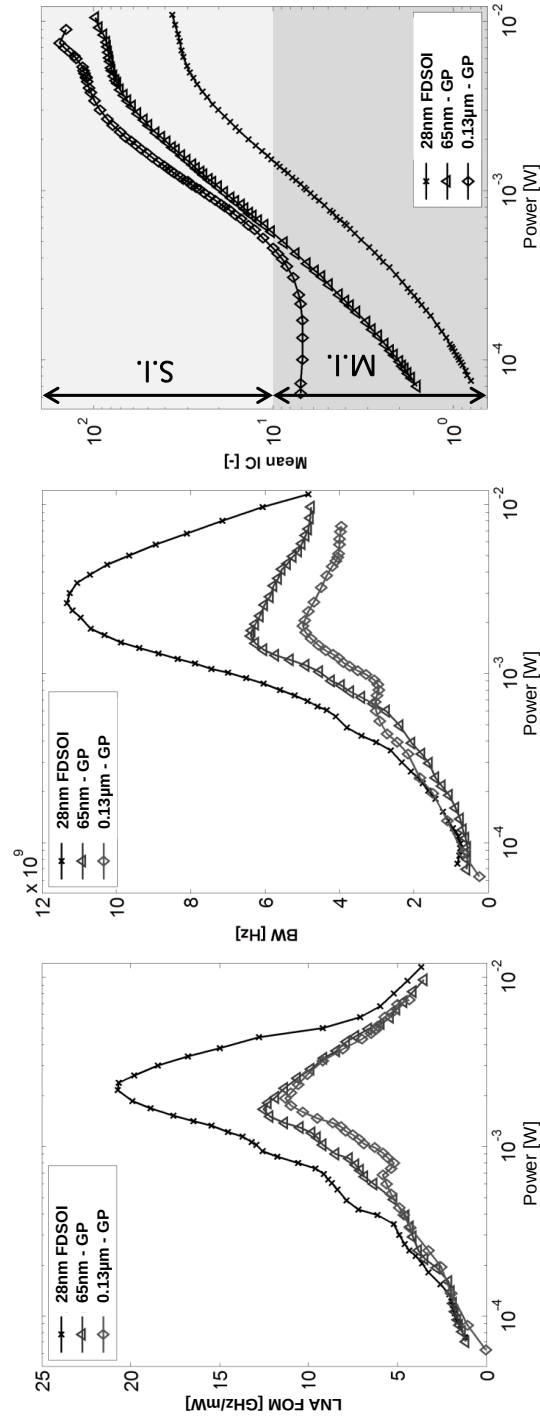


Fig. 3.12. Evolution of $FoM_{LNA,1}$, BW and mean IC with technology scaling.

when we scale down the technology node. We also observe that, at $1mW$, the optimum LNA designed features a mean IC of 10 which is the optimum design point from the FoM_{dev} point of view.

3.4.2 Impact of voltage scaling

As illustrated in Fig. 3.13, there is a power at which the LNA achieves the higher $FoM_{LNA,1}$. Interestingly, at lower V_{DD} values, this optimal point is obtained at lower power at the cost of a lower $FoM_{LNA,1}$. The higher $FoM_{LNA,1}$ value is achieved at the minimum $30nm$ gate length. Using larger lengths indeed degrades the $FoM_{LNA,1}$ through a BW degradation due to a f_T reduction (Fig. 3.13). The reduction of V_{DD} causes only a slight reduction of the maximum BW. Fig. 3.13 also shows the evolution of NF with power as well as the IIP3 for the optimal points. The maximum IIP3 is reduced when scaling V_{DD} and the optimal IIP3 is brought down to lower power. Finally, Fig. 3.13 shows the impact of gate length upsize on IIP3 and NF. As expected and due to the plotting with respect to the total power, we see limited impact of gate length variation on NF. When looking at the linearity, drawing conclusions is more challenging as the framework does not optimize with respect to IIP3. Nevertheless, we can see that from $L_g = 30nm$ to $L_g = 50nm$ the IIP3 is improved due to an increased intrinsic gain gm/gd . Over $L_g = 50nm$, achieving the BW target becomes challenging for the framework and the increased biasing lead to lower IIP3 values.

3.4.3 Impact of back biasing

Fig. 3.14 shows the impact of the back biasing on the minimum NF and maximum $FoM_{LNA,1}$ achievable with the sizing framework. Moderate BB is helpful as it allows to achieve close to 0.5dB of reduction in the minimum NF achievable. The $FoM_{LNA,1}$ is also boosted by 26% with a moderate BB. At large BB, the reduction of the intrinsic gain of the devices reduces the RF performances achievable by the wideband LNA and both the minimum NF and $FoM_{LNA,1}$ are rising for $FBB > 1V$.

Fig. 3.15 further illustrates the penalty in term of minimum NF achievable induced by the supply voltage scaling and how moderate forward back biasing of M_1 and M_2 can help mitigate this effect. With 500mV of FBB voltage at $V_{DD} = 0.4V$, we can improve the minimum NF while strongly reducing the power at which 5dB NF is achieved. As suggested in Fig. 3.2, this is a result of the widened design space accessible by the sizing framework leading to a higher maximum IC achievable in the limited voltage headroom.

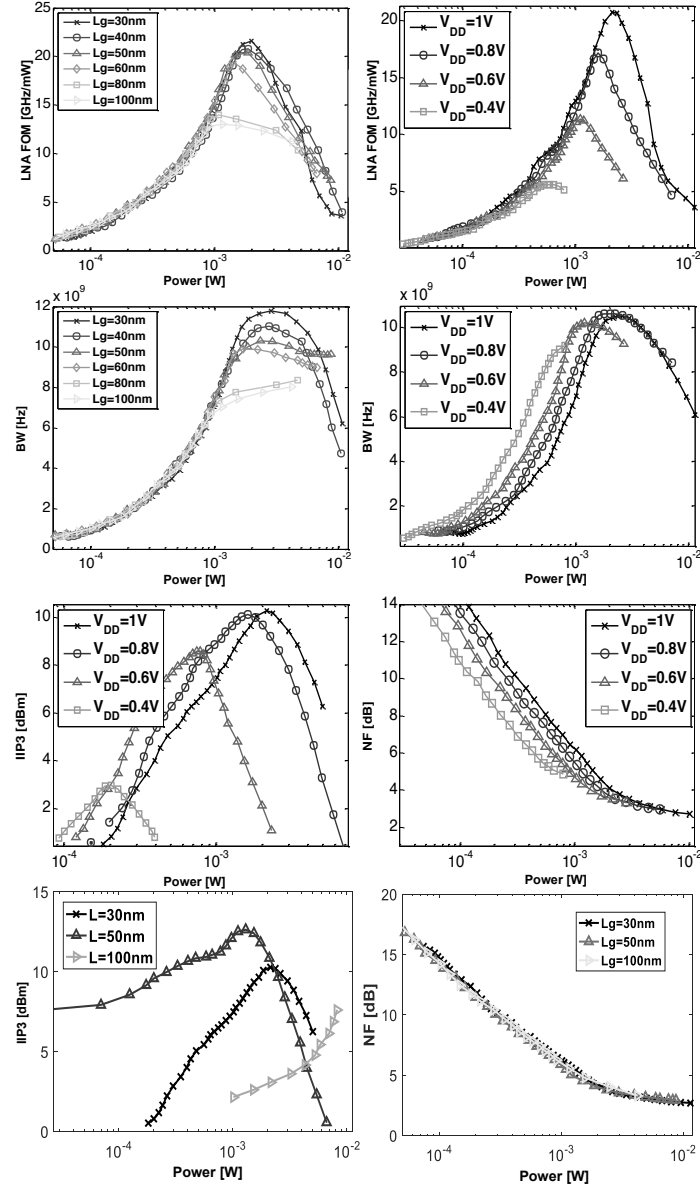


Fig. 3.13. Evolution of $FoM_{LNA,1}$, BW, IIP3 and NF with transistor length and V_{DD} in 28nm FDSOI.

3.5 DISCUSSION & CONCLUSIONS

Fig. 3.16 illustrates the NF performance of the wideband LNA sized at nominal voltage and at ULV with FBB as well as recently published wideband LNA

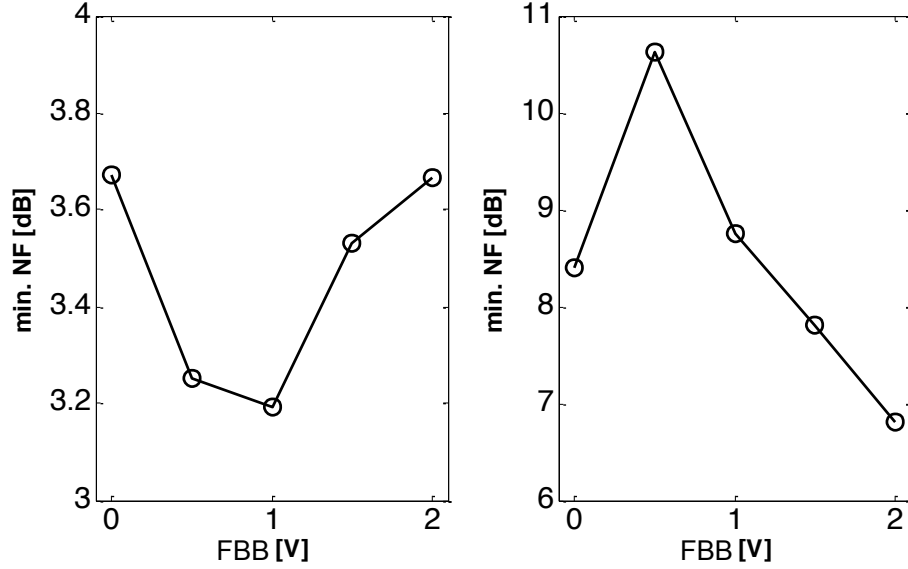


Fig. 3.14. Evolution of minimum NF and maximum $FoM_{LNA,1}$ achievable depending on the back biasing voltage.

detailed in Tab. 3.3. At nominal voltage, we are able to achieve lower NF for a power budget between 1mW and 3mW compared to the state-of-the-art. At ULV, this NF curve is shifted to lower power at the cost of a minimum achievable NF higher compared to LNA sized at nominal voltage.

Fig. 3.17 shows the comparison between the two FoM_{LNA} taking or not into account the IIP3 and the state-of-the-art in order to include it in a fair performance assessment. We can observe that the LNA sized at nominal voltage outperforms the state-of-the-art by at least $2\times$ in terms of $FoM_{LNA,1}$. The $FoM_{LNA,1}$ is strongly diminished when we operate at ULV but we are able to achieve comparable values to the state-of-the-art at power below 1mW. The same conclusions can be drawn from the examination of $FoM_{LNA,2}$ but we need to keep in mind that the results presented in this work are only based on simulations and not on measurements.

In order to compare the results of our framework to recently published wideband LNAs, we select two design points from Fig. 3.17: one at ULV and one at nominal voltage. The point selected at ULV targets the absolute minimum power while the point at nominal voltage is selected at the maximum of $FoM_{LNA,1}$. The sizing values obtained with the proposed sizing methodology are shown in Table

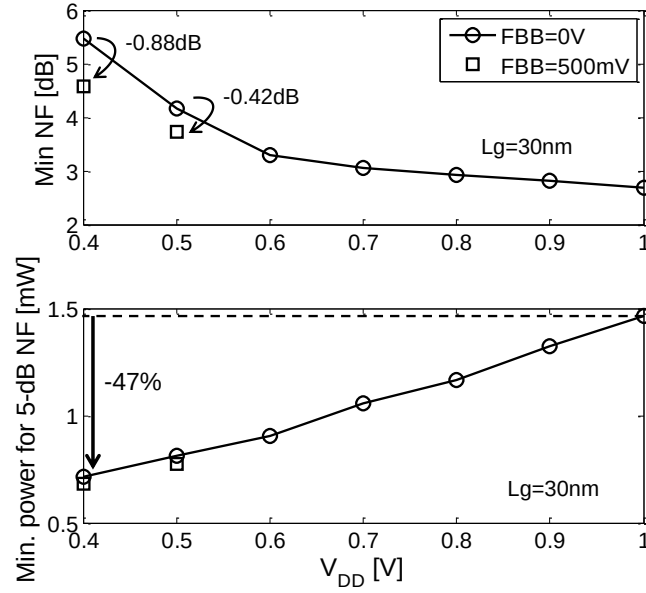


Fig. 3.15. Evolution of minimum NF and power for 5dB NF with V_{DD} .

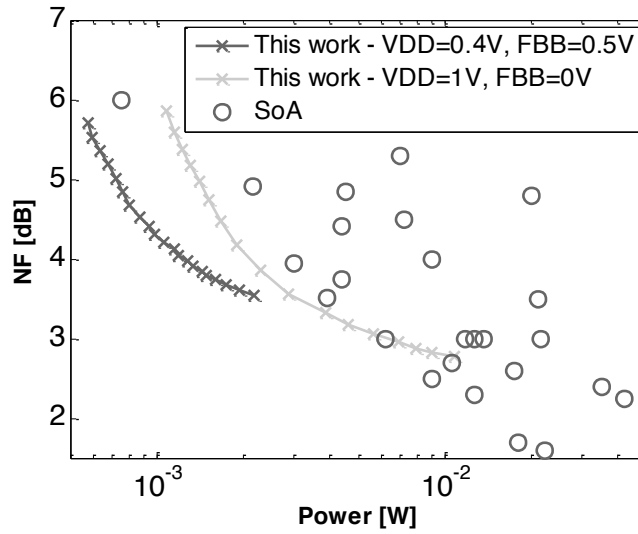


Fig. 3.16. Comparison of the state-of-the-art of wideband LNAs (with a BW over 1GHz) based on the NF.

3.2 The performances of both of these LNAs are summarized and compared to the state-of-the-art in Table 3.3.

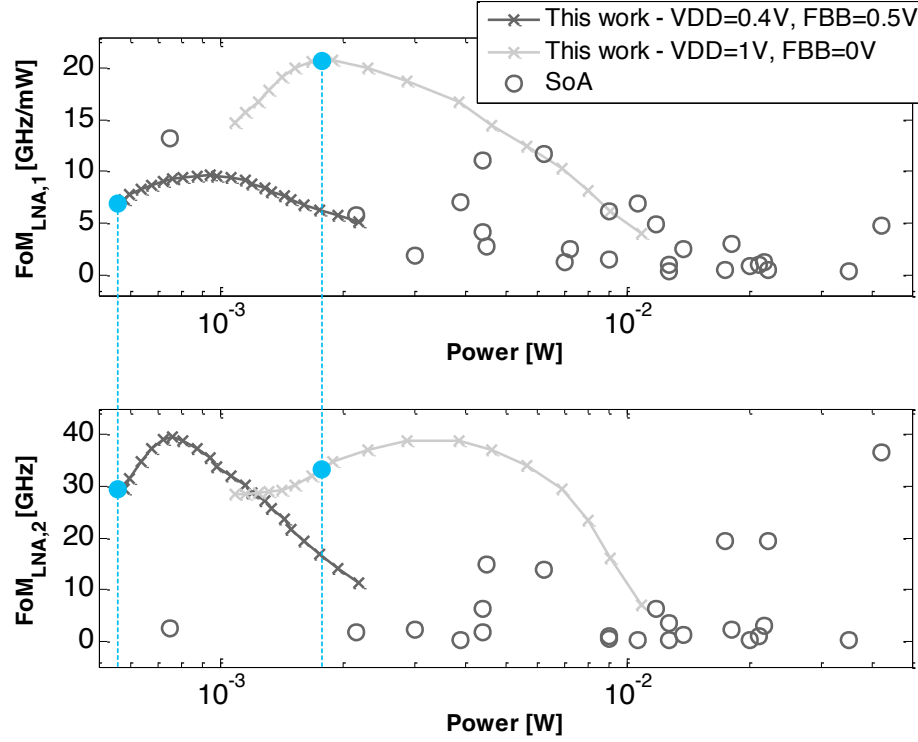


Fig. 3.17. Comparison of the state-of-the-art of wideband LNAs (with a BW over 1GHz) based on the $FoM_{LNA,1}$ and $FoM_{LNA,2}$. The selected design points are highlighted in blue targeting an absolute minimum power and a maximum $FoM_{LNA,1}$ value.

Table 3.2. Optimal sizing values at 30nm device length

This work	M1	M2	RL1	RL2	RB
$V_{DD} = 0.4V$ $FBB = 0.5V$	119 μm	83.7 μm	500 Ω	570 Ω	80 Ω
$V_{DD} = 1V$ $FBB = 0V$	139 μm	98.4 μm	200 Ω	180 Ω	330 Ω

Fig. 3.18 represents the evolution of 2 typical SDR-type constraints with technology and voltage scaling. We see that the bandwidth constraint is the most severe in 0.13 μm CMOS but that the increasing f_T with technology scaling mitigate this limit. In 65nm, a 6GHz bandwidth constraint will be more strict than the 5dB NF requirement but if we target only 5GHz, then the main constraint switches to the NF. For 28nm FDSOI, the minimum power is set by the NF

Table 3.3. Comparison with state-of-the-art of recent wideband LNA

Paper	Bandwidth [GHz]	Architecture	Balun?	Inductor?	Power [mW]	NF [dB]	IIP3 [dBm]	Tech.	A_V [dB]	$FoM_{LNA,1}$ [GHz/mW]	$FoM_{LNA,2}$ [GHz]
[31]	0.002-2.3	NC	No*	No	18	1.7	-1.5	90nm	21	2.99	2.11
[32]	0.1-5.9	NC	Yes	No	6.2	3	0.7	0.13 μ m	21.9	11.7	13.7
[33]	0.1-2	NC	Yes	No	3	4.15	0.5	0.13 μ m	7.6	1.9	2.14
[25]	0.2-3.8	NC	No*	No	5.7	3.4	-4.2	0.13 μ m	19	4.17	1.66
[2]	0.2-5.2	NC	Yes	No	21	3.5	0	65nm	13	0.99	0.99
[34]	0-10	NC	Yes	No	13.7	3.3	-3.5	65nm	10.5	2.46	1.1
[3]	0.002-1.6	NC	No	No	35	2.4	0	0.25 μ m	13.7	0.3	0.3
[35]	1.2-11.9	NC	No	Yes	20	5.1	-6.2	0.18 μ m	9.7	0.8	0.19
[36]	0.8-2.1	NC	No	No	17.4	2.6	16	0.13 μ m	14.5	0.48	19.2
[37]	2-4.6	Cascode CS bandpass filter	No	Yes	12.6	2.3	-7	0.18 μ m	9.8	0.91	0.18
[38]	0.05-1	NC	No*	No	22.1	1.6	16.6	0.13 μ m	12.4	0.42	19.35
[39]	0-2.1	NC	No*	No	12.6	3	10.5	0.13 μ m	5.2	0.3	3.42
[40]	2.3-9.2	Cascode CS + ind. degeneration	No	Yes	9	4	-6.7	0.18 μ m	9.3	1.48	0.32
[41]	0.1-6.5	NC	No	Yes	10.6	3.3	-16	0.18 μ m	18.5	4.9	6.2
[42]	3.1-10.3	NC	No	Yes	10.6	3.3	-16	0.18 μ m	18.5	6.9	0.17
[43]	2.7-9.1	Distributed	No	Yes	7	4.5	NA	0.13 μ m	10	1.21	NA
[19]	0.5-8.2	resistive feedback	No	No	42	2.6	8.8	90nm	25	4.8	36.4
[23]	2.6-10.5	CG + matched input network	No	Yes	2.15	4.9	-5.4	0.18 μ m	10.4	5.8	1.67
[24]	2.6-10.2	2-stage CG + CS	No	Yes	7.2	5	NA	90nm	12.5	2.44	NA
[28]	3.1-10.6	2-stage CG + CS	No	Yes	3.89	3.51	-13.8	0.18 μ m	13.2	7.08	0.29
[27]	3.1-10.6	Cascode CS + matched input net.	No	Yes	21.6	3	4	90nm	10.48	1.16	2.93
[20]	0.1-20	Cascode CS + resistive feedback	No	Yes	12.6	4.4	-2.5	90nm	12.7	11.1	6.25
[22]	3.1-10.6	2-stage resistive feedback	No	Yes	9	2.5	-8.5	0.13 μ m	15.1	6.1	0.86
[21]	1.3-10.7	Cascode CS + inductive peak.	No*	Yes	4.5	5.3	7.4	0.18 μ m	8.5	2.7	14.9
[29]	0.1-7	Cascode CS + resistive feedback	No	Yes	0.75	6	-7	90nm	12.6	13.1	2.34
This work $V_{DD} = 0.4V$ $FBB = 0.5V$	0-6.3	NC	Yes	No	0.55	5.6	8.9	28nm FDSOI	15	7.3	29.4
This work $V_{DD} = 1V$ $FBB = 0V$	0-11.7	NC	Yes	No	1.8	4.1	13.5	28nm FDSOI	15	20.7	34.8

* differential output but requires differential input.

constraint only. We also observe that 28nm FDSOI allows 23% power savings compared to 0.13 μ m under both bandwidth and NF constraints. The excess f_T can further be traded for power efficiency through ULV operation down to 0.5V while improving the minimum power set by the NF constraint. A reduction of the supply voltage yields a linear reduction in the minimum power to meet the NF constraint, although it degrades the minimum achievable NF. With a 0.5V FBB in FDSOI, it is possible to meet both the bandwidth and the NF constraints at 0.4V with 54% power savings compared to 1V operation, thereby reaching sub-mW operation.

In this chapter, we studied the impact of technology and voltage scaling for ultra-low-power RF design from the device point of view up to the circuit level. We illustrated the potential of 28nm FDSOI at device level to trade f_T for power

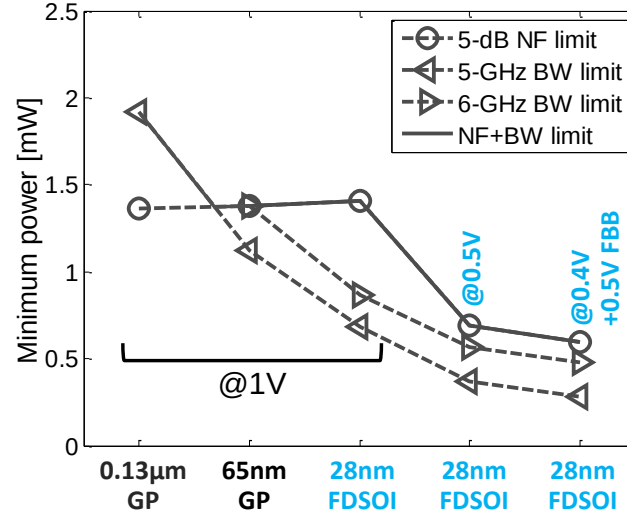


Fig. 3.18. Evolution of the minimum power limit set by bandwidth and noise figure constraints.

efficiency to keep high FoM_{dev} value even in moderate inversion. At circuit level, we showed that NF minimization under constraints for wideband noise-cancelling LNA leads to competitive RF performances for SDR applications. ULV operation is possible in 28nm FDSOI thanks to the high f_T and allows reaching sub-1mW power with acceptable RF and noise performances. We also showed that, combined with moderate FBB, ULV operation saves 47% power at 5dB NF. We demonstrated that technology and voltage scaling on the noise-cancelling LNA leads to a shift of the dominant design constraint from bandwidth to noise as shown in Fig. 3.18.

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CHAPTER 4

SLEEPTALKER: AN ULTRA-LOW VOLTAGE
UWB TRANSMITTER SOC FEATURING
PROGRAMMABLE PULSE SHAPING,
ADAPTIVE-FBB-BASED CHANNEL
SELECTION AND PVT COMPENSATION

Abstract

Achieving wireless communications at 5-30Mb/s in energy-harvesting Internet-of-Things (IoT) applications requires energy efficiencies better than 100pJ/bit. Impulse-radio ultra-wideband (UWB) communications offer an efficient way to achieve high data rate at ultra-low power for short-range links. We propose a digital UWB transmitter System-on-Chip (SoC) designed for ultra-low voltage in 28nm FDSOI CMOS. It features a PLL-free architecture, which exploits the duty cycling nature of impulse radio through aggressive duty cycling within the pulse modulation time slot for high energy efficiency and minimum jitter accumulation. Wide-range on-chip adaptive Forward Back Biasing (FBB) is used for threshold voltage reduction, PVT compensation and tuning of both the carrier frequency and the output power. To ensure spectral compliance with output power regulations without the use of bulky and expensive off-chip filters, a programmable pulse shaping functionality is integrated in the digital power amplifier based on a 7-9GS/s 5-bit current DAC. Operated at 0.55V, it achieves a record energy efficiency of 14pJ/bit for the transmitter alone and 24pJ/bit for the complete SoC with embedded power management. The transmitter SoC occupies a core area of 0.93mm².

Contents

4.1	Introduction	79
4.2	Architecture of the duty-cycled PLL-free TX system	81
4.3	Design and implementation of the TX	83
4.4	SoC integration	96
4.5	Experimental Validation	101
4.6	Conclusion	110

4.1 INTRODUCTION

The deployment of the IoT ubiquitous sensing paradigm is constrained by the development of the four functions usually embedded in a Wireless Sensor Node (WSN) as shown in Fig. 1.1. To avoid the economical cost and environmental footprint of battery replacement [1], the WNSs need to operate on an energy-harvesting basis. This introduces strong constraints on the power consumption of the sensing, data processing and RF transceiver, which communicates the sensed data to the cloud. Data processing such as feature extraction or compression can help reducing the power consumption by reducing the required data rate. However, even with strong on-chip data processing, fitting the radio component inside the harvesting power budget is challenging. Many new wireless solutions tackling this have recently appeared such as [2] or [3]. They usually solve the power problem with duty-cycled radios taking advantage of the low data rate requirement of the sensing applications. However, applications such as vision or large distributed WSN networks, call for medium data rates above 5Mb/s or for low communication latency.

Impulse Radio Ultra-Wideband (IR-UWB) communication is a promising solution for high data rate, short-range and low-power communication due to the duty-cycled nature of the output signal as well as the potential for low-complexity and low-power transmitter (TX) architectures [4]. These characteristics have been the driving force behind the development of the IEEE 802.14.4a standard [5] covering data rates from 0.11 to 27.24Mb/s. Nevertheless, current full 802.15.4a TX can hardly achieve energy efficiency better than 200pJ/bit which corresponds to a prohibitive communication power around 3.5mW at 27Mb/s.

There are three critical functions that need to be carefully designed in an IR-UWB TX in order to achieve high energy-efficiency: the frequency synthesis, the power amplification and the spectrum compliance. Frequency synthesis can be done with a PLL [23] [16] which is difficult to fit in the tight power budget set by the application or with an LC-tank-based oscillator [24] [19] [25] [26] [27] integrating bulky inductors. Both of these solutions also feature a long start-up time limiting the duty-cycling capabilities. Alternatively, delay-element-based edge recombination [28] [29] [30] or ring oscillators [31] [21] can achieve lower power consumption and faster settling time. Unfortunately, the delay element tuning usually implemented through current starving reduces the jitter performance as well as the ability to operate with a reduced supply voltage.

Power amplification can be achieved with an analog RF amplifier [28] [23] at the cost of a large static power dissipation or with a digital power amplifier [4] [32]. However, digital implementations feature high DC spectrum component that may lead to violation of the stringent FCC regulation [6].

Spectrum compliance is a critical challenge for a fully-integrated IR-UWB TX. Previous work rely on balun or off-chip filters [16] [27] [28] to filter the low-frequency content generated by digital power amplifiers imposing large on-chip passive elements or off-chip components. In [25], [4] and [28], on-chip filtering solutions based on finite impulse response filter integrated in the pulse generation or in the power amplifier are proposed in order to achieve a high level of integration.

This chapter presents SleepTalker: a fully-integrated versatile IR-UWB TX System-on-Chip (SoC) compliant with the IEEE 802.15.4a standard and implemented in 28nm FDSOI. The key contributions of this work are the following ones.

- A PLL-free architecture is proposed with an aggressive duty cycling of the local oscillator is used within the Binary Position Modulation (BPM) time slot to reduce jitter accumulation and power consumption.
- Programmable pulse shaping is implemented by a digital Power Amplifier (PA) to avoid the need for bulky off-chip filters while meeting spectral compliance with the FCC regulation [6].
- High-speed Ultra-Low-Voltage (ULV) digital implementation enabled by the 28nm FDSOI process with wide-range $\pm 1.8\text{V}$ Forward Back Biasing (FBB) and new retentive True Single Phase Clocked (TSPC) flip-flops.
- On-chip adaptive FBB for tuning both the Carrier Frequency (CF) of the Back-Bias-Controlled Ring Oscillator (BBCO) as local oscillator between 3.5 and 4.5GHz for channel selection and the PA output power.
- Continuous-time NMOS/PMOS current matching loop through adaptive FBB with a back-gate-driven amplifier for voltage range compatibility.
- Embedded power management featuring a high-density DC/DC converter for 0.55V generation and butterfly-connected charge pumps to generate the $\pm 1.8\text{V}$ used for the FBB generation.

The prototype presented in this chapter can be though as a demonstrator of the key concepts analyzed in Chapter 2. We indeed show how adaptive BB can be used in digital RF architecture to achieve high energy-efficiency while still maintaining high speed at the frequency is constrained by the communication standard.

This chapter is organized as follows. The TX architecture is presented in Section 4.2. The design and implementation of key blocks are detailed in Section 4.3. Section 4.4 describes the SoC architecture and Section 4.5 presents the measurement results and performance comparison to the related state-of-the-art.

4.2 ARCHITECTURE OF THE DUTY-CYCLED PLL-FREE TX SYSTEM

Impulse radio ultra-wideband communication stand-out by their inherently duty-cycled nature enabling high efficiency transmitter design. The IEEE 802.15.4a standard [5] aims at maximizing this feature by concatenating pulses into bursts while maintaining a constant Pulse Repetition Frequency (PRF) to keep the average output power constant over a wide range of data rates from 0.11Mb/s to 27.24Mb/s.

To take advantage of the strongly duty-cycled nature of IEEE 802.15.4a IR-UWB signals, we aim at aggressively duty-cycling the majority of the TX right from the Local Oscillator (LO) with a PLL-free architecture.

Three levels of duty cycling are implemented. First, the packet-level baseband keeps the rest of the TX idle between two transmitted packets. Second, at symbol-level, the TX is idle in both guard intervals as well as in the unused BPM time slot (Fig. 4.1). Finally, the LO is enabled (ENABLE_LO signal) within the BPM time slot only when the pulse burst need to be emitted with a granularity of 16ns i.e. half of the reference 31.25MHz clock period, as described in Fig. 4.1. In the fast 27.24Mb/s data rate, the LO is running during 1/4 of the 64ns symbol clock period. In slower data rates, the LO is running for maximum 32ns except in the 0.11Mb/s data rate for which the LO should run for the total burst duration of 64ns. Such an aggressive duty cycling of the LO directly results in strong power savings as the subsequent TX logic is idle when the LO output remains static.

Fig. 4.2 illustrates the TX architecture. It is built from a single 31.25MHz reference crystal clock from which all necessary high-frequency clocks are generated in the duty-cycled frequency synthesis block. It features a 3.5-4.5GHz LO whose frequency is divided to generate a 500MHz internal clock with a 2ns period corresponding to the pulse duration. The calibration of the LO frequency is performed periodically as triggered by the TRIG.CALIB signal by a calibration loop built around the BBCO. The TX covers 7 data rates defined in the 802.15.4a standard summarized in Table 4.1. The symbol clock generated from the 31.25MHz reference varies depending on the selected data rate from 122kHz to 15.6MHz.

To perform the within-BPM LO duty cycling, the coarse burst position inside the BPM time slot is computed with a 32ns time resolution with the output of the IEEE 802.15.4a Linear Feedback Shift Register (LFSR) implementing the pulse position scrambling in the symbol-level baseband. Inside this 32ns window, the pulse-level baseband implements the fine-grain burst positioning by enabling the pulse-shaping power amplifier through the ENABLE_PA signal during only the burst duration ranging from 2ns to 32ns (64ns in the 0.11Mb/s data rate). Finally, a high-efficiency digital PA performs programmable pulse shaping for compliance with output power spectrum regulations. An SPI port is used for

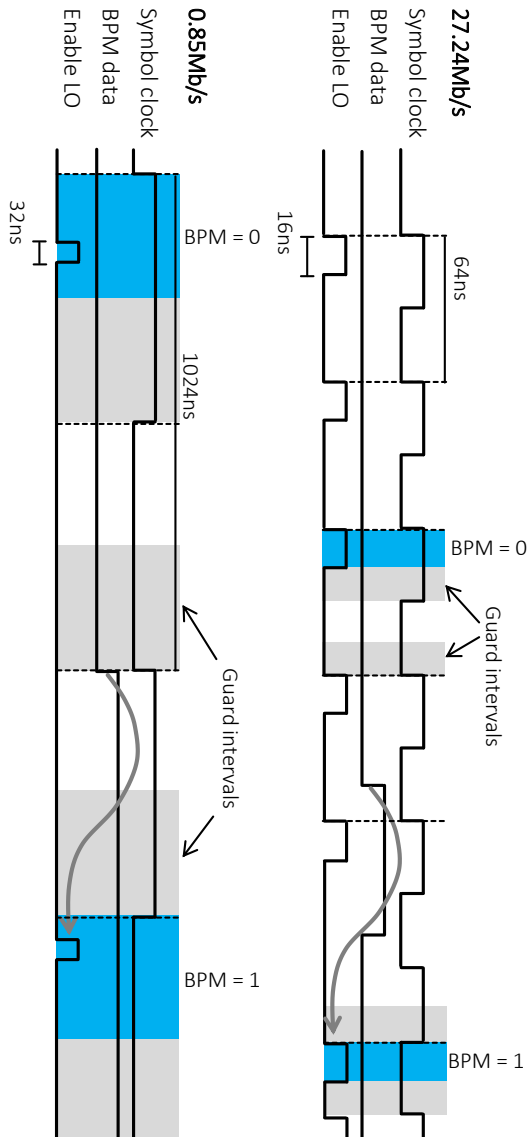


Fig. 4.1. Aggressive LO duty-cycling principle illustrated by waveforms of the LO enabling signal for two data rates. At high data rate (top), the LO is active for a quarter of the symbol duration which corresponds to the BPM time slot and half a reference crystal-clock cycle. At low data rate (bottom), the LO is active for one cycle of the crystal clock and the position of the pulse inside the quarter symbol duration is computed in the symbol-level baseband.

Table 4.1. Supported IEEE 802.15.4a data rates

Mode ID	Channels [GHz]	# Burst positions per symbol	burst duration [ns]	Symbol rate [Ms/s]	Data rate [Mb/s]	Mean PRF [MHz]
1	3.5	32	32	0.98	0.85	15.6
	4.0					
	4.5					
2	3.5	32	4	7.8	6.81	15.6
	4.0					
	4.5					
3	3.5	32	2	15.6	27.24	15.6
	4.0					
	4.5					
4	3.5	128	64	0.12	0.11	3.90
	4.0					
	4.5					
5	3.5	128	8	0.98	0.85	3.90
	4.0					
	4.5					
6	3.5	128	4	1.95	1.70	3.90
	4.0					
	4.5					
7	3.5	128	2	3.90	6.81	3.90
	4.0					
	4.5					

sending data and programming configuration registers, which include pulse-shape registers.

The packet-level baseband clocked at 31.25MHz is synthesized from standard cells along with the SPI interface and configuration registers. The rest of the TX results from a full-custom design. The symbol-level baseband is clocked at 31.25MHz. The pulse-level baseband uses the 500MHz clock extracted from the LO through the frequency divider.

Fig. 4.3 illustrates the interest of duty-cycling on the power consumption of the TX during a symbol. M0 corresponds to the mode where only the synthesized TX is running. M1 corresponds to the mode where the signal Enable_LO is asserted and where the LO is running along with the synthesized TX except for the PA and the pulse-shaping logic. M2 corresponds to the mode where all the TX is running and where the PA is emitting.

The design of the LO and duty-cycled frequency synthesis is described in Section 4.3.1, the pulse-shaping digital PA in Section 4.3.2 and the solutions for ULV digital implementation up to 4.5GHz in Section 4.3.3.

4.3 DESIGN AND IMPLEMENTATION OF THE TX

4.3.1 Duty-cycled frequency synthesis

The IEEE 802.15.4a bursts are modulated both by Binary Position Modulation (BPM) and Binary Phase-Shift Keying (BPSK) which implies a strong requirement

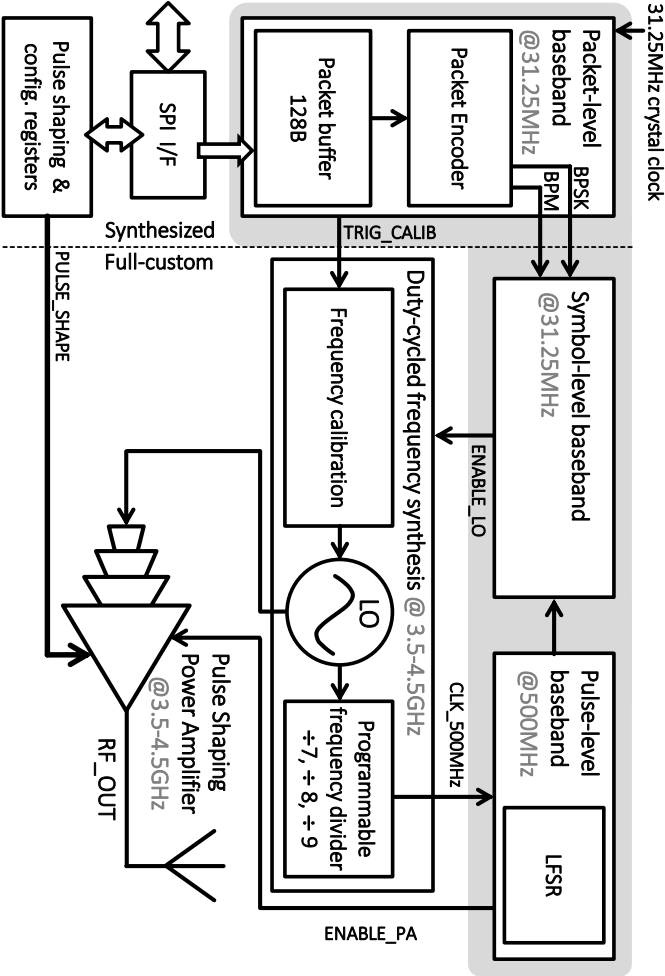


Fig. 4.2. Architecture of the TX. The baseband is partitioned between crystal-frequency blocks synthesized from standard cells and aggressively-duty-cycled high-frequency full custom blocks.

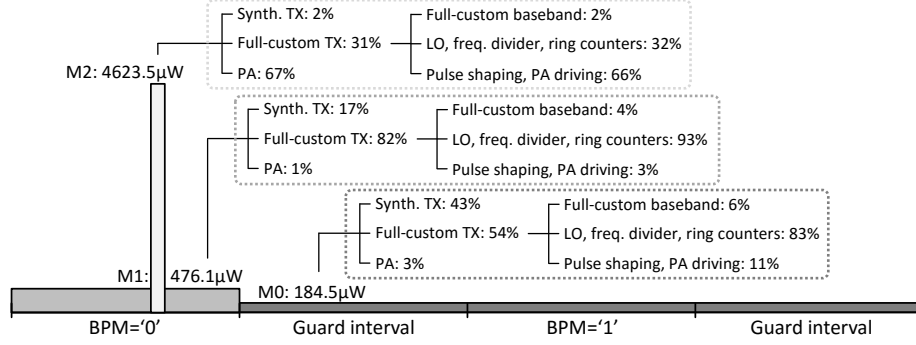


Fig. 4.3. Simulated power breakdown between the different parts of the TX depending on the duty-cycling mode during the symbol duration.

on the frequency accuracy and stability for correct demodulation. Following the analysis from [21], we can define an upper bound for the total phase noise at the end of the burst in order to ensure correct demodulation of the BPSK encoded data. By taking some margin into account, we set the maximum phase noise allowable to $\pi/4$ which corresponds to a maximum accumulated jitter of 27.7ps after 32ns at 4.5GHz. However, the aggressive duty cycling of the LO prevents the use of a PLL to improve jitter performances because of the prohibitive settling time of PLLs and forces the choice of an architecture based on a free-running LO. LC-based oscillators can offer good jitter performances but at the cost of high power, large area and large settling time. To avoid these drawbacks, previous implementations of low-power TX relied on Ring Oscillators (RO) duty-cycled to a quarter of the symbol period. However, in the case of low data rate, the quarter symbol period is quite long and lead to a high accumulated jitter due to the degraded phase noise of RO compared to LC oscillators. Fig. 4.4(a) shows a high accumulated jitter for a current-starved differential RO at nominal voltage and for a run time corresponding to the worst symbol-duration case in the 0.11Mb/s data rate of IEEE 802.15.4a. As shown in Fig. 4.4(a), the proposed within-BPM LO duty cycling proposed in Section 4.2 significantly limits the jitter accumulation. Nevertheless, it is still prohibitive for BPSK data encoding. Therefore, we further improve jitter by optimizing the LO as follows.

- We avoid current starving in the LO thanks to FBB-based frequency tuning. The FBB is used to modify the delay of the RO delay elements and tune the CF to the selected IEEE 802.15.4a channel. The LO is thus a back-bias-controlled oscillator (BBCO).

- We use a differential multiple-pass ring oscillator based on feedforward loops similar to the one proposed in [7]. The 7-stage architecture illustrated in Fig. 4.4(b) improves both the switching speed as well as the noise performance thanks to its faster transitions.

The proposed BBCO element consists of an input pair M1-2 and a feedback latch M5-6-7-8-9-10 as shown in Fig. 4.4. During transition, the positive feedback of the latch leads to sharper transitions but it also slows down the cell by resisting to the change of the state of the delay element. The penalty in term of frequency is compensated by lower jitter thanks to sharper transitions as shown in Fig. 4.5. Furthermore, the transition time remains sharp even for lower frequencies leading to more constant jitter performance over the tuning range. The latch is sized such that a good tradeoff between minimum mean delay and feedback strength is achieved to balance the output frequency and the accumulated jitter.

To compensate the delay penalty induced by the feedback latch and further accelerate the RO, we use a multiple-pass architecture similar to [7] and [8] to push the oscillation period below $N \times$ the delay element delay time. A feedforward path between the delay element is implemented through the addition of M3-4. These devices are thus prematurely activated before the transition of the element enhancing the charge of the outputs.

Fig. 4.5 illustrates how the addition of the feedback latch and the feedforward path help achieving lower transition-time standard deviation from cycle to cycle and thus lower accumulated jitter.

The proposed BBCO is enabled by slightly modifying two of the seven delay elements in the chain as depicted in Fig. 4.6. These cells implements the NOR and NAND functions in order to gate the oscillation in the main path as well as in the feedforward path. They are sized to feature the same delay as the regular delay elements in order to keep the maximum tuning frequency above 4.5GHz taking PVT into account.

As show in Fig. 4.4(a), reducing the run time of the LO from $1/4$ of the symbol duration to only one cycle of the crystal clock leads to more than $10 \times$ reduction of the accumulated jitter. When reducing the supply voltage down to 0.55V and applying 1.1V of FBB to keep the frequency constant, the accumulated jitter is further reduced by $10 \times$. Overall, the proposed ULV multiple-pass RO with aggressive within-symbol duty cycling achieves a total reduction of the accumulated jitter of $500 \times$.

In order to calibrate the frequency of the free-running LO, we integrate it inside a calibration loop described in Fig. 4.7. The BBCO output is divided by a programmable frequency divider to generated a 500MHz clock. A control logic compares the divided LO output to a reference crystal clock at 31.25MHz and adapts the BB voltage command `CMD_CF` to lock the LO frequency on the desired 3.5 to 4.5GHz channel. A 10-bit DAC generates the NMOS BB voltage

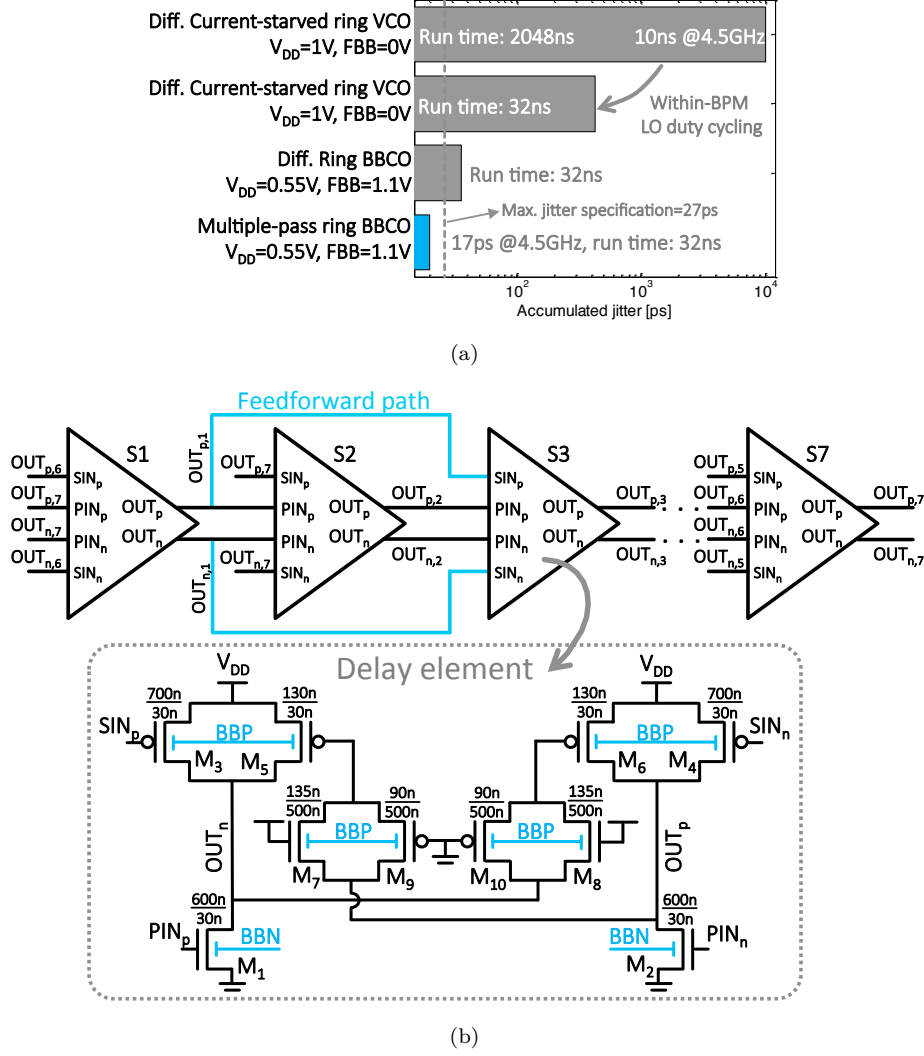


Fig. 4.4. Local oscillator: (a) simulated accumulated jitter performances at 4.5GHz and (b) architecture of the proposed multiple-pass back-bias-controlled oscillator. The frequency is controlled through the FBB voltages applied to the NMOS (BBN) and the PMOS (BBP) of the delay element.

(BBN_{LO}) and a current matching loop adapts the PMOS BB voltage (BBP_{LO}) to keep the NMOS/PMOS ON current ratio constant as described in Section 4.4.3. The calibration of the free-running BBCO is done before starting a packet transmission.

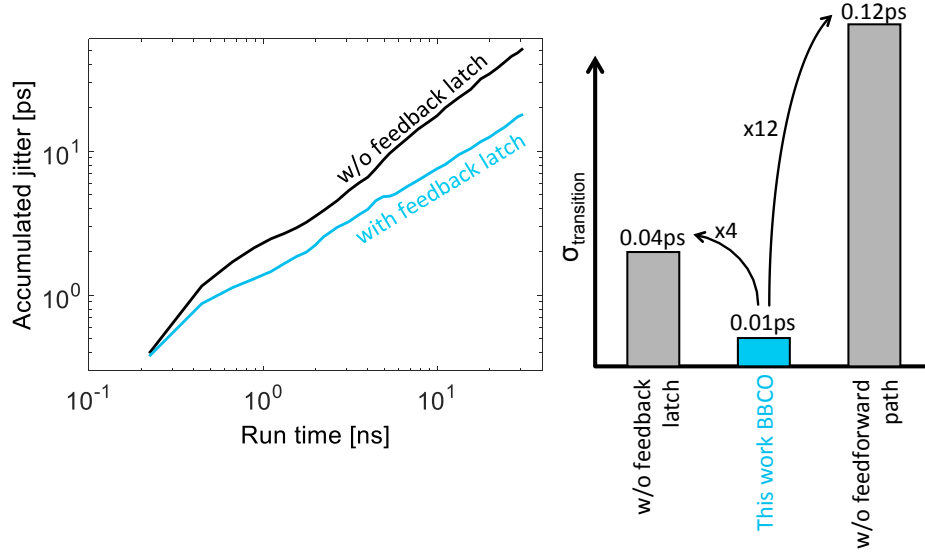


Fig. 4.5. Simulated accumulated jitter of the presented BBCO with and without the feedback latch and the feedforward path. The accumulated jitter over a 32ns run time is reduced by almost 3 $\times$ by the addition of the feedback latch (left) and the transition-time standard deviation is divided by 12 $\times$ when implementing the feedforward path.

4.3.2 Pulse Shaping Power Amplifier

Designing pulse generator without high-order off-chip filtering to avoid emissions in the 960-1610 MHz restricted band [6] is challenging as FCC regulation mask limits the maximum emitted power in that band to XX dBm/MHz (Tab. 4.2). As described by [4], capacitive coupling of the digital PA output does not provide a sufficient roll-off to meet the FCC regulation limit when emitting in the 3-5GHz UWB bands.

In this work, we propose a fully-digital pulse shaping filter integrated within the PA to improve the roll-off. Fig. 4.8 illustrates the spectral impact of shaping a rectangular pulse to a Gaussian pulse with the same duration. For an ideal Gaussian shaping, the spectral content in the 960-1610 MHz band can be reduced by more than 20dB which can directly be used to increase the maximum output power while meeting the FCC regulation.

Fig. 4.8 further shows the impact of the amplitude resolution of the pulse shaping on the resulting spectrum. It is possible to meet the restrictions in the 960-1610 MHz band with a 5-bit resolution on the Gaussian shape with a minimum power and area overhead. To implement the shaping functionality, the

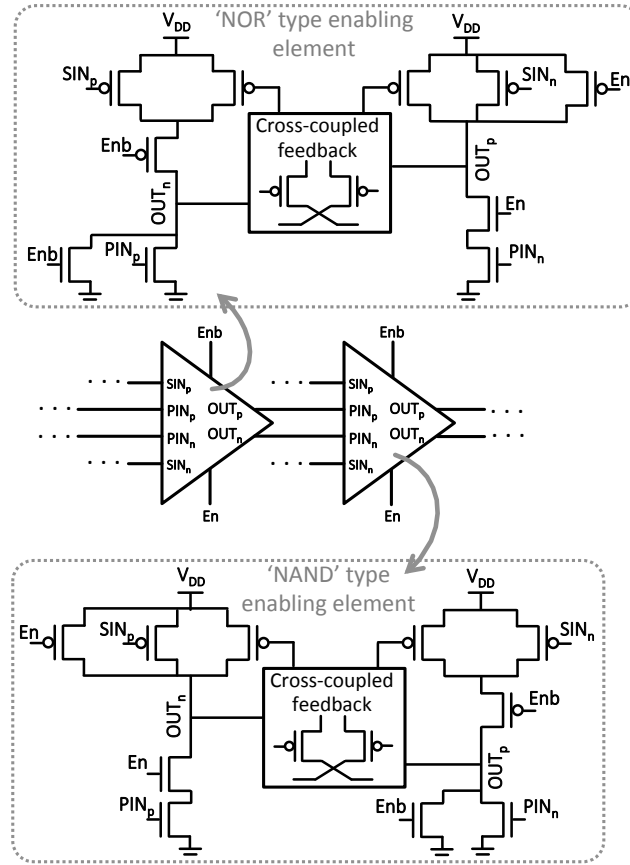


Fig. 4.6. Schematic of the enabling logic embedded in the BBCO.

Table 4.2. UWB average emission limits

Frequency band [MHz]	Indoor applications dBm/MHz	Hand held & outdoor dBm/MHz
0.009-960	§15.209*	§15.209*
960-1610	-75.3	-75.3
1610-1990	-53.3	-63.3
1990-3100	-51.3	-61.3
3100-10600	-41.3	-41.3
10600-22000	-51.3	-61.3

* Regulation rules from FCC §15.209 are in application below 960MHz.

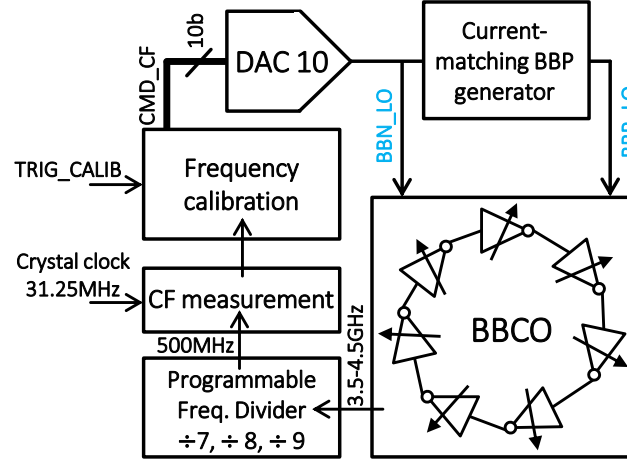


Fig. 4.7. Block diagram of the BBCO frequency calibration loop through adaptive-FBB.

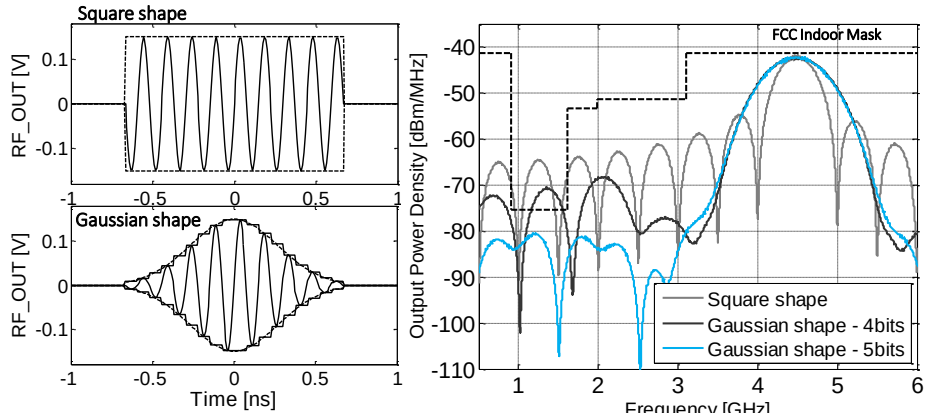


Fig. 4.8. Left: square and Gaussian ideal pulse shapes. Right: impact of the pulse shape on the output power spectral density. For the same maximum power inside the band, the square-shaped pulse features significant power in 960-1610MHz restricted band. The Gaussian-shaped pulse shows a higher out-of-band filtering and increasing filtering effect for higher amplitude resolution.

digital power amplifier is split in independent parallel stages to act as a 32-stages current DAC.

Fig. 4.9 illustrates the impact of the sampling rate on the output power density spectrum of the pulses. If the sampling is performed at the LO central frequency,

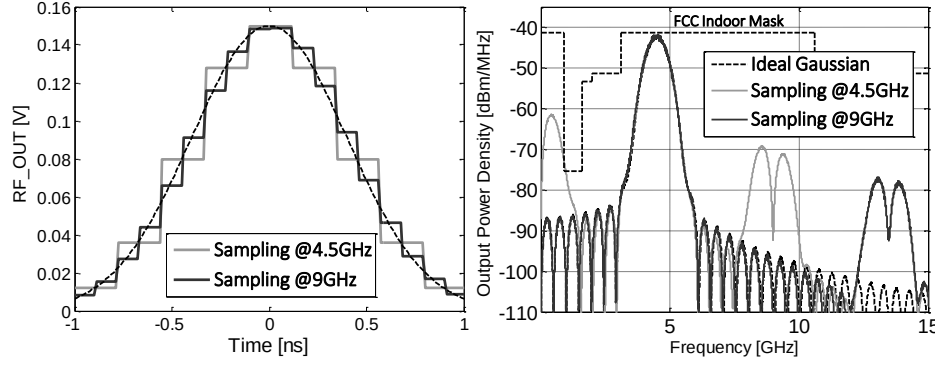


Fig. 4.9. Impact of the pulse shape time resolution. Left: Gaussian shape approximated with 9 ($@f_{LO}$) or with 18 ($@2 \times f_{LO}$) time steps. Right: spectral folding caused by the sampling frequency of the shape. A sampling at f_{LO} leads to a folding peak at DC and spectral content in the 0.96-1.61GHz band, which violates the FCC regulation mask. Quantization at $2 \times f_{LO}$ eliminates the folding around DC.

spectral folding will cause significant power close to the restricted 960-1610MHz band that will not be sufficiently attenuated by the 1st order roll-off of the coupling capacitance. To avoid this problem, the PA and pulse shaper is operated at $2 \times$ the LO frequency which pushes the spectral folding away from the restricted bands.

The complete Pulse-shaping PA architecture is described in Fig. 4.10. The dual ring counters are clocked on the LO positive and negative phase and generate 7 to 9 enable signals with duty-cycle varying from $1/7$ to $1/9$ depending on the selected channel from 3.5GHz to 4.5GHz. The symbol-level baseband generates the BPSK-encoded and scrambled data giving the phase of the pulse. The shape envelope information is contained in the pulse shaping registers. The ring counter outputs are used to cycle through the 18 bits of the pulse shape and to control the enabling of each of the 32 stages. The BPSK-encoded data select the LO phase to use in the stage to modulate the pulse. Pulse modulation is conducted inside each stages and buffering is inserted to drive the PA output stage as shown in Fig. 4.10.

The PA output stage is a tri-state inverter sized so that the 32 parallel stages with mid-range back biasing are able to drive the antenna with a peak-to-peak voltage of 350mV at 4.5GHz. The tri-state output stages offer 2 advantages as they can be completely turned-off to save power between bursts and they allow the TX to share the antenna with a receiver. Adaptive FBB is used to tune the RF output power and to compensate for PVT variations by controlling the current of the PA output stage.

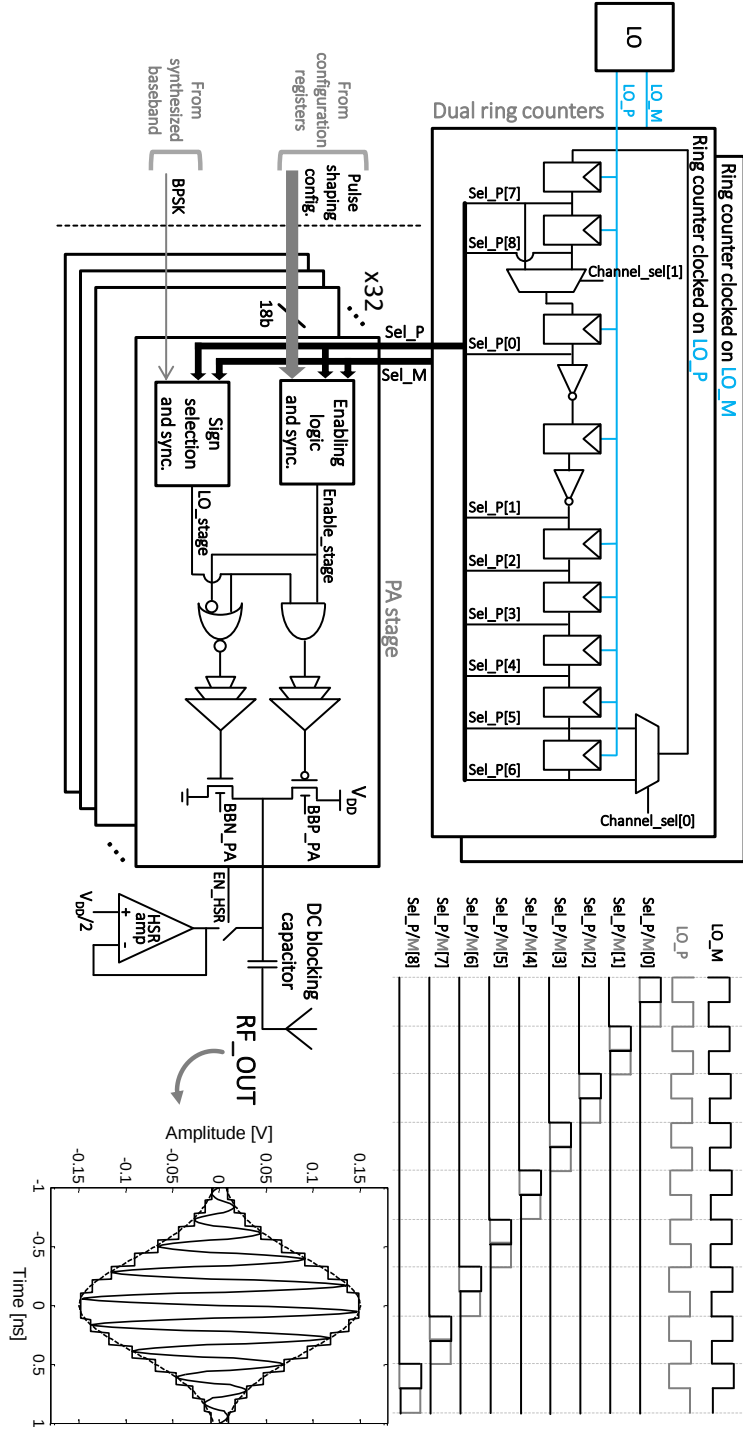


Fig. 4.10. Architecture of the programmable pulse-shaping digital PA. The pulse shaping functionality is implemented by a 5-bit 9Gs/s current DAC controlled by the ring counters outputs. The PA output is precharged at $V_{DD}/2$ by a High-Slew-Rate (HSR) amplifier and a DC blocking MiM capacitor filters the DC value. Right: sequencing stage-select signals generated by the ring counters and simulated RF output waveforms.

Between pulses, the PA output is precharged to $V_{DD}/2$ to maximize the output pulse swing. Indeed, due to mismatch in the phase of the signals driving the PMOS and NMOS of each output stages and the enabling signal of the stages and precharge amplifier, the output voltage at the end of the pulse can be different than $V_{DD}/2$. In order to be ready for the next pulse, the precharge amplifier should be able to bring the output node back to $V_{DD}/2$ in less than 16ns which is the duration of 1 guard interval in the fastest data rate.

In conventional class-A OTA, the slew rate is linked to the bias current and to the multiplication factor of the current mirror between the input and output stage leading to a fundamental tradeoff between slew rate and quiescent current. In our application, the slew rate should be high enough to achieve the $17V/\mu s$ specification to bring the DC level back to $V_{DD}/2$. Unfortunately, the quiescent current is also a critical specification of the OTA as we do not benefit from duty cycling. To reach these requirements, we designed a High-Slew-Rate (HSR) precharge amplifier based on a super-class-AB OTA from [12] and illustrated in Fig. 4.11. It features an adaptive biasing of the input differential pair depending on the large differential input signal to automatically boost the bias current and achieve high slew rate while maintaining a low quiescent current. In addition to the adaptive biasing, it features a local common-mode feedback first described in [13] implemented with two $10k\Omega$ matched resistors in order to boost the current efficiency. The HSR is supplied on the 1.2V supply in order to reach the stringent slew-rate requirement. Two common-source stages up-convert the inputs from the 0.55V domain for voltage compliance and an enabling signal EN_HSR disconnects the HSR output to the output of the PA stages during the pulse emission as shown in Fig. 4.10.

Fig. 4.11 illustrates the adaptive biasing as well as Monte-Carlo post-layout simulations of the tri-state outputs converging after the end of a pulse.

4.3.3 ULV High-Speed Digital Implementation

Operating digital ULV circuits above 3GHz is challenging due to the significant speed penalty of the near-threshold MOSFET operation. The long propagation delay can be dealt with by fine-grained pipelining at the expense of an increased clock load [9]. Near-threshold operation also implies a high penalty in term of output transition time. For a fixed operation frequency, the longer output transition time limits the maximum acceptable fanout as shown in Fig. 4.12 which cannot be improved by fine-grain pipelining. The 28nm FDSOI technology can help to alleviate the clock distribution challenge. Compared to 65nm GP bulk CMOS, 28nm FDSOI CMOS is shown in Fig. 4.12 to achieve higher maximum fanout, lower minimum V_{DD} and lower total energy in an inverter chain with a fan-out of one (FO1) thanks to its better electrostatic characteristics and lower capacitances.

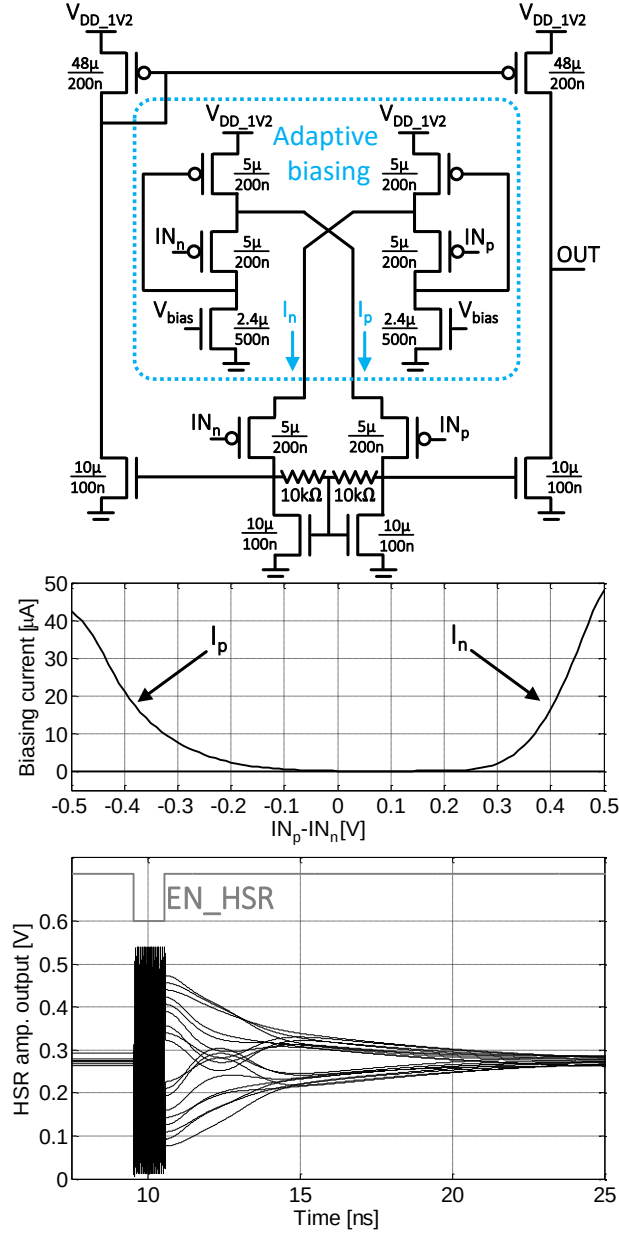


Fig. 4.11. Schematic of the HSR amplifier along with post-layout simulations of the adaptive biasing and Monte-Carlo post-layout simulations of the amplifier output which is driven to $V_{DD}/2$ after the pulse.

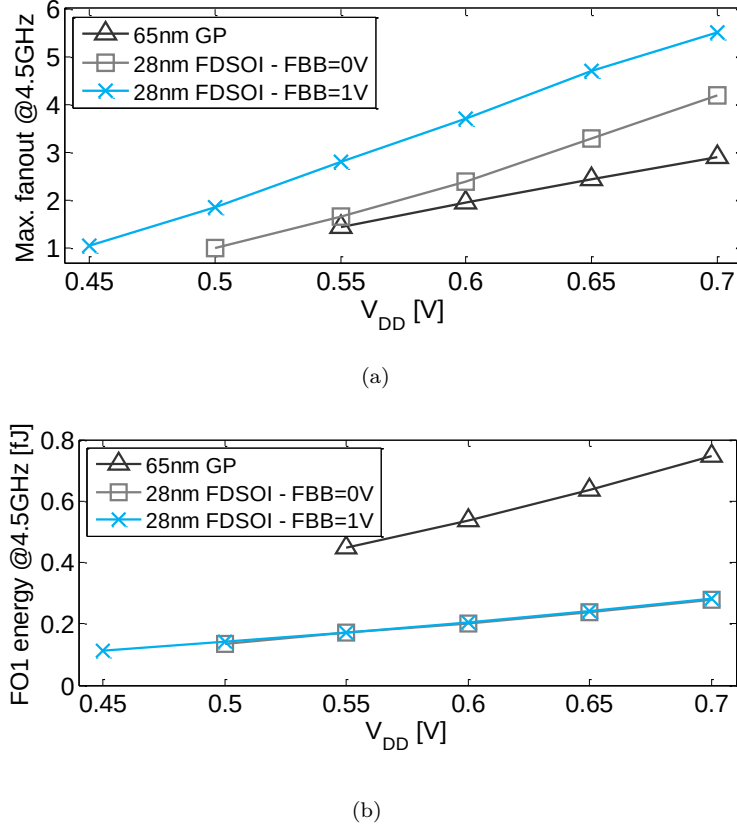


Fig. 4.12. Fan-out limitation due to ULV operation at 4.5GHz from post-layout SPICE simulations of an inverter chain: (a) maximum fanout at 0.55V allowing a 10-to-90% transition time lower than 20% of the period at 4.5GHz and (b) total energy of an FO1 inverter chain switching at 4.5GHz.

Forward back biasing allows higher frequency operations through a V_T reduction [29], Fig. 4.12 also shows that it offers a maximum fanout increased by 1 compared to the $FBB = 0V$ situation and has a negligible energy overhead when switching at frequencies over 1GHz. At 0.55V, the maximum fanout is increased by 2 $\times$ when the FBB is increased from 0V to 1V.

The voltage scaling impact on the maximum usable fanout at 4.5GHz leads to increased constraints on the clock tree. Standard scan master-slave flip-flops from the foundry library are too slow to operate the dual ring counters or the frequency divider at 3.5GHz to 4.5GHz. The maximum frequency of operation for the frequency divider in post-layout simulations is limited to 4.98GHz taking

into account 3σ local variability as shown in Fig. 4.13 which leaves only a small design margin.

To increase the design headroom, we designed new flip-flops based on TSPC architecture from [11]. It offers a reduced variability on the Clock-to-Q timing thanks to the single phase clock, which allows removing the clock inverter stage. However, TSPC flip-flops lose the data after a few hundred of nanoseconds following the clock edge as illustrated in Fig. 4.13. To circumvent this problem, we added a data retention feedback loop in the output stage of the flip-flop to guarantee data retention when the clock is low. At system level, we forced both phases of the LO to be gated at the low logic level to ensure that the frequency divider and the dual ring counters are in data retention.

The clock load of a single flip-flop is reduced by 38% compared to master-slave architecture. At block-level, using the new TSPC flip-flops in the frequency divider leads to a +73% improvement in maximum frequency of operation and -24% in total power extracted from post-layout simulations.

Compared to the pre-layout results of Chapter 2., we manage to achieve timing closure at 4.5GHz which is almost $10\times$ higher than the fastest synthesized ARM M0 core thanks to the reduced clock load and higher speed of the TSPC and to the slightly higher supply voltage. Indeed, the supply voltage is raised from 0.35V in Chapter 2. to 0.55V in this prototype which is around 200mV higher than V_T .

4.4 SOC INTEGRATION

The SleepTalker SoC shown in Fig. 4.14 requires a single 1.2V external supply in addition to the digital I/O voltage and features the TX described in Section 4.2, an on-chip switched-capacitor DC/DC converter to generate the core 0.55V supply voltage, a charge-pump-based generator supplying the $\pm 1.8V$ to the back-biasing generator, the FBB generators and an always-on sleep controller.

In sleep mode, the DC/DC converter performs power gating on the 0.55V blocks. The sleep controller remains on in sleep mode and is thus supplied from the external 1.2V supply. To reduce its leakage power, the sleep controller is implemented with regular- V_T devices. The transition from sleep mode to active is completed in less than 1ms and can be done between 2 packet transmissions.

4.4.1 DC/DC Converter

The 0.55V core voltage distributed to the TX is generated by a multi-mode switched-capacitor network DC/DC converter integrated on-chip with MiM capacitors and supplied by the 1.2V external supply. The DC/DC converter first presented in [14] features a low-power mode, a Medium-Power (MP) mode and a power gating mode. The MP mode is used in this SoC to generate the 0.55V core supply voltage with an output power up to 5mW. The MP mode uses two 2-way

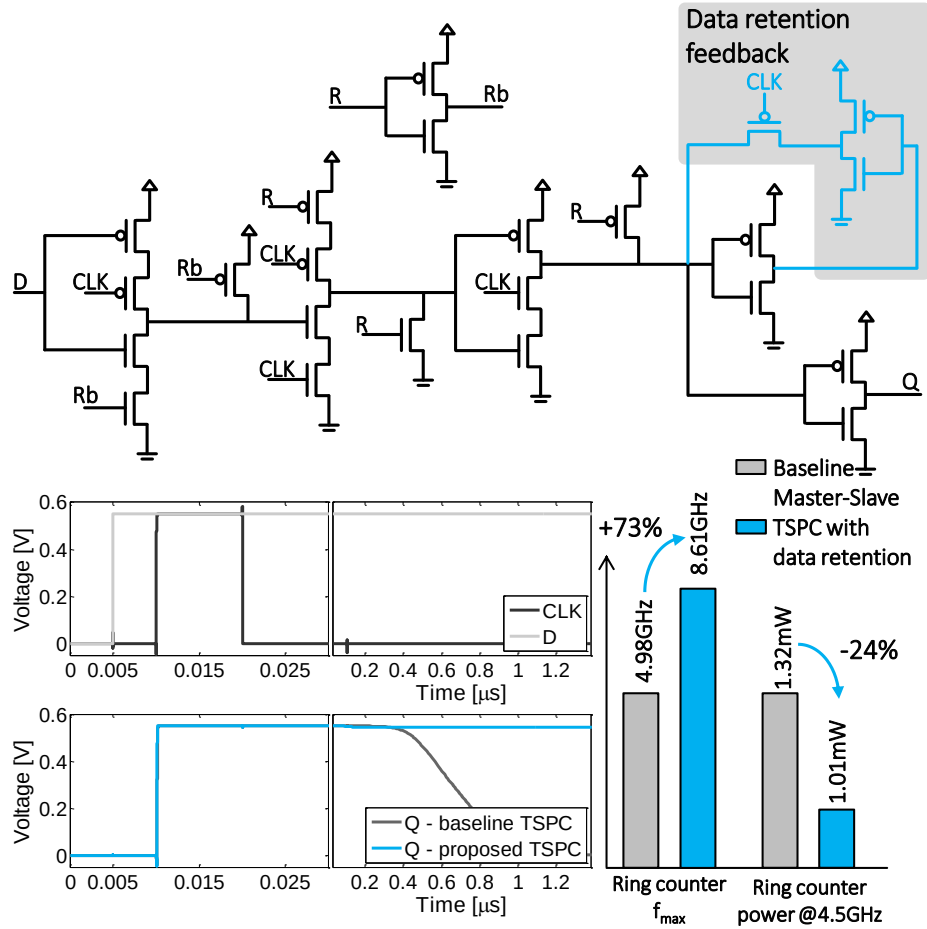


Fig. 4.13. TSPC flip-flop schematic featuring the data retention feedback loop. The TSPC-based frequency divider shows a 24% power reduction and a 73% increase in the 3σ -worst-case maximum frequency extracted from Monte-Carlo post-layout SPICE simulations. The data retention feedback loop guarantees data retention when the clock is low as opposed to baseline TSPC architecture.

interleaved switched-capacitor networks to mitigate the output ripple and FBB is applied to increase switches conductance. The regulation mechanism is based on pulse skipping modulation which allows the converter to keep a high power conversion efficiency over a wide load range. It uses a $10\mu F$ external capacitor.

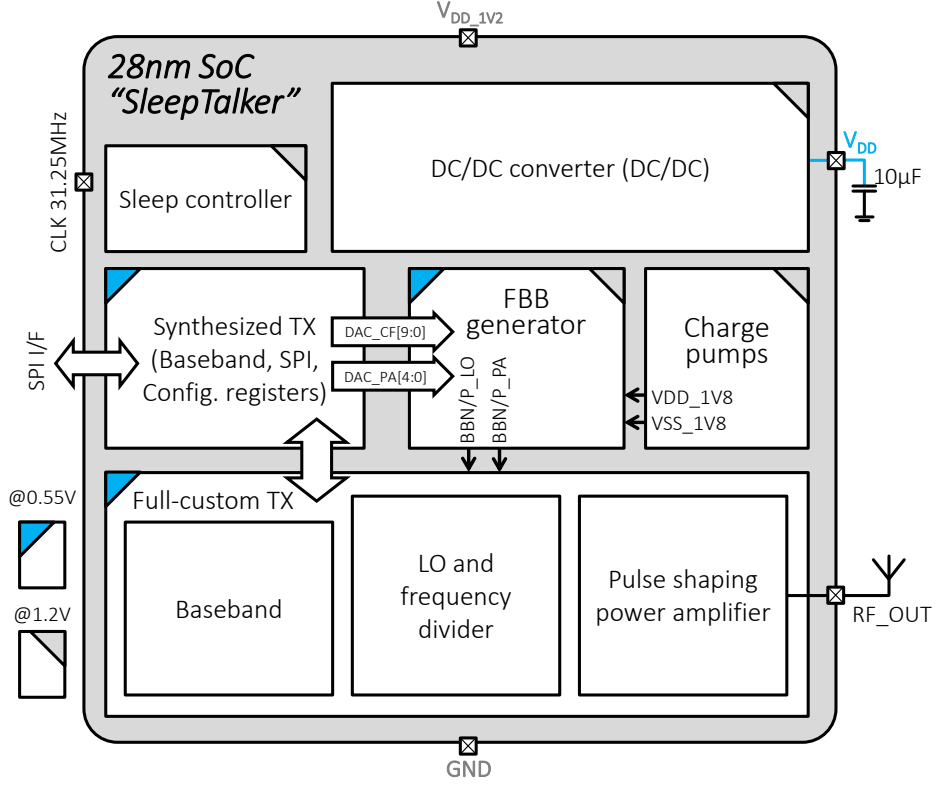


Fig. 4.14. SoC architecture.

4.4.2 +1.8V/−1.8V On-Chip Generation

To supply the FBB generator, we need to generate +1.8V/−1.8V supply voltages (V_{DD_1V8} and V_{SS_1V8}) from the 1.2V external supply voltage. This is done with two charge-pump circuits based on the Dickson architecture with MiM capacitors, clocked by the 31.25MHz crystal clock. As shown in Fig. 4.15, pulse-skip modulation is used to regulate both charge-pump output voltages by comparing them with a 0.55V reference voltage through a resistive feedback divider. In sleep mode, the charge pumps are disabled by gating their clock (GCLK signal).

In Dickson architecture, the output voltage and the load regulation is limited by the V_T drop on the MOS diodes. To reduce the V_T of the MOS diodes, we use a butterfly connection based on dynamic back biasing. As shown in Fig. 4.15, the PMOS (resp. NMOS) diodes in the charge pump that generates V_{DD_1V8} (resp. V_{SS_1V8}) are strongly forward back biased at V_{SS_1V8} (resp. V_{DD_1V8}).

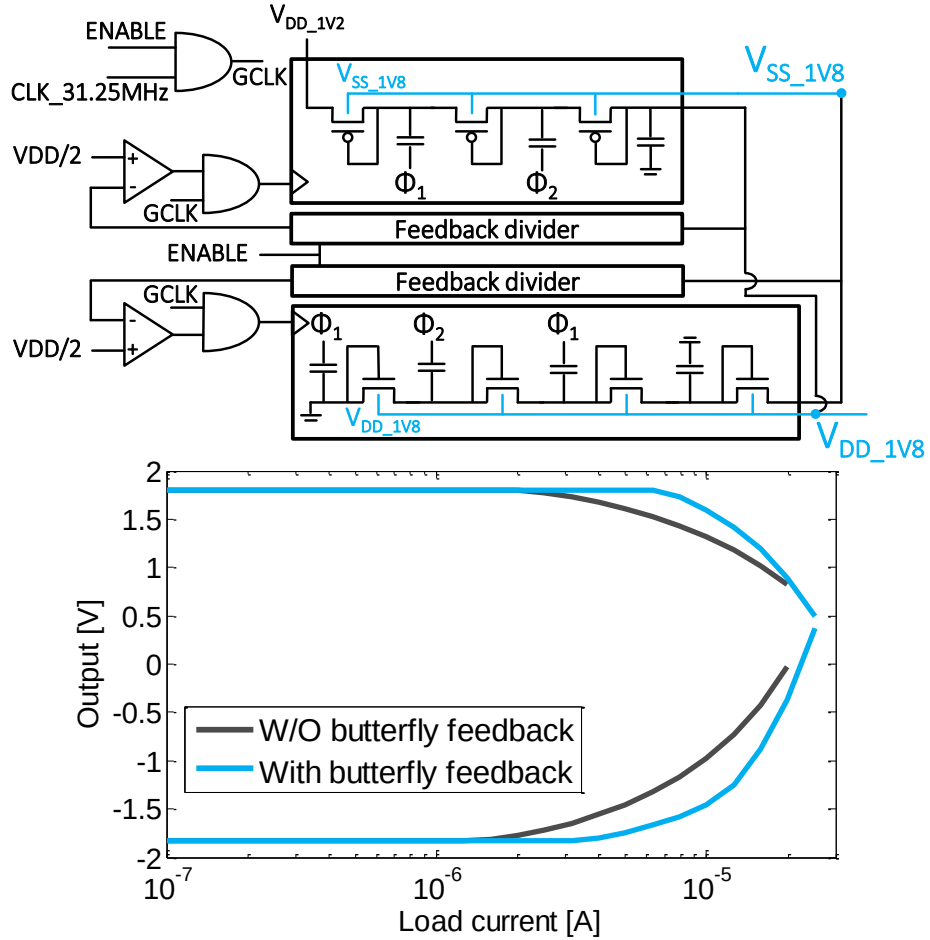


Fig. 4.15. Proposed butterfly-connected regulating charge pumps to generate the $\pm 1.8V$ FBB supplies: schematic and simulated load regulation.

This does not increase the sleep-mode leakage power as both V_{DD_1V8} and V_{SS_1V8} are grounded in sleep mode when the charge pumps are disabled.

Fig. 4.15 shows that the load current range for 5% output voltage drop is extended by a factor $2.5\times$ thanks to the proposed butterfly connection.

4.4.3 Forward Back Biasing Generator

The generation of the NMOS back biasing voltage (BBN) is implemented by 2 capacitive DACs depicted in Fig. 4.16 over a $[0; 1.65V]$ voltage range. The BBN

voltage of the full-custom TX is generated by a 10-bit DAC to achieve fine tuning of the CF to the selected 802.15.4a channel with 5MHz frequency resolution. The output buffer is a Miller-compensated 2-stage OTA sized to maximize PSRR to limit the impact of supply noise on the LO frequency accuracy. As the output of a capacitive network DAC drifts due to the leakage current of the switches, a refresh of the DAC is mandatory to avoid frequency drift during transmission. To do so, the packet-level baseband performs a refresh of the DAC before each 802.15.4a packet composed of maximum 83 preamble symbols and maximum 1209 data symbols. For the lowest 0.11Mb/s data rates, the packet duration exceeding 10ms imposes heavy constraints on DAC switches leakage. To relax these design constraints, the DAC refresh is conducted during each guard interval. The worst-case regarding the DAC output drift is then obtained when transmitting in the 0.85Mb/s data rate where the packet duration can be as long as $1300\mu s$. The DAC switches are thus sized to achieve less than 1 LSB of drift over $1300\mu s$. The BBN applied to the output stages of the PA does not require high accuracy as it is used only to compensate the impact of PVT variations on the output power by increasing or decreasing the peak-to-peak amplitude of the pulses. To generate this BBN, a 5-bit capacitive DAC is used with architecture, output buffer and refresh pattern similar to the 10-bit DAC controlling the CF.

The FBB voltages to be applied to the PMOS (BBP) inside the full-custom TX and the digital PA output stages are generated by continuous-time current-matching loops shown in Fig. 4.16 similar to [15]. Replicas of an inverter or of a PA output stages are used to determine the correct BBP that needs to be applied to balance the current between the NMOS and the PMOS. An output buffer supplied by -1.8V is then used to drive the back gate capacitance of all the devices of the full-custom TX. The inputs of the amplifiers driving the back gates at BBP are in the ULV domain while the output can be driven to up to $\pm 1.8V$ leading to a voltage compatibility challenge. To circumvent this, the output buffer is a Miller compensated 2-stage OTA with a bulk-driven NMOS input pair. This allows voltage range compatibility between the OTA implemented with thick-oxide 1.8V I/O transistors and the 0.55V replica implemented with thin-oxide core devices without the use of level-shifting.

4.4.4 Physical Implementation

The SoC floorplan including I/O pad and on-chip decoupling capacitance repartition is illustrated in Fig. 4.17.

The *SleepTalker* test chip first presented in [33] was designed and manufactured in a 10-metal 28nm FDSOI CMOS process with MIM capacitance option. Fig. 4.18 shows the 0.93mm^2 die microphotograph with an active area of 0.55mm^2 and only 0.095mm^2 for the TX. The fabricated dies were encapsulated in QFN40 packages with unsealed top lid for on-die measurements.

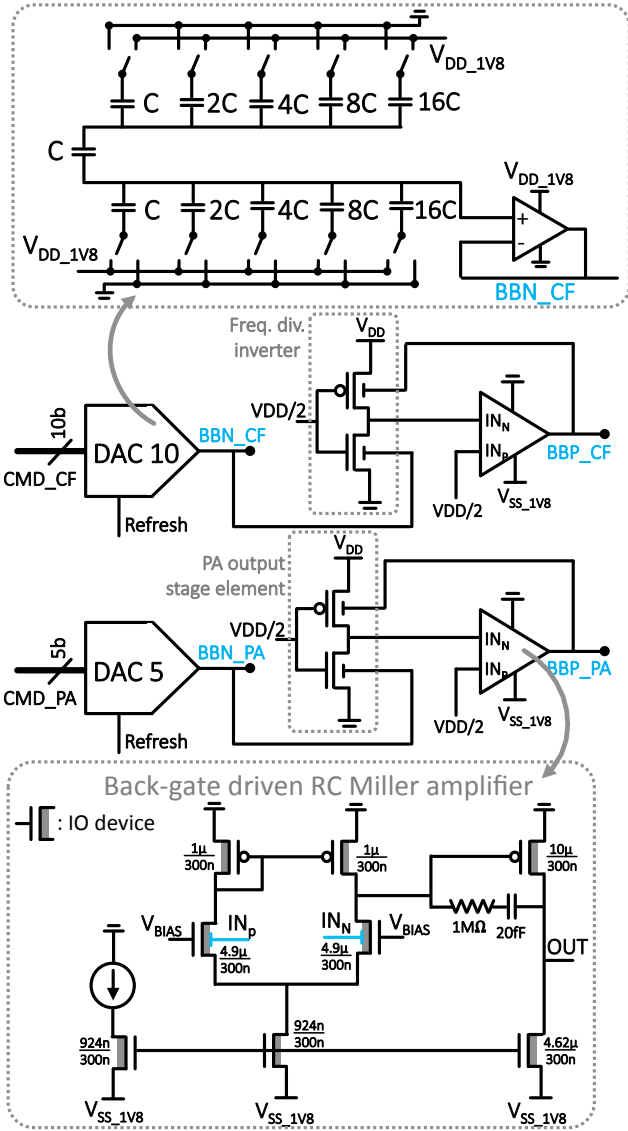


Fig. 4.16. FBB generator architecture. BBN is generated by DACs (DAC10 and DAC5) to tune the LO frequency for channel selection and the PA output power. The corresponding BBP voltages are generated from the BBNs through a current matcher structure with a back-gate-driven amplifier.

4.5 EXPERIMENTAL VALIDATION

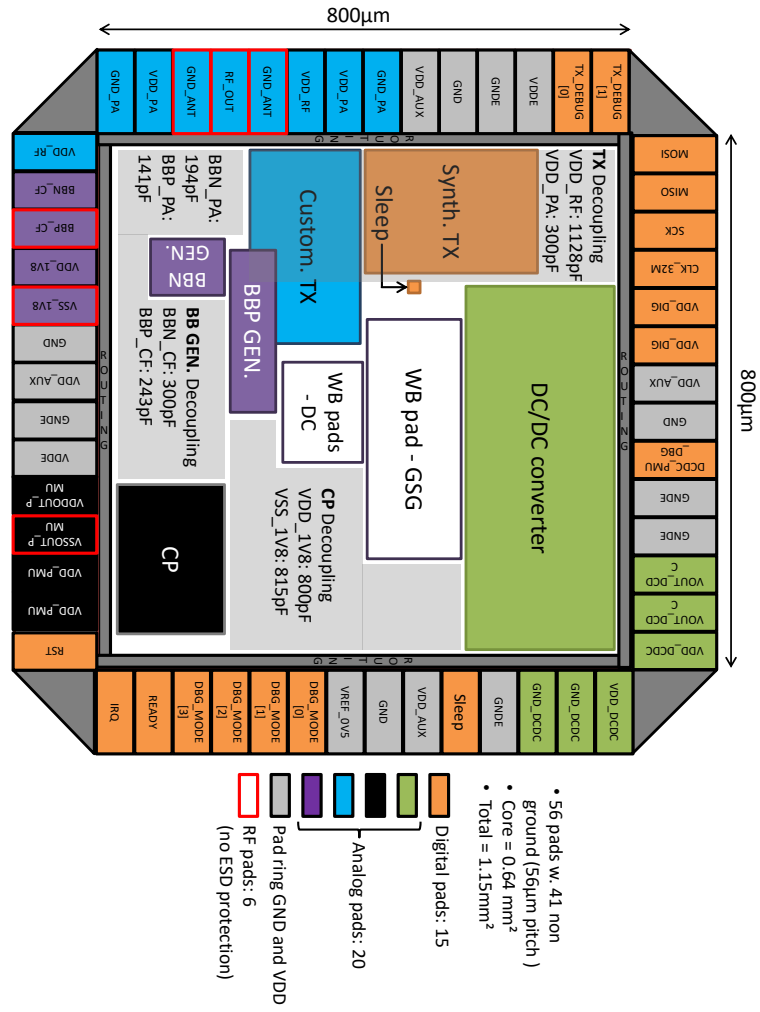


Fig. 4.17. SoC floorplan.

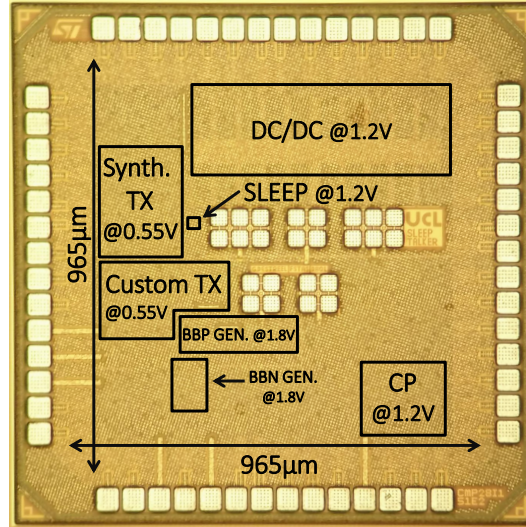


Fig. 4.18. SleepTalker die microphotograph. The SoC core area is 0.93mm^2 and the TX only occupies 0.095mm^2 .

4.5.1 Experimental Setup

The packaged dies were mounted on custom RF ROGERS 4350 PCB daughter boards interfaced with a custom mother board and a Nucleo STM32 microcontroller development board for communication and configuration through SPI I/F as illustrated in Fig. 4.19. For debug and independent measurements purpose, the output voltages from the DC/DC and from the charge pumps are connected to external pads. Three independent supplies are available for the synthesized and full custom parts of the TX as well as for the PA output stage to allows quantification of the power repartition. Fig. 4.20 illustrates the characterization setup for on-die as well as temperature measurements.

The BBN and BBP voltages applied to the full-custom TX are connected to dedicated pads for characterization purposes of the 10-bit DAC. The 5-bit DAC BBN output and its associated BBP applied to the PA stage are connected to on-die DC probing pads visible in the center of the die in Fig. 4.18. In a debug and measurement mode, the output of the LO drives an RF GSG pad also visible in the die microphotography in Fig. 4.18.

The default setup, unless specified otherwise in the following paragraphs, is based on room temperature ($\simeq 25^\circ\text{C}$) on typical dies, with an external $V_{DD1V2} = 1.2\text{V}$.

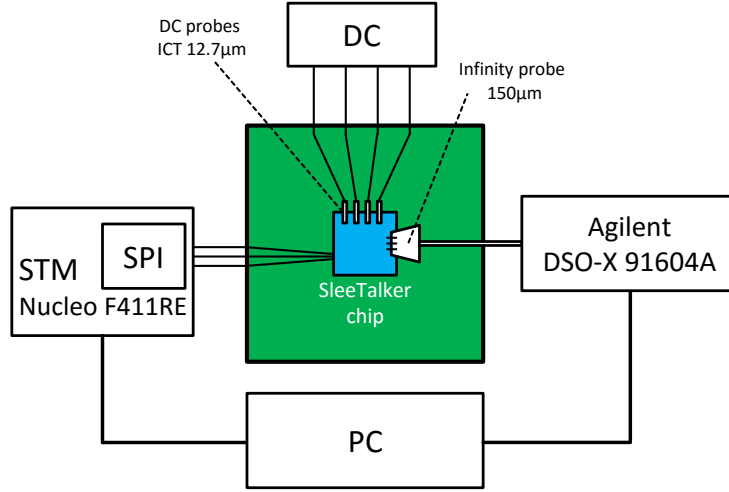


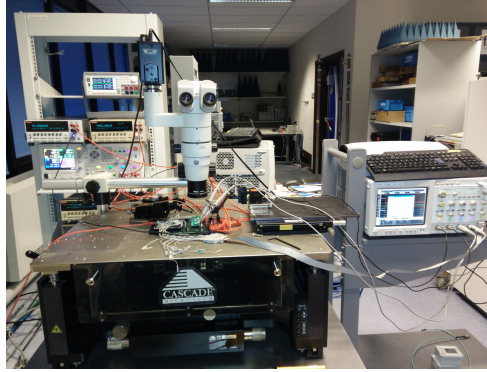
Fig. 4.19. Test fixture schematic.

Fig. 4.21 shows the measured output voltage of the switched-capacitor DC/DC supplied at 1.2V in medium-power mode. The measured peak efficiency in MP mode is 86% at 2.5mW load power and 84% at 380μW.

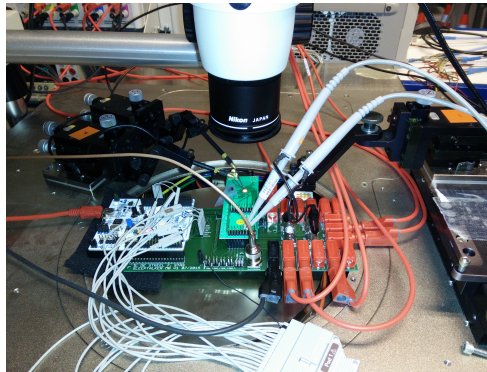
4.5.2 Back-Biasing Generation

Functional validation of the BBN and BBP controlling the LO frequency are shown in Fig. 4.22(a). The measured BBN and BBP ranges are respectively [0;1.6V] and [0;-1.7V]. We can observe that the current-matching loop applies a stronger FBB on the PMOS compared to the NMOS FBB which indicates a strong mismatch between NMOS and PMOS in the near-threshold domain. Such mismatch was already studied in [29]. Fig. 4.22(b) illustrates the NMOS/PMOS mismatch by showing the BBN/BBP gap for 8 measured dies originated from a single wafer. Without the current-matching adaptive FBB, this NMOS/PMOS mismatch would lead to strong robustness degradation.

Fig. 4.22(c) shows the output drift of the 10-bit DAC depending on the command value. In the worst case, the time for a 1-LSB drift is 2ms which allows us to perform the refresh operation between the transmitted packets except for the 0.11Mb/s data rate. The output characteristic and DNL of the 10-bit DAC are presented in Fig. 4.22(d). Below 0.2V, the 10-bit DAC saturates leading to poor effective resolution for the LO frequency. However, as shown in Section 4.5.3, the TX will not operate in this range even on 802.15.4a channel 1.



(a)



(b)



(c)

Fig. 4.20. Experimental setup for on-die BB and LO measurements on a Cascade prober (a. and b.) and temperature measurements in an Espec climatic chamber (c.).

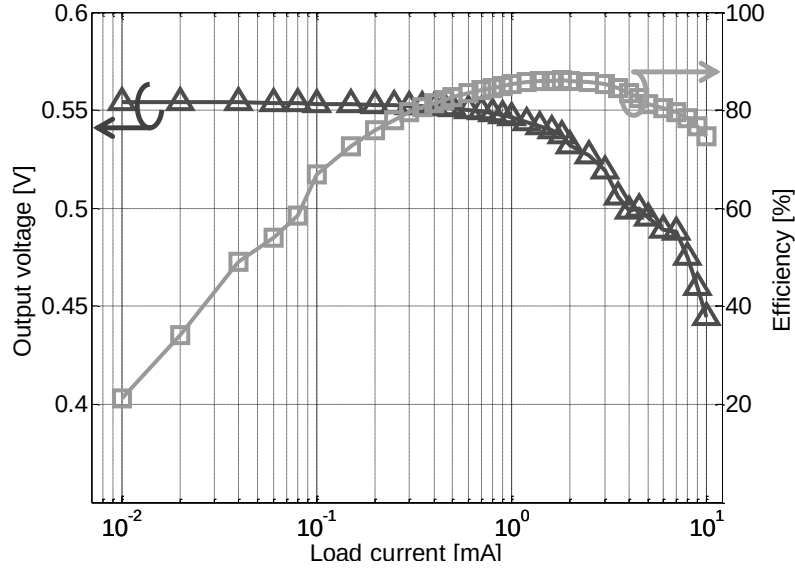


Fig. 4.21. Measured load regulation and efficiency of the DC/DC converter.

4.5.3 Carrier Frequency Tuning with Adaptive FBB

The FBB impact on the BBCO frequency is illustrated in Fig. 4.23(a). In nominal conditions, a wide range of frequencies from 2.4GHz to 5.5GHz can be achieved and the 3 targetted 802.15.4a channels are well centered inside the tuning range. Fig. 4.23(a) also shows that operations in the 3 channels remain possible for temperatures down to -40°C or up to 85°C . Fig. 4.23(a) presents the frequency drift over 8 measured dies that is compensated by the FBB tuning loop.

The calibration loop is demonstrated in Fig. 4.23(b) for the 3 channels. The typical lock time is $2.2\mu\text{s}$ and the maximum lock time observed at startup is $573\mu\text{s}$.

4.5.4 TX Performances

The TX functionality was assessed in the seven data rates and for the three channels from 3.5GHz to 4.5GHz. We successfully measured pulses at a supply voltage of 0.55V and validated the pulse shaping functionality at up to 9GS/s.

Fig. 4.24 illustrates measured output pulses with square and Gaussian shape. The pulses are asymmetrical which leads to a mismatch in rise and fall times at the input of the PA output stage. This comes from the strong observed mismatch between NMOS and PMOS, which is not fully compensated by the current-matching adaptive FBB. Indeed, the BBP voltage saturates at -1.7V whereas

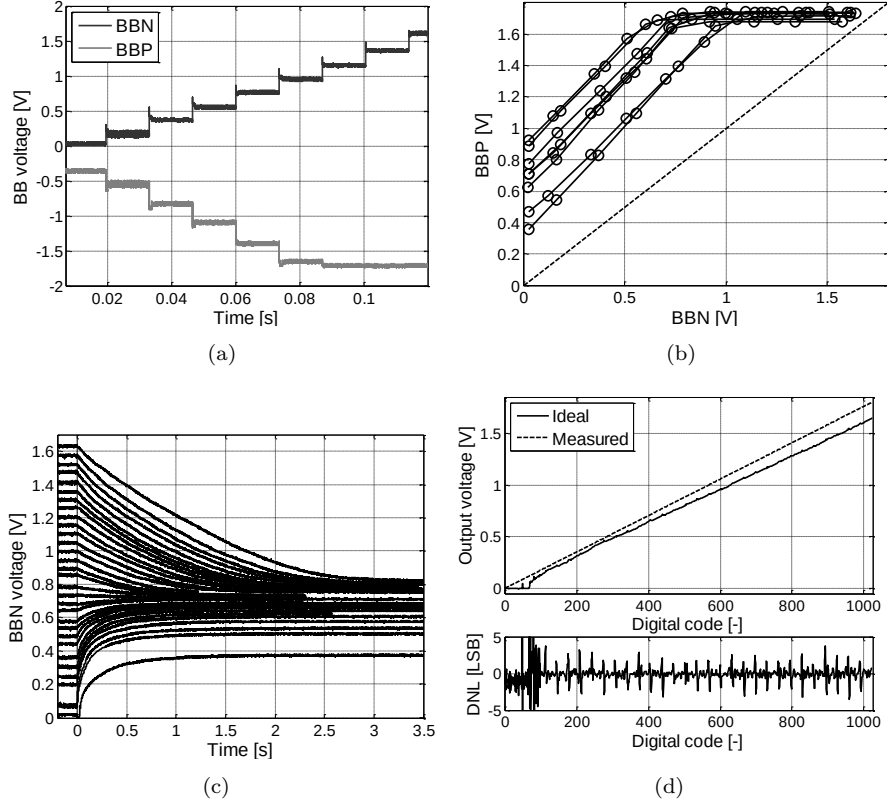


Fig. 4.22. Measured characteristics of the FBB generation: (a) functionality demonstration of the 10-bit DAC and of the BBP generated by the current matching loop, (b) BBP/BBP mismatch spread over 8 dies, (c) 10-bit DAC decay without refresh depending on the starting value, (d) DNL of the 10-bit DAC.

a voltage around -2.1V would be required for full NMOS/PMOS mismatch compensation. In the PA stage, if the command of the 5 bit DAC controlling the applied BBN is too high, the BBP chosen by the current matching loop also saturates at -1.7V leading to compressed pulses in the negative phases. This asymmetric pulse shape contains more energy in low frequencies even after the first-order attenuation of the coupling capacitance leading to a reduced maximum allowable output power to meet the FCC regulations.

Fig. 4.24 also shows how the pulse shape modifies the measured output power spectrum density. With a Gaussian shape, we achieved around 8 to 10dB of attenuation in the 960-1610MHz restricted band. Varying the FBB applied on the PA output stages lead to a 5dB tuning range on the output power. The measured

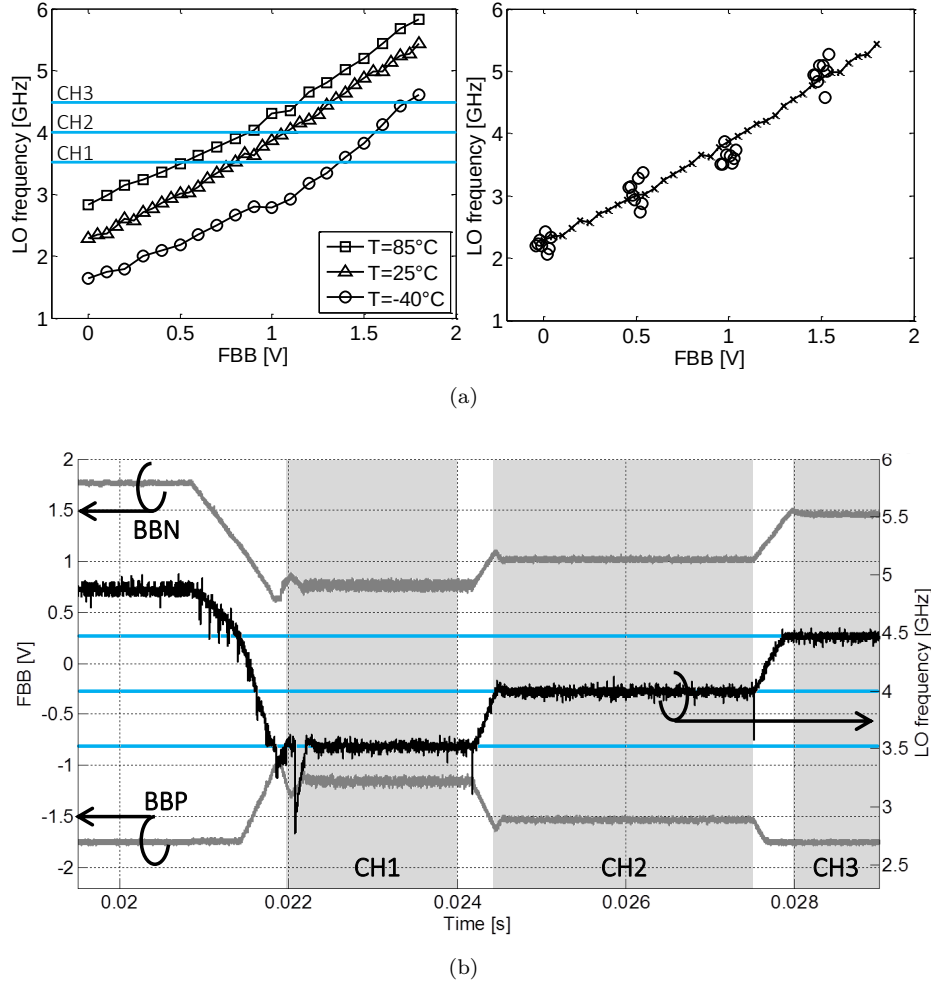


Fig. 4.23. (a) Left: measured LO frequency tuning range with FBB to compensate for temperature variations in the 3 targeted channels. Right: LO frequency variation over 8 dies for FBB from 0V to 1.5V. (b) Automatic LO frequency tuning demonstration over the 3 channels.

peak output power is -50dBm/MHz while respecting the FCC mask and the total output power is -20dBm.

The TX power breakdown is shown in Fig. 4.25. The combination of the full-custom baseband, LO, frequency divider, dual ring counters and pulse shaping are accounting for almost 60% of the total TX power. The PA output stages and their driving chains consumes equivalent power compared to the synthesized part of the TX.

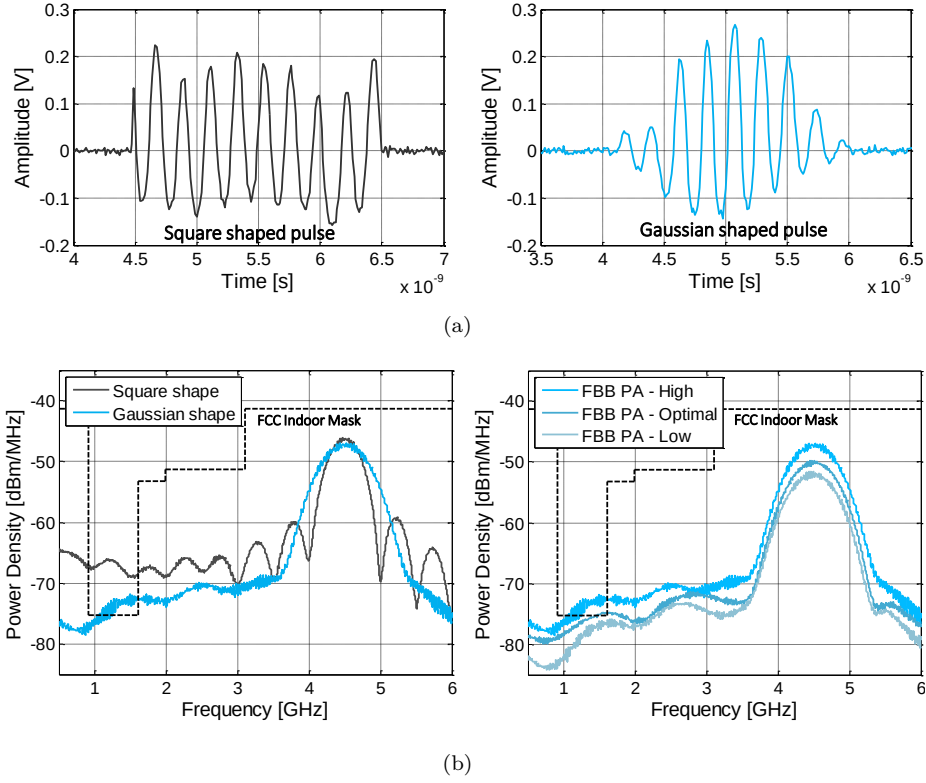


Fig. 4.24. Measured TX output temporal and spectral characteristics: (a) square- and Gaussian-shaped measured pulses, (b) power spectral densities depending on the pulse shape and the FBB applied on the PA.

4.5.5 Comparison to the State-of-the-Art

The complete SoC consumes $650\mu W$ at 27.24Mb/s leading to an energy per bit of 24pJ/bit . When considering only the TX with its synthesized and full-custom parts along with the FBB generator, the power consumption is only $380\mu W$ which corresponds to a record-breaking 14pJ/bit at 27.24Mb/s . Fig. 4.26 compares the energy efficiency of several 802.15.4a or proprietary UWB TX or transceivers depending on the data rate. *SleepTalker* achieves the lowest energy per bit over the 0.11Mb/s to 27.24Mb/s data rate range and improves by $16\times$ the energy efficiency of the best 802.15.4a TX [16]. [17] [18] [19] achieved closer results compared to this work with proprietary UWB communication schemes.

Table 4.3 compares the performances of recent IEEE 802.15.4a TX or transceivers. The proposed UWB TX is the first designed in 28nm FDSOI CMOS. The combined use of coarse to fine grain duty cycling, advanced CMOS

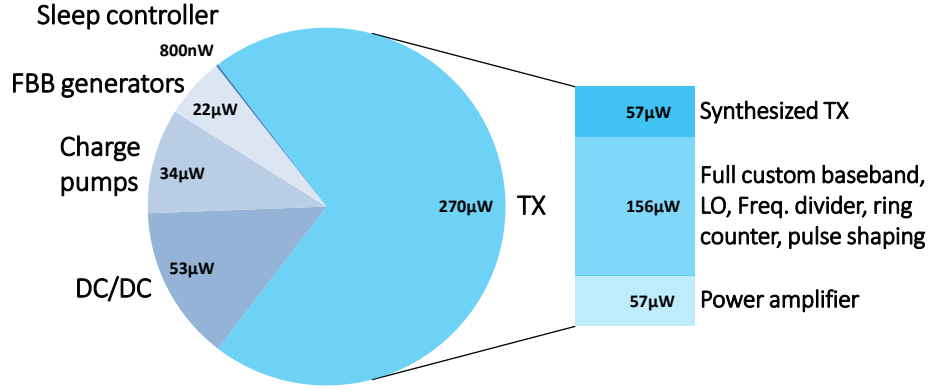


Fig. 4.25. SoC and TX power breakdown.

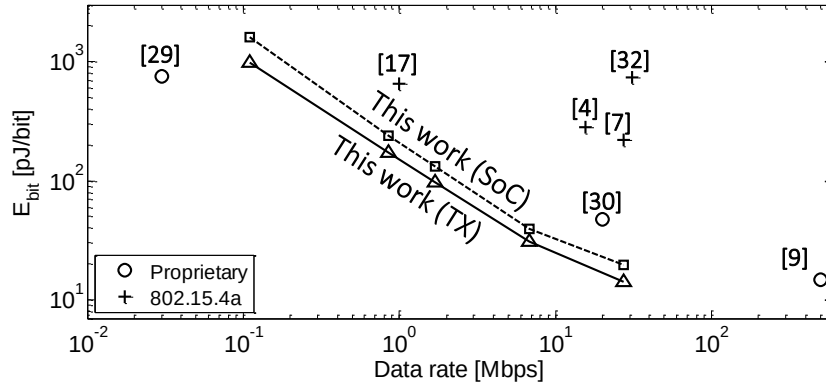


Fig. 4.26. Energy efficiency comparison with recent IR-UWB transmitters.

process, ULV operation enabled by FBB-induced V_T reduction and high-speed design explains the obtained ultra-low power consumption.

4.6 CONCLUSION

We demonstrated the first ULV 802.15.4a IR-UWB transmitter. It is also the first RF SoC in 28nm FDSOI and it fully exploits its forward back-bias capabilities for tuning RF performances. The transmitter achieves ultra-low power with $380\mu W$ at 27.24Mb/s and the high frequency of part of the TX was obtained by V_T reduction through FBB. A low power and FBB tunable BBCO is proposed and adaptive FBB is also used to compensate for the exacerbated PVT sensitivity

Table 4.3. Measured performances compared to the IEEE 802.15.4a compliant TX state-of-the-art

	[20]	[21]	[4]	[22]	[16]	This work
Process	90 nm	90 nm	90 nm	0.18 μ m	0.13 μ m	28nm FDSOI
Data rate [Mb/s]	0.11, 0.85, 6.8	16	15.6	27.24	0.11, 0.85, 1.7, 6.81, 27.24	0.11, 0.85, 1.7, 6.81, 27.24
Active power [μ W]	168300	650	4360	NA	5980	TX: 380 SoC: 650
Energy per bit [pJ/bit]	24700 @ 6.8Mb/s	650 @ 1Mb/s	280 @15.6Mb/s	740 @27.24Mb/s	219 @27.24Mb/s	TX: 14 SoC: 24 @27.24Mb/s
Die area [mm ²]	NA	0.066	0.07	4.5	RF: 7.5 Dig. BB: 24.7	TX: 0.095 SoC: 0.93
Supply Voltage [V]	3.3	1	1	1.8	1.2	External: 1.2 Core: 0.55* BB: +/-1.8*
Output swing [mV _{pp}]	~400	~100	165-710	NA	Up to 720	Up to 350
LO freq. range [GHz]	3.5-6.5	3-10	2.1-5.7	3-9	3.5-4.5	3.5-4.5

* Generated on-chip.

at ULV as well as for precise local oscillator frequency tuning to match one of the 3 channel frequency covered by the TX. Compliance with regulation masks is ensured by programmable pulse shaping and its power overhead is mitigated by the use of a ULV digital power amplifier. The high energy efficiency, small die area (0.93mm²) along with the full on-chip integration and the capability of operating on energy harvesting sources illustrate the potential of IEEE 802.15.4a compliant UWB communications for wireless sensor nodes targeting the Internet-of-Things.

Finally, this silicon prototype further serves as a demonstrator of the interest of using FBB for VT reduction to achieve timing closure in high-speed ULV logic. It also proves that adaptive FBB can effectively compensate PVT variations with limited power and area overheads for the closed-loop BB generation and distribution.

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CONCLUSIONS AND PERSPECTIVES

In this thesis, three questions related to high-performance ULV design have been investigated:

- How does FDSOI with its back biasing capability influence the energy/speed tradeoff in ULV digital circuits?
- How does FDSOI with its back biasing capability influence the power/performances in analog/RF circuits?
- How can the back biasing capability be used to design ULV radios while meeting the specifications of communication standard?

For each question, notable innovations have been proposed and studied through analytical models, numerical simulations and silicon demonstrator.

In the first 2 questions, we looked at improvements regarding the performance/energy tradeoff for ULV digital circuits (Chapter 2) and for analog/RF circuits (Chapter 3). In both cases, we started the analysis at micro level (gate/device) and confirmed the findings or the innovations at macro level (IP/circuit). Methodology as well as key results for digital and analog/RF functionalities of typical WNS at micro and at macro level are summarized in Fig. O.27.

O.6.1 How does FDSOI with its back biasing capability influence the energy/speed tradeoff in ULV digital circuits?

To answer this first question, we first looked at how ULV circuit performances evolve with technology scaling. We confirmed that increasing short-channel effect and variability in sub-90nm bulk technologies limit the improvement in MEP level and frequency that we can achieve and even harm these factors-of-merit in 45nm (Fig. O.27). In order to keep benefiting from technology scaling, we have to transition towards more advanced nodes featuring technology-level innovations such as high- κ metal gate for the 28nm bulk. But using LP 28nm bulk leads to a MEP achieved at lower frequency compared to GP process at previous technology nodes. This can be acceptable when designing classical WNSs featuring

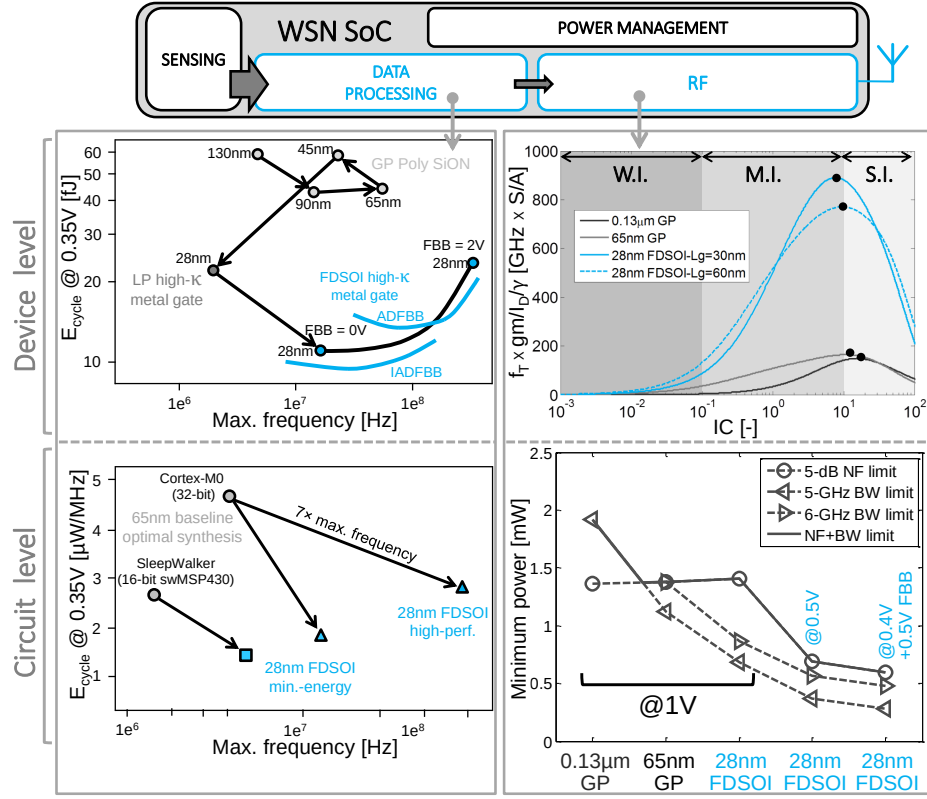


Fig. O.27. Summing up the main results and findings for the digital data processing and for the analog/RF functionalities. A key plot at device/gate level and at circuit/IP level is selected for both.

low computational load but the trend is to move toward computation-intensive embedded data-processing to limit the amount of data to be transmitted wirelessly to the cloud. Furthermore, the MEP level is only achieved at a given V_{DD} and frequency of operation which can be far from the required frequency harming the energy per operation. We showed that tunability of the MEP can be achieved through V_T modulation.

Using 28nm FDSOI allow us to achieve enhanced MEP frequency and reduced MEP level thanks to a strong mitigation of short-channel effects linked to an improved electrostatic control of the channel. We proposed to use the wide range of back-biasing to shift the MEP at higher frequency and to adapt the clock frequency to the fluctuating computational workload.

We also analysed the impact of NMOS/PMOS systematic mismatch on MEP position as well as on robustness. We provided a new method for systematic mismatch compensation along with two compensation schemes targeting absolute minimum energy or boosted frequency of operation. As shown in Fig. O.27, adaptive and inverse adaptive FBB further extend the range of frequencies that leads to an energy minimum and thus stretch the design space. Such adaptive schemes used to modify the speed/energy trade-off can reduce the MEP level by 18% and increase the speed by $36\times$. When looking at robustness, they can also provide a gate count improvement up to a factor of 6 while maintaining a 95% yield.

At IP level, we proved that FDSOI is an interesting solution to achieve absolute energy minimization at low speed or a higher-speed MEP. Compared to 65nm bulk, synthesis results show that the speed of ULV microcontrollers in 28nm FDSOI can be boosted by a factor of 7 in 28nm FDSOI and the E_{CYCLE} can be reduced by 64% with a mix of overdrive FBB voltages. We also showed that mixing FBB during synthesis can lead to energy-efficient implementations for a wide range of frequencies of operation and that a microcontroller core synthesized at high speed can be kept energy-efficient even at low speed when a lower FBB is applied in operation.

In this chapter, we aimed at giving a qualitative analysis of the phenomena in play when optimizing an ULV digital circuit supported by hypothesis validation through quantitative results extracted from realistic testbenches.

An interesting research direction for future work would be to first investigate the practical implementation of the FBB and DFBB schemes at layout level to minimize the die area and energy consumption overhead for FBB generation, routing and optimum tracking. The overhead of these circuitries will be mitigated by the size and complexity of the IP. The curvature of the MEP curve with V_{DD} and the spacing between the optimal frequency of operation and the actual throughput requirement can also cause strong energy per operation penalty. These reasons make difficult any predictions regarding an approximate range of energy reduction gained by ULV operations enhanced through FBB as it is strongly dependant on the application requirements and implementation details. However, we proved the interest of FBB for achieving high-speed ULV logic through the SleepTalker silicon demonstrator thanks to V_T mitigation and also to differential FBB between NMOS and PMOS.

O.6.2 How does FDSOI with its back biasing capability influence the power/performances in analog/RF circuits?

In order to analyze the impact of BB on analog/RF circuits, we first studied the impact of technology scaling on analog/RF figures-of-merit at device level such as f_T , g_m/g_d , noise or intrinsic linearity. Fig. O.27 recalls the evolution of

the device-level RF figure-of-merit depending on the inversion level of the device to show how the increase in f_T pushes the FoM higher with technology scaling. We then leveraged this high FoM_{dev} for power by operating at lower inversion level and we showed that scaling the V_{DD} in 28nm FDSOI can still lead to high performances compared to older technologies.

At circuit level, we proposed a sizing framework to optimally size a noise-cancelling LNA based on precise small-signal modelling. This framework allowed us to analyze, at circuit level, the impact of V_{DD} scaling and how technology scaling, moderate inversion design and FBB can help mitigating the performance reduction linked to this scaling. We showed that NF minimization under constraints for wideband noise-cancelling LNA leads to competitive RF performances for SDR applications. ULV operation is possible in 28nm FDSOI thanks to the high f_T and allows reaching sub-1mW power with acceptable RF and noise performances. We also showed that, combined with FBB, ULV operation saves 47% of the power at 5dB NF. We demonstrated that technology and voltage scaling on the noise-cancelling LNA leads to a shift of the dominant design constraint from bandwidth to noise (Fig. O.27).

O.6.3 How can the back biasing capability be used to design ULV radios while meeting the specifications of communication standard

To illustrate the potential of BB to enable ULV RF circuits, we designed an ULV RF SoC implementing an IR-UWB transmitter codenamed SleepTalker. It is the first ULV IEEE 802.15.4a IR-UWB transmitter and the first RF SoC in 28nm FDSOI. It fully exploits the forward back-bias capabilities of FDSOI for functionality tuning of RF performances such as carrier frequency or output power, V_T mitigation and PVT tuning.

The SleepTalker prototype occupies 0.93mm² and was fabricated and tested successfully.

The transmitter achieves ultra-low power with 380μW at 27.24Mb/s which corresponds to a record-breaking 14pJ/bit for the TX-only and 24pJ/bit when considering the complete SoC. A low power and FBB tunable BBCO is proposed and adaptive FBB is also used to compensate for the exacerbated PVT sensitivity at ULV as well as for precise local oscillator frequency tuning to match one of the 3 channel frequencies covered by the TX. Compliance with regulation masks is ensured by programmable pulse shaping and its power overhead is mitigated by strong duty-cycling of the power amplifier. The high energy efficiency, small IC area along with the full on-chip integration and the capability of operating on energy harvesting sources illustrate the potential of IEEE 802.15.4a compliant UWB communications for wireless sensor nodes targeting Internet-of-Things applications.

The author's vision

This dissertation is heavily based on technology aware design and extensive exploration of circuit and technology interactions. Over the last decade, this trend gained popularity in the IC world and especially in the research community. The predicted and already appearing saturation of Moore's law due to scaling limitations of classical CMOS is, to the author's opinion, pushing the designer to go further in the exploitation of the technology's potential at circuit level. Smart technology and circuit co-design can help mitigate the impact of unavoidable parasitic effects appearing with deeply-scaled CMOS and thus can extend Moore's trend. Regarding the analog/RF design, it is the author's conviction that sub-45nm CMOS technologies, whose development is mainly driven by digital applications, bring the intrinsic transistor performances to a new level. The RF community is only starting to adopt those technologies as well as to learn how to mitigate the lower V_{DD} and intrinsic gain to eventually fully benefit from their high- f_T and wide BB range (for FDSOI). Delivering low-cost, highly-integrated, wideband and versatile transceiver while controlling the DC power consumption will require extensive technology-aware design techniques and poses an exciting challenge for the future.

APPENDIX A

WIDEBAND LNA SMALL SIGNAL MODEL

In this dissertation, we set up a methodology for efficient sizing of a noise-cancelling LNA as discussed in Section 3.3. In this appendix, we present the generated small-signal model developed in Matlab to enable fast exploration of the design space. Both the traditional model from the state-of-the-art and the model developed in this work are implemented to allow comparison. The equations are synthesized in Fig. A.1.

```

1  function [Zin1, Zin2, AVP1, AVN1, AV1, AV_err1, AVP2,
2      AVN2, AV2, AV_err2, NF, F, FM1, FM2, FRL1RL2, NF_2,
3      F_2, FM1_2, FM2_2, FRL1_2, FRL2_2, FRB_2, TFM1, TFM2,
4      TFRL1, TFRL2, TFRB, VXM1, VOPM1, VOMM1, VOPM2, VOMM2,
5      VXRL1, VOPRL1, VOMRL1, VXRL2, VOPRL2, VOMRL2, VXRb,
6      VOPRB, VOMRB, TFRS] = LNA_modeling(gm1, gm2, RL1, RL2
7      , RB, gd1, gd2, gam_M1, gam_M2)
8
9  RS = 50; % Antenna equivalent resistance
10
11  Zin1 = 1./ ( gm1 + 1./RB ); % Input impedance SoA model
12  Zin2 = 1./ ( gm1 + gd1 + 1./RB - (RL1.*gd1.*(gm1+gd1))./(RL1
13      .*gd1+1) ); % Input impedance GDS model
14
15  k = 1.3806488e-23; % Boltzmann constant
16  T = 298; % Temperature in K
17
18  % ----- Small Sig model -----
19  AVP1 = RL1.*gm1; % SoA model:
20      Positive branch gain
21  AVN1 = -RL2.*gm2; % SoA model:
22      Negative branch gain

```

```

16 | AVP2 = (RL1.*(gm1+gd1))./(gd1.*RL1+1);           % GDS model:
    |     Positive branch gain
17 | AVN2 = -(RL2.*gm2)./(gd2.*RL2+1);               % GDS model:
    |     Negative branch gain
18 | AV1 = AVP1-AVN1;                                % SoA model:
    |     total gain
19 | AV2 = AVP2-AVN2;                                % GDS model:
    |     total gain
20 |
21 | AV_err1 = AVP1+AVN1;                             % SoA model:
    |     gain difference between branches
22 | AV_err2 = AVP2+AVN2;                             % GDS model:
    |     gain difference between branches
23 |
24 |
25 | % ----- Small Sig noise model SoA -----
26 | FM1 = (gam_M1.*gm1.*((RL1-RS.*gm2.*RL2).^2))./(RS.*(AV2
    |     .^2));           % SoA model: Noise contrib. from M1
27 | FM2 = (gam_M2.*gm2.*(RL2.^2).*((1+gm1.*RS).^2))./(RS.*(
    |     AV2.^2));       % SoA model: Noise contrib. from M2
28 | FRL1RL2 = ((RL1+RL2).*((1+gm1.*RS).^2))./(RS.*(AV2.^2));
    |           % SoA model: Noise contrib. from RL1 and
    |           RL2
29 | F = 1+FM1+FM2+FRL1RL2;
    |
    |           % SoA
    |     model: total F
30 | NF = 10*log10(F);
    |
    |           %
    |     SoA model: total NF
31 |
32 | % ----- Small Sig noise model GDS -----
33 | RX = 1./(1./RS+1./RB);                           % Equivalent
    |     resistance at the drain of M1
34 | VXM1 = 1./(gm1+gd1+(1+gd1.*RL1)./RX);             % Voltage at
    |     the drain of M1
35 |
36 | TFRS = AV2.*Zin2./(RS+Zin2);                     % GDS model: transfer
    |     function from RS to OUT
37 |

```

```

38 VOPM1 = (RL1.*(gm1+gd1).*VXM1)./( (1+gd1.*RL1) ) - RL1
      ./(1+gd1.*RL1);    % GDS model: M1 to positive branch
      OUT
39 VOMM1 = -(gm2.*RL2.*VXM1)./( (1+gd2.*RL2) );
      % GDS model: M1 to negative
      branch OUT
40 TFM1 = VOPM1 - VOMM1 ;
      % GDS
      model: transfer function from M1 to OUT
41
42 VOPM2 = 0;                % GDS model: M2 to
      positive branch OUT
43 VOMM2 = -RL2./(1+gd2.*RL2);    % GDS model: M2 to
      negative branch OUT
44 TFM2 = VOPM2 - VOMM2;        % GDS model: transfer
      function from M2 to OUT
45
46 VXRL1 = gd1./(gm1+gd1+1./RX+(gd1.*RL1)./(RX));
47 VOPRL1 = (RL1.*RL1.*gd1.*(gm1+gd1))./( (gm1+gd1+1./RX+gd1
      .*RL1./RX).*(1+gd1.*RL1) ) + RL1./(1+gd1.*RL1);
      % GDS model: RL1 to positive branch OUT
48 VOMRL1 = -(gm2.*gd1.*RL2.*RL1)./( (gm1+gd1+1./RX+gd1.*RL1
      ./RX).*(1+gd2.*RL2) );
      % GDS model: RL1 to
      negative branch OUT
49 TFRL1 = VOPRL1 - VOMRL1;
50
51 VXRL2 = 0;
52 VOPRL2 = 0;                % GDS model: RL2 to
      positive branch OUT
53 VOMRL2 = -RL2./(1+gd2.*RL2);    % GDS model: RL2 to
      negative branch OUT
54 TFRL2 = VOPRL2 - VOMRL2;        % GDS model: RL2 to
      negative branch OUT
55
56 VXRB = -(1+gd1.*RL1)./( (gm1+gd1+1./RX.*(1+gd1.*RL1) )
      );
57 VOPRB = -(RL1.*(gm1+gd1))./( (gm1+gd1+1./RX.*(1+gd1.*RL1
      ) ) ) ;
      % GDS model: RB to
      positive branch OUT

```

```

58 VOMRB = +(gm2.*RL2.*(1+gd1.*RL1))./( (gm1+gd1+1./RX.*(1+
      gd1.*RL1)).*(1+gd2.*RL2) ); % GDS model: RB to
      negative branch OUT
59 TFRB = VOPRB - VOMRB;

      % GDS model: RB to negative branch OUT
60
61 FM1_2 = (gam_M1.*gm1.*((TFM1).^2))./(RS.*((AV2.*Zin2./(RS
      +Zin2)).^2)); % GDS model: Noise contrib. from M1
62 FM2_2 = (gam_M2.*gm2.*((TFM2).^2))./(RS.*((AV2.*Zin2./(RS
      +Zin2)).^2)); % GDS model: Noise contrib. from M2
63 FRL1_2 = (1./RL1).*((TFRL1).^2)./(RS.*((AV2.*Zin2./(RS+
      Zin2)).^2)); % GDS model: Noise contrib. from
      RL1
64 FRL2_2 = ((TFRL2).^2)./(RL2.*RS.*((AV2.*Zin2./(RS+Zin2))
      .^2)); % GDS model: Noise contrib. from
      RL2
65 FRB_2 = ((TFRB).^2)./(RB.*RS.*((AV2.*Zin2./(RS+Zin2))
      .^2)); % GDS model: Noise contrib. from
      RB
66
67 F_2 = 1+FM1_2+FM2_2+FRL1_2+FRL2_2+FRB_2; % GDS
      model: total F
68 NF_2 = 10*log10(F_2); % GDS
      model: total NF
69
70
71 end

```

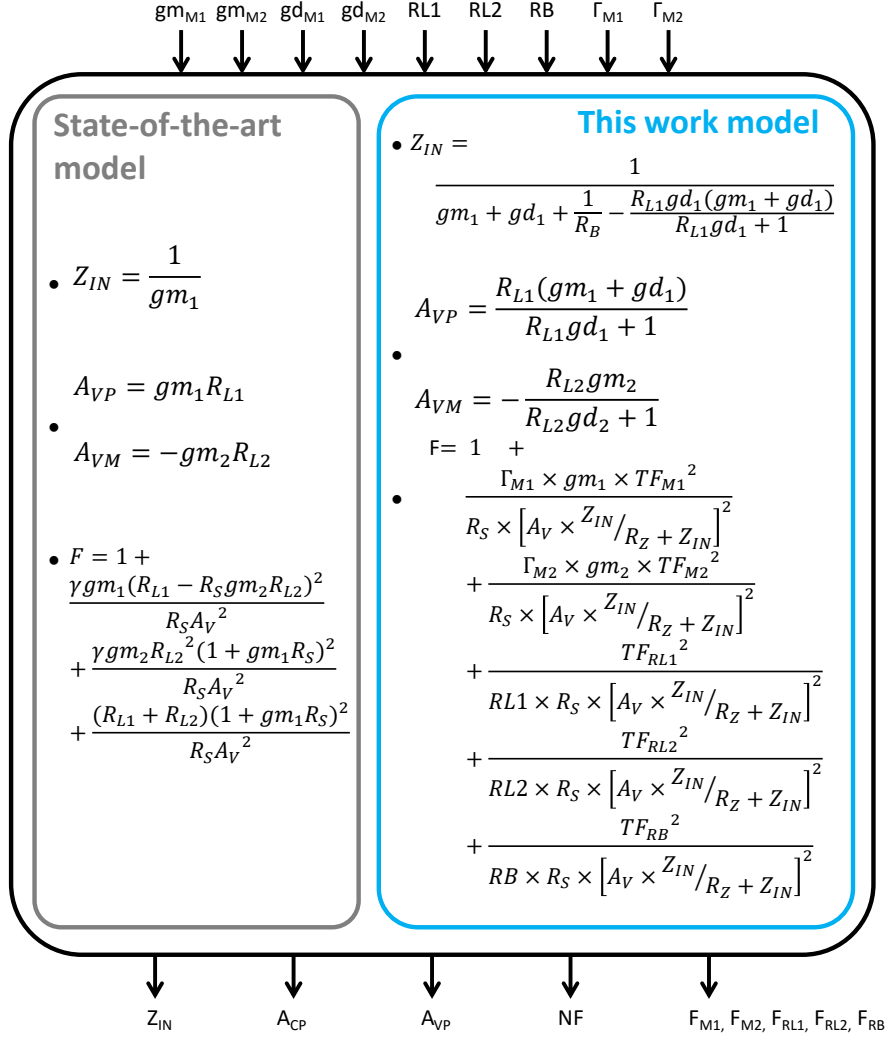


Fig. A.1. Equations of the LNA small-signal model from the state-of-the-art and from this work giving the analytical values of the input impedance, the differential gain and the noise figure.