RF harmonic distortion modeling in silicon-based substrates including non-equilibrium carrier dynamics

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***Abstract*— In this paper, a simulation methodology is presented that takes carrier dynamics into account, disallowing instantaneous changes in substrate carrier concentrations, and providing more accurate estimations of harmonic distortion (HD) components. Using this method, we simulated the HD components introduced in a CPW line on various flavors of Si-based substrates. The results are compared to measured HD components over a wide range of bias points and at three fundamental excitation frequencies from 900 MHz to 4 GHz. It is shown that carrier relaxation times are of first importance for understanding the HD levels introduced by Si-substrates at RF frequencies and above. Furthermore, characteristic dips in the extracted HD components, for increasing fundamental power, are evaluated and shown to be tightly linked to the position of the device's DC bias voltage relative to the substrate's flatband voltage. The new simulation tool is also capable of capturing these typical dips in the HD curves, and provides physical insight into the reasons behind their existence.**

***Index Terms*—Harmonic distortion, high-resistivity Si substrate, large-signal analysis, non-linear characterization.**

I. Introduction

Semiconductors are non-linear materials by nature, as their local electrical resistivity depends on the voltage that is applied to them (field effect). This means that a semiconductor's carrier distribution, and therefore its equivalent impedance towards a ground node, vary as a function of the applied time-dependent signal. Passive elements designed on such non-linear substrates will present harmonic distortion (HD) between their inputs and outputs, modifying the desired waveform and deteriorating the quality of the information present.

Modeling the distortion introduced by non-linear substrates in overlying devices is a real challenge, as at RF frequencies the carrier responses lag behind the applied signal. Works such as [1] made first attempts at such modeling, but because they based their methods on small-signal C(V) and G(V) parameters obtained over a range of DC biases, carrier dynamics and response times were neglected, and it was assumed that the local carrier concentrations could vary instantaneously in response to a rapid large-signal variation. This lead their simulation results to be systematically overestimated when compared with the electrical measurements of silicon-on-insulator (SOI) samples. At RF frequencies and beyond, rapid large-signal variations do not allow for carrier equilibriums to be achieved, and the carrier concentrations never have time to converge to those that were extracted under DC equilibrium. Rather, the entire substrate below and around the device shares in a non-equilibrium state, in which carriers are constantly being generated, recombined or physically displaced to minimize the non-equilibrium in response to the rapid large-signal perturbation. Because carrier responses lag behind the applied voltage at RF frequencies, carrier dynamics are required to be taken into account when modeling for the substrate induced HD.

In this paper, a simulation methodology is presented that takes into account carrier dynamics, disallowing instantaneous changes in substrate carrier concentrations, and providing more accurate estimations of HD components. Using this new method, we simulated the HD components introduced in a CPW line on various substrates. The results are compared with measured HD components on three Si-based substrates: high-resistivity (HR-) SOI (nominal bulk resistivity >3 kΩcm), standard resistivity (Std-) SOI (nominal bulk resistivity 5-20 Ωcm), and trap-rich (TR-) SOI; for three input fundamental frequencies: 900 MHz, 2 GHz and 4 GHz; and over a range of bias conditions from -30 V to +30 V.

II. Measurements of Substrate Induced Harmonic Distortion Components and Dependence on DC Bias

A. Harmonic distortion in CPW lines on SOI substrates

Large-signal measurements of CPW lines were performed on-wafer using a dedicated setup [2] based on an Agilent 4-port PNA-X vector network analyzer. A single tone, with fundamental frequency of 900 MHz, 2 GHz or 4 GHz, is injected into one port of the CPW line on each substrate. The power of this input tone, that we shall denote as H'1, is swept from -30 dBm to +25 dBm using 50 Ω reference port impedances, and the output is

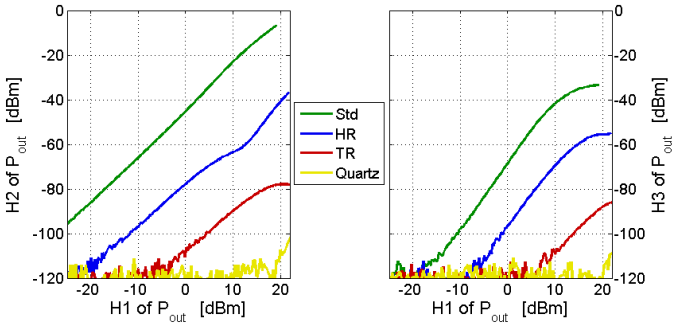

Fig. 1. Comparison of measured HD levels at 900 MHz induced in a 50 Ω 8 mm-long CPW line, biased at 0 V, on various Si-based substrates.

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retrieved by a spectrum analyzer. Due to the non-linear behavior of Si-based substrates signal distortion is introduced and the output is in general a multi-tone signal, with a fundamental component, denoted as H1, along with harmonic components at all integer multiples of the fundamental frequency, denoted as H2, H3 and so on. The H2 and H3 components of the power at the output of the CPW (biased at 0 V) on each substrate are plotted against the power of the fundamental component H1 in Fig. 1, at 900 MHz. The electrical characteristics of Std and HR substrates are strongly voltage-dependent [3]-[4]. Consequently, these two substrates show high HD levels. On the other hand, quartz acts as a pure dielectric material, introducing almost no HD at all into the CPW lines.

By introducing a poly-Si trap-rich layer beneath the BOX of a nominally HR substrate, strong reduction in the HD components is achieved [5]-[7]. The traps at the Si/SiO_2 interface effectively pin the Fermi-level near mid-gap. Contained to a narrow energy range by these traps, the position of the Fermi-level is rendered much less voltage-sensitive, improving the linearity of the substrate and reducing the distortion in signals propagating through overlying transmission lines.

B. Dips: biasing the CPW close to substrate flat-band voltage

Because the Fermi-level in TR substrates is pinned, the measured HD components show very little DC voltage sensitivity [1]. In contrast, Std and HR substrates HD levels drastically vary by up to 35 dBm when shifting the DC bias of the line as can be seen from Fig. 2. HD curves in these highly voltage sensitive Si-substrates almost always present characteristic dips when biased near their flatband voltages, as illustrated.

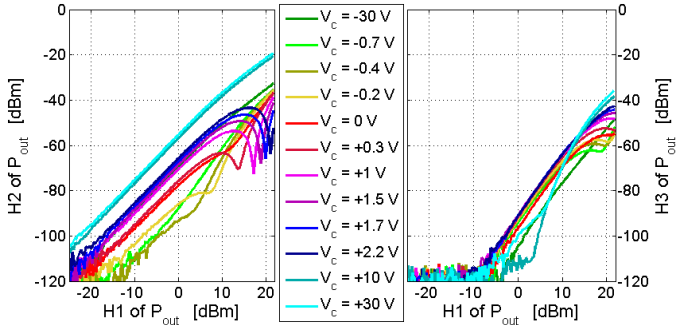

Fig. 2. Measured HD at different DC biases for a 900 MHz input to a CPW line on a HR (>3 kΩcm) N-type substrate with a flatband voltage of -1.4 V.

Dips in the H2(H1) and H3(H1) power curves are observed, and their location along the H1 axis is dependent on DC bias. C-V measurements of the wafer revealed a flatband voltage around -1.4 V, and it is shown in Table I that the dips occur at the power levels corresponding approximately to the peak voltage amplitudes that sweep through the device's flatband region from the DC bias point. Using equation (1), the peak amplitude V_{pk} (in Volts) of the voltage wave at the output of the CPW line is obtained from the measured H1 component (in dBm) in a 50 Ω system.

$$V_{pk} = 10^{\frac{H1-10}{20}} \quad (1)$$

TABLE I
AMPLITUDES AT DIP FOR DIFFERENT DC BIASES

DC bias V_{DC} [V]	0.3	1.0	1.5	1.7	2.2
Power H1 at dip [dBm]	13.7	17.3	18.8	20.0	21.2
Amplitude V_{pk} at dip [V]	1.53	2.32	2.75	3.16	3.63
V_{DC}-V_{pk} [V] (close to V_{FB})	-1.23	-1.32	-1.35	-1.46	-1.43

This relationship is used to pass from the H1 power levels in the 2nd row of Table I to the corresponding voltage amplitude in the 3rd row of the table. For example, when the CPW is biased at +1.0 V, a large signal amplitude of 2.3 V (17.3 dBm) is necessary to sweep through the flatband point with the RF signal, while a large signal amplitude of 2.6 V (11.2 dBm) is necessary when biasing the device at +2.2 V. Each time the large-signal voltage amplitude on the line sweeps the RF signal through the flatband region, a dip in the HD curves are observed. The origin of these dips is discussed further in Section III.C.

III. CARRIER DYNAMICS AT RF FREQUENCIES

At RF frequencies, large signals pulse the substrate from accumulation to inversion (for example) on the first half-cycle of the sinusoidal voltage in a fraction of a nanosecond, requiring majority carriers to be pushed away from the interface and recombine in the bulk, and minority carriers to be generated and displaced to the interface in large quantities. At RF frequencies the carriers do not have time to reach an equilibrium distribution before the second half-cycle of the RF voltage pulses the structure back from inversion to accumulation.

A. Finite response time of free carriers

To investigate the response times of carriers in Si substrates, a MOS capacitor structure on a 1 kΩcm HR N-type substrate is defined for simulation using Silvaco Atlas software, to account for carrier dynamics, recombination, and generation processes [8]. A voltage step, with a ramp time of 1 ps is applied to the MOS capacitor, pulsing it rapidly from strong inversion to strong accumulation. The results presented in the left graph of Fig. 3 show that the carriers at the surface respond in around 1-10 ns to the applied voltage step due to their finite inertia. This corresponds to the majority carrier dielectric relaxation time in

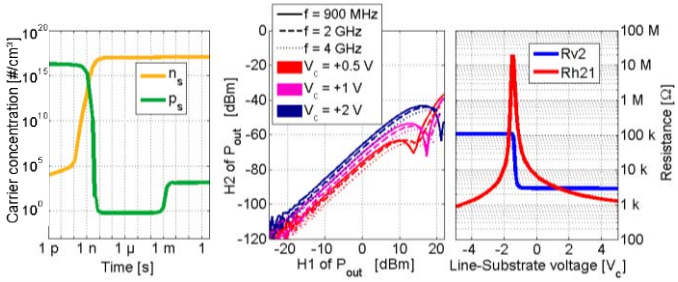

Fig. 3. Left: simulated dynamic surface carrier response in a MOS capacitor pulsed from strong inversion to strong accumulation on an N-type HR-SOI substrate (1 kΩcm). Middle: measured HD at different DC biases and fundamental frequencies input to a CPW line on a HR N-type substrate (>3 kΩcm). Right: $R^{Stat}(V)$ voltage dependence of the circuit model substrate resistors obtained through DC static simulations (results shown only between -5 and +5 V).

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the silicon substrate that are swept away from the surface in a few nanoseconds. Although almost all variations occur within this time-frame we note that full equilibrium is reached only after around 1 ms. Before this time, carriers are rearranged spatially within the considered volume in response to the electrical pulse, but it is only after a few milliseconds that thermal generation and recombination processes allow for the final carrier concentrations to be reached in the structure [8] (absolute total number of carriers in the entire volume to change).

Equation (2) gives the dielectric relaxation time of a substrate with resistivity ρ and permittivity ϵ [9]. For a 1 kΩcm silicon substrate this time corresponds to 6.6 ns, agreeing with the above transient simulation.

$$\tau \approx 2\pi\rho\epsilon = 6.6 \text{ ns} \quad (2)$$

It should be noted that this response time can vary significantly when introducing high trap densities, and/or many deep-level generation/recombination centers near the surface [10].

The middle graph of Fig. 3 plots the CPW output component H2(H1) on the HR substrate at a few DC bias points for varying input fundamental frequencies. This component is reduced by 2 dB from 900 MHz to 2 GHz, and is further reduced by 3 dB from 2 GHz to 4 GHz. These reductions in HD are directly linked to the finite response time τ of the carriers. As the product $f\tau$ is increased the substrate carriers respond less in amplitude to the rapid signal, and the substrate non-linearities are attenuated.

B. Modeling of non-linear substrates with carrier dynamics

Fig. 4 presents a voltage and time dependent circuit model of a CPW line on a lossy semiconductor substrate. It takes into account carrier variations beneath the signal conductor. The 15 resistive elements beneath and around the line highlighted in red are modeled as voltage and time-dependent. All other resistors are located in regions unaffected by the varying line voltage and are defined as purely linear elements. Capacitors are also

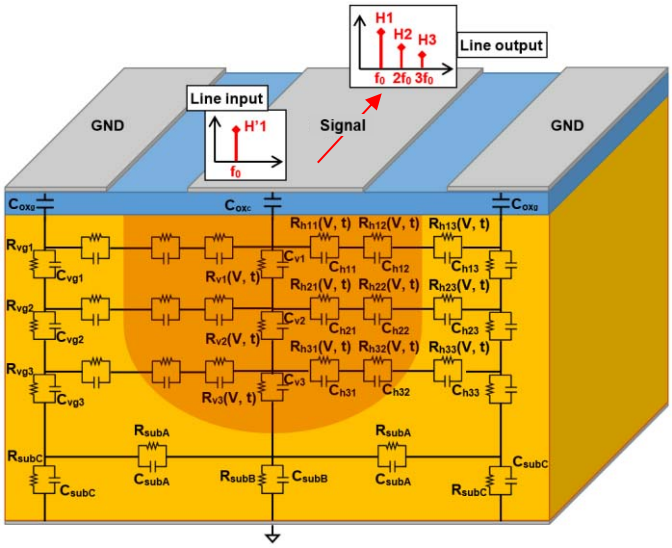

Fig. 4. Voltage and time-dependent substrate circuit model.

defined as linear elements because physically it is the local resistivity that varies with the large-signal, not the permittivity. Resistors R_{vn} and R_{hn1} model the resistive nature of the silicon volume directly below the signal line, whereas resistors R_{hn2} model thin transition regions slightly to the left and to the right of the signal line. All 15 resistive elements are calculated by integrating the carrier distribution profiles extracted from Silvaco Atlas substrate simulations over a wide range of DC points, which in turn give us the static values of each resistance as a function of voltage: $R^{Stat}(V)$. The static curves of 2 of the 15 non-linear resistors are given in the right graph of Fig. 3. If carrier inertia is not taken into account, and we consider that any change in the line voltage results in an instantaneous change in these resistive elements, then the variations in these resistances would be seriously over-estimated at high frequencies. Denoting the carrier relaxation time as τ, serious errors result for frequencies around and beyond $1/\tau$, at which the HD levels would be highly over-estimated.

Our model solves for the voltage waveform at the end of the line using a finite-difference time-domain (FDTD) method taking into account the voltage dependent variations of the resistive substrate elements. To account for carrier inertia we disallow instantaneous variations in the non-linear resistors. At each time step i, the voltage is ramped from V_i to V_{i+1}, and the resistor variations are calculated as follows:

$$R_{i+1} = R^{Stat}(V_{i+1}) - \exp(-\Delta t/\tau) \cdot (R^{Stat}(V_{i+1}) - R_i) \quad (3)$$

where τ is a time constant parameter introduced to account for the lagging of the resistance variations behind the applied signal. Equation (3) reduces simply to $R^{Stat}(V_{i+1})$ if $\Delta t/\tau$ is large. This is the case for fast responding substrates (τ is very low), and/or for low frequency signals (f_0 is very low so Δt is very large). In the RF domain, Δt will be of the order of a fraction of a nanosecond or shorter, and as we have seen from the transient response of a MOS capacitor (see Fig. 3 left), the carrier concentrations have response times of the order of the nanosecond, making carrier relaxation of first importance in RF applications on Si-based substrates.

C. Origin and modeling of dips in HD curves

As can be seen from the static $R^{Stat}(V)$ curve in Fig. 3, the voltage-response of R_{h21} is non-monotonic, and the sign

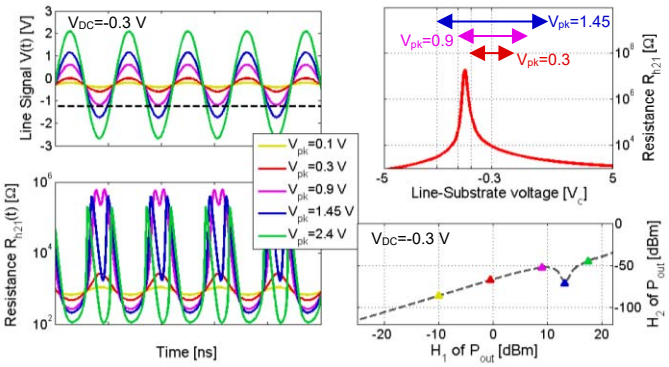

Fig. 5. Time-domain analysis of dips using the circuit model in Fig. 4.

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change in the slope occurs close to the flatband voltage of approximately -1.4 V. Fig. 5 analyzes the response of resistor R_{h21} through time when varying the voltage amplitude applied around a DC bias point of -0.3 V. The simulated H2(H1) power curve is also reprinted at this bias voltage, and the voltage amplitudes of interest can be found marked on this curve. The analysis shows that when the RF voltage sweeps through the non-monotonic point, close to the flatband voltage, then the H2 component dips down (blue data). When the resistance ceases to monotonically increase with the applied voltage, but suddenly decreases over the last part of the negative cycle of the large signal RF voltage wave, this resistance appears more linear because its direction of variation suddenly changes, instead of continuing along the same non-linear trend.

As was the case for the measurements, the dips from the modeling results also present dependence on DC bias, as shown in Fig. 6.

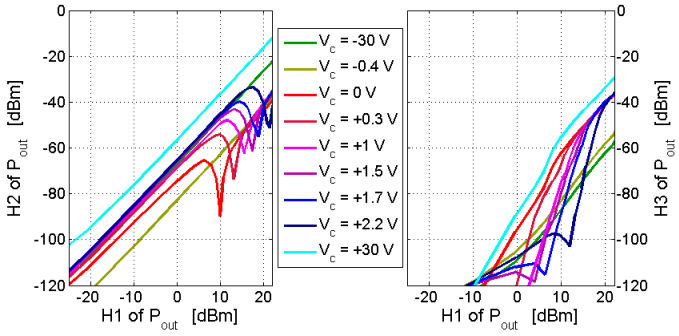

Fig. 6. Simulated HD at different DC biases for a 900 MHz input to a CPW line on a HR N-type substrate characterized by a flatband voltage of -1.4 V.

Furthermore, this new modeling approach enables the HD components to no longer be drastically over-estimated. Indeed, by taking carrier inertia and relaxation into account from (3), the model of a CPW on the HR-SOI substrate allows for more realistic simulations: a reduction of approximately 15 dB follows from the introduction of a time constant of the order of a nanosecond as compared to simulations that allow for instantaneous substrate variations (obtained by setting $\tau = 0$).

The modeling results in Fig. 6 were obtained by simulating a calibrated substrate in order to get a close fitting to the measurement results in Fig. 2 over the entire DC voltage range. The nominal bulk resistivity and interfacial charge density in the simulated HR-SOI substrate were tailored to agree well with the substrate CV measurements in terms of flatband voltage (-1.4 V) and capacitance response. Then, the time constant parameter that enabled the best fitting of the simulated HD levels to the measured HD levels was found to be 1.3 ns. Under these conditions, the reader is invited to observe the agreement between simulations and measurements by comparing Fig. 2 and Fig. 6, in particular in terms of absolute HD levels, and their dependence on DC bias, as well as the location of the dip in the H2 components along the H1 axis at the different DC bias points.

IV. Conclusion

In this work, substrate carrier dynamics were considered for the first time in HD simulations for RF applications. The results show that carriers lag the RF signal with time constants on the order of nanoseconds, which when taken into account, enable the model to estimate more accurately the induced HD. Furthermore, bias-dependent dips in measured HD curves were presented and discussed for the first time. Their presence is shown to be due to the signal sweeping through the flatband region of the device, and the new modeling method is shown to be able to reproduce this behavior and help explain it.

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