Porous Silicon Waveguides for Integrated Sub-THz Systems

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***Abstract*—This letter presents the first experimental demonstration of a new type of silicon-integrated sub-terahertz (THz) waveguide, based on porous silicon (PS). The waveguide (WG) is realized on an ultralow-resistivity (ULR) silicon substrate using a single-step electrochemical anodization that codefines material and geometry, eliminating deep reactive-ion etching (DRIE) and wafer bonding. A coplanar-waveguide-to-PS-WG transition enables direct on-wafer characterization. The fabricated PS WG is targeted for D-band operation and exhibits a measured attenuation loss of 0.7 dB/mm at 140 GHz, in excellent agreement with full-wave simulations. This confirms the validity of the codesign approach. Combining low loss, simplified fabrication, and inherent material tunability, the proposed PS WG offers a promising route toward highly integrated sub-terahertz passive components and enables future gas and biosensing applications.**

***Index Terms*—D band (110–170 GHz), porous silicon (PS), sub-terahertz (sub-THz) integration, transition, ultralow resistivity (ULR), waveguide (WG).**

I. Introduction

SUB-TERAHERTZ (THz) technology is attracting growing attention for future applications in high-speed communication, imaging, and spectroscopy [1], [2]. However, the realization of highly compact sub-THz (100–300 GHz) systems remains challenging because traditional planar transmission lines such as microstrip and coplanar waveguides suffer from high loss (>1 dB/mm) at these frequencies [3]. For this reason, low-loss rectangular waveguides (WGs) fabricated by computer numerical control (CNC) milling of metal blocks have long been used to build high-performance sub-THz systems. Yet, such split-block approaches are unsuitable for large-scale integration due to their bulky size, serial processing, and high fabrication costs.

To overcome these limitations, silicon-integrated WGs based on MEMS fabrication have been introduced. Deep reactive-ion etching (DRIE)-based MEMS WGs represent a key milestone in the pursuit of integrated sub-THz systems, as they allow fine control of WG cross sections and benefit from wafer-level processing [4], [5], [6], [7]. Thanks to their precisely defined geometry and smooth sidewalls, such micromachined WGs can achieve extremely low propagation losses, with reported attenuation levels as low as 0.007–0.013 dB/mm in the D band (110–170 GHz) [8]. It makes MEMS WGs one of the most attractive solutions for high-frequency integration. Nevertheless, their manufacturing remains highly complex and costly. DRIE is strongly pattern-dependent and requires careful process optimization to obtain smooth vertical sidewalls in order to minimize conductor losses. Furthermore, most DRIE WG implementations necessitate wafer bonding [5], [7], [9], which further increases cost and process complexity. In an alternative perspective, porous silicon (PS) has emerged as a promising material for high-quality transmission lines and passive devices on silicon due to its adjustable electrical and optical properties. PS also features several beneficial properties, including high resistivity (HR), low losses, minimal crosstalk, and excellent linearity [10], [11], [12]. In this letter, we introduce a fundamentally new integration scheme based on PS (for which a theoretical study was presented in [12]). Unlike metastructures or conventional MEMS WGs, this approach directly forms the WG core within an ultralow-resistivity (ULR) silicon substrate by electrochemical anodization. It thus codefines both material and geometry in a single step, eliminating DRIE and wafer bonding steps. PS waveguides have been studied in optics for light guiding and sensing [13], [14]. At sub-THz frequencies, however, confinement arises from conductivity contrast between the HR PS core and the ULR Si substrate, rather than refractive index contrast. This letter demonstrates for the first time a D-band PS waveguide exploiting these properties for integrated sub-THz systems. In the future, this platform could further leverage the benefits of porous Si by supporting the fabrication of sub-THz gas or bio sensors [15], [16]. Section II details the concept of the PS WG platform, describes the fabrication process, and presents its electrical behavior. Section III illustrates the fabricated devices with CPW-to-PS-WG transitions for on-wafer characterization. The characterization setup and extracted attenuation loss are also presented. For the first time, the successful propagation of a D-band signal within a PS WG integrated on a ULR Si substrate is demonstrated. Within this sub-THz range, the D band is strategically chosen in this study as it is one of the bands targeted for 6G [17], [18], and because CMOS technologies have already demonstrated a lot of capabilities in this frequency range [19], [20].

II. D-Band PS Waveguide

A. Concept of PS WG

The PS WG concept is illustrated in Fig. 1(a). It features an HR core of PS [16] embedded within a ULR Si substrate (resistivity $\rho_{Si} \leq 1$ m$\Omega \cdot$ cm) and a metal layer covering

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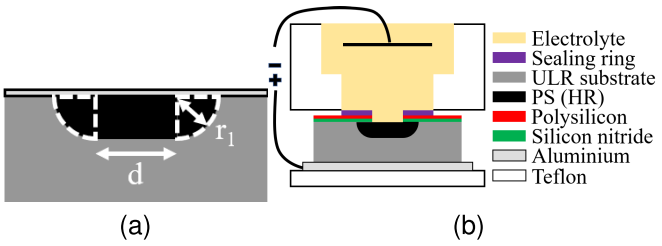

Fig. 1. (a) Cross-sectional profile of PS WG concept. (b) Schematic of the PS fabrication cell.

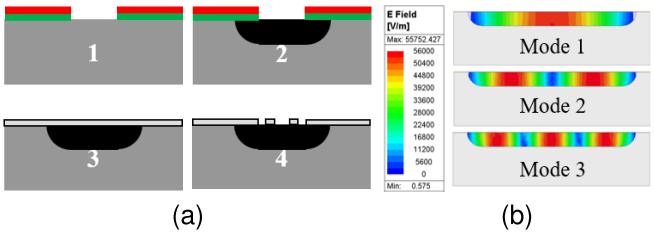

Fig. 2. (a) Detailed fabrication process steps. (b) Modes analysis of "U-shaped" PS WG.

its top surface. In this configuration, the substrate behaves similar to the "metal" part of conventional WGs, owing to its ultralow resistivity. The PS core of the WG is built through electrochemical etching of the bulk ULR silicon using an anodization cell as shown in Fig. 1(b). The mask that defines the region for anodization consists of undoped polysilicon, introduced for chemical resistance to the electrolyte, on top of silicon nitride that presents electrical insulation and avoids anodization of the polysilicon (PolySi). As PS anodization is an almost isotropic process featuring both vertical and horizontal growth [14] [see white dashed area in Fig. 1(a)], the resulting PS core exhibits a U-shaped profile (d is the opening width of the hard mask and r_1 is the horizontal growth dimension), which also corresponds to the depth of the PS core.

B. Fabrication Process

Fig. 2(a) shows the detailed PS WG fabrication process.

1) Deposition and patterning of annealed plasma enhanced chemical vapor deposited (PECVD) Si_3N_4 (100 nm) and low-pressure chemical vapor deposited (LPCVD) PolySi (300 nm) stack on a 3-in ULR Si wafer.
2) Anodization is performed on exposed ULR Si substrate under tunable current density conditions (20 mA/cm^2 selected for this experiment).
3) Hard mask removal and 1-μm-thick aluminum layer deposition by e-beam evaporation.
4) Aluminum patterning with a Cl-based plasma etching.

C. PS WG Electrical Behavior

To keep the dominant mode of the proposed PS WG over the D band, the overall cross section width ($d + 2r_1$) of 1200 μm is chosen. The horizontal underetch equals the depth of the PS layer, which we set to 100 μm to reduce the etching time and at the same time ease the design of the CPW-to-PS-WG transition (see Section III). Numerical simulations performed with HFSS show that, like conventional rectangular WGs, the fundamental mode is TE_{10}, and the second and third higher order modes are TE_{20} and TE_{30}, respectively. Fig. 2(b) shows the cross-sectional views of the electric field distributions in the PS WG, with rainbow colors indicating the field intensity.

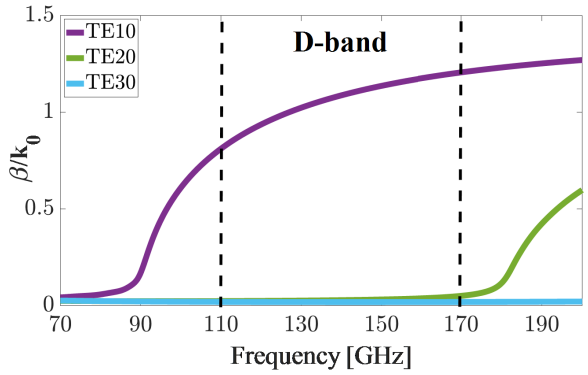

Fig. 3. Normalized propagation constant of the first three modes for the studied D-band PS WG.

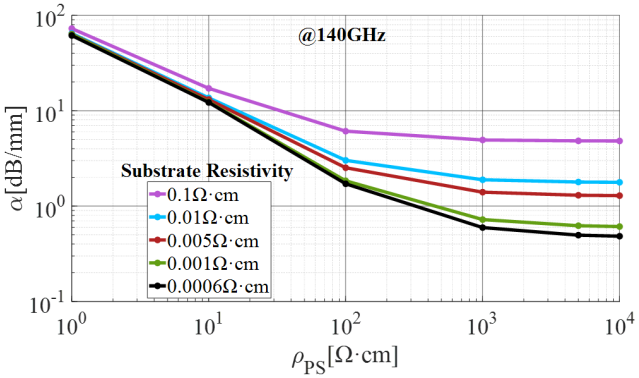

Fig. 4. Simulated attenuation losses as a function of PS resistivity and for varying values of substrate resistivity at 140 GHz (d = 1000 μm and r_1 = 100 μm).

The mode cutoff frequencies for the studied PS WG also rely on the electrical properties of the PS core material. In D band, for the chosen etching current density (20 mA/cm^2) and ρ_{Si} = 1 m$\Omega\cdot$cm, a PS permittivity ($\varepsilon_{r,PS}$) value around 2.6 and a PS resistivity (ρ_{PS}) value above 1 k$\Omega\cdot$cm are extracted using a CPW lines set and following the same procedure as in [21]. Simulation result of normalized propagation constant (β/k_0) in Fig. 3 shows that given those conditions, the second higher order mode is excluded from the studied D band. The chosen WG dimensions are those used to design the CPW-to-PS-WG transition presented in Section III-A.

To understand the relative contributions to total losses from ρ_{PS} and ρ_{Si}, a sensitivity analysis is performed by sweeping both parameters. Indeed, a lower ρ_{PS} is expected to increase conduction within the WG core, leading to higher core losses, while a higher ρ_{Si} results in greater field densities—and consequently higher currents—within the ULR substrate, contributing to higher "equivalent conductor loss." As shown in the Fig. 4, for a fixed ρ_{Si}, the loss versus ρ_{PS} curves eventually reach a plateau where total losses are dominated by Si substrate losses. This plateau is solely determined by ρ_{Si} and increases (indicating reduced total losses) as ρ_{Si} becomes lower. It shows that, given the conditions of ρ_{Si} = 1 m$\Omega\cdot$cm

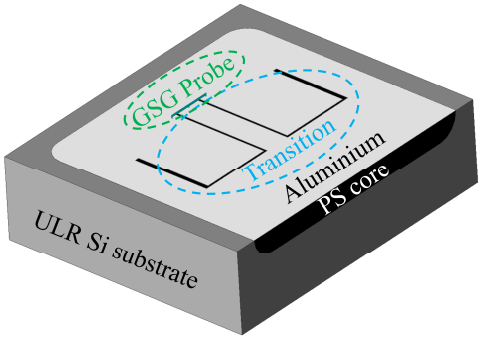

Fig. 5. Schematic of the designed D-band PS WG and transitions (shown as a half-cut model for clarity).

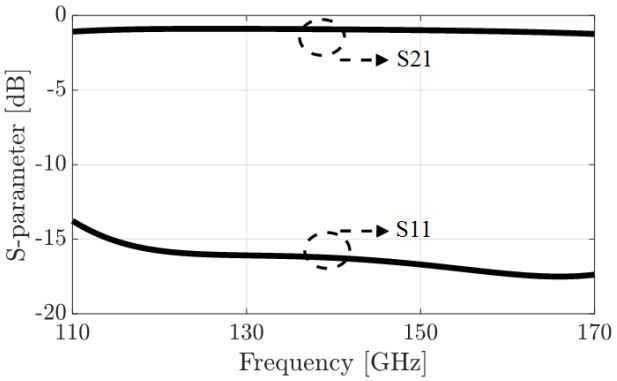

Fig. 6. Simulated S-parameters of the CPW-to-PS-WG transition alone.

and $\rho_{PS} = 1\ k\Omega \cdot cm$, the proposed PS WG has a predicted attenuation constant of 0.7 dB/mm at 140 GHz.

III. Experimental Results

A. Fabricated Samples

To perform on-wafer probing, a CPW-to-PS-WG transition is designed for the D-band U-shaped PS WG in the HFSS environment, which converts the quasi-TEM CPW mode from GSG probes to the WG TE_{10} mode. The general view of the half-cut model is shown in Fig. 5. The transition is made using a folded slotted dipole antenna as in [21] and is reoptimized through extensive parameter sweeps for impedance matching across the D band. The final design corresponds to the best-performing configuration obtained from the parameter sweeps. The simulated S-parameters of a single transition (Fig. 5) are presented in Fig. 6, showing good impedance matching ($S_{11} < -15$ dB) and approximately 1-dB insertion loss across the entire D band.

Fig. 7(a) presents a microscopic top-view image of the fabricated PS WG. The dark margin around the device indicates the horizontal growth of the PS below the Aluminum layer. Fig. 7(b) shows a SEM cross-sectional image, the PS growth at the mask edge extends by 100 μm in both horizontal and vertical directions as expected from the isotropic nature of the silicon anodization process.

B. Electrical Characterization

On-wafer small-signal characterization of the fabricated PS WG is conducted using an MPI THz prober station, equipped

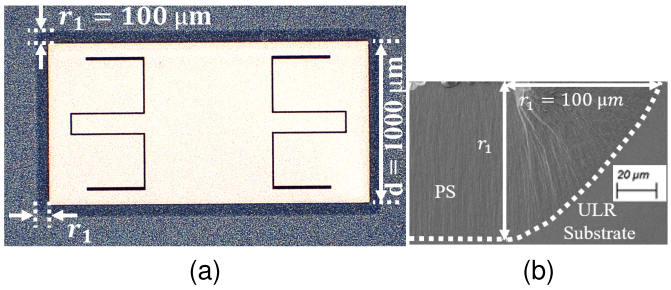

Fig. 7. (a) Top view of fabricated PS WG. (b) SEM image of the cross-sectional view at the PS WG horizontal growth area.

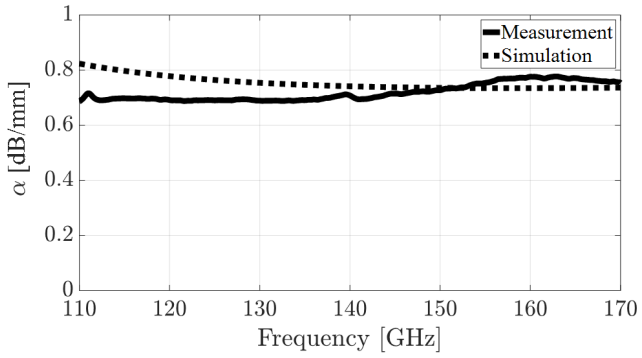

Fig. 8. Extracted attenuation loss of the proposed PS WG after de-embedding.

TABLE I

Performance of Previously Reported Integrated Sub-THz Transmission Line in D Band

Ref	TL type	Losses (dB/mm)
[3]	CPW	0.69 @ 130 GHz
	Microstrip	0.90 @ 130 GHz
	Stripline	1.67 @ 130 GHz
[23]	SIW	0.4–0.6 @ 110–170 GHz
[24]	Microstrip	2.16 @ 140–170 GHz
[8]	DRIE-based Si WG	0.007–0.013 @ 110–170 GHz
This work	PS WG	∼0.7 @ 110–170 GHz

with a KEYSIGHT N5291A vector network analyzer, and VDI D-band frequency extenders. Additionally, a pair of INFINITY D-band GSG probes with a 100 μm pitch from FormFactor is employed. Probe-tip thru-reflect-reflect-match (LRRM) calibration is performed using a 138-357 CAL-KIT from FormFactor.

Fig. 8 presents the extracted losses after line-to-line (L–L) de-embedding (using PS WG lengths of 4 and 6 mm) [22], showing a value of 0.7 dB/mm at 140 GHz, which aligns well with the simulation in Fig. 4. A total of 601 frequency points was sampled across the D band. The measured attenuation loss exhibits a slightly lower value than the simulation at the lower end of the D band and a slightly higher value at the upper end. Though the measured and simulated loss values tend to agree in magnitude over the entire D band, they exhibit slightly opposite trends as the frequency increases. We believe that this discrepancy may arise from several factors that have not been captured in the simulations, such as the inhomogeneity of PS material, potential surface roughness effects, and other nonidealities of the fabricated geometry that are not included in the simulations. As summarized in Table I, the proposed PS waveguide achieves 0.7 dB/mm, already competitive with

or better than conventional planar lines, while relying on a simple fabrication. Although DRIE-based WGs offer lower loss, their process complexity is significantly higher. The PS platform thus provides a unique balance between low loss, simplified integration, and material tunability for practical sub-THz systems. Our analysis also demonstrates that the fabricated sample approaches its theoretical performance limit for the ULR wafer used in this study, as further increases in ρ_{PS} would yield little improvement in loss reduction. The data further indicate that WG performance enhancement could be achieved through the implementation of substrates with lower resistivity. For example, a predicted value of 0.5 dB/mm can be obtained (improvement of 29%) if a $\rho_{\mathrm{Si}} = 0.6\ \mathrm{m\Omega \cdot cm}$ substrate (the lowest specified value available from our wafer supplier) is used, which will be investigated in future works.

IV. Conclusion

This letter presents the first experimental demonstration of a PS WG integrated in a ULR silicon substrate for D-band applications. Using a single-step electrochemical anodization, the WG material and geometry are codefined, eliminating DRIE and wafer bonding. A dedicated CPW-to-PS-WG transition enables direct on-wafer characterization. The fabricated PS WG achieves 0.7 dB/mm at 140 GHz—lower than conventional planar transmission lines—while offering simpler processing and higher integration than DRIE-based WGs. Simulations and measurements indicate further loss reduction to 0.5 dB/mm with substrates of lower resistivity. Combining low loss, simplified fabrication, and inherent material tunability, the proposed PS WG provides a practical platform for integrated sub-terahertz components and future gas or biosensing applications.

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