

Self-Cascode Current-Voltage Curve-Construction Algorithm from Single MOSFET Measurements for Analog Figures-of-Merit Extraction

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Abstract— This paper proposes a curve extraction method for I-V curves and analog figures-of-merit of self-cascode MOSFET associations (SC) using a code that exploits I-V curves of single transistors as input. The method was validated by using experimental measurements of fabricated SC and the very single transistors that compose them. The results indicate a very low error between the SC generated by the code and the measured reference for operation in saturation regime and above threshold voltage, for both the I-V curves and their derivatives. This method is then valid for the assessment of the SC structures in new technologies, avoiding experimental dedicated layouts or complex setups.

Index Terms— Self-Cascode; Analog Characterization; Silicon-On-Insulator; Composite Transistor.

I. INTRODUCTION

The scaling of devices has been essential to the development of new technologies and structures, ensuring proper electric output while consuming less power, occupying less area and providing more design flexibility [1]. However, this has not come without its challenges, as the output conductance (g_D) degradation due to channel length modulation effect and high electric field near the drain becomes more significant with the downscaling of transistors [2].

In analog circuit design, the increase of g_D is responsible for a reduced output voltage gain (A_V). This relationship is also influenced by the transconductance (g_m), the Early voltage (V_{EA}) and the transconductance to drain current ratio (g_m/I_{DS}), as shown in eq. 1 [3].

$$A_V = \frac{g_m}{g_D} = \frac{g_m}{I_{DS}} \cdot V_{EA} \quad (1)$$

Both g_D and g_m will increase for devices with shorter channel lengths, but only the increment of the former is desirable for a higher voltage gain. There are many circuit design techniques used as an approach to this problem. One of them is the Self-Cascode (SC) association of MOSFETs [4]. This configuration consists in associating two transistors in series while short-circuiting their gates, as shown in Fig. 1. The assigned nodes refer to the entire structure when in italic black and to the single transistors when in bold red. In this paper, the transistor closest to the drain node of the association will be referred as MD, while the one closest to the source node will be MS.

The SC can be considered a single device with separated channels associated in series. Initially conceived as a way to reduce the Kink effect in bulk MOSFETs [5], in FD SOI

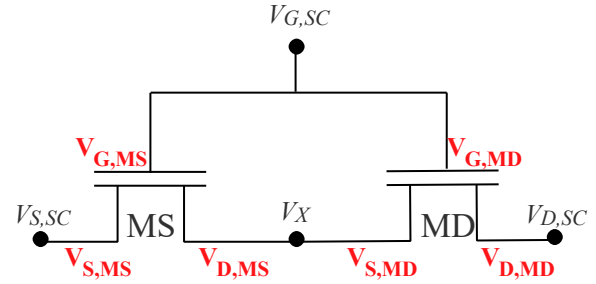


Fig. 1 Schematic of the Self-Cascode Association.

(Fully Depleted Silicon-On-Insulator) transistors its main advantage is the structural limitation for the channel modulation effect, reducing g_D . Still, because of the drain voltage division between MS and MD, MD will saturate before, increasing its resistance and resulting in an effective channel length of the entire structure that lays somewhere in between L_S and $L_S + L_D$. As such, advantages observed in devices with shorter channels can still be maintained, such as higher g_m , I_D and cutoff frequency [1]. Of course, there will be a compromise concerning the occupied area of the final composite transistor which has to be taken into consideration for an optimized circuit design.

The SC composed by transistors of identical threshold voltages (V_T) is referred to in this work as Symmetrical Self-Cascode (S-SC). There is an enhancement that can be made by lowering the V_T of MD. Therefore, because of how the gate and drain biases (V_G and V_D , respectively) are distributed on MS and MD within the association, MD will reach strong inversion and saturation for an even lower V_G and V_D than MS when compared to the S-SC, adding to its advantages. This structure is named Asymmetrical Self-Cascode (A-SC) [6], [7]. Previous studies have shown its benefits for analog circuit applications such as amplifiers and current mirrors [6],[8]. Design options concerning doping concentrations and channel length combinations have been studied in the references [9],[10]. Because of these advantages and analog circuit design potential, this work will focus on providing a coding method to facilitate its experimental electrical assessment.

II. SELF-CASCODE STRUCTURE

For new technologies, the electrical characterization of A-SC structures might promote some obstacles. If the association is not already fabricated on the chip, the results might be affected by parasitics related to extra cables to connect the pads and probes. Providing different chuck biases between

the two transistors is also a challenge, if the V_T control provided by the back gate bias of some SOI technologies is desired to be studied. In some setups, the quantity necessary probes might not even fit inside the measurement chamber. Because of that, a coding solution that can predict the electrical behavior of the SC based on the results of single transistors provides more accessibility to its study.

Before going into the code itself, it is necessary to present the particularities of the voltage-current relationship of the SC. Its behaviour can be summarized by the gate voltage, the drain voltage and the drain current relationships, all in reference to the source nodes of the association and each individual transistor, given in eq. 2, 3 and 4, respectively. The notations here used are similar to the ones shown in Fig. 1, the reference to the source node of each device and the entire composite transistor. When SC is used in subscript, it refers to the nodes of composite transistor as a whole. When MS or MD are used in subscript, it refers to the nodes of each sub-transistor.

$$V_{GS,SC} = V_{GS,MD} + V_{DS,MS} \quad (2)$$

$$V_{DS,SC} = V_{DS,MS} + V_{DS,MD} \quad (3)$$

$$I_{DS,SC} = I_{DS,MS} = I_{DS,MD} \quad (4)$$

Completing the equations of the nodes of the SC but not vital for constraining the biases of the SC is the definition of $V_X - V_{S,SC} = V_{DS,MS}$.

As stated before, the S-SC ensures that $V_{GS,MS} > V_{GS,MD}$. Because of this, MD will run in saturation for a larger range of $V_{GS,SC}$ than MS, allowing for the MS transistor to dictate the electrical behaviour of the association regarding threshold voltage, whereas MD acts as an active load, since it will increase the small-signal output impedance (and hence gain) while behaving as a resistor in regards to the DC point.

Even though the A-SC is essentially different from the S-SC because of the lower V_T of MD, structurally both are similar. Because of that, the prior equations are valid for both, ensuring that the code will be adequate for both structures.

III. SELF-CASCADE CONSTRUCTING ALGORITHM

The input of the algorithm consists of two I-V characterization tables: one for the transistor corresponding to MS, one for the transistor corresponding to MD, both of them containing results for the gate voltage, drain voltage and drain current, all referred to the source node. The gate and drain voltages must preferably display step and range values compatible with the desired SC output table.

The algorithm will then make a preliminary construction of the SC, searching every combination of the input tables where the voltage constraints proposed by eq. 2 and eq. 3 are respected. To explain it in more detail, a resulting $I_{DS,SC}$ vs. $V_{GS,SC}$ goal table will be used as an example.

An estimation of the end goal $V_{GS,SC}$ range can be made from the limits of the single transistor tables. The rule of thumb adopted in this instance of the algorithm is simply using the lower limit of V_{GS} provided by the single transistor

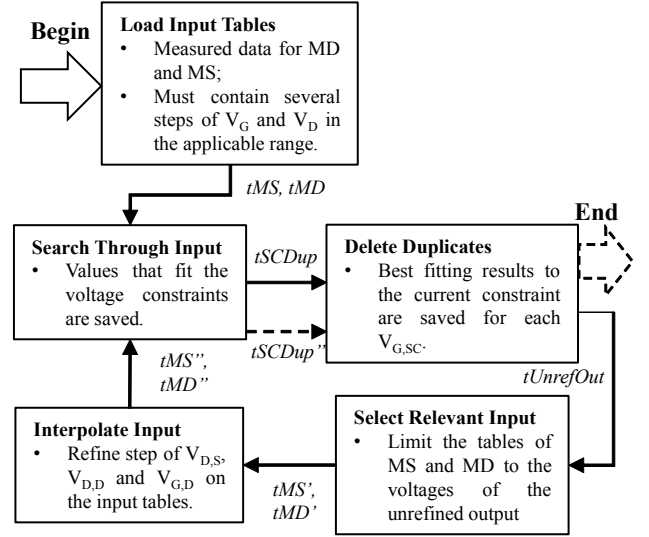


Fig. 2 Schematic of the SC constructing algorithm.

tables (opting for the maximum value if this limit is different between MS and MD) as the lower limit for the range, and the maximum for the maximum. This is not the most optimized approach that can be used, as of course while $V_{GS,MS}$ is the same as $V_{GS,SC}$, the $V_{GS,MD}$ limits are lower, because it depends on $V_{DS,MS}$. Still, for the preliminary construction with a larger step, this is sufficient for the tested devices. The preliminary step to be used should be similar to the ones adopted in the input tables, both for V_{DS} and V_{GS} . The goal of $V_{DS,SC}$ can be user defined with the restriction of being within the input tables V_{DS} range.

With the goal voltage bias defined, the algorithm will run through it point-by-point. For each occurrence, valid points of V_{GS} will be selected for MD, as for MS it is simply the same as $V_{GS,SC}$. The valid drain voltages are selected in the input by finding every V_{DS} less than the goal $V_{DS,SC}$ minus a step. Then the table of valid biases for MD is resorted in an opposite direction, so that the sum of point-to-point elements of $V_{DS,MS}$ and $V_{DS,MD}$ will result in the desired goal $V_{DS,SC}$. To do that it is also necessary to repeat the values of the table MS to match the height of table MD. This is a simple task, as table of valid biases for MD will always have a number of elements multiple to the height of table of valid biases for MS. This operation makes sure that $V_{DS,MS}$ and $V_{DS,MD}$ answer to the constraint on eq. 3. After that, because all the rows are aligned and matching, $V_{GS,MS}$ and $V_{GS,MD}$ can be selected according to eq. 2. This ends the $V_{GS,SC}$ bias run through.

Notice that this method will produce several valid voltage combinations for one single $V_{GS,SC}$ point. The table containing all of these combinations will then be searched in a way that, for every gate bias point, only the combination that best fits the constraint described on eq. 4 is going to be selected. With this, the reduced preliminary table ($tUnrefOut$) is finished.

However, many parameter extraction methods involve the derivative of I-V curves, which are sensitive to abrupt variations of current. It is important that the end result consists of smooth transitions, and often this is not the case straight from the step used for the measured characterization of the single

transistors. Because of that, the input tables are interpolated to provide refined voltage combinations. The preliminary table will function here as a range setter, to avoid too big tables that might overwhelm the systems memory capacities. For this work, the step used for the measured results are of 10 mV for both V_{GS} and V_{DS} , and a refined step of 0.1 mV.

Then, the same constructing functions are recalled and they go through the same explained process, forming the final result.

A code flow schematic that summarizes the algorithm is presented in fig. 2, where tMS and tMD are the single transistors measured data, tSCDup is the preliminary SC goal table with only the voltage constraints applied, tUnrefOut is the preliminary SC goal table with only the values most fitting to eq. 4, tMS' and tMD' are the single transistor tables with only the selected data discriminated by tUnrefOut, which will be interpolated to refine the data points and form tMS'' and tMD'' and tSCDup'' which is the SC goal table with only the voltage constraints applied.

IV. VALIDATION OF CURRENT-VOLTAGE CONSTRUCTING

A. Devices and Specifications

The measurements were made using FD SOI planar nMOSFETs of the technology fabricated at Université catholique de Louvain, of technological node of 2 μm [11]. Devices of channel width of 20 μm were measured, being those with channel length of 1 μm measured for MS and of 1 μm or 10 μm for MD. This technology features front oxide, buried oxide and active silicon layer thicknesses of 31 nm, 390 nm and 80 nm, respectively. The channel doping concentration for MS is of $5 \times 10^{16} \text{ cm}^{-3}$ and for MD it is of 10^{15} cm^{-3} , which is similar to the intrinsic doping concentration of the silicon wafer. The same transistors that were measured individually were also assembled forming an A-SC.

For the code, the software MATLAB R2018a was used.

B. Characteristic Curves

For this work, the focus remained on the accuracy of the prediction of the current-voltage behaviour of the composite transistor. Tables corresponding to the I-V characterization of the single transistors that compose the A-SC were used as input to the algorithm, as well as the goal voltage of either V_{GS} or V_{DS} , depending if the desired SC characterization is of I_{DS} vs. V_{DS} or vs. V_{GS} , respectively. The output tables of the code were compared with the characterization of fabricated A-SCs (named *reference* on the figures and explanations).

First, the curves of the drain current as a function of the gate voltage for the shorter devices are displayed in Fig. 3. For the whole presented gate bias range, the triode region of the drain current bias as a function of V_{GS} is the most easily seen, showing good accuracy. In Fig. 4, the same plot is displayed but in logarithmic scale, allowing for the lowest currents to be more clearly observed, confirming that the constructed output is accurate even at very low currents. This reflects also in a good match when comparing the subthreshold slope (SS), as seen in Table I.

For the I_{DS} vs. V_{GS} curves, it was possible to calculate the relative error against the measured reference. It is displayed

Table I. Subthreshold Slope (mV/dec). $L_S = 1 \mu\text{m}$.				
	$V_D = 1 \text{ V}$		$V_D = 1.5 \text{ V}$	
	Constructed	Reference	Constructed	Reference
$L_D = 1 \mu\text{m}$	74.91	76.59	74.91	76.14
$L_D = 10 \mu\text{m}$	73.46	74.84	73.48	74.68

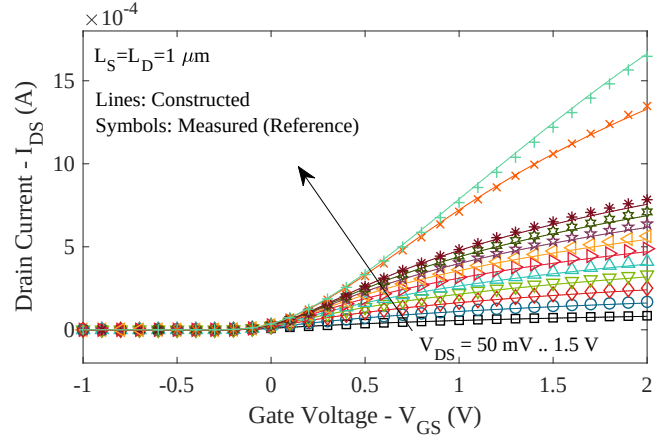


Fig. 3 I_{DS} as a function of V_{GS} for an A-SC transistor with $L_S = L_D = 1 \mu\text{m}$.

as a function of V_{GS} in Fig. 5. It can be seen that the error is consistently lower than 8% for V_{GS} above $V_{T,MS}$.

The accuracy is proportional to the intensity of I_{DS} regarding the resistance of the channel. For example, by reducing the gate bias, the channel becomes more resistive. The opposite relation can be seen when analyzing associations composed by different channel lengths on MD: while an L_D of 10 μm is, of course, a larger resistive load and lower drain current than the L_D of 1 μm , the error is increased for the latter.

The accuracy of the algorithm when predicting the drain current behaviour with the drain voltage bias was also verified. The I_{DS} vs. V_{DS} curves for V_{GS} between -0.2 V and 0.8 V are presented in Fig. 6 for $L_D = 1 \mu\text{m}$ and in Fig. 7 for $L_D = 10 \mu\text{m}$. A good match was also achieved, as shown in Fig. 8, where the relative errors are compared. In the entire V_{DS} range, the error between the measured reference stayed below 10%.

C. Analog Figures-Of-Merit

Although the algorithm provides acceptable error percentages when analysing the drain current, for analog applications there are figures-of-merit that depend on derivatives of

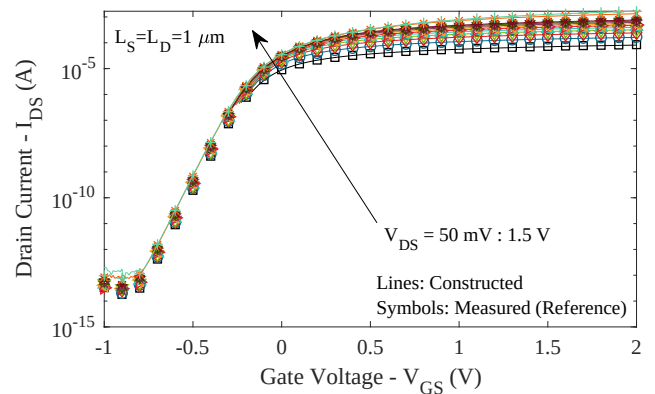


Fig. 4 I_{DS} as a function of V_{GS} for an A-SC transistor with $L_S = L_D = 1 \mu\text{m}$ in logarithmic scale.

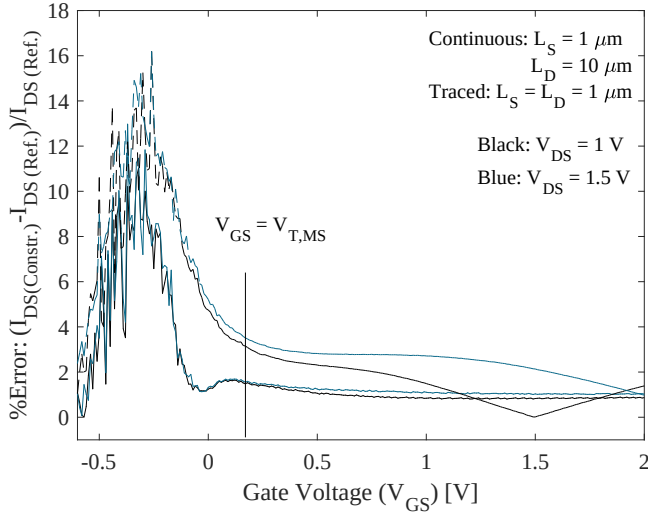


Fig. 5 %Error between constructed and measured (reference) self-cascodes I_{DS} as a function of V_{GS} . Transistors of $L_S = 1 \mu\text{m}$, $L_D = 1 \mu\text{m}$ and $L_D = 10 \mu\text{m}$.

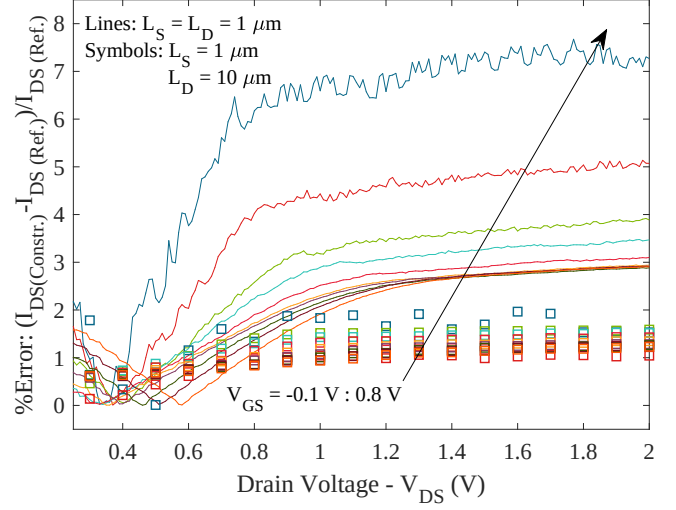


Fig. 8 %Error vs. V_{DS} for SCs with $L_S=L_D=1 \mu\text{m}$ and $L_S=1 \mu\text{m}$ and $L_D=10 \mu\text{m}$.

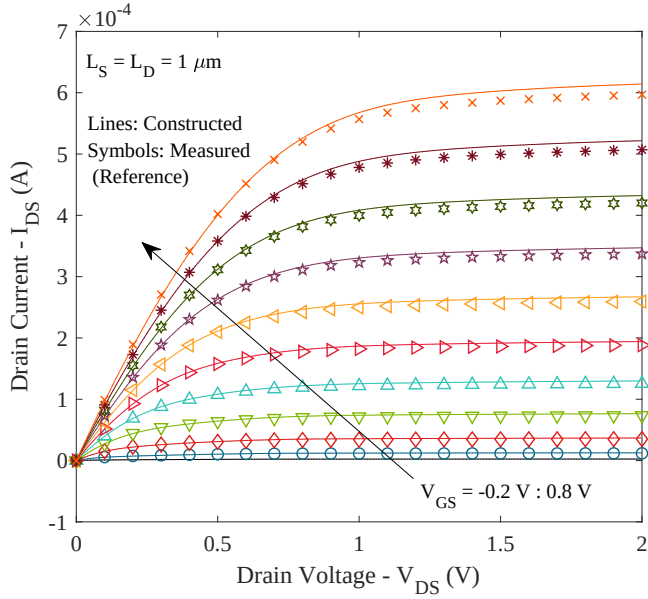


Fig. 6 I_{DS} vs. V_{DS} with $L_S=L_D=1 \mu\text{m}$.

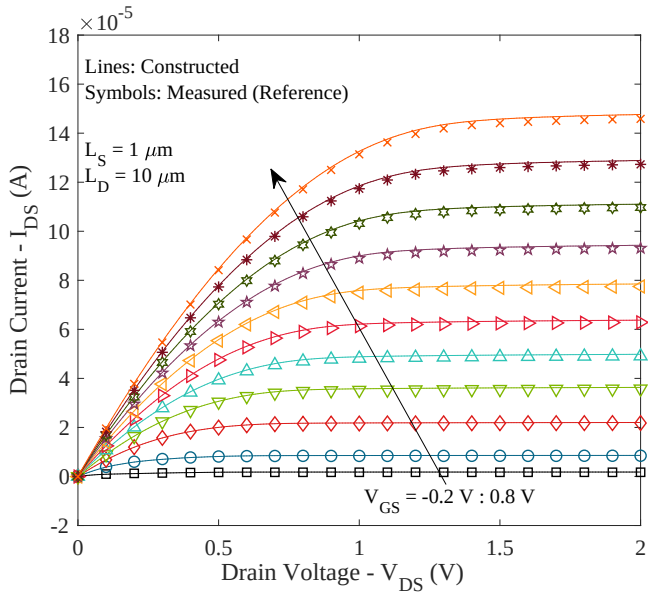


Fig. 7 I_{DS} vs. V_{DS} with $L_S=1 \mu\text{m}$ and $L_D=10 \mu\text{m}$.

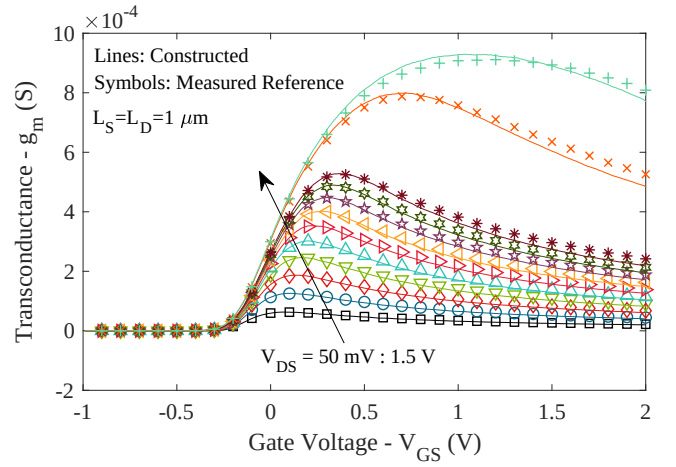


Fig. 9 g_m vs. V_{GS} for SCs with $L_S=L_D=1 \mu\text{m}$.

I-V curves, such as g_m (transconductance) and g_D (output conductance). Because of that, these curves are presented in Figs. 9, 10, 11, 12. For g_m , the error in the worst case when considering a V_{DS} of 1.5 V and a V_{GS} above V_T is of 3% for the A-SC with L_D of 10 μm and of 6% for the A-SC with L_D of 1 μm . In fig. 11, for the A-SC biased in saturation, the larger difference between the constructed and reference values for g_D was of 10^{-5} S.

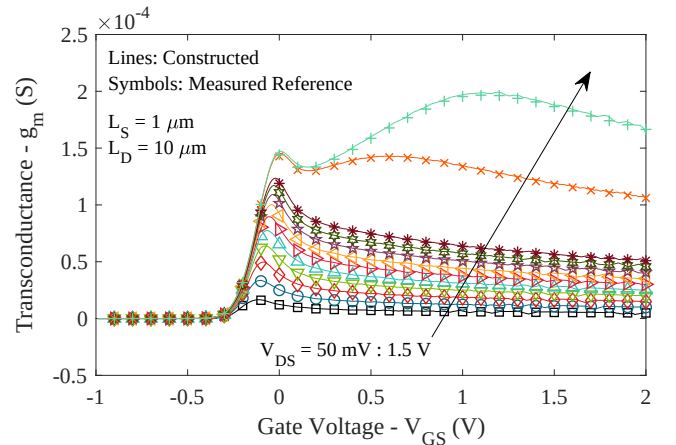
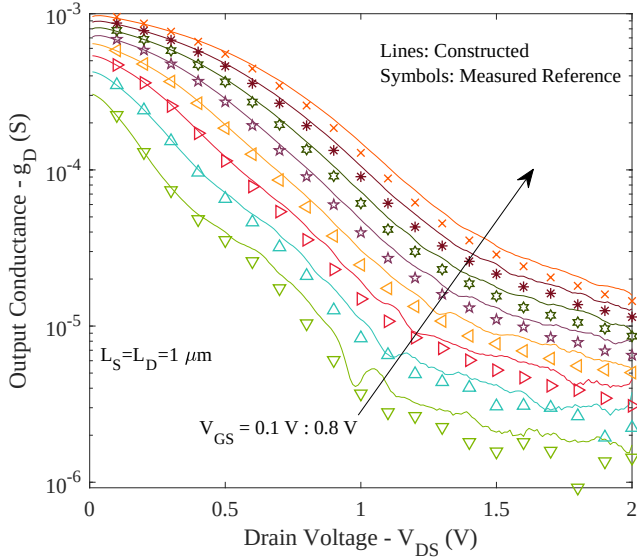
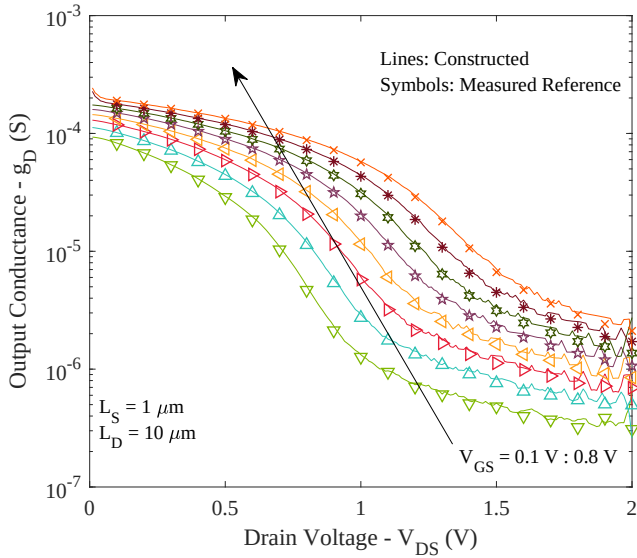


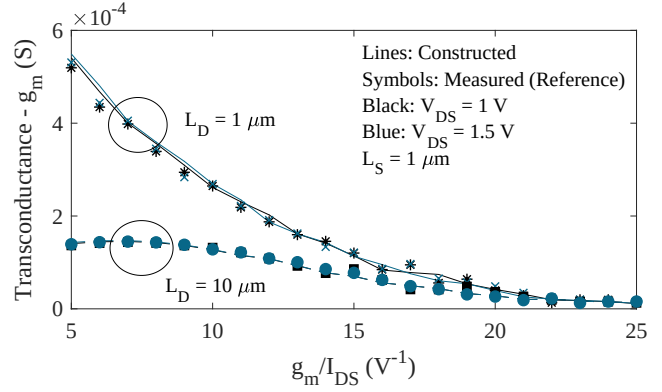
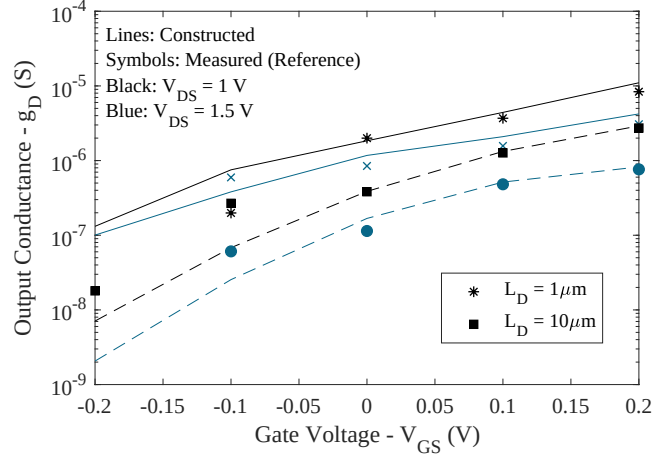
Fig. 10 g_m vs. V_{GS} for SCs with $L_S=1 \mu\text{m}$ and $L_D=10 \mu\text{m}$.

Fig. 11 g_D vs. V_{DS} for SCs with $L_S=L_D=1 \mu\text{m}$.Fig. 12 g_D vs. V_{DS} for SCs with $L_S=1 \mu\text{m}$ and $L_D=10 \mu\text{m}$.

As it could be seen on eq. 1, the g_m/I_{DS} also relates closely to A_V . Not only that, but it offers a way to quantify how responsive the drain current output is to a gate voltage variation without dependency upon devices dimensions. Because of that, it is an important parameter for analog circuit design and, when plotted against g_m , provides an interesting way to benchmark technologies [12]. The comparison of the transconductance as a function of the g_m/I_{DS} is presented in Fig. 13. The extraction of analog parameters from the output generated by the algorithm is accurate for a wide range of g_m/I_{DS} , that includes strong and weak inversion regimes. This means that qualitative comparisons of the structures are reliable using this characterization method.

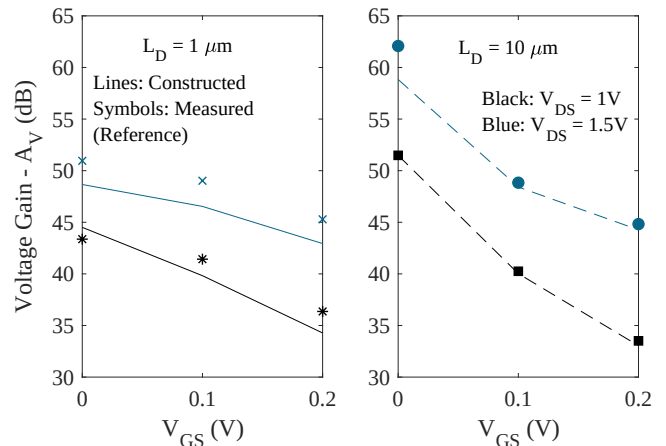
The g_D as a function of V_{GS} extracted for V_{DS} of 1 V and 1.5 V is presented in Fig. 14. Thus, it can be seen that the code can provide results that follow trends regarding different voltage biases and channel lengths accurately, even for the output conductance.

Finally, the voltage gain was extracted and it is presented as a function of the V_{GS} for V_{DS} of 1 V and 1.5 V in Fig. 15.

Fig. 13 g_m vs. g_m/I_{DS} for SCs with $L_S=1 \mu\text{m}$ and $L_D=1 \mu\text{m}$ or $10 \mu\text{m}$.Fig. 14 g_D vs. V_{GS} for SCs with $L_S=1 \mu\text{m}$ and $L_D=1 \mu\text{m}$ and $10 \mu\text{m}$.

The difference of the gain extracted from the code results and the reference reaches 2.5 dB on 49 dB maximum for the A-SC with $L_D=1 \mu\text{m}$ and of 3.2 dB on 62 dB maximum for the A-SC with $L_D=10 \mu\text{m}$.

The benefits on the g_m , g_D and A_V that are observed for the A-SC that features a longer L_D is related to the increase of the added resistance when the structure is operating in saturation [9]. This can be noticed when analyzing the intermediate node voltage (V_X) as a function of V_{GS} for V_{DS} of 1 V and 1.5 V, as presented in Fig. 16. The drop on V_X that happens when increasing L_D will affect the transcon-

Fig. 15 A_V vs. V_{GS} for SCs with $L_S=1 \mu\text{m}$ and $L_D=1 \mu\text{m}$ or $10 \mu\text{m}$.

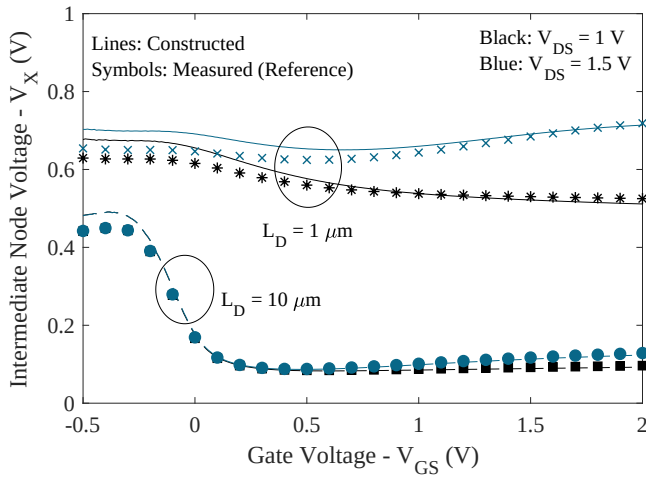


Fig. 16 V_X vs. V_{GS} for SCs with $L_S=1\ \mu\text{m}$ and $L_D=1\ \mu\text{m}$ and $10\ \mu\text{m}$.

ductance and output conductance in a positive way, which is explained in detail in [9]. Still, it is important to notice that the algorithm is capable of following the trend of V_X .

V. CONCLUSION

This paper presented a code that can accurately predict the behaviour of the DC characteristics of a SC from the I-V tables of the single transistors that compose it. The code was validated by comparing the drain current as a function of the gate and drain biases, as well as their derivatives. By comparing analog figures of merit, it could be seen that the code provides a good match for experimental self-cascodes biased above V_T . This method is validated for DC electric assessment of the SC structures in new technologies, avoiding experimental dedicated layouts or complex set-ups.

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