Note: Fast and reliable fracture strain extraction technique applied to silicon at nanometer scale

Vikram Passi,[1,2,a)] Umesh Bhaskar,[1] Thomas Pardoen,[3] Ulf Sodervall,[4] Bengt Nilsson,[4] Goran Petersson,[4] Mats Hagberg,[4] and Jean-Pierre Raskin[1]
[1]*Institute of Information and Communication Technologies, Electronics and Applied Mathematics (ICTEAM), Université catholique de Louvain, Place du Levant, 3, 1348 Louvain-la-Neuve, Belgium*
[2]*IEMN/ISEN, UMR CNRS 8520, Avenue Poincaré, Cité Scientifique, 59652 Villeneuve d'Ascq Cedex, France*
[3]*Institute of Mechanics, Materials and Civil Engineering (IMMC), Université catholique de Louvain, Place Saint Barbe, 2, 1348 Louvain-la-Neuve, Belgium*
[4] *Nanofabrication Laboratory, Department of Microtechnology and Nanoscience-MC2, Chalmers University of Technology, SE-41296, Göteborg, Sweden*

(Received 17 August 2011; accepted 3 October 2011; published online 15 November 2011)

Simple fabrication process and extraction procedure to determine the fracture strain of monocrystalline silicon are demonstrated. Nanowires/nanoribbons in silicon are fabricated and subjected to uniaxial tensile stress along the complete length of the beams. Large strains up to 5% are measured for nanowires presenting a cross section of 50 nm × 50 nm and a length of 2.5 μm. An increase in fracture strain for silicon nanowires (NWs) with the downscaling of their volume is observed, highlighting the reduction of the defects probability as volume is decreased. © *2011 American Institute of Physics*. [doi:10.1063/1.3655464]

Several pioneering studies have shown that when confined to submicron dimensions, many materials—including metals, semiconductors, ceramics, and polymers—exhibit unexpected and potentially useful properties completely different from their bulk counterpart. The observed size effects on material properties at nanoscale are partially due to the larger surface-to-volume ratio than the bulk counterpart, which can make materials more reactive. Together with surface effects, quantum effects start to dominate the behaviour of materials at the nanoscale which modify not only the optical, electrical, magnetic, and chemical properties, but also the physical properties of materials. Silicon nanowires have attracted tangible attention, thanks to their unique electrical and mechanical properties at the nanometer scale. Study of silicon mechanical properties at the nanometer scale is challenging due to the random distribution of the intrinsic defects (point, line, area, and volume defects) which give rise to brittle failure behaviour.

The most widely used technique to test thin films, wires, or beams is nano-indentation, see Refs. 1 and 2, where an atomic force microscope tip is continuously pressed on the test material with the measurement of the applied load and the penetration depth. Although this method is rather simple to handle, the data extraction and calibration procedure for the force and displacement measurement is complex. In addition, the size of the analyzed object is limited by the finite size of the indenter tip (radius of around 50 nm) due to which it can hardly be applied to wires with width smaller than 100 nm, and substrate effects cannot be avoided for very thin films.[3]

A variety of methods based on freestanding clamped-clamped beams or cantilevers have been proposed[4] using different loading devices. Microtensile testing stage concepts using piezoelectric actuators have been initially proposed by Sharpe and co-workers[5,6] and based on electrostatic actuators by Tsuchiya *et al.*[7,8] Other integrated tensile testing methods based on microelectromechanical system (MEMS) fabrication techniques have been introduced by Haque and Saif,[9,10] where uniaxial tensile and cantilever bending tests of micrometer and submicrometer-scale freestanding specimens using MEMS actuators are demonstrated. Bending of freestanding cantilever beams using ultrasonic excitation (resonant measurements) has been reported in Ref. 11 to extract the mechanical material properties. Bending strength using atomic force microscope of freestanding cantilevers of silicon[111] grown by vapor-liquid-solid (VLS) method are reported in Refs. 12 and 13. Fracture stress up to 18 GPa has been measured for VLS grown silicon nanowires,[12] though it must be noted that the presence of a bending contribution does not involve a homogeneous stress state over the sample thickness. Recently, the use of polymethyl-methacrylate (PMMA) as a force mediating polymer has been demonstrated, where by tuning the electron beam exposure, heating and selective removal of PMMA, strain was applied on Si NWs fabricated using a top-down approach. The authors demonstrated applied compressive strain of 24% on 30 nm-diameter pillars.[14]

In this note, we report a novel fabrication method which makes use of internal stress present in a so-called actuator material (silicon nitride in our case) to deform a test material (silicon nanowires).[15] Figure 1 shows the schematic of the simple fabrication process. The starting material is a silicon-on-insulator (SOI) substrate with a top-silicon 50 nm-thick, a buried silicon-dioxide 400 nm-thick, and a 780 μm-thick handle silicon substrate. SOI substrate offers two advantages, the first one being easy access to high quality monocrystalline silicon which is the top layer and the second one is the use of the buried silicon-dioxide as the sacrificial layer which will be etched away in a hydrofluoric acid (HF) solution to release the microstructures without attacking silicon.

a)Electronic mail: vikram.passi@isen.iemn.univ-lille1.fr.

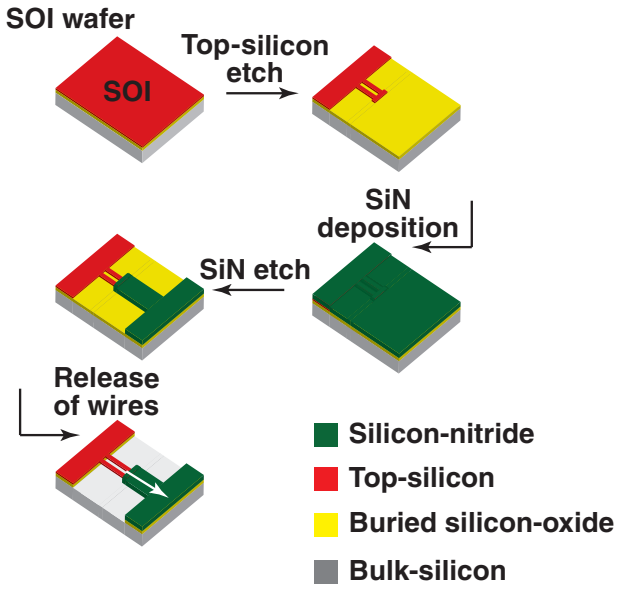

FIG. 1. (Color online) Process steps for the fabrication of silicon nanowires/nanoribbons with on-chip application of loading through the release of the internal stress present in silicon nitride beam.

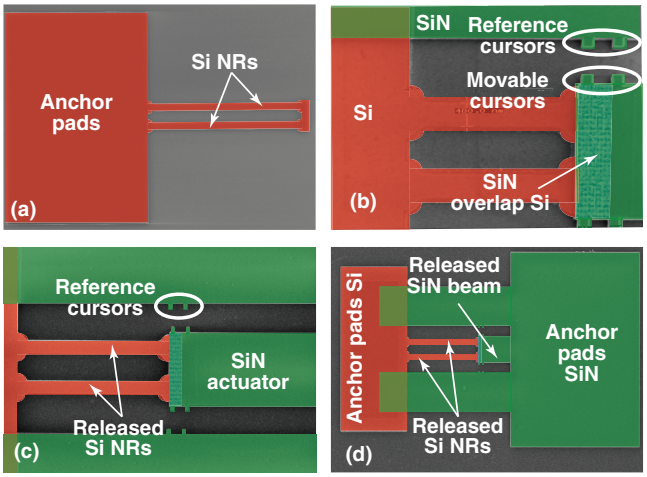

FIG. 2. (Color online) Scanning electron microscope micrographs at various stages of processing (top view): (a) after the etching of the top-silicon layer and removal of the resist, (b) after etching of the LPCVD silicon nitride and (c) after the etching of the buried-oxide using HF-10% and drying the wires with the use of critical point drying, and (d) one complete test structure showing the different layers.

The process begins with a cleaning step in a mixture of sulphuric acid + hydrogen peroxide solution followed by deionized (DI) water rinse. The wafer is dipped in solution of HF-1% to remove the chemical oxide and rinsed with DI water. Silicon nanowires of width 50-nm (Figure 2(a)) and nanoribbons of width 500-nm are patterned using electron beam lithography. It is worth noting that many sample geometries and dimensions can be designed for tensile loading: (i) samples with a dog-bone geometry in order to capture the uniform large strain response up to after necking, (ii) samples with notches or precracks with varying radius of curvature in order to analyze the effect of the stress state on the material deformation and fracture, and (iii) samples with single or multiple holes in order to address damage mechanisms at very small scale and related size effects. Modifying the dimensions of the samples such as width or thickness is straightforward. Then, low-pressure chemical vapor deposited (LPCVD) silicon nitride which has internal stress of ~1 GPa is deposited and patterned using CF_4 chemistry, maintaining at the same time very high selectivity with SiO_2. The silicon nitride is patterned in such a way that part of the SiN overlaps the patterned Si sample in the region shown in Figure 2(b). Finally, the buried silicon-dioxide is etched away by immersing the sample in HF-10% solution with a time sufficient to release the SiN and Si beams. The released structures are then dried using critical point drying in order to avoid any stiction effects (Figure 2(c)). Finally, the displacement u of the various released microstructures is measured by simple inspection of the wafer under microscope.

Though the experimental section described above is relatively simple, it is crucial to accurately quantify the displacement u of the released microstructures. The measurement of u is carried out directly by taking scanning electron microscope (SEM) images of the microstructures region where the distance between the movable and reference cursors can be captured as shown in Figure 3(b). The resolution of the SEM is around 20 nm, which accounts for some inaccuracies in the measurement. For each Si specimen size characterized by a specific width and length, a series of 15 tensile test structures (Fig. 2(d)) with various widths and lengths of SiN beams are designed and built to impose a strain level to Si NWs varying between 0.1% and 5.5%. Twenty identical dies covering approximately half of a 3-inch SOI wafer were fabricated and measured to build up statistics on the fracture strain of monocrystalline Si nanoribbons and nanowires which represents 300 tests per specimen dimension, hence 1800 tests in total. For each die, the applied strain to the Si NW corresponding to the last unbroken specimen is recorded, leading to a list of 20 strain values.

Figures 3(a), 3(b), 3(d), and 3(e) show the displacement of cursors u from which the strain imposed to the nanowires and nanoribbons, respectively, can be inferred. These images are taken after the release of the sacrificial SiO_2 layer. Figures 3(c) and 3(f) show broken 50 and 500 nm-wide wires, respectively. The relative displacement of the cursors patterned on the reference beams and on the actuator beams are measured using SEM images. The imposed strain ε is equal to u/L_0, where L_0 is the length of the specimen before release.

Figure 4 shows the relationship between the fracture true strain (in %) and the volume of the deformed specimen. True strain is calculated using the formula, $\varepsilon = \ln(L_1/L_0)$, where L_0 is the original length of the Si specimen before release and L_1 is the elongated length of the silicon nanowire after release given by $(L_0 + u)$.

The maximum strain measured without failure is equal to 4.9% for a 50 nm-wide, 2.5 μm-long wire, and 4.7% for a 500 nm-wide, 2.5 μm-long wire, respectively. Minimum values of strain are 3.1% for 50 nm-wide and 2% for 500-nm wide beams, respectively. Statistical data are obtained by releasing 20 samples for each width. The unfilled triangles and diamonds are those obtained by the tensile test method described in this note, for wires of 50 and 500 nm-widths, respectively, whereas the unfilled circles are those

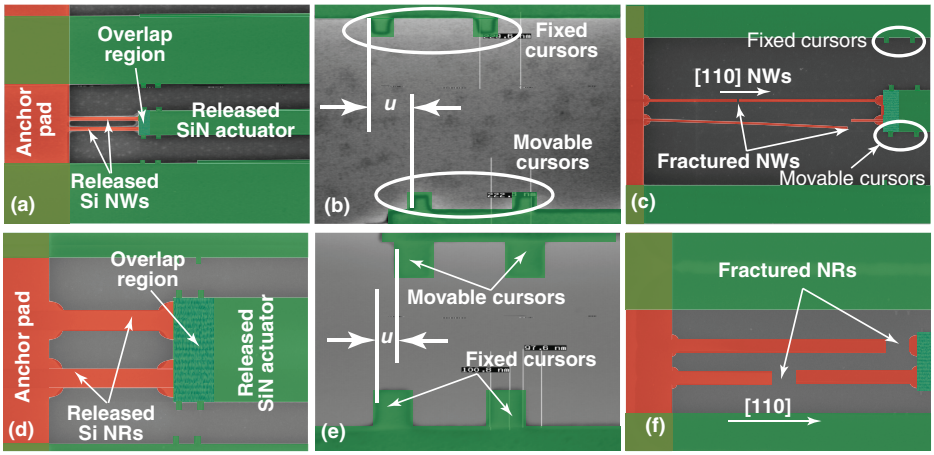

FIG. 3. (Color online) Scanning electron microscope micrographs of wires top views showing (a) example of not broken well-released nanowires, (b) zoom on the cursors showing the displacement u, (c) example of broken nanowires with a 50 nm-width, (d) example of not broken nanoribbons, (e) zoom on the cursors showing the displacement u, and (f) examples of broken nanoribbons with a 500 nm-width.

of micro-scale silicon beams fabricated and tested using the same method.[16] The unfilled squares are the values corresponding to Si thin-films where large beams of silicon were fabricated and subjected to tensile testing methods such as electrostatic grip and on-chip tensile testing.[6]

In conclusion, a simple process for fabricating silicon nanowires/nanoribbons and micro-scale beams under large strain has been developed. Scanning electron microscope images at various processing steps and after successful release are shown. Comparison of the fracture strain of silicon nanowires and beams is performed with values reported in literature from which an increase of percent fracture strain for decreasing specimen volume is observed. This is attributed to the fact that as the volume decreases, there is a reduction of defect density. Using this method, reproducible large strains $>3\%$ are attained for the narrowest nanowires (50-nm wide). Larger values of fracture strain can be achieved by further reducing the volume of the silicon (doing so will reduce the volume defects), and by reducing the defects density by making a hydrogen gas (H_2) or forming gas (N_2H_2) annealing at high temperature.

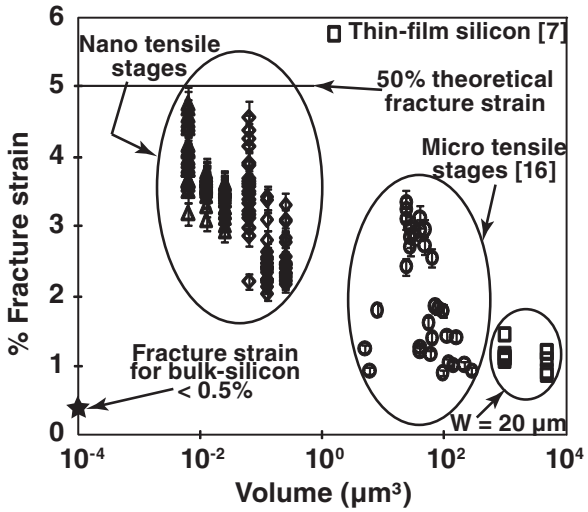

FIG. 4. Variation of the fracture strain as a function of the specimen volume (μm^3) for wires fabricated using top-down approach. The failure strains obtained by the method presented in this note are compared with values from the literature for various geometries and methods of fabrication and testing.

The method reported in this note is versatile and generic, and can be used to determine the fracture strength of any material virtually and for micrometer down to nanometer scale range specimens.

The authors express gratitude for access to MC2, Nanofabrication Laboratory, Chalmers University of Technology, Department of Microtechnology and Nanoscience, Sweden. The authors would especially like to thank the European Network of Excellence NANOSIL (FP7-IST-NoE-216171) and MINATIS consortia for funding this research.

[1] W. C. Oliver and G. M. Pharr, J. Mater. Res. **7**, 1564 (1992).
[2] Y.-S. Sohn, J. Park, and G. Yoon, Nanoscale Res. Lett. **5**, 211 (2010).
[3] X. Chen and J. J. Vlassak, J. Mater. Res. **16**, 2974 (2001).
[4] B. C. Prorok, Y. Zhu, H. D. Espinosa, Z. Guo, Z. Bazant, Y. Zhao, and B. I. Yakobson, *Encyclopedia of Nanoscience and Nanotechnology*, edited by H. S. Nalwa (American Scientific Publishers, 2004), Vol. 5, pp. 555–600.
[5] W. N. Sharpe, O. Jadaab, G. M. Beheim, G. D. Quinn, and N. N. Nemeth, J. Microelectromech. Syst. **14**, 903 (2005).
[6] J. Gaspar, M. Schmidt, J. Held, and O. Paul, Mater. Res. Soc. Symp. Proc. **1052**, 15 (2008).
[7] T. Tsuchiya, O. Tabata, J. Sakata, and Y. Taga, Trans. IEEJ Sens. Micromach. Soc. **116-E 10**, 441 (1996).
[8] T. Tsuchiya, M. Hirata, N. Chiba, R. Udo, Y. Yoshitomi, T. Ando, K. Takashima, Y. Higo, H. Ogawa, and K. Ozaki, J. Microelectromech. Syst. **14**, 1178 (2005).
[9] M. A. Haque and M. T. A Saif, Exp. Mech. **43**, 248 (2003).
[10] M. A. Haque and M. T. A. Saif, J. Microelectromech. Syst. **10**, 146 (2001).
[11] H. C. Tsai, J. M. L. Tsai, H. C. Chang, and W. Fang, in *Proceedings of the International Conference on Solid State Sensors, Actuators, and Microsystems*, 8–12 June 2003, p. 452.
[12] S. Hoffmann, I. Utke, B. Moser, J. Michler, S. H. Christiansen, V. Schmidt, S. Senz, P. Werner, U. Gosele, and C. Ballif, Nano Lett. **6**, 622 (2006).
[13] M. J. Gordon, T. Baron, F. Dhalluin, P. Gentile, and P. Ferret, Nano Lett. **9**, 525 (2009).
[14] S. Walavalkar, A. P. Homyk, M. D. Henry, and A. Scherer, J. Appl. Phys. **174**, 124314 (2010).
[15] S. Gravier, M. Coulombier, A. Safi, N. André, A. Boé, J.-P. Raskin, and T. Pardoen, J. Microelectromech. Syst. **18**, 555 (2009).
[16] U. Bhaskar, V. Passi, A. Zulfiqar, U. Södervall, B. Nilsson, G. Petersson, M. Hagberg, T. Pardoen, and J.-P. Raskin, Adv. Mat. Res. **276**, 117 (2011).