OpenDesc: From Static NIC Descriptors to Evolvable Metadata Interfaces

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Abstract

Modern NICs offer rich functionalities, but host-side software lacks a unified way to express or adapt to their capabilities. Instead, developers rely on device-specific code and ad-hoc glue layers, leading to duplication, reduction to the lowest common denominator, inefficiency, and poor reuse. As NICs grow more flexible, the lack of a shared interface description becomes a core architectural bottleneck.

We propose **OpenDesc**, a common description interface based on P4. While P4 is typically used to define the data plane, we additionally repurpose it to allow the NIC and host to describe their roles in packet exchange.

The host declares an intent, specifying what functionalities should be implemented by the NIC. Fixed-function NICs describe what functionalities they can provide and their interface. Programmable NICs describe the constraints of their interface. OpenDesc uses the combinations of intents and capabilities to select a NIC-compatible descriptor format and compile a NIC-specific driver code that is tailored to the application's intent. Missing features are implemented in software, or pushed to the programmable pipeline if available.

We showcase a prototype OpenDesc compiler that can select the fittest interface from the NIC interface description, and generate the associated host code for multiple NICs. The OpenDesc prototype enables access to the metadata sent from the NIC in eBPF through XDP or userlevel programs directly accessing the NIC descriptors. Our compiler is a first step towards enabling a generated minimalist driver datapath that can leverage the growing capabilities of increasingly feature-rich NICs.

CCS Concepts

• **Networks** → **Network adapters**; **Programmable networks**; • **Software and its engineering** → Source code generation.

Keywords

SmartNIC, Offload, P4, Metadata Interface

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1 Introduction

Modern network interfaces have outgrown their original role. Once simple *Dumb DMA* engines, NICs now carry out a wide range of tasks: checksum verification, flow hashing, timestamping, encryption, tunneling, even limited forms of scheduling and stateful processing. At the same time, host-side software has grown more dependent on these capabilities to save CPU cycles and increase throughput [3, 16, 20, 24, 27, 39].

In a typical system, the host and NIC coordinate using descriptor queues: structured memory regions shared via Direct Memory Access (DMA). These descriptors control how packets are sent and received, and they encode metadata, such as timestamps, hashes, protocol state, offload flags, and more. However, each vendor defines this metadata differently. Even the presence or absence of a field is vendor-specific, and the layout may change with firmware updates, product revisions, or the addition of new features [2].

This problem will only get worse in the future. Programmable NICs can implement new parsing logic [32], configure match-action pipelines [4, 19, 30, 50], and insert custom metadata [53]. This raises two challenges. First, custom new features often introduce a need to exchange metadata with packets, such as cryptographic context for AES offload [21] and more generally L5 offloads [38]. Dedicated queues for off-path offloads can even be used to exchange (partial) packets with specific metadata, for instance for RegEx offload [29], or chunk of payloads instead of packets with TCP offload [22, 28]. What is exchanged with the SmartNIC accelerators often reduces to a pointer, a length, plus some specific accelerator-dependent metadata. It is not possible for a single interface to match all those use-cases. Second, the behavior now depends on the program currently running on the NIC. One device might, in one configuration, generate a timestamp and a flow hash; in another, it might expect the host to supply steering hints or scheduling directives. A single NIC becomes both a producer and consumer of metadata, depending entirely on the deployed data plane.

Exposing the ever-growing capabilities of modern NICs to software remains fragmented and ad hoc. Kernel stacks like Linux' one use heavyweight abstractions such as `sk_buff` to store metadata, which hurts performance [6, 42, 47]. XDP [16] improves efficiency by narrowing the interface, but supports only a limited subset of metadata, and requires manual coordination between drivers and applications for additional

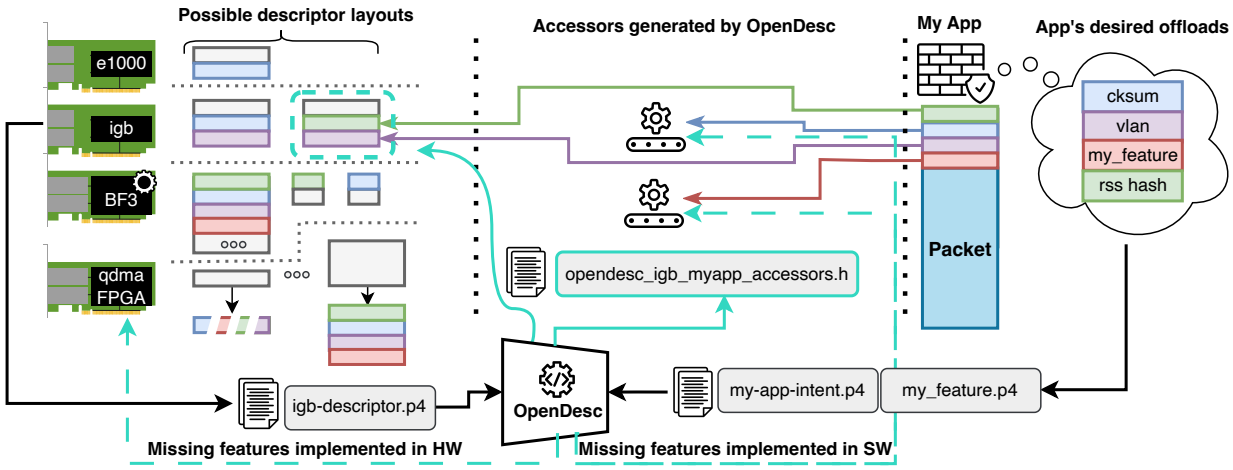


Figure 1: OpenDesc is the bridge between various descriptor formats of fixed and programmable NICs, and various application and drivers layouts

fields. Embedding drivers in applications through a clean-slate approach can offer performance benefits [6, 7, 35, 41], but is difficult to maintain and scale to multiple NICs. Other works moved the descriptor data inside the packet itself [47], reimplemented them in software pipelines [14], or just removed them [43]. This highlights the tension between standardization and performance, but ultimately falls short of offering a unified, dynamic metadata handling mechanism across devices.

We present OpenDesc, a model and implementation to describe the NIC-host communication semantics using P4, extended with some code annotations. P4 is used as a declarative interface contract. This contract describes metadata fields, types, semantics, and directionality. With it, software frameworks can auto-generate parser code, validate NIC behavior, and negotiate features. NICs become self-describing; host applications become portable. The result is a network I/O path that is simpler, more predictable, and more future-proof.

We further extend on the motivation behind our work and previous work in Section 2. We describe the interface in Section 3. We propose a prototype compiler that transforms a given NIC interface description and application intent into a descriptor layout and application accessor in Section 4. We conclude with open research areas in Section 5.

2 Why OpenDesc?

To cope with diversity in NICs' descriptors and features, each software stack writes its own interpretation logic. Linux drivers extract nearly all possible metadata into large `sk_buff` structure. As this interface is slow [6, 42, 43, 47], XDP [48] was introduced and provide a least-common-denominator through `xdp_buff` fields. However, XDP descriptors do not contain any offload information, such as the packet's timestamp or RSS hash. XDP, therefore, proposes 3 accessors (at the time of writing), which are defined by a few drivers, to fetch the supplementary data from the NIC descriptor if the compiled eBPF program accesses it. Every new offload requires coordination between firmware teams, driver authors, framework maintainers, and application developers. For instance, the BPF accessors only cover 3 of the 12 metadata information available in NVIDIA Mellanox ConnectX descriptors. Kernel bypass solutions like Netmap [42] choose the path of least-common-denominator, a buffer pointer and the packet length. DPDK [25] has per-driver code, setting some of the 128bytes DPDK descriptor space `rte_mbuf`. Although the `rte_mbuf` structure is already quite large, it eventually became insufficient to store the growing number of offloads [8]. DPDK, therefore, introduced an indirection layer that copies metadata based on numerous configuration flags [9], a mechanism that has itself become a performance bottleneck [35, 47].

This process consumes engineering time. It ossifies innovation: even if a NIC supports a new offload, it is only useable if all the relevant software is updated to match. Worse, it fragments the ecosystem. There is no standard way for a host to ask, "What metadata can you give me for this packet?" Nor for a NIC to declare, "Here is the structure and meaning of what I will write." Even the XDP accessor model cannot cope with dynamic pipelines, as its static accessors would need to be defined according to the programmable pipeline currently running on the programmable NIC.

Observing the slowness introduced by the jungle of metadata in DPDK, TinyNF [35] observed a 1.7x throughput improvement by simply re-implementing the driver for a single NIC. Similarly applications like VPP [7], Caladan [10] or Cornflakes [41] moved away from DPDK and implemented direct userlevel support for the NVIDIA ConnectX NICs, because the datapath of DPDK became too slow for them. Cornflakes particularly highlights the problem. To offload protobuf-like serialization, Cornflakes needs to write many TX descriptor entries to benefit from the scatter/gather support of the NIC, offloading serialization. Allocating many DPDK structures proved too slow just to write a series of lengths and offsets in the TX ring, leading authors to re-implement a "mini-DPDK" [41]. This is, of course, not a practical solution as it needs a lot of engineering effort to stay compatible with every firmware update, and scale to more devices. X-Change [6] collapsed DPDK's datapath driver and DPDK application into a unified runtime using link-time optimization (LTO). This reduces transformation overhead, leading to an increase of 70% for the throughput and a reduction of 28% for the latency. X-Change requires a complete rewrite of the driver datapath code and remains limited to fixed functions. Most recently, ASNI [47] proposed aggregating packets and their descriptors within a larger packet, known as an ASNI frame. ASNI, therefore, circumvents the problem by embedding metadata within the packet buffer itself. Still, ASNI only works with programmable NIC and does not allow to dynamically find out if a feature is available or not as the layout of the descriptor is fixed, only enabling or disabling some fields. ENSO [43] replaces descriptor rings with a streaming model. This led to a 6x throughput improvement for raw payload processing, but does not enable the exchange of packet metadata with the NIC. Therefore, the model collapses if the application needs to recompute metadata such as a hash in software [47]. Furthermore, by removing the indirection provided by the descriptors, ENSO does not allow packets to be processed in a different order from the one in which they were received without copying them. SoftNIC [14] addresses the problem by introducing a software-emulated NIC as a middle layer, implementing complex functions (e.g., parsing, shaping, classification) in software pipelines.

Following the guidelines of these previous works would result in reimplementing support for each NIC in every application. Essentially, this is equivalent to reimplementing DPDK drivers, but with a distinct datapath for each application. SoftNIC highlights this tension: While it unifies application-facing APIs, it requires developers to define detailed software pipelines per target NIC to fill in missing functionality – without any standardized way for the NIC to describe what it does or does not provide.

In OpenDesc, we propose to generate the variable portion of the datapath according to the specification of the NIC, and the needs of the application. The rest – which is a vast majority – of the drivers' code remains intact.

Figure 1 shows an overview of OpenDesc. We consider an application that wants to receive the checksum of a packet, the decapsulated vlan TCI, the RSS hash and the result of a specific feature, for instance the key of a key-value-store request as done in previous work [20]. Each NIC comes with a P4 definition of its descriptor parser and completion serializer. Fixed-function NICs declare the supported layouts; older NICs like the early Intel e1000 series supported only a single descriptor, giving the computed IP checksum of the packet. Newer Intel NICs came with a bigger descriptor that can contain the RSS hash, or the checksum, but not both. One of the layouts must be chosen; the other 3 features must be recomputed in software. Some partially programmable NICs like the NVIDIA BlueField 3 enable a field for specific metadata computed through a series of Match-Action tables, recently programmable in P4 [30]. However, the complete descriptor that can potentially fit the 4 offloads is large. One might prefer to use the compressed descriptor format that the NIC also supports, which might contain only the hash, or only the checksum. Finally, fully programmable NICs, like those using the Xilinx QDMA API [1], have fully programmable descriptors of 8, 16, 32 or 64 bytes.

The OpenDesc compiler infers what fields the NIC can provide, synthesizes parser and accessor logic, and aligns host and NIC capabilities automatically. This decouples applications from specific NIC quirks. We propose each offload feature to come with a reference P4 implementation. If hardware lacks capability, OpenDesc can delegate to software (e.g., a SoftNIC-like augmentation) using P4-to-software compilers [5, 44, 49]. For programmable NICs, missing features can therefore be pushed to the NIC using one of the numerous P4-to-device compilers [19, 30, 45, 50, 52]. We note our current prototype compiler only lists the missing features for the given NIC, and the one left out after considering all possible layouts (more in §4), but does not currently offload or compile the P4 code to software.

OpenDesc builds on a long line of work on SmartNICs, but provides a missing cornerstone: explicit, declarative *descriptor semantics* that bridge the gap between hardware capabilities and software needs.

Other prior systems than the one mentioned above have tackled parts of the problem, often by moving functionality rather than defining a shared language. Even the emerging P4-based NIC architecture efforts leave descriptor semantics open. The P4 Portable NIC Architecture (PNA) [32] explicitly recognizes that NICs need on-card message processing for DMA, segmentation, etc., but defers all details of descriptor formats to the NIC vendor. FlexNIC [20] offloads some host processing into the NIC itself, allowing applications to install

simple match-action rules on the NIC hardware. Both PNA and FlexNIC give no prescription for how a host should interpret NIC metadata fields and how to put both on the same page.

Clara [40] and Alkali [23] explore related gaps: Clara builds a performance model of how network functions use NIC resources, and Alkali provides an intermediate representation to target diverse NIC hardware. We explore how performance interfaces of packet operations can be used to tailor the choice in OpenDesc in Section 5.

In summary, past work has addressed programmability, performance, and even interface alternatives, yet all rely on implicit, hard-coded metadata interpretations. OpenDesc bridges this gap by introducing a *descriptor-level semantic contract*.

3 OpenDesc interface

What a NIC produces or consumes should not be inferred from vendor documentation, reverse engineering, or constant trial-and-error integration. It should be declared in a language understood by both ends of the link. A compiler can act as a mediator: map what the host wants to consume to what the NIC can produce, based not on identical formats but on shared structure and intent. The goal is not uniformity, but semantic alignment.

P4 is typically used to describe how programmable data planes parse packets and apply match-action logic. In our setting, we repurpose P4 not only to define forwarding behavior but also to describe interface semantics, which means specifying what metadata is exchanged between the host and NIC, where it appears, and how it should be interpreted. We select P4 as it is a domain-specific language designed solely for describing the data plane behavior of network devices. It also proposes a suitable bit-wise header description format, at the heart of OpenDesc. While some alternatives, such as eBPF, could be appropriate, they are often too expressive, which complicates the analysis of the parser code. We elaborate on the tradeoffs of P4 in Section 5.

Each direction of the packet (TX and RX) involves a producer and a consumer. In RX, the NIC produces metadata such as flow hashes, timestamps, and checksum status; the host consumes it. On TX, the host produces intent – such as requesting segmentation, tagging, or offload parameters – and the NIC consumes it. These metadata structures vary by pipeline, firmware, and device capability and must be described explicitly.

Each direction, TX and RX, involves a producer and a consumer of metadata. On TX, the host sets the packet to be transmitted along with some offload hints. On RX, the NIC DMAes the received packet along with some precomputed results such as flow hashes and timestamps. These

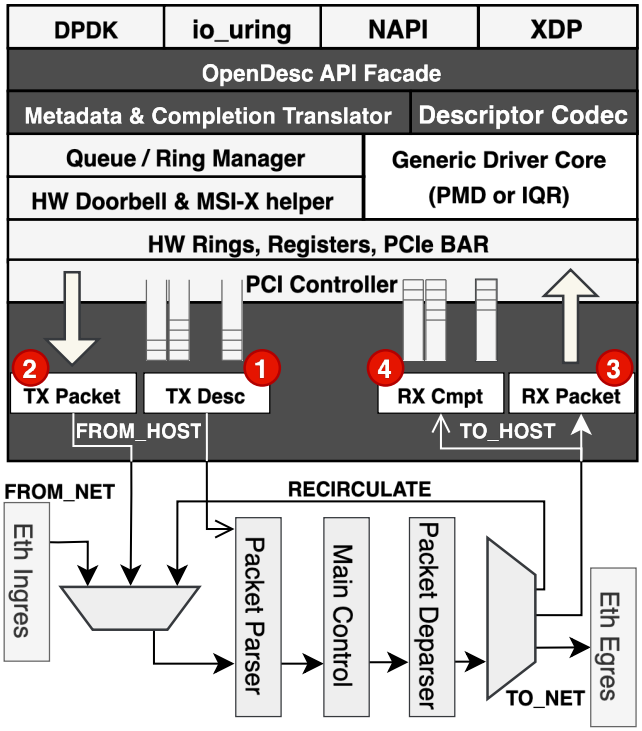


Figure 2: OpenDesc Architecture.

interactions can be categorized into five channels, as shown in Figure 2:

- **TX Desc** 1 **:** Transmit descriptors posted by the host, containing buffer addresses, lengths, and offload flags or parameters.
- **TX Packet** 2 **:** The packet payload itself, which the NIC's DMA engine reads from host memory to process/transmit onboard.
- **RX Packet** 3 **:** The packet payload received from the wire, which the NIC's DMA engine writes into host memory.
- **RX Cmpt** 4 **:** Completion records written by the NIC back to the host, indicating the status of a received packet and containing computed metadata such as flow hashes or timestamps.
- **Control Channel (Implicit):** Configuration and control messages, typically handled out-of-band via mechanisms like MMIO writes to hardware registers

Packet data follows a predefined path (e.g., following PNA) through a pipeline, with a (perhaps programmable) parser, control, and deparser. But descriptor metadata requires additional machinery. We introduce two additional blocks, positioned logically outside the packet path, which describe how descriptors and completions are interpreted or emitted:

- **Descriptor Parser:** interprets the host's posted TX

descriptor. This typically involves raw memory mapped through DMA and converted into structured fields. It may depend on the context of the queue or the ring layout.

- **Completion Deparser:** emits metadata from NIC to host in the form of RX completions. This includes computed hashes, timestamps, and offload results.

In OpenDesc, these roles are explicit as part of the pipeline description. The relevant components appear as follows.

The *Descriptor Parser* shown in Figure 3 is a P4 parser element that interprets a stream of bytes (of type `desc_in`) using some context information–such as per-queue layout or descriptor size–to guide the parsing logic. It outputs a structured collection of header fields that can be subsequently accessed by the main packet processing pipeline or by the completion logic (discussed next). The parser is designed as a templated component, allowing each NIC implementation to define its own descriptor parsing strategy tailored to its specific layout and semantics.

The *Completion Deparser* shown in Figure 4 abstracts the completion channel, which is DMA-ed back to the host to convey both the status of the received packet and the associated computed metadata. This control block is placed at the final stage of the pipeline, where it has access to both the parsed descriptor (that is, the output of the `DescParser`) and the metadata produced by the pipeline logic itself (represented by the `pipe_meta` parameter). Its role is to serialize the relevant fields from these inputs into a well-defined byte stream that is emitted to host memory. For example, if the pipeline computes a 5-tuple flow hash, the `pipe_meta` piggybacks this value, and then the `CmptDeparser` ensures that this value is emitted at the correct offset within the completion structure, aligned with the expectations of the host-side facade API. This alignment ensures proper interception and interpretation of metadata by the application.

The application declares its intent metadata as a simple P4 `header` type as shown in Figure 5. Certain fields may or may not be present depending on the NIC capabilities. We use `@semantic` annotations to tag each field with a semantic name that corresponds to a native type recognized by OpenDesc. The application can define new `@semantic` annotations that are tied, for instance, to a new feature that will be offloaded in a programmable NIC or future NICs.

We note applications might use multiple OpenDesc instance with different intents to obtain different queues tailored for different kind of traffic. This is orthogonal to the declarative interface itself.

4 Compiler Mapping

We implement an OpenDesc prototype compiler that bridges a NIC's metadata behavior and an application's declared intent. The prototype is implemented in C++, building on the p4c frontend for parsing and IR analysis. The compiler currently showcases how the declarative interfaces can be used to select the best descriptors supported by the NIC and generate accessors to the descriptor for an application.

In what follows, we describe the key steps of the process.

1. Control-flow graph extraction. The compiler parses the body of CmptDeparser once, replacing each `emit` statement by a vertex and each conditional by two directed edges labeled with the branch predicate that guards them. A root-to-leaf walk in this graph $G = (V, E)$ is called *completion path*, forming a concrete metadata layout that the NIC may emit under a given context. Each vertex $v \in V$ carries three static properties that can be determined by symbolic evaluation. Figure 6 illustrates this process: the right-hand side shows the original P4 logic of a simplified `CmptDeparser` for the Intel `e1000` newer NICs. The left-hand side depicts its corresponding control-flow graph, in which the branch on `ctx.use_rss` (i.e., a config variable) selects between emitting a single RSS 32bits hash or two alternative metadata fields (`ip_id` and `csum`). Each node in the graph corresponds to a static `emit` call and carries three properties used for analysis: the emitted bit range, the associated semantic meaning (e.g., `rss`, `ip_checksum`), and its byte size.

$\text{bits}(v)$	contiguous byte range committed by v
$\text{sem}(v)$	subset of Σ that those bytes encode
$\text{size}(v)$	$\lvert\text{bits}(v)\rvert$ in bytes

2. Path characterization. For a path $p = (v_0, \ldots, v_k)$ let

$$\text{Prov}(p) = \bigcup_{i=0}^{k} \text{sem}(v_i), \qquad \text{Size}(p) = \sum_{i=0}^{k} \text{size}(v_i).$$

Applications request the set $\text{Req} \subseteq \Sigma$ that appears in their intent header. Every semantic $s \in \text{Req} \setminus \text{Prov}(p)$ must be computed in software. A SoftNIC-like framework emulates each missing semantic at a run-time cost: $w : \Sigma \to \mathbb{R}_{>0} \cup \{\infty\}$.

3. Optimization problem. The compiler chooses a completion path by solving the following optimization.

$$\min_{p \in \text{Paths}(G)} \Big(\underbrace{\sum_{s \in \text{Req} \setminus \text{Prov}(p)} w(s)}_{\text{SoftNIC cost}} \quad \underbrace{\text{Size}(p)}_{\text{DMA completion footprint}} \Big) \tag{1}$$

The DMA completion footprint is a positive real value proportional to the size of the completion descriptor for the path p, and favors paths with smaller completions.

The first element minimizes CPU overhead; the second one favors shorter descriptors, which reduce DMA bandwidth. If

```
parser DescParser<
 typename H2C_CTX_T, typename DESC_T>(
    desc_in          desc_in,
    in   H2C_CTX_T h2c_ctx,
    out  DESC_T    desc_hdr
);
```

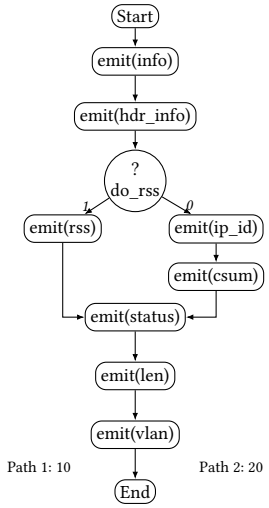
Figure 3: Descriptor parser template

```
control CmptDeparser<
  typename C2H_CTX_T,
  typename DESC_T,
  typename META_T>(
    cmpt_out       cmpt_out,
    in  DESC_T     desc_hdr,
    in  META_T     pipe_meta
);
```

Figure 4: Completion deparser template

```
header intent_t{
  @semantic("rss")
  bit<32> rss_val;
  @semantic("vlan")
  bit<16> vlan_tag;
  @semantic("ip_checksum")
  bit<16> csum;
}
```

Figure 5: Semantic annotations




```
@card2host
control CmptDeparser(
    cmpt_out out,
    c2h_ctx_t  ctx,
    in  h2c_desc_t   dh,
    in  meta_t   m) {
    apply {
        out.emit(m.pkt_info);
        out.emit(m.hdr_info);
        if (ctx.use_rss == 1) {
            out.emit(m.rss_hash);
        } else {
            out.emit(m.ip_id);
            out.emit(m.csum);
        }
        out.emit(m.status_error);
        out.emit(m.length);
        out.emit(m.vlan);
    }
}
```

Figure 6: Simple completion serializer for `e1000`. Left: control flow graph of the serializer program. Right: P4 logic of the `CmptDeparser` that emits completion fields based on a single bit context.

the first element is ∞ for every path, the program is rejected as unsatisfiable.

Because production NICs expose only a handful of completion paths (two in `e1000`, many formats for MLX5, one per installed queue in fully-programmable cards like those based on QDMA), optimization degenerates into enumerating a small finite set and picking the best element of (1). Figure 6 provides the running example: when both `rss` and `csum` are requested, the compiler prefers the right branch because it is assumed that the software rss is cheaper than recomputing the csum (using the cost given for the annotated feature).

4. Host stub synthesis. After selecting an optimal path $p^\star$ the compiler emits:

- *Constant-time accessors* for every $s \in \mathrm{Prov}(p^\star)$ that read the relevant bit slice directly.
- *SoftNIC shims* for the remaining semantics. Each shim is a thin wrapper around a library routine that implements s. Currently, the user is informed of missing s and is responsible for providing a linkable software implementation. We envision to automatically compile the routine from a given P4 reference implementation using existing compilers [31, 49].

The metadata can then be accessed using the generated accessor functions that read a fixed offsets relative to the beginning of the descriptor. Using XDP, access to the descriptor can be bounded and therefore read safely from an eBPF program. In future work, we want to enable the use of the accessors in DPDK by enabling a hook on the descriptor, much like XDP is doing for kernel drivers. The accessors can also be used by applications directly manipulating the NIC, allowing to adapt to new offloads and firmware upgrades.

5 Discussion and future work

Our work establishes a foundation for portable, semantics-aware NIC–host interfaces. Although our current prototype focuses on completion metadata extraction, broader challenges remain in describing the full interface, reasoning about offload trade-offs, and targeting diverse hardware. In what follows, we outline several directions to extend OpenDesc's scope and impact.

Synthesizing the complete driver datapath Future work is required in order to express the dynamics of the interface atop the limited scope of the descriptors' content. An application could use batched descriptors, as ASNI [47] proposes, or a streaming interface, as Enso [43] introduces, according to the application's potential for optimal performance on a given NIC. Enabling a description of the interface semantics, such as how the device moves from one descriptor to the next, would enable generating the full datapath driver code.

Feature equivalence In OpenDesc, we propose the use of annotations that define the functionality desired by the application. This choice posits that a clear definition of all possible features should be provided so vendors and applications can agree on the semantics of the metadata header. A reference implementation should also be shipped for each functionality to be synthesized in software, or the programmable hardware if available. Several research efforts focused on compiling P4 code to the specifics of SmartNICs [11, 12, 46, 54, 55], showing that P4 is suitable to describe NIC functionalities. Future work could enable the ability to use symbolic execution, as done in previous work on network functions and NIC

code [33, 36, 37], to understand if a feature described in the NIC is equivalent to a feature described in application code and avoid the need for standardization of functionalities.

Stateful offloads OpenDesc does not currently implement stateful features, though in principle they could be described using P4 primitives such as registers or externs. Since these constructs are used only as a descriptive mechanism and are not mapped to hardware resources, their number or size is not a constraint. Nonetheless, a more generic and extensible abstraction will be needed to express such stateful behaviors in a portable way across NICs.

Limits of P4 for defining complex offloads P4's restrictions also come with limitations in what can be expressed to define complex offloads. Certain metadata extends beyond per-header information, requiring context that spans multiple packets or even depends on inspecting payload bytes, such as pattern-matching. However, we still believe P4 is suitable for the *interface* itself. While the idea that all features could be *entirely* defined in a unique language is undoubtedly appealing, the application demands have to match the vendors' definitions. If both sides describe a very complex offload, the slightest difference will conclude that the feature is not available in the NIC. Even for something relatively simple, such as the RSS hash, we realized a symbolic analysis approach wasn't going to work as implementations from vendors differ slightly and offer different hashing schemes. However, the user only wants a mash-up of bits that is consistent per-connection and as different as possible between connections. The implementation details are less relevant for the user. This is why, in the end, we resorted to using annotations. P4, however, enables access to more complex offloads through *extern*, special externally implemented objects or functions that can be invoked from P4 code. Future work could tie externs to a given implementation, using an appropriate language for a complex feature. There is, however, no need for the interface to be able to peak in the feature itself. Multiple previous works such as Floem [34], iPipe[26], or Alkali [23] enable some languages to define functionalities that can be compiled to different targets. While these compilers could be used to define some complex functionalities, more research is needed to assert if the opposite is true: whether the limits of each target (FPGA, ASICs, muti-core NICs, ...) can be expressed using a unique language.

Performance and programmable constraint Not all features might be actionable at the same time, and programmable NICs offer constrained resources. Given all applications' intent, an open question is still whether a feature should be offloaded to the NIC even if technically possible, or if sometimes using a software counterpart is not more desirable. On the NIC side, Pipeleon [55] computes a performance cost for a given P4 program for multiple SmartNICs. Iyer et al. [18] advocate for a clear NIC performance interface. LogNIC [13] proposes a packet-centric approach to model the performance of a SmartNIC and its accelerators. P4All [15] proposes elastic structures in P4 programs to dynamically size storage requirements when programming P4 pipelines. On the host side, PIX [17] enables building a performance model of network functions. OpenDesc presents the opportunity to combine these works for a more opportunistic placement beyond the question of whether a feature is available or not. Similarly, Menshen [51] tackles the issues of isolation when concurrent pipelines run in a programmable RMT architecture, which could be informed by the application's intents to provide isolation inside NICs.

SIMD and architecture-dependent optimization Most DPDK drivers implement another version of the driver datapath using SSE (128-bit) to read 4 descriptors at a time, and one for different architecture (Altivec or Neon). This pose a burden on maintainance. OpenDesc could be extended to generate SIMD accessors instead, taking also advantage of wider lanes to process more packets in parallel.

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