Efficient Small-Signal Extraction Technique for Ultra-Thin Body and Ultra-Thin Box FD-SOI transistor

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***Abstract* — In this paper, an efficient extraction technique is proposed for determining all extrinsic and intrinsic element values of SOI-UTBB transistors. Starting from measured S-parameters and using simple Z- and Y-matrix transformations, the proposed technique exploits the independent gate resistance value under DC bias conditions to first extract the extrinsic elements values and then the intrinsic ones. The obtained results are verified through successful comparison between simulated and measured S-parameters up to 40GHz.**

***Index Terms* — Modeling, parameter extraction, small-signal, UTBB FD-SOI transistor.**

I. Introduction

Modeling and characterization of MOS SOI transistors at high frequencies have attracted a lot of attention of many researchers [1]–[4]. One crucial step in this process is the accurate evaluation of all extrinsic and intrinsic element values of their electrical equivalent circuit. Many characterization methods have been proposed to extract such parameters, usually combining measured and simulated data.

Compared to the method presented in [1], which is applicable only if the transistor is in saturation, the proposed approach [2] is valid for any bias conditions.

It started by extracting the value of the gate resistance R_{ge} at zero bias condition following the method given in [2]. This value was found nearly constant for any bias conditions, which is in agreement with the literature [2], [5]. Then, by fixing the value of R_{ge}, we obtained a system of equations, which allowed determining the extrinsic elements. The next step was to extract the intrinsic elements. This new method was successfully applied to an Ultra-thin body and ultra-thin box FD-SOI transistor of gate length L = 30 nm and width W = 120 µm over the frequency range up to 40 GHz.

II. RF Extraction of the Extrinsic Parameters

The equations describing the extrinsic and intrinsic part of the circuit shown in Fig. 1 are given by the following form for the subsequent extraction.

$$Z = Z_e + Y^{-1} \quad (1)$$

$$Y_{int} = Y - Y_e \quad (2)$$

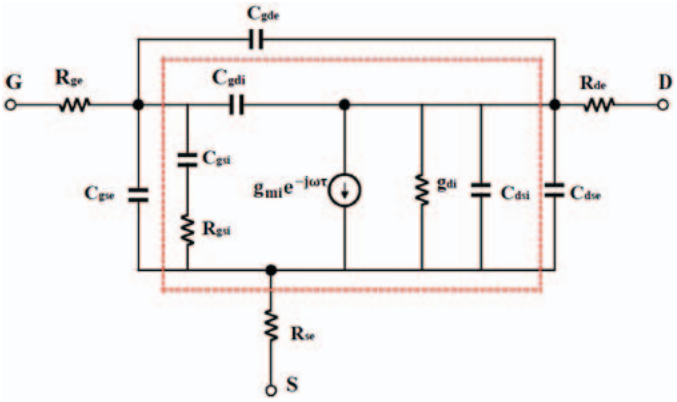

Fig. 1.small signal equivalent small signal circuit model for UTBB FD-SOI transistor.

with

$$Z_e = \begin{vmatrix} (R_{ge} + R_{se}) & R_{se} \\ R_{se} & (R_{de} + R_{se}) \end{vmatrix}$$

$$Y_e = \begin{vmatrix} j\omega(C_{gse} + C_{gde}) & -j\omega C_{gde} \\ -j\omega C_{gde} & j\omega(C_{dse} + C_{gde}) \end{vmatrix}$$

and

$$Y = \begin{vmatrix} j\omega\left(\frac{C_{gsi}}{1 + j\omega R_{gsi} C_{gsi}} + C_{gse} + C_{gde}\right) & -j\omega C_{gde} \\ \frac{g_{mi} e^{-j\omega\tau}}{1 + j\omega R_{gsi} C_{gsi}} - j\omega C_{gde} & g_{di} + j\omega(C_{dse} + C_{gde}) \end{vmatrix}$$

A. Extraction of the parasitic resistances

The parasitic resistances (R_{ge}, R_{se}, R_{de}) are then extracted from a set of S-parameters at $V_{ds} = V_{gs} = 0$ V. the real parts of Z-parameter's transistor can be expressed as [1]:

$$\mathrm{Re}(Z_{ij}(\omega)) = \mathrm{Re}(Z_{eij}(\omega)) + \frac{A_{ij}}{\omega^2 + B} \quad (i, j) \in \{1, 2\} \quad (3)$$

where ω is the angular frequency. B and A_{ij} state respectively for the real and frequency independent expressions involving only the shunt extrinsic elements as defined in [1].

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Thus, the extrinsic series resistances R_{ge}, R_{se}, and R_{de} can be deduced using the parametric curves defined in a two dimensional plane $[x_1, x_2]$ by

$$\mathrm{Re}(Z_{ij}(\omega)) = \mathrm{Re}(Z_{kl}(\omega)) \quad \text{Where } \{i, j\} \neq \{k, l\} \qquad (4)$$

From (3), these curves must be straight lines, with intercept at the origin $[0, x_{20}]$ and slope α as given in [1]. Combining the obtained equations formed by varying the indices i, j, k, and l, it is possible to build a set of linear equations from which the series resistances can be determined. Note that it is not possible to extract the three resistances from cold measurements, because at $V_{gs}= V_{ds}=0$ V, the transistor is OFF. Therefore, assuming $\mathrm{Re}(Z_{12}) = \mathrm{Re}(Z_{21})$, the curve $\mathrm{Re}(Z_{12})$ versus $\mathrm{Re}(Z_{21})$ will give a straight line starting from the origin with a slope of 45° (α=1) [2]. The method described in [2] was used to extract the gate resistance.

B. Extraction the extrinsic capacitance

The extrinsic capacitances can be directly determined from the imaginary part of the Y-parameters at $V_{ds}= V_{gs}=0$ V using the following equations.

$$\mathrm{Im}(Y_{11}) = j\omega(C_{gse} + C_{gde}) \qquad (5)$$

$$\mathrm{Im}(Y_{12}) = \mathrm{Im}(Y_{21}) = -j\omega C_{gde} \qquad (6)$$

$$\mathrm{Im}(Y_{22}) = j\omega(C_{dse} + C_{gde}) \qquad (7)$$

Thus, C_{gde} was determined directly from (6) while the gate source capacitance C_{gse} was deduced from (5). Finally, the drain source capacitance C_{dse} was obtained from (7).

III. Extraction of the Intrinsic Parameters

After de-embedding the extrinsic resistances (R_{ge}, R_{se}, R_{de}), and the parasitic capacitances (C_{gde}, C_{gse}, C_{dse}), the analysis of the small signal equivalent circuit of the intrinsic part allowed obtaining the Y–parameter matrix $[Y_{int}]$[3].

$$R_{gsi} = \mathrm{Re}\left(\frac{1}{Y_{11int} + Y_{12int}}\right) \qquad (8)$$

$$C_{gsi} = -\left(\frac{1}{\omega\,\mathrm{Im}\left(\frac{1}{Y_{11int} + Y_{12int}}\right)}\right) \qquad (9)$$

$$C_{gdi} = -\left(\frac{1}{\omega\,\mathrm{Im}\left(\frac{1}{Y_{12int}}\right)}\right) \qquad (10)$$

$$g_{di} = \mathrm{Re}\left(Y_{22int}\right) \qquad (11)$$

$$g_{mi} = -\left|\frac{Y_{21int} - Y_{12int}}{Y_{11int} + Y_{12int}}\right| \frac{1}{\mathrm{Im}\left(\frac{1}{Y_{11int} + Y_{12int}}\right)} \qquad (12)$$

VI. Results and Discussion

The extrinsic resistances of the UTBB FD-SOI transistor are determined using method [2] as depicted in Fig. 2 and Fig. 3. The values of extracted parasitic capacitances at $V_{ds}=V_{gs}=0$ V are illustrated in fig. 4. It can be noted that these capacitances are nearly frequency-independent, while their values are: C_{gde}=30 Ff, C_{gse}=35 Ff and C_{dse}=8 Ff.

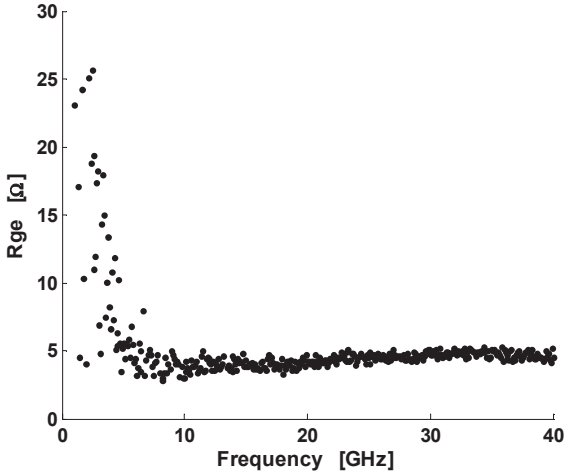

Fig. 2. Representation of the gate resistance versus frequency in the 0.04-40 GHz band for a UTBB FD-SOI transistor with W = 120 µm and L_{eff} = 30 nm at $V_{gs} = V_{ds} = 0$ V.

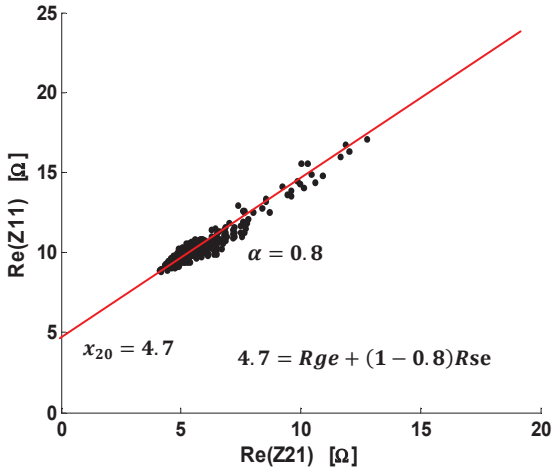

Fig. 3. Parametric plot of resistances in the 0.04-40 GHz band for a UTBB FD-SOI transistor with *W* = 120µm and L_{eff}= 30nm at $V_{gs}= V_{ds}= 0$ V.

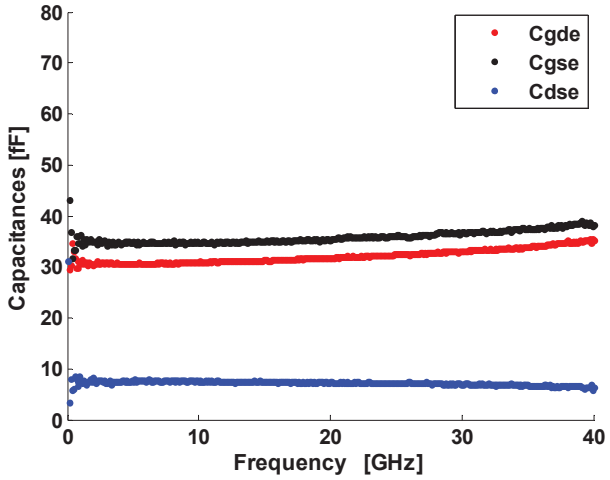

Fig. 4. Representation of the parasitic capacitances versus frequency in the 0.04-40 GHz band for a UTBB FD-SOI transistor with W = 120 µm and L_{eff} = 30 nm at V_{gs} = V_{ds} =0 V.

In Fig. 5 the intrinsic elements g_{mi}, g_{di} were extracted as a function of frequency parameters. The extracted intrinsic elements are nearly frequency-independent. As shown in Fig. 6, an excellent agreement has been found between measured and simulated S-parameters at V_{ds} = 1 V and V_{gs} = 0.95 V, thus demonstrating that the proposed extraction approach is accurate and reliable.

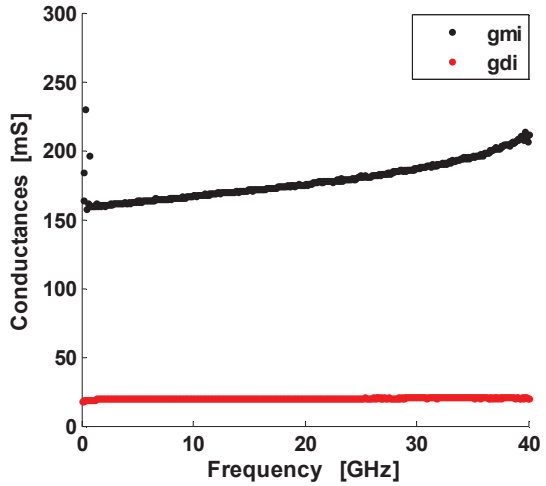

Fig. 5. Extracted values of the conductances vs. frequency in the 0.04-40 GHz band for a UTBB-FD SOI transistor with W = 120 µm and L_{eff} = 30 nm at V_{gs} = 0.95 V and V_{ds} = 1 V.

VI. Conclusion

In this article, an accurate extraction technique is presented. The extrinsic elements are extracted at a single bias point which is a zero bias condition (V_{gs}= V_{ds}=0 V). The intrinsic parameters are extracted by very simple Y-parameter analysis after removing the extrinsic resistances and the parasitic capacitances. It is verified that the extraction technique is accurate. The simulation results agree well with the measurement data.

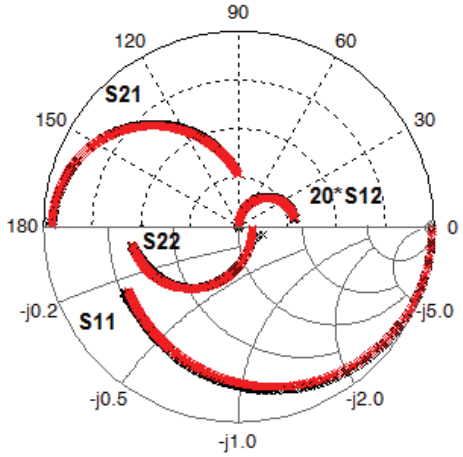

Fig.6. Measured (x black) and modeled (x red) S-parameters in the 0.04-40 GHz band for a UTBB FD-SOI transistor with W = 120 µm and L_{eff} = 30 nm at V_{gs} = 0.95 V and V_{ds} = 1 V.

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