IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received 29 July 2025, accepted 24 August 2025, date of publication 27 August 2025, date of current version 3 September 2025.

Digital Object Identifier 10.1109/ACCESS.2025.3603422

RESEARCH ARTICLE

Low-Power Wide-Range Time-to-Digital Converter for Time-of-Flight Range Finders

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ABSTRACT Time-to-digital Converters (TDCs) are increasingly considered to offer low complexity and scaling-friendly implementations in embedded applications, replacing voltage-domain analog-to-digital converters (ADCs). Hence, TDCs have been popular in embedded and typically resource-constrained sensing applications such as Time-of-Flight (ToF) or Lidar range finders, to convert time-domain data (travel time) into digital data. Yet, TDCs can suffer from relatively high power dissipation and a large footprint when a wide dynamic range and high resolution are required, which is the case for ToF applications. To tackle these challenges, this paper presents a power and area-efficient TDC architecture, with direct application in ToF measurements. The proposed architecture is based on a Nutt topology, offering a wide dynamic range up to 1.6 ms. In addition, the architecture is made event-based by utilizing gated ring oscillator GRO based TDCs, dissipating power only for a short duration in specific measurement windows. As a result, power dissipation is significantly reduced compared to state-of-the-art implementations (up to 55x). The proposed TDC has been implemented in 65-nm CMOS technology. It occupies only $100\,\mu\text{m} \times 340\,\mu\text{m}$ including integrated serializers. It features a scaling-friendly implementation with all-digital control and readout circuits, opening the path for easier integration in embedded sensing scenarios.

INDEX TERMS Gated ring oscillator, LiDAR, time-based sensor, time-of-flight, time-to-digital converter, ultrasonic range finders.

I. INTRODUCTION

Time-to-digital converters (TDCs) have been increasingly utilized in various sensing applications, to directly convert time-domain data into digital bits as an alternative to voltage-domain analog-to-digital converters (ADCs). In particular, TDCs have been recently popular in Time-of-Flight (ToF) measurements [1], [2], [3]. TDCs offer smaller size, lower complexity, and better scalability for deep sub-micron technologies compared to more traditional ADC schemes [4]. For instance, TDCs are utilized in ToF laser ranging to determine the travel time of an intense laser pulse by monitoring its reflection, which occurs when hitting an object in proximity. The travel time can be translated into distance (the distance between the object and the receiver) or more complex information, like the case of 3D imaging.

Fig. 1 shows a laser ranging receiver [1]. The receiver is composed of an avalanche photodiode (AVD), a low-noise preamplifier, and a post-amplifier (amplification channel) to detect and amplify the weak reflected pulses. The amplification channel is followed by one or more event-triggered parallel channels which are triggered when the amplified reflected pulses exceed a certain threshold voltage V_{th}. As shown in Fig. 1, a comparator is used to generate timing information about the threshold crossings. The timing information $\Delta T = t_{stop} - t_{start}$ is then digitized by the employed TDC.

Likewise, TDCs can be used in ultrasonic ranging to determine the travel time of an ultrasonic wave by monitoring its reflection (echo).

The associate editor coordinating the review of this manuscript and approving it for publication was Poki Chen.

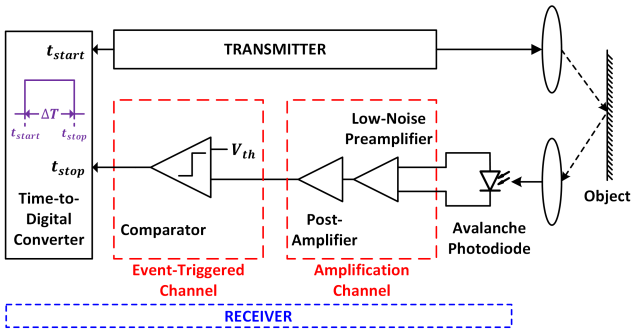


FIGURE 1. Laser Ranging Receiver.

In terms of requirements for these applications, laser range finders are required to cover a wide distance range, from 10 cm to 20 m, corresponding to ∼667 ps to ∼134 ns in the time-domain range, while ultrasonic range finders cover relatively lower distance range to target millimeter distance resolution (nanoseconds to milliseconds time-domain range). To enable the wide dynamic range and high resolution required by range finders, one practical solution, known as the Nutt architecture, is to combine a coarse-resolution TDC with two fine-resolution TDCs (interpolators) [5], [6]. The coarse-resolution TDC extends the dynamic range, while the fine-resolution TDCs compensate for the coarse quantization errors at the start and end of the measurement period.

Key challenges in Nutt's architecture are the power dissipation and the complexity of the interpolators. For instance, in existing implementations, the interpolators continuously dissipate a dynamic peak power. In addition, complex control circuits are needed to synchronize between the coarse and fine TDCs in the case of multi-level interpolation.

To tackle these challenges, in this work, we propose to modify the Nutt architecture to improve the dynamic range, simplify the design, and reduce the power consumption. Hence, our main contributions are:

(1) We propose an event-based structure, which dissipates power only during short measurement windows and allows us to extend the full dynamic range of the Nutt TDC without impact on efficiency. For that, we utilize a gated ring oscillator (GRO) for the fine-resolution TDC, which can be easily paused in between measurements. As a result, power dissipation is significantly reduced, up to 55 times compared to state-of-the-art implementations, while still supporting a wide input dynamic range up to 1.6 ms. Moreover, when no measurement is active (idle mode of operation), the power dissipation is reduced to a few tens of micro-watts (8.2 μW at 20 MHz clock frequency), achieving significant power savings in event-triggered sensing scenarios.

(2) The proposed TDC features a scaling- and area-friendly implementation, with all-digital control and readout circuits to simplify its integration in complete sensor systems. In addition, the proposed control and readout circuits allow event-based operations and overcome sampling errors.

Overall, the proposed TDC occupies only 100 μm × 340 μm (including integrated serializers) in a 65-nm CMOS implementation.

The rest of the paper is organized as follows. Section II presents a background on TDCs with a focus on popular architectures. Section III introduces the proposed TDC architecture and the circuit implementation details, which allow a wide dynamic range and low-power dissipation. Section V shows the simulation results of the TDC implementation in 1V 65-nm CMOS technology. A conclusion is given in Section VI.

II. BACKGROUND ON TDCS

Generally, the building blocks of a TDC can be categorized into two main components: (1) A delay generator or time reference that determines the time resolution (quantization least-significant-bit LSB in nano/picoseconds); (2) a readout circuit that executes an architecture-dependent logic to output a digital code proportional to the input time duration being measured.

Several techniques have been introduced in the literature to realize picoseconds delay generators/time references and readout circuits, summarized in review publications [7], [8]:

1) DELAY LINE TDC

In this topology, the basic delay generator is realized by cascading delay elements in a chain (delay line).

As shown in Fig. 2a, the readout utilizes the delay line by tracking its status as the *start* signal propagates. An array of registers samples the line status at the rising edge of the *stop* signal, and generates a thermometer code that represents how many delay elements have passed between the rising edge of the *start* and *stop* signals. Thus, the TDC performs a quantization with a resolution equal to the gate (buffer) delay. The digital binary code at the output uses a thermometer-to-binary converter logic.

Despite their simple structure, delay line TDCs suffer from poor area efficiency when the application requires a high dynamic range. For example, achieving an N-bit dynamic range requires 2^N delay elements. Thus, delay line TDCs are not suitable for applications that demand a wide range.

2) RING OSCILLATOR BASED TDC

Another method to build delay generators uses free-running ring oscillators (ROs). ROs are relatively popular designs, owing to their simple structure and ability to generate multiple phases, used to form a quantization grid with a resolution as low as the delay of a single inverting stage. Moreover, unlike delay line TDCs, we can reuse the delay elements in an RO (in its loop configuration), allowing a high dynamic range and achieving excellent area efficiency compared to delay lines.

Fig. 2b shows the readout circuit, which utilizes the quantization grid by tracking the RO's phases. This can be accomplished by employing phase registers, encoders, and a counter. The RO-based TDC readout can be coupled with

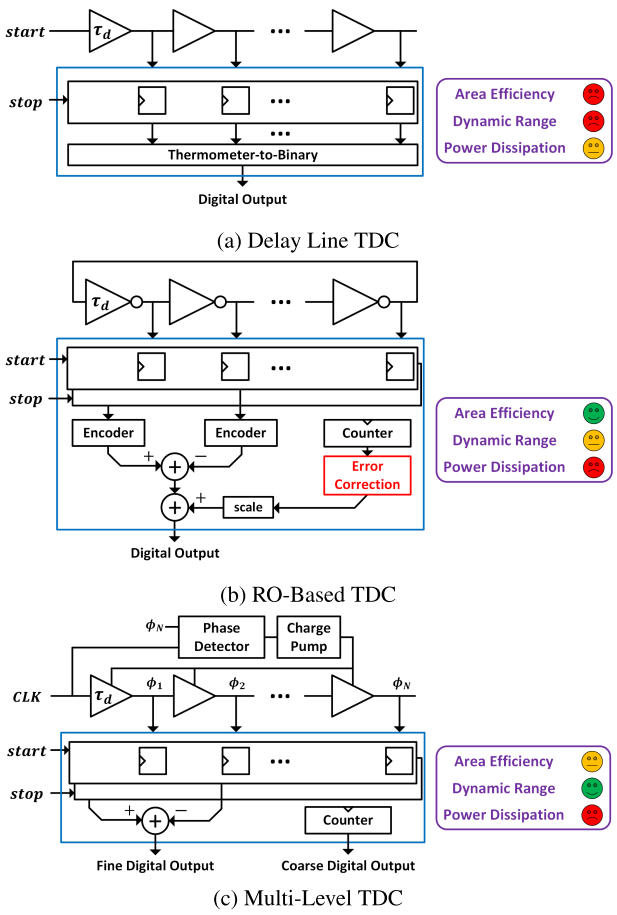


FIGURE 2. TDC Architectures.

error correction blocks to address asynchronous sampling errors. The error correction can compensate for the counter's phase-to-output delay and avoid the output glitch duration, using several temporally separated counter samples (samples at different sampling instants), from which we can deduce an error-free sample [9], [10]. For the same purpose, other schemes employ a lookup table (LUT) and logic to achieve delay-free readout [11].

RO based TDCs have good metrics in terms of dynamic range (tens of nanoseconds) and area efficiency. However, they dissipate high dynamic power dominated by the oscillator, which limits their usage in low-power applications.

3) MULTI-LEVEL TDC

As an architectural alternative, multi-level TDCs aim to achieve simultaneously a high resolution and a wide dynamic range. The basic principle is to employ a coarse-resolution TDC with a wide dynamic range but high residual error, together with fine-resolution TDC (also called interpolator) to resolve the residual error from the coarse level.

Fig. 2c shows simplified block diagram of a multi-level TDC, employing a counter-based TDC, and a delay-locked loop (DLL) stabilized delay line interpolator [12]. The counter-based TDC provides a coarse quantization step equal to the clock period T_{CLK} (time reference), while the delay

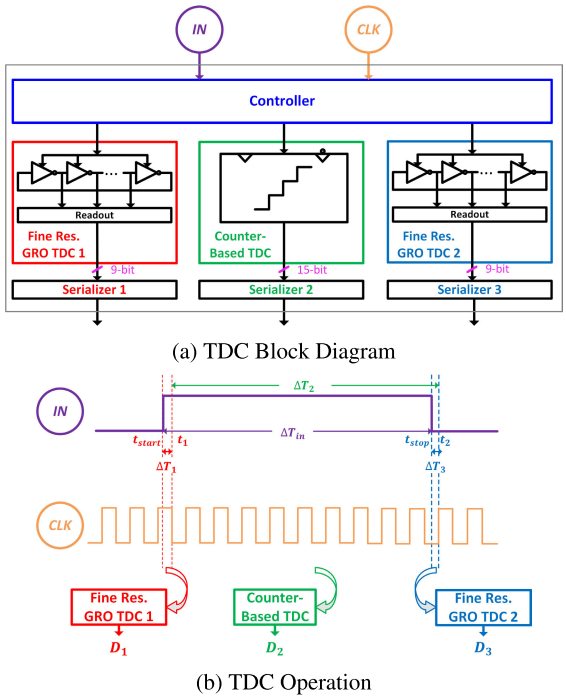


FIGURE 3. Proposed TDC Block Diagram and Operation.

line interpolator provides a fine quantization step equal to a fraction of the clock period.

To achieve a higher resolution, extra levels of interpolation can be added. However, this requires additional circuits to ensure synchronization between all levels of interpolation [13]. This overhead can in turns increase the complexity and power dissipation, which is suboptimal for embedded applications.

Hence, the goal of this work is to improve the power efficiency of multi-level (Nutt) TDCs by proposing a distinct architecture that utilizes GRO TDCs, to simultaneously achieve a wide dynamic range and low-power dissipation. The proposed architecture and implementation details are presented in the following section.

III. PROPOSED TDC ARCHITECTURE

A. BLOCK DIAGRAM AND OPERATION PRINCIPLE

Fig. 3 shows the block diagram and the operation principle of the proposed TDC architecture. Fig. 3a details the architecture comprising a controller, a counter-based coarse TDC, two GRO-based fine TDCs, and three event-triggered serializers (one serializer for each TDC).

First, the coarse-grained counter-based TDC quantizes the input duration ΔT_{in} with a coarse quantization step $T_{coarse} = 0.5T_{clk}$ using a dual-edge counter:

$$\Delta T_{in} \xrightarrow{\text{Coarse Quantization}} \Delta T_2 \tag{1}$$

The counter-based quantization offers the capability to support a wide dynamic range determined by the counter's number of bits and the clock period T_{clk} (time reference). However, as shown in Fig. 3b, large quantization errors

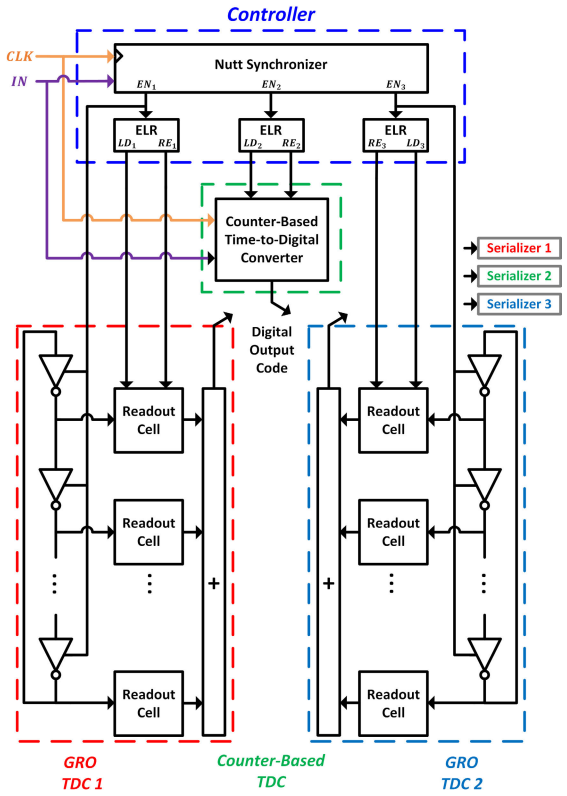


FIGURE 4. Proposed TDC Implementation.

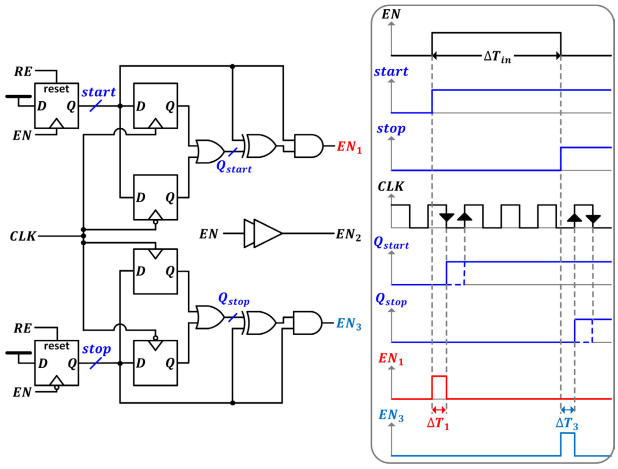


FIGURE 5. Dual-Edge Nutt Synchronizer.

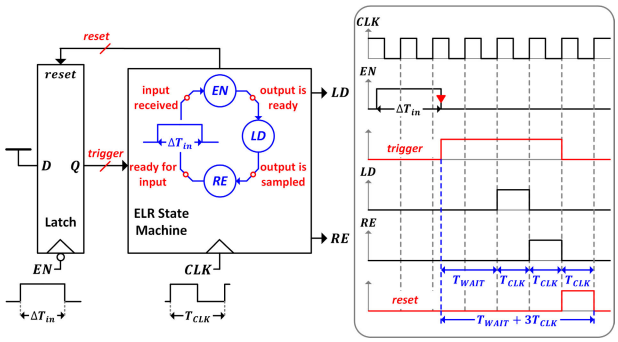


FIGURE 6. ELR Controller.

(ΔT_1, ΔT_3) are introduced at the beginning and at the end of each measurement. These errors correspond to the time between the effective measurement start or stop, denoted t_{start} and t_{stop} respectively, and the next clock edge of the counter. Hence, both ΔT_1 and ΔT_3 are comprised in the range $[0, 0.5T_{clk}]$. We call these errors *residues*.

To avoid introducing a large error in the system, these residues are fed into additional GRO based TDCs, obtaining finely quantized outputs added to the coarse-grained output for error compensation. As a result, the total quantization error $e_{q,tot}$ is determined by the fine quantization step $T_{fine} = \tau_d$ of the GRO based TDCs instead of T_{clk}, where τ_d is the delay of a single inverting stage $\ll T_{clk}$.

This process is described by (2)-(3), where $e_{q,1}, e_{q,3} \in [-T_{fine}, +T_{fine}]$ are the GRO based TDC quantization errors, modeled in appendix A.

$$\Delta T_{in} = \Delta T_1 + \Delta T_2 - \Delta T_3 \xrightarrow{\text{Fine Quantization}} \Delta T_{out} \quad (2)$$

$$\begin{aligned} \Delta T_{out} &= D_1 T_{fine} + D_2 T_{coarse} - D_3 T_{fine} \\ &= \Delta T_{in} + e_{q,1} - e_{q,3} = \Delta T_{in} + e_{q,tot} \\ e_{q,tot} &\in [-2T_{fine}, +2T_{fine}] \ \forall \ \Delta T_{in} > 0.5T_{clk} \end{aligned} \quad (3)$$

To accommodate a wide input dynamic range up to 1.6 ms, we choose 15 bits for the counter-based TDC (D_2) and 9 bits for the GRO based TDCs (D_1, D_3), respectively. This leads to a total of 33 bits which can be combined in the integrated serializers to limit the number of output pins.

B. CIRCUIT IMPLEMENTATION DETAILS

Fig. 4 shows the implementation of the proposed TDC. More details about the controller, the GRO based TDC, and the event-triggered serializers are given:

1) CONTROLLER

The controller generates and feeds the timing information and control signals to the TDCs.

a: NUTT SYNCHRONIZER

To generate the timing information (ΔT_1, ΔT_2, and ΔT_3), we employ a dual-edge Nutt synchronizer as shown in Fig. 5.

It synchronizes the input signal (EN) rising and falling edges (start and stop events) to the nearest rising or falling clock edge, by using flipflops in a parallel configuration.

The dual-edge sensitive and parallel synchronization process does not introduce any offset, to limit the GRO based TDC ON time (dynamic range) to $0.5T_{clk}$ instead of $2T_{clk}$ in standard implementations. Thereby, the power dissipation and complexity of the GRO based TDC are significantly reduced, with negligible metastability/edge-colliding errors at low clock frequencies 20 MHz to 80 MHz. To eliminate metastability errors at higher clock frequencies, the circuitry can be easily modified by cascading additional flipflops at the cost of introducing an extra offset. The timing diagram of the proposed synchronizer is shown in Fig. 5.

b: ELR CONTROLLER

To generate the control signals, we propose the enable-load-reset ELR controller shown in Fig. 6. The proposed all-digital controller utilizes an event-triggered state machine that is triggered by the falling edge of the *EN* signal, indicating that an input (ΔT_{in}) is received, which then enables consecutive state transitions between *EN*, *LD*, and *RE* states.

In the *EN* state (initial state after trigger), we process the received input. The time between the *EN* state and the transition to the *LD* state can be controlled to allow enough time T_{WAIT} (multiple clock cycles) for the TDC output to be ready.

In the *LD* state, we fire the *LD* signal to sample the output data. The falling edge of the *LD* signal is used to indicate that a TDC sample is ready and trigger the serializer.

Finally, in the *RE* state, the *RE* signal is fired to reset the readout circuits and get them ready for the next measurement.

The ELR timing diagram is shown in Fig. 6, where T_{WAIT} and the pulse widths of *LD*, *RE*, and internal ELR reset signal are one or more clock cycles T_{clk}.

We implemented 2 versions of the ELR controller: (1) T_{WAIT} = 1 to 2 clock cycles, the pulse widths of *LD*, *RE*, and internal reset signal = 1 clock cycle (see Fig. 6); (2) T_{WAIT} = 6 to 7 clock cycles, the pulse widths of *LD*, *RE*, and internal reset signal = 3 clock cycles.

The later version is integrated into this work. The TDC's conversion time in this case is 15 to 16 clock cycles.

Since the TDC processing time is considered in the ELR operation, it overcomes partial sampling errors [9], [14] without the need to apply expensive error correction algorithms.

2) GRO BASED TDC

Fig. 7 shows the employed GRO based TDC. It comprises a gated ring oscillator and a counter-based readout. In addition, the ELR controller is utilized to control the TDC's operation.

a: COUNTER-BASED READOUT

The counter-based readout circuitry shown in Fig. 7 comprises 13 identical cells (1 cell for each oscillator tap) and an adder. Each cell has a dual-edge counter and an output sampler (D-flipflops array). The proposed readout utilizes the oscillator's quantization grid by performing phase accumulation. The dual-edge counters, which have their value incremented when a rising or falling edge occurs, are used for this purpose. The digital output is obtained by summing the sampled output of the counters.

With an all-digital implementation, the readout circuitry is highly scalable and easy to reconfigure for different numbers of oscillator stages and/or different dynamic ranges (number of bits). In addition, it is easily controlled by the proposed ELR state machine as follows:

- When the *EN* signal is high (the oscillator is ON), the dual-edge counters operate to perform the phase accumulation.

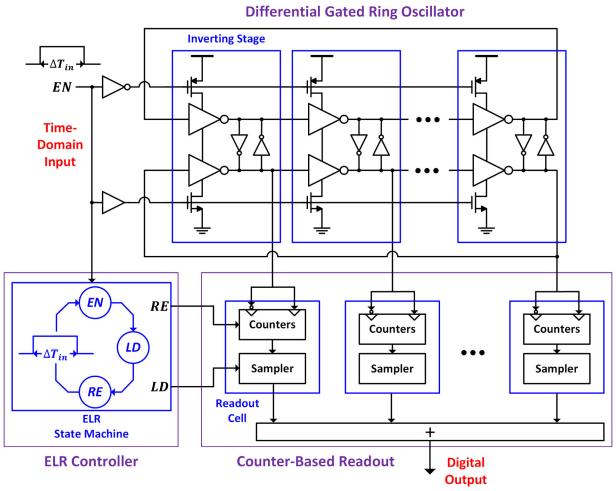


FIGURE 7. GRO Based TDC.

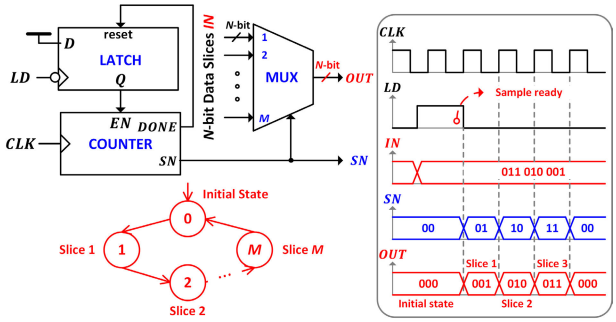


FIGURE 8. Serializer.

- Afterwards, when the *EN* signal transits to low, the ELR state machine is triggered. The state machine allows enough time for the output to be ready, avoiding the glitch duration of the counters, then it fires *LD* signal to sample the counters output.
- Finally, a reset *RE* is fired (counters value = 0) to make the readout ready for the next measurement.

In this way, we allow efficient event-triggered operations with robustness against sub-sampling errors.

b: GATED RING OSCILLATOR

A 13-stage differential GRO is employed to generate a quantization grid with $LSB = \tau_D \simeq 115$ ps. More details about the grid are presented in Section IV.

The proposed RO design uses non-minimally sized transistors to limit the differential non-linearity DNL due to local process variations (device mismatches). Additionally, the design minimizes DNL errors due to the systematic layout asymmetry by shuffling the order of the inverting stages to equalize the horizontal wires connecting them. Specifically, the delay variations are minimizied by improving the layout symmetry.

With these techniques, we tackle the static non-linearity errors when the oscillator is enabled. The DNL and integral

non-linearity INL errors are kept below 0.09 LSB and 0.17 LSB, respectively (see the DNL/INL plots in Fig. 12).

On the other hand, when the oscillator is gated (oscillation ceased), leakage and charge errors can significantly affect the TDC's performance. Indeed, leakage can pull the oscillator phases to illegal states, potentially introducing multiple counting errors in the following measurement, when the RO is enabled (oscillation restarted). For example, leaky PMOS transistors pull the oscillator phase to VDD instead of holding it unchanged when the oscillator is gated. This leads to fast transients (extra edges) when the oscillator is enabled such that it reaches a legal state, thereby corrupting the quantization grid and causing counting errors.

To reduce this effect, we employ latch loads to pull the oscillator phases to the nearest legal state and prevent the leaky transistors from pulling the oscillator phases (see the loads of the inverting stages in Fig. 7).

3) SERIALIZER

To reduce the required number of output pins, we employed an event-triggered serializer for each TDC. The proposed serializer block and timing diagram are shown in Fig. 8. The serializer is triggered by the falling edge of the *LD* signal. It slices the data into multiple slices through a state machine. The initial state of the state machine resets the outputs to 0, and in the following states, the data slices are fed to the pins from LSB to MSB. After serializing all data slices, the state machine returns to the initial state to be ready for a new operation. The output of the counter *SN* is used for synchronizing with external circuits.

In our implementation, the GRO based TDCs output is sliced into 3 slices, 3 bits each. While the counter-based TDC output is sliced into 3 chunks, 5 bits each. In this way, the number of data pins is reduced from 33 bits to 11 bits.

IV. SIMULATION RESULTS AND PERFORMANCE METRICS

Fig. 9 shows the layout of the proposed TDC including the serializers. The TDC functionality and performance are validated by performing post-layout simulations with device noise enabled. The control/timing signals and the digital outputs are shown in Fig. 10 verifying the TDC operation at 50 MHz clock frequency and 1 μs ΔT_{in}. The GRO based TDCs are only enabled as determined by EN_1 and EN_2, followed by the activation of the ELR state machine, and triggering the serializer *SN* signals that synchronize the process of slicing the data (indicating the slice number). The combined slices from each serializer form the digital outputs D_1, D_2, and D_3, respectively. For the 1 μs measurement sample shown in Fig. 10, the digital outputs are 42, 100, and 41, respectively.

The resultant error in this sample is $+1T_{fine} = 115$ ps (τ_D).

Other measurements samples in the nanosecond range (ΔT_{in} = 57 ns, 58 ns, 59 ns, 60 ns, 61 ns, 62 ns, and 63 ns) are shown in Fig. 11, confirming the TDC performance over wide range, with the measurement errors e_{tot} bounded to $[-2T_{fine}, +2T_{fine}]$ range as given by (3) for various ΔT_{in}.

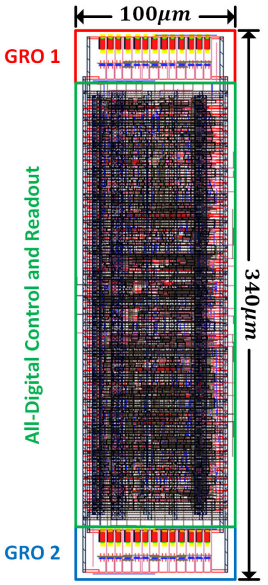


FIGURE 9. Proposed TDC Layout.

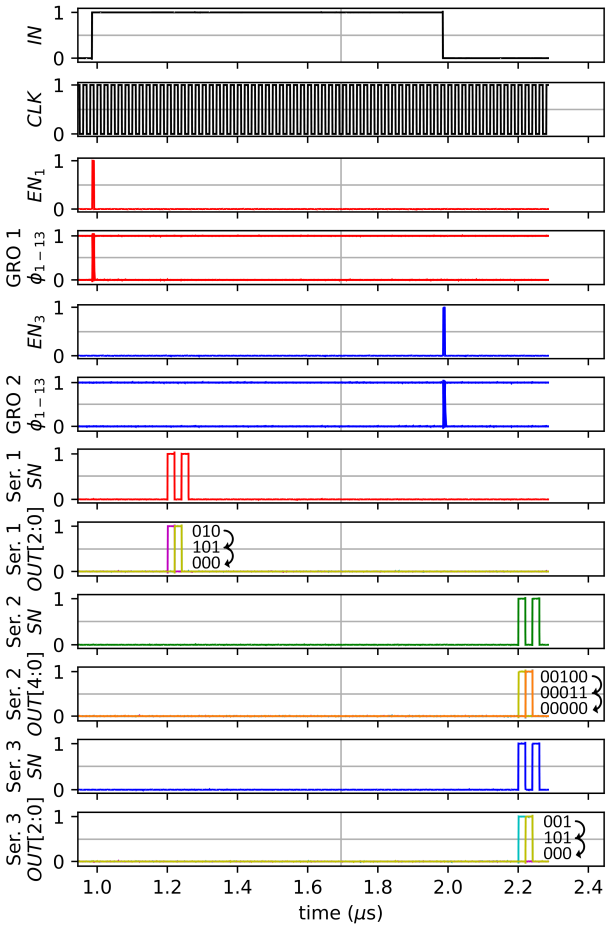


FIGURE 10. Post-Layout Transient Simulation.

More specialized post-layout simulations (with device noise enabled) are performed to further examine the TDC performance metrics:

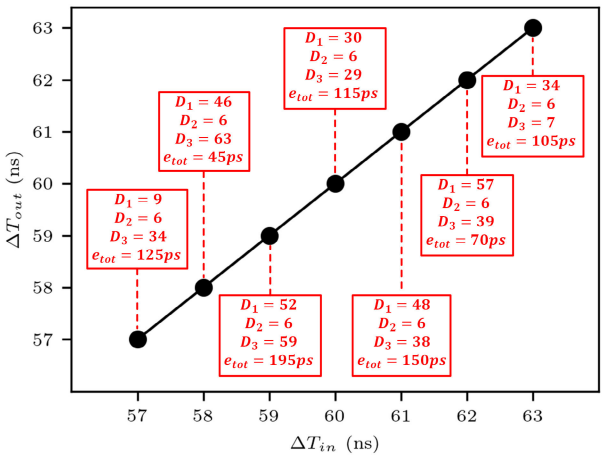


FIGURE 11. Nanosecond Measurement Samples.

A. DYNAMIC RANGE AND CONVERSION RATE

To confirm the ability of the TDC to adapt to various dynamic ranges as desired, we repeat the same procedure at 20 MHz and 80 MHz clock frequencies. Table 1 summarizes the TDC's metrics in terms of dynamic range, conversion rate, and sampling rate. Here, the maximum clock frequency $\simeq 80$ MHz is determined by the speed of the digital circuits, while the minimum clock frequency $\simeq 20$ MHz is determined by the GRO based TDC dynamic range. Any clock frequency within this range can be utilized. Furthermore, the TDC's conversion time T_{conv} is constant, equal to a few clock cycles (16 clock cycles in this implementation) as determined by the ELR state machine which considers the readout glitches and latency. In this case, the conversion rate $f_c = 1/16T_{clk}$. However, the sampling rate f_s in the time domain varies according to the required dynamic range ($\Delta T_{in,max}$):

$$f_s = \frac{1}{\Delta T_{in,max} + T_{conv}} \tag{4}$$

A longer $\Delta T_{in,max}$ requires a lower sampling rate. The proposed TDC adapts to higher rates at lower $\Delta T_{in,max}$.

TABLE 1. TDC Dynamic Range and Sampling Rate.

CLK Freq. (f_{clk})	Dyn. Range (ΔT_{in})	Conv. Rate (f_c)	Samp. Rate (f_s)
20 MHz	1.6 ms (max)	1.25 MHz	0.6 kHz
	1 μs		0.5 MHz
	100 ns		1.11 MHz
50 MHz	0.65 ms (max)	3.125 MHz	1.5 KHz
	1 μs		0.75 MHz
	100 ns		2.38 MHz
80 MHz	0.4 ms (max)	5 MHz	2.4 kHz
	1 μs		0.83 MHz
	100ns		3.33 MHz

TABLE 2. TDC Power Dissipation.

CLK Freq. (f_{clk})	Conv. Rate (f_c)	Power Diss. (p_{diss})	Idle Power Diss. (p_{idle})
20 MHz	1.25 MHz	39.37 μW	8.20 μW
50 MHz	3.125 MHz	45.85 μW	17.12 μW
80 MHz	5 MHz	56.07 μW	26.10 μW

B. POWER DISSIPATION

The TDC's power dissipation (including the integrated serializers) is characterized as shown in Table 2. The dissipation is proportional to the average ON time of the GRO TDCs, and the clock frequency. At low clock frequencies, the power dissipation of the GRO based TDCs dominates because of their longer ON times $\in]0, 0.5T_{clk}]$. In our test benches, the oscillator ON time is around $0.25T_{clk}$ (the average case).

Additionally, the TDC's idle power dissipation (when no measurement is active) is characterized. As shown in Table 2, only 8.2 μW is dissipated at 20 MHz clock frequency. This confirms the ability of the proposed TDC to enable efficient event-triggered sensing.

TABLE 3. FoM Comparison.

Ref.	FoM (pj/conv) The lower, the better
This work (20 MHz)	5.61×10^{-6}
This Work (50 MHz)	6.44×10^{-6}
This work (80 MHz)	8.00×10^{-6}
TCAS-I'17 [15]	1.16
TCAS-II'22 [3]	22.21×10^{-3}
TCAS-II'23 [2]	32.90×10^{-3}
TIAM'25 [16]	2.17×10^{-3}-2.52×10^{-3}
SSCL'23 [17]	0.88
TCAS-II'22 [18]	2.61
TCAS-II'24 [19]	0.30

C. STATIC LINEARITY

Fig. 12 shows the quantization grid formed by GRO 1 and GRO 2. An average $T_{LSB} \simeq 115.16$ ps and 116.69 ps is obtained for the GROs as shown in Fig. 12b.

The grid LSB is determined by the average time difference between two consecutive edges. The 1.53 ps difference in the LSB is a static offset due to interconnects asymmetry.

Fig. 12c shows DNL and INL errors of the GRO based TDCs, which arise from the step width deviations with respect to the obtained T_{LSB}. Thanks to the utilized techniques, the DNL and INL errors are kept below 0.09 LSB (0.17 LSB peak-to-peak) and 0.17 LSB (0.24 LSB peak-to-peak), respectively.

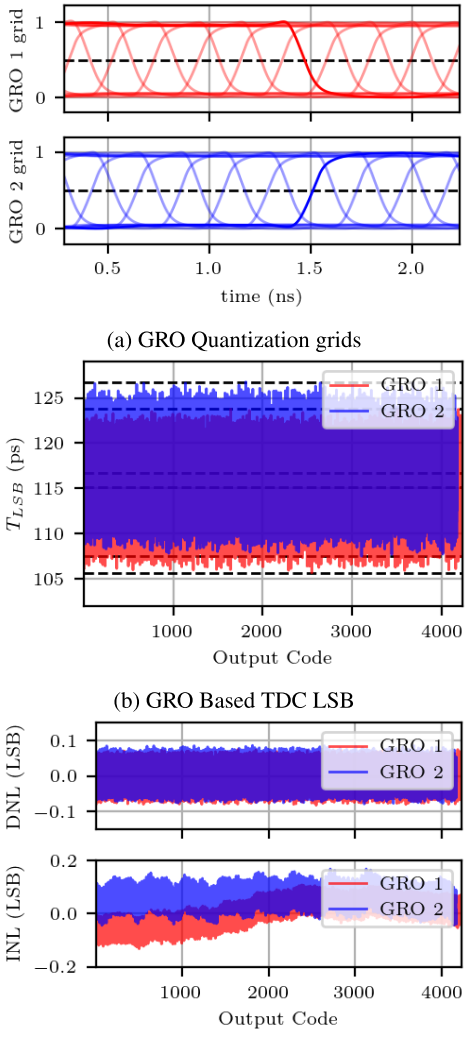
D. EFFECT OF LOCAL MISMATCHES

To characterise the effect of the local oscillators' mismatches, we built a model to estimate the quantization error $e_{q,tot}$ when the GRO TDCs T_{LSB} differ by an offset τ_{offset}.

TABLE 4. Comparison of State-of-the-Art Time-to-Digital Converters.

Ref.	Tech. (nm)	TDC Architecture	Applications	No. of Bits	Resolution (ps)	Range (ns)	$INL_{p\text{-}p}$ (LSB)	Conversion Rate (MHz)	Area (μm^2)	Power Diss. (μW)
TCAS-I'17 [15]	180	GRO	LiDAR	11	147	297	3	2	1700	1170[a]
TCAS-II'18 [20]	45	Delay-Line	Generic	5[b]	25-69	0.8-2.2	N/A	4000	360000	16000
TCAS-I'22 [21]	180	GRO	LiDAR	11	50	102	2.18	N/A	1500	1300[a]
TCAS-II'22 [3]	65	Osc.-Based	ToF Imaging	12	24.5	100	10	125	1920	1030
TCAS-II'23 [2]	350	Osc.-Based	LiDAR	11	40	82[c]	2.08	100	1350	2190
JSSC'19 [22]	65	Osc.-Based	ToF Depth	14	61-204	1×10^3-3.34×10^3	3	N/A	550	200-500
TIAM'25 [16]	130	GRO	Generic	11[c]	80-160	163-238	1.73	500	576	590-940[a]
SSCL'23 [17]	90	PLL-Based	Generic	14	18	206	0.81	0.45	19276	2500
TCAS-II'22 [18]	65	Vernier	LiDAR	17	19.5	2500	5.5	0.999	432000	51400
TCAS-II'24 [19]	65	GRO	Generic	10	3.1	3.2	6.9	36	13000	1410
This Work	65	Nutt w/ GRO	ToF/LiDAR	9,15,9[d]	2 ×115	**0.4 $\times10^6$-1.6 $\times10^6$**	**0.24**	1.25-5	34000	**39.37-56.07**

[a]Power is characterized when TDC is operating continuously
[b]Equivalent no. of bits from 32-bit thermometer output code
[c]Estimated
[d]20-22 equivalent number of bits, 11 data bits after serializing



(a) GRO Quantization grids

(b) GRO Based TDC LSB

(c) GRO Based TDC DNL and INL

FIGURE 12. GRO TDCs Quantization Grids and Linearity.

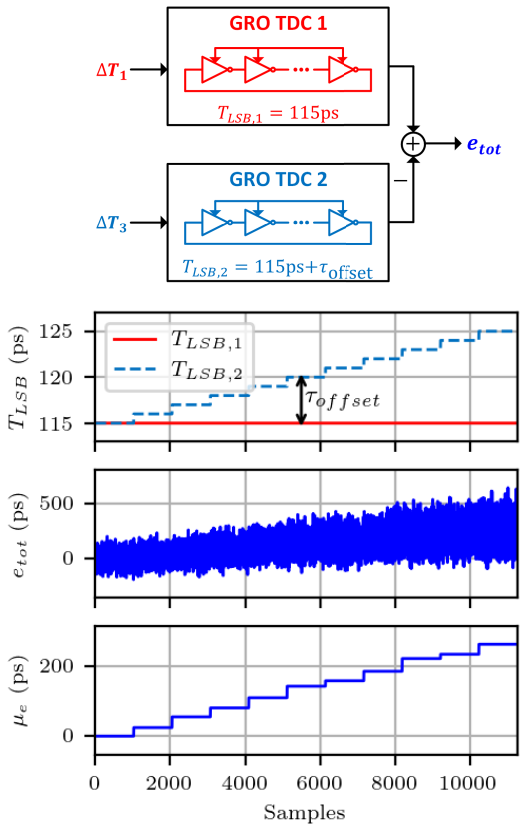


FIGURE 13. Quantization Error Model with Oscillators' Mismatches.

As shown in Fig. 13, the model quantizes 11×1024 samples: 1024 samples for each $\tau_{offset} \in [0, 10]$ ps.

When $\tau_{offset} = 0$, $e_{q,tot} \in [-2T_{fine}, +2T_{fine}]$ as presented in equation (3). While, as τ_{offset} increases, $e_{q,tot}$ increases.

This puts an upper limit $\simeq$ 4ps for the overall average offset between the quantization grids generated by the oscillators, such that quantization error is kept within the ideal range ($|e_{q,tot}| < 2T_{fine}$).

In the proposed implementation, an overall offset $\simeq$ 1.5 ps is noticed (see Fig. 12b), which is well below the upper limit suggested by the model.

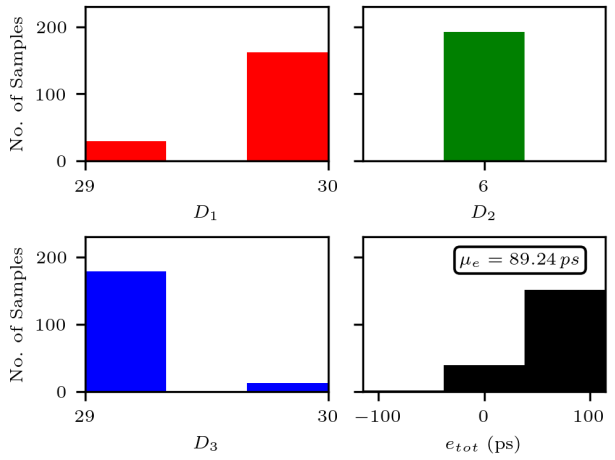


FIGURE 14. Monte-Carlo Simulation with Oscillators' Mismatches.

In addition to the model, we continued our verification by performing Monte-Carlo simulation. Fig. 14 shows the outputs of several post-layout test samples at $\Delta T_{in} = 60$ ns. As shown, the error is kept in the expected range for all the samples (192 samples), with 89.24 ps mean value (μ_e).

E. FIGURE-OF-MERITS AND COMPARISONS TO STATE-OF-THE-ART

The energy per conversion figure of merit (FoM) given in (5)-(6) is typically adopted to evaluate the performance of TDCs, combining information on power dissipation, conversion rate, and dynamic range (number of bits) [8]:

$$FoM = \frac{\text{Power Diss.}}{\text{Conversion Rate} \times 2^{\text{Linear Bits}}}$$

$$\text{Linear Bits} = \text{Bits} - \log_2(INL + 1) \quad (5)$$

$$= \log_2\left(\frac{\text{Range}}{\text{Resolution}}\right) - \log_2(INL + 1) \quad (6)$$

As shown in Table 3, the proposed TDC achieves an excellent FoM compared to the work in relevant references, thanks to the low-power dissipation and the wide dynamic range. We used the peak-to-peak INL and the rate $= f_c$ (conversion rate) to calculate the FoM. Additionally, the detailed comparison presented in Table 4 demonstrates that the proposed TDC achieves satisfactory overall performance metrics for embedded sensing applications.

V. CONCLUSION

This paper presents a TDC architecture to target time-of-flight LiDAR and ultrasonic range finders. The proposed TDC shows competitive metrics in terms of dynamic range and power dissipation. It supports up to 1.6 ms dynamic range, and dissipate power as low as 39.37 μW in active mode and 8.20 μW in idle mode. Moreover, it only occupies 100 μm $\times$340 μm in 65-nm CMOS implementation including integrated event-triggered serializers.

APPENDIX A
QUANTIZATION MODEL OF GRO BASED TDC

The quantization in a TDC is performed by utilizing the quantization grid generated by a delay generator or a time reference. For a GRO based TDC, the grid is generated by the ring oscillator, with a resolution (T_{fine}) determined by the time difference between two consecutive edges (see Fig. 12).

As show in Fig. 15, we model the process of quantizing a time duration $\Delta T = t_2 - t_1$ in two steps, each introducing a quantization error:

(1) The first edge time-instant t_1 (rising edge) is quantized, introducing a quantization error $e_{q,\text{rising}} \in [0, T_{fine}]$.

$$t_1 \xrightarrow{\text{Quantization}} t_1 + e_{q,\text{rising}} \quad (7)$$

(2) The second edge t_2 (falling edge) is quantized, introducing another quantization error $e_{q,\text{falling}} \in [0, T_{fine}]$.

$$t_2 \xrightarrow{\text{Quantization}} t_2 + e_{q,\text{falling}} \quad (8)$$

Since the duration being quantized (ΔT) equal to $t_2 - t_1$, the total quantization error $e_{q,\text{total}}$ is determined as given by equations (9)-(11).

$$\Delta T \xrightarrow{\text{Quantization}} \Delta T_Q \quad (9)$$

$$\Delta T_Q = (t_2 + e_{q,\text{falling}}) - (t_1 + e_{q,\text{rising}})$$

$$= \Delta T + (e_{q,\text{falling}} - e_{q,\text{rising}}) = \Delta T + e_{q,\text{total}} \quad (10)$$

$$e_{q,\text{total}} = e_{q,\text{falling}} - e_{q,\text{rising}}; \in [-T_{fine}, +T_{fine}] \quad (11)$$

This model follows the generic TDC models presented in [23].

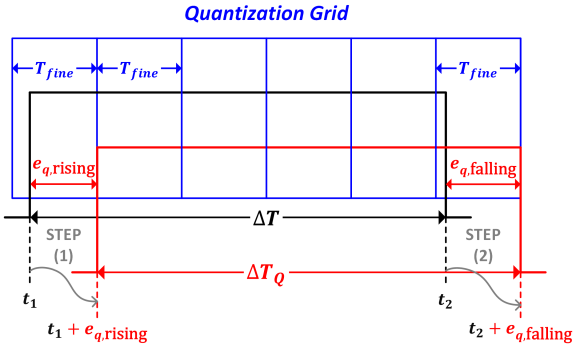


FIGURE 15. GRO Based TDC Quantization Model.

REFERENCES

[1] S. Kurtti, J.-P. Jansson, and J. Kostamovaara, "A CMOS receiver–TDC chip set for accurate pulsed TOF laser ranging," *IEEE Trans. Instrum. Meas.*, vol. 69, no. 5, pp. 2208–2217, May 2020.

[2] J. Hu, D. Li, X. Wang, R. Ma, Y. Liu, and Z. Zhu, "A 40-ps resolution robust continuous running VCRO-based TDC for LiDAR applications," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 70, no. 2, pp. 426–430, Feb. 2023.

[3] F. Arvani and T. C. Carusone, "A reconfigurable 5-channel ring-oscillator-based TDC for direct time-of-flight 3D imaging," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 69, no. 5, pp. 2408–2412, May 2022.

[4] C. Niclass, C. Favi, T. Kluter, M. Gersbach, and E. Charbon, "A 128 × 128 single-photon image sensor with column-level 10-bit time-to-digital converter array," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2977–2989, Dec. 2008.
[5] R. Nutt, "Digital time intervalometer," *Rev. Sci. Instrum.*, vol. 39, no. 9, pp. 1342–1345, Sep. 1968.
[6] J. Kostamovaara and R. Myllylä, "Time-to-digital converter with an analog interpolation circuit," *Rev. Sci. Instrum.*, vol. 57, no. 11, pp. 2880–2885, Nov. 1986.
[7] Z. Cheng, X. Zheng, M. J. Deen, and H. Peng, "Recent developments and design challenges of high-performance ring oscillator CMOS time-to-digital converters," *IEEE Trans. Electron Devices*, vol. 63, no. 1, pp. 235–251, Jan. 2016.
[8] R. Scott, W. Jiang, and M. J. Deen, "CMOS time-to-digital converters for biomedical imaging applications," *IEEE Rev. Biomed. Eng.*, vol. 16, pp. 627–652, 2023.
[9] K.-C. Choi, S.-W. Lee, B.-C. Lee, and W.-Y. Choi, "A time-to-digital converter based on a multiphase reference clock and a binary counter with a novel sampling error corrector," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 59, no. 3, pp. 143–147, Mar. 2012.
[10] O. Järvinen, V. Unnikrishnan, W. Siddiqui, T. Korhonen, K. Koli, K. Stadius, M. Kosunen, and J. Ryynänen, "A 100–750 MS/s 11-bit time-to-digital converter with cyclic-coupled ring oscillator," *IEEE Access*, vol. 9, pp. 48147–48156, 2021.
[11] E. Helal, E. Alvarez-Fontecilla, A. I. Eissa, and I. Galton, "A time amplifier assisted frequency-to-digital converter based digital fractional-N PLL," *IEEE J. Solid-State Circuits*, vol. 56, no. 9, pp. 2711–2723, Sep. 2021.
[12] J.-P. Jansson, A. Mantyniemi, and J. Kostamovaara, "A CMOS time-to-digital converter with better than 10 ps single-shot precision," *IEEE J. Solid-State Circuits*, vol. 41, no. 6, pp. 1286–1296, Jun. 2006.
[13] J.-P. Jansson, A. Mantyniemi, and J. Kostamovaara, "Synchronization in a multilevel CMOS time-to-digital converter," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, no. 8, pp. 1622–1634, Aug. 2009.
[14] V. Unnikrishnan and M. Vesterbacka, "Mitigation of sampling errors in VCO-based ADCs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 7, pp. 1730–1739, Jul. 2017.
[15] I. Vornicu, R. Carmona-Galan, and A. Rodriguez-Vazquez, "Arrayable voltage-controlled ring-oscillator for direct time-of-flight image sensors," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 11, pp. 2821–2834, Nov. 2017.
[16] J. Hu, J. Ma, Y. Ping, X. Wang, D. Li, R. Ma, and Z. Zhu, "A GRO-based configurable TDC with 80/160-ps resolution in single-channel and interleaving mode," *IEEE Trans. Instrum. Meas.*, vol. 74, pp. 1–10, 2025.
[17] J.-C. Liu and Y.-X. Chen, "DPLL-based VRO of time-to-digital converter," *IEEE Solid-State Circuits Lett.*, vol. 6, pp. 45–48, 2023.
[18] W. Zhang, R. Ma, X. Wang, H. Zheng, and Z. Zhu, "A high linearity TDC with a united-reference fractional counter for LiDAR," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 69, no. 2, pp. 564–572, Feb. 2022.
[19] X. Lu, J. Wu, Z. Wang, Y. Xiang, L. Liu, P.-I. Mak, R. P. Martins, and M.-K. Law, "A 0.013 mm^2 3.2-ns input range 10-bit cyclic time-to-digital converter using gated ring oscillator with phase domain reset in 65-nm CMOS," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 71, no. 8, pp. 3635–3639, Aug. 2024.
[20] S. Ur Rehman, M. M. Khafaji, C. Carta, and F. Ellinger, "A 16 mW 250 ps double-hit-resolution input-sampled time-to-digital converter in 45-nm CMOS," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 65, no. 5, pp. 562–566, May 2018.
[21] J. Hu, X. Wang, D. Li, Y. Liu, R. Ma, and Z. Zhu, "A 50-ps gated VCRO-based TDC with compact phase interpolators for flash LiDAR," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 69, no. 12, pp. 5096–5107, Dec. 2022.
[22] A. Ronchini Ximenes, P. Padmanabhan, M.-J. Lee, Y. Yamashita, D.-N. Yaung, and E. Charbon, "A modular, direct time-of-flight depth sensor in 45/65-nm 3-D-stacked CMOS technology," *IEEE J. Solid-State Circuits*, vol. 54, no. 11, pp. 3203–3214, Nov. 2019.
[23] S. Henzler, *Time-to-Digital Converters*. Cham, Switzerland: Springer, 2010.

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