A Combined Analytical and Simulation-based Methodology for Quantifying the Noise-Power-Area Trade-offs in Biomedical Amplifiers

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***Abstract*—Low-noise operation is one of the most important performance criteria for low-power amplifiers targeting biopotential acquisition. While advanced circuit architectures exist to minimize the intrinsic noise, an analytical formalism is still lacking to estimate the lowest achievable noise level without performing extensive circuit-level optimizations. This work proposes a hybrid methodology mixing theoretical analyses and a limited number of simulations to estimate and minimize the input-referred noise and the noise efficiency factor of various biomedical amplifiers topologies. Compared to previous works, accurate bias-dependent noise models are obtained thanks to simulations of single devices and allow this methodology to successfully take into account the thermal and flicker noise sources from MOS transistors analytically. The optimal noise-current-area trade-off is then derived, showing the fundamental limits of the architecture. In this paper, the proposed methodology is applied to a current-reuse amplifier topology designed for two applications. The specifications for each application are obtained from a system-level perspective, including an input high-pass filter whose noise is considered analytically. Simulation-based optimization results show a good agreement with the analytical approach, proving that the methodology can be used for noise estimation, comparison between architectures, and to extract meaningful design guidelines.**

***Index Terms*—Biomedical amplifier, analytical noise modeling, low-power, noise efficiency factor (NEF), flicker noise, noise power spectral density (PSD), band-pass filtering.**

I. Introduction

BIOMEDICAL systems-on-chip (SoCs) are key components for various applications such as motor function recovery [1], implanted stimulation devices [2] and patient monitoring [3]. Among those, implantable or wearable sensor devices used for biopotential recording were widely studied in the last twenty years [3]–[11]. In such SoCs, the analog front end (AFE) is often a bottleneck regarding the power consumption as low noise is required. Among the biopotential recording applications, AFEs targeting electrocardiogram (ECG) monitoring are studied in [3]–[6], and the analog circuitry for various electroneurogram (ENG) applications is the subject of [7]–[10]. While those applications differ in terms of signal amplitude, bandwidth and power consumption, their AFEs are required to reach a certain trade-off between the intrinsic noise injected on top of the signals by the analog blocks, and the power consumption of those circuits. Fig. 1 shows a typical biomedical SoC used for biopotential recording. It includes an AFE, a digital back end for signal processing, a clock and power management unit and a radio transceiver (TRX) for RF communication. The implementation of the AFE differs from one application to another, but it usually consists of amplifiers, filters and an analog-to-digital converter (ADC). In applications targeting biopotential acquisition, a high-pass filter (HPF) is often included at the input of the system to suppress the electrode offset and to attenuate low-frequency interference. Non-attenuated interference could lead to amplifier saturation, making the useful signal invisible to the digital back end. The amplifier can be split into two different structures: (i) a low-noise amplifier (LNA) optimized for low noise and low power, and (ii) a high-gain amplifier optimized for high gain and low power. The noise from the high-gain amplifier is less critical for the global signal-to-noise ratio (SNR) as the signal is already pre-amplified by the LNA. A band-pass filter (BPF) is then added at the end of the conditioning chain to attenuate the low-frequency noise originating from the LNA, and to avoid aliasing by the ADC. In many applications, the system is powered by a low-capacity battery, necessitating ultra-low power consumption. Besides, most biopotential signals captured by the electrodes have a very low amplitude, ranging from a few µV to several mV, depending on the target application. Very low noise is thus required to keep a sufficient SNR, making the noise-power trade-off an important metric for LNA design.

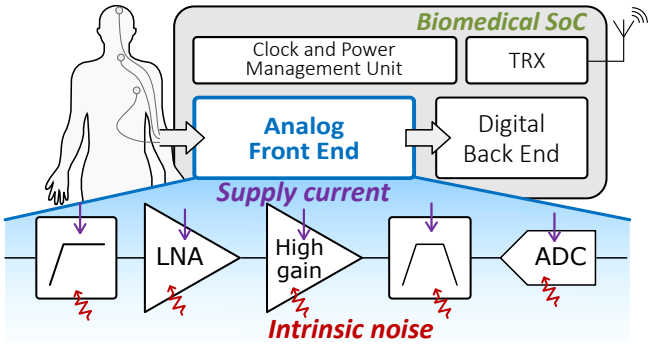

Fig. 1. Simplified view of a typical biomedical SoC, explicitly showing the usual components of the AFE: a high-pass filter, a low-noise amplifier (LNA), a high-gain amplifier, a band-pass filter and an analog-to-digital converter (ADC). The electrodes on different parts of the human body illustrate the various applications that require low-noise AFEs.

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Architectural solutions have been investigated to reduce the thermal noise of low-power biomedical amplifiers, going from weak-inversion differential pairs [8] and current-reuse (CR) topologies [4], [5], [9] to stacked structures [6] and switched-capacitor amplifiers [12]. While many works analytically explain their achievements in the minimization of the thermal noise of the amplifier, flicker noise is often not optimized analytically [8], [9], [13]. However, as detailed in [14], reduction of the intrinsic flicker noise comes at the price of additional silicon area, adding a new dimension to the usual noise-power trade-off. On top of the intrinsic noise from the amplifier, the impact of the HPF on the total noise is sometimes not discussed [9], [10], [15], even though the contribution of its components can be significant as the filter is placed at the system input. Chopping is a technique commonly used to reduce the effects of flicker noise in biomedical amplifiers. It works by modulating the input signal to a frequency band higher than the noise corner frequency f_c of the amplifier. While chopper amplifiers may suffer from a low input impedance, such architectures have been implemented in many previous works [6], [7], [16]–[18] for their efficient attenuation of flicker noise. Noise analyses and optimizations for chopper amplifiers have been thoroughly described in [19]. To avoid overlapping between the flicker noise and the signal in the output spectrum, the chopper frequency must be higher than $f_c + f_H$ where f_H is the upper bandwidth limit of the useful signal. [19] also indicates that the input impedance of the chopper amplifier is inversely proportional to the chopper frequency. It could then be worth to minimize the amplifier noise corner frequency prior to chopping.

This work addresses the aforementioned challenges by developing an analytical methodology for noise modelling and optimization, including thermal and flicker noise from multiple blocks. This methodology can be applied to different usages: (i) a quick estimation of the optimal noise-power-area trade-off of an amplifier and its input HPF, (ii) an easy comparison of the noise performance of different topologies, and (iii) guidelines for the sizing of low-noise biomedical amplifiers. The accuracy of the analytical models is ensured through bias-dependent noise coefficients extracted from simulations. The minimization of the noise corner frequency is studied with respect to the area overhead required to reduce the flicker noise. In our cases, with a large area budget, the flicker noise can be made lower than the thermal noise in the frequency bandwidth of interest. This paper is organized as follows. First, Section II describes the goals and outputs targeted by the presented analysis. Section III describes the methodology in details with developments on noise models and on the noise bandwidth. Then, Section IV applies the presented methodology to a CR amplifier topology and compares the results to simulation-based optimizations. Finally, Section V provides concluding remarks.

II. Noise, Power and Area trade-off

This paper proposes a methodology to quantify the noise-power-area trade-off in biomedical amplifiers. The novelties of this methodology come in three different goals linked to noise

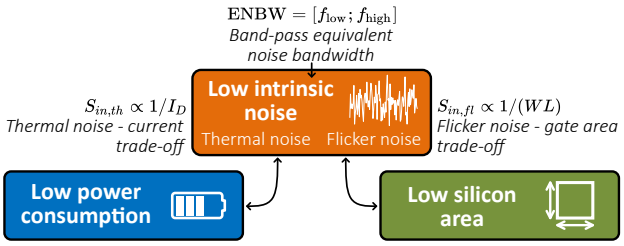

Fig. 2. Illustration of the interconnections between current consumption, gate area and input-referred noise. The input-referred noise is computed from the thermal noise PSD (dependent on the current consumption) and the flicker noise PSD (dependent on the total gate area). Those PSDs are then integrated following the bounds given by the equivalent noise bandwidth.

TABLE I
Parameters of the considered applications

	ECG	VENG
Signal amplitude	1 mV	20 µV
Useful bandwidth	[1 - 250] Hz	[0.3 - 10] kHz
Max. IRN	$<$1 μV_{RMS}	μV_{RMS} range
Electrode type	Surface	Cuff

computation, such as illustrated by the three arrows in Fig. 2. First, the relationship between the thermal noise power spectral density (PSD) and the current consumption is often discussed in the literature when deriving the input-referred thermal noise of an amplifier [6]–[8], [11]. The noise efficiency factor (NEF) is commonly employed to characterize this trade-off [11] and will be further discussed in Section III-C. This work proposes to use bias-dependent noise models to enhance the accuracy of the estimation of the thermal noise PSD with regards to current consumption, and to extract design guidelines for optimal performance. The dependence of the noise models on the inversion level of the devices can indeed lead to significant insights for the sizing and biasing of the transistors. Second, the trade-off between the flicker noise and the gate area is well-known at device level, since the flicker noise is often modeled as inversely proportional to the gate area of the MOSFET. Thus, quantifying the relationship between area and flicker noise at circuit level can lead to an estimation of the required amplifier area for a given flicker IRN level and vice-versa. The impact of limited area on the transistors biasing is also discussed in this paper. Finally, once the IRN PSD is known, it is necessary to determine over which bandwidth the PSD must be integrated to compute the total noise power. These integration bounds are often computed by means of the equivalent noise bandwidth (ENBW), using the upper bound of the useful signal bandwidth. However, many biopotential recording applications also require an attenuation of low-frequency interference and thus include band-pass filtering of the useful signal. Up to the authors' best knowledge, no strict formalism exists to determine the ENBW in case of high-pass filtering as applied to biopotential acquisition. Combining these three approaches allows to fully quantify the interconnections between input-referred noise, current consumption and required area.

In this paper, the methodology is illustrated by analysing

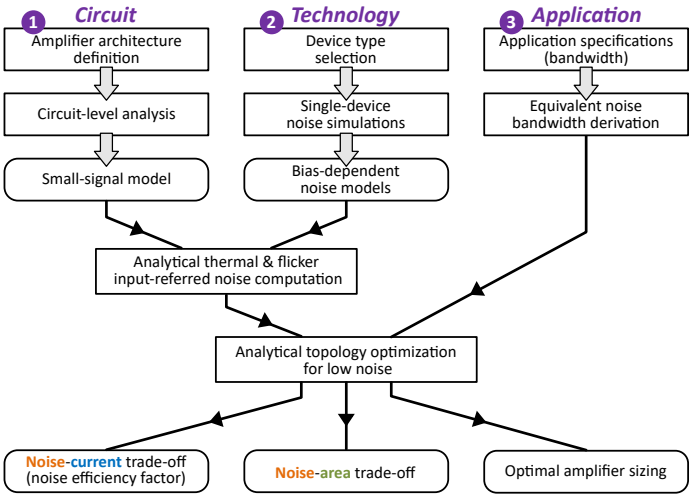

Fig. 3. Flow chart illustrating the proposed methodology with its three axes (circuit, technology and application) and its outputs.

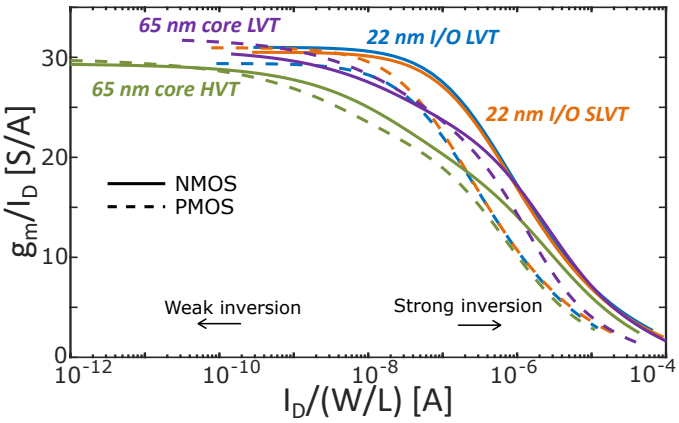

Fig. 4. g_m/I_D vs drain current normalized to the transistor aspect ratio, for N (solid) and P (dashed) MOSFETs in different threshold voltage flavors and nodes (65 nm core: LVT, HVT; 22 nm I/O: LVT, SLVT). Curves extracted for $W = 100$ µm, $L = 1$ µm and $V_{DS} = 1.2$ V.

a CR amplifier and its associated input high-pass filter. The amplifier is designed for two representative applications. First, we study the case of ECG signals, whose low bandwidth makes flicker noise non-negligible. Next, vagus nerve electroneurogram (VENG) is the second application studied in this work. Vagus nerve recording can be used to measure several physiological signals such as blood pressure fluctuations [20]. Recently, it was also shown that markers of epileptic seizures can be detected in the VENG, paving the way for minimally invasive closed-loop vagus nerve stimulation [21]. The proposed methodology can be used for any biopotential acquisition application where the noise-power-area trade-off is a critical figure of merit, such as for neural spikes recording [22].

Table I provides a summary of the typical parameters of the considered applications. The large differences in bandwidth calls for different trade-offs, which enriches and generalizes the discussion of the proposed methodology. In general, low-noise operation is required in both applications for high-precision signal processing. The noise specifications originate from published works for ECG and VENG signal acquisition [4], [10], [21], [23], while the signal amplitude depends on the type of electrode used. As the studied circuits are optimized for biomedical applications working in or on the human body, a temperature of 37°C is assumed in this work, although the methodology can be applied to systems operating over a wide range of temperatures. In addition to the different applications and to show that the methodology works with a wide variety of MOSFETs, the amplifier is simulated in two different CMOS technologies: core transistors in 65-nm bulk CMOS and I/O devices in 22-nm fully depleted silicon-on-insulator (FD-SOI). I/O MOSFETs with minimum channel length of 34 nm have been selected in 22 nm for their better noise performance than the core devices in that node. Many AFEs targeting biomedical purposes are implemented in sub-micron nodes such as 0.18 µm [5], [6], [9]. In this work, more advanced nodes are chosen as the SoC often requires a fast and low-power digital back end to perform heavy embedded processing.

III. Proposed Methodology

Fig. 3 illustrates the proposed methodology used to quantify the noise-current-area trade-off of biomedical amplifiers, such as detailed in Section II. The starting point of the methodology is divided into three different axes. First, the bioamplifier topology is defined and its small-signal model in the signal bandwidth is computed based on classical methods. In the second axis, the devices implementing the amplifier are defined, namely the considered technology node and transistor flavors. Bias-dependent noise models are extracted from simulations of those components. Spectre, the circuit simulator from Cadence, and compact models provided by the foundries for 65-nm et 22-nm technologies are used to simulate the transistors and the circuits. On the third axis, the useful signal bandwidth is defined based on the target application and the ENBW is derived. From the amplifier small-signal representation and the bias-dependent noise models of the devices, the thermal and flicker IRN PSDs are computed analytically. Thanks to the analytical expressions representing the thermal and flicker IRN, the sizing of the amplifier can be optimized through the inversion level of the transistors and the g_m/I_D methodology [24]. The impact of other types of devices such as resistors can also be quantified. As a result, the analytical expressions represent the minimum noise that can be reached with the topology, as a function of the current consumption and the required gate area. The noise-current-area trade-off is then quantified for the amplifier in a certain technology implementation. Finally, thanks to the pre-computed ENBW, the input-referred noise power and voltage can be computed from given current and area budgets. In this section, the g_m/I_D methodology, the device-level noise models, and the computation of the ENBW are described.

A. g_m/I_D Design Methodology

The g_m/I_D methodology, presented in [24] and extended to short-channel CMOS technologies in [25], is based on a quantity defined as the ratio between the transistor transconductance over its drain DC current, and expressed in S/A or

in V^{-1}. As detailed in [26], g_m/I_D is an indicator of the inversion level of the transistor. The methodology, used for transistor sizing in analog design, exploits the link between the drain current I_D of a device normalized to its width-to-length ratio (W/L), and its g_m/I_D. Fig. 4 depicts the g_m/I_D-$I_D/(W/L)$ curves for N and P-channel devices in different threshold voltage flavors and in both of the technology nodes used in this work. The curves are only shown for $W = 100$ µm and $L = 1$ µm, but the dimensions do not significantly impact the results in case of long-channel devices. Short-channel effects have been observed for lengths below 200 nm and 100 nm in 65-nm core and 22-nm I/O devices, respectively. In analog amplifiers, transistor lengths larger than the minimum length of the technology are usually preferred to improve the matching of the devices, reduce the flicker noise, avoid short-channel effects, and maximize the intrinsic gain of the MOSFETs. Therefore, channel lengths around 1 µm are assumed in this work. It will be shown that, in the absence of very strict area constraints, the optimal sizing only includes lengths in the µm range. The maximum transconductance to drain current ratio that can be reached in the exponential subthreshold regime with a given transistor flavor can be extracted from Fig. 4. As detailed in [24], the maximum g_m/I_D can also be expressed as

$$\left(\frac{g_m}{I_D}\right)_{\max} = \frac{1}{nV_T}, \tag{1}$$

where n is the body factor of the transistor and V_T is the thermal voltage. Hence, the value extracted from Fig. 4 can be used to compute the body factor of the device which will be used for noise modelling. It is important to keep in mind that this value of the body factor is only valid in weak inversion. Additionally, Fig. 4 shows that there is a plateauing trend in the g_m/I_D - $I_D/(W/L)$ curve toward weak inversion. In this regime, it is therefore possible to vary I_D at constant dimensions by at least a decade without affecting much the g_m/I_D of the device. This effect will be used in the rest of this work to sweep over multiple values of current while maintaining the transistor in weak inversion.

B. Bias-Dependent Noise Modeling

In order to fully describe the noise-current-area trade-off in an amplifier, it is necessary to develop a model for the noise coming from each device. This section presents a model of the noise sources in resistors (thermal) and MOS transistors (thermal and flicker) that only rely upon circuit-level quantities available to the designer, upgraded with technology-dependent and bias-dependent parameters obtained from simulations.

Regarding resistors, only thermal noise is considered. It is modeled as a current source in parallel with the resistor. The noise PSD is given by

$$S_{i_R} = 4kT/R, \tag{2}$$

where k is the Boltzmann constant, T the absolute temperature, and R the resistance value.

Circuit designers often model the MOSFET channel thermal noise as

$$S_{i_d} = \frac{8}{3}kTg_m. \tag{3}$$

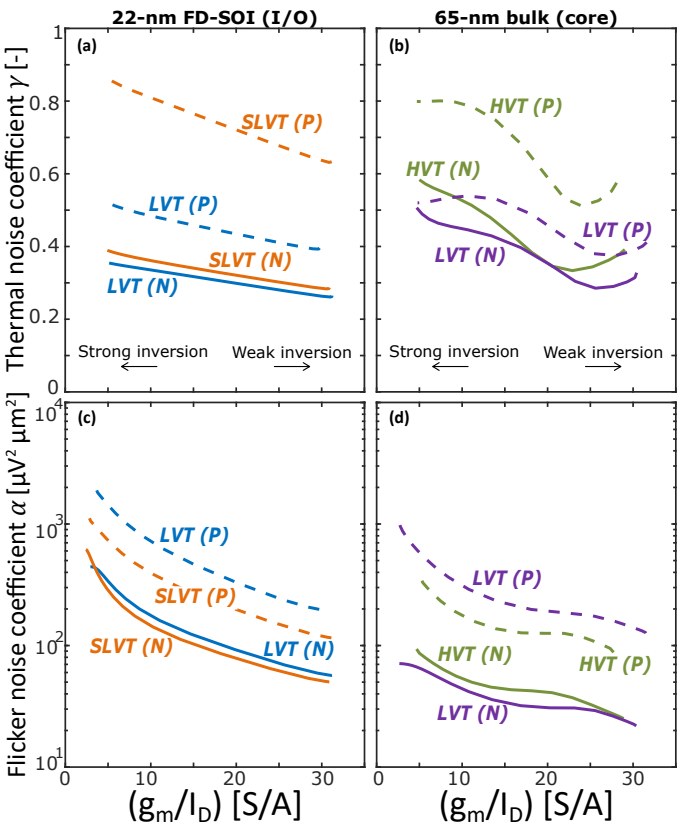

Fig. 5. Noise coefficients in 65-nm bulk core transistors (LVT, HVT) and 22-nm FD-SOI I/O transistors (LVT, SLVT) at device level for N (solid) and P (dashed) MOSFETs. Dependencies of the thermal (a), (b) and flicker (c), (d) noise coefficients on g_m/I_D are shown. Curves extracted for $W = 100$ µm, $L = 1$ µm and $V_{DS} = 1.2$ V.

However, this model only holds for long-channel devices in saturation and in strong inversion regime [27], [28]. For a more complete model over different levels of inversion, we propose to use

$$S_{i_d} = 4kT\gamma g_m. \tag{4}$$

This model is valid for transistors in the saturation regime [27], which is often the case for transistors used in amplifiers. In this work, we thus use the model from (4) and consider variations of γ with the inversion level. To this end, MOS transistors are simulated with fixed V_{BS} and V_{DS}, sweeping V_{GS} to cover different inversion levels. The drain current and the transconductance g_m are evaluated, and the channel thermal noise PSD is obtained from NOISE AC simulations based on well-established foundry models. The γ parameter is then extracted from the noise PSD. This study was conducted for LVT and SLVT I/O transistors in 22 nm and LVT and HVT core devices in 65 nm. The results are shown in Figs. 5(a) and (b), where the γ coefficient is plotted as a function of the inversion level, quantified by the g_m/I_D ratio of the transistor. These curves were extracted at different transistor dimensions and at different V_{DS}, yet no significant differences could be observed. Fig. 5 shows that γ always remains between 0.25 and 1.0 for these transistors. It is generally lower in weak inversion than in strong inversion. For the 65-nm node, the γ coefficient slightly increases in very weak inversion due to body effect.

Modeling flicker noise, on the other hand, is a tough task because its PSD can span over multiple orders of magnitude depending on the transistor bias, its dimensions and the frequency [29], [30]. While the flicker noise can be modeled accurately with physical equations, this work proposes to represent it with quantities easily available to the analog designer. In [30] it is shown that the flicker noise of a MOSFET can be modeled as a voltage source at its gate with a PSD given by

$$S_{v_g}(f) = \frac{\alpha}{(WL)f^{1+\xi}}, \tag{5}$$

where α and ξ are parameters that generally depend on the transistor flavor, bias conditions, and dimensions. ξ is expected to be close to 0 to approach the $1/f$ behavior. A study similar to what is explained for thermal noise is conducted for flicker noise to estimate the curves for α and ξ. The V_{GS} of the transistor is swept in simulation while the other bias voltages are maintained constant. The flicker noise PSD is then extracted and the α and ξ coefficients are derived from the PSD. Figs. 5(c) and (d) show the dependency of the α coefficient on g_m/I_D, for both considered technology nodes. No significant dependency of α on W and V_{DS} is observed. However, α can decrease by a factor up to 2 when the length L is below 1 µm due to the dependence of the mobility on the channel length, such as described in [31]. These variations could be taken into account in our methodology by using different mappings for the α coefficients, depending on the channel length. However, our designs do not use lengths below 1 µm for the input transistors of high-precision amplifiers, unless in case of strict area constraints. Simulations show that the flicker noise coefficient α decreases as the device goes to weak inversion, which is confirmed by [29]. At channel lengths above 1 µm, carrier number fluctuations dominate the flicker noise, resulting in lower variations of the α coefficient with g_m/I_D in weak inversion [30], [32]. Fig. 5 also shows that P-channel devices have a higher flicker noise coefficient than N-channel transistors, meaning that at identical dimensions and g_m/I_D, the gate-referred flicker noise at 1 Hz is higher in P-channel transistors for the considered deep submicron technologies. This conclusion is similar to [32], [33]. Finally, the exponent ξ is found to be constant with bias and dimensions and to only depend on the transistor flavor. Its absolute value is lower than 0.2 in all studied cases. It should be noted that the flicker noise modeled as such depends on the accuracy of the foundry models. As those are usually less accurate than thermal noise models, the final results only give an order of magnitude of the flicker noise rather than exact values.

The dependencies of the noise coefficients γ and α, shown in Fig. 5 could be analytically represented by nonlinear models to accurately predict the noise at every possible g_m/I_D value. However, analytical nonlinear curve fitting would complicate the models with highly technology-dependent parameters. Analytical developments and optimizations of low-noise circuits would then become more challenging. Moreover, low-noise amplifiers tend to contain transistors either in weak or strong inversion, avoiding the need for an accurate curve fitting over the whole range of g_m/I_D. Instead, upper and lower bounds can be extracted from Fig. 5 for γ and α and later be used for circuit-level noise modeling.

C. Noise Equivalent Bandwidth

Since there exists a trade-off between current consumption and circuit-level thermal noise immunity, the NEF metric is introduced in [34] and is defined as

$$\mathrm{NEF} = v_{\mathrm{in,RMS}}\sqrt{\frac{I_{\mathrm{tot}}}{4kTV_T f_H \pi/2}}, \tag{6}$$

with $v_{\mathrm{in,RMS}}$ the RMS total IRN of the amplifier expressed in V, I_{tot} the current consumption of the circuit, and f_H the upper frequency limit that is application-dependent. This definition of NEF is equivalent to normalizing the IRN voltage to the thermal noise voltage of an ideal bipolar transistor, with an additional factor 2 in the noise power. However, this definition only holds when first-order low-pass-filtering is assumed at the amplifier output. The frequencies considered for the computation of $v_{\mathrm{in,RMS}}$ and NEF should be defined in case of band-pass filtering. This section proposes a formalism for the bandwidth to consider in this case. Also, as the definition of the NEF assumes negligible flicker noise, the general impact of $1/f$ noise on the NEF is discussed.

The ENBW is a commonly used metric applied to describe the bandwidth over which noise must be integrated to obtain the noise power. Fig. 6(a) represents this ENBW in the case of an amplifier with an in-band gain A_v and an output white noise PSD N_W, expressed in V/V and V^2/Hz, respectively. To compute the NEF, a first-order low-pass filter (LPF) with a cut-off frequency f_H is assumed at the amplifier output [11]. This virtual filter emulates the behavior of the subsequent elements in the signal chain. The intrinsic low-pass filtering of the amplifier is neglected in comparison with the virtual LPF at the output. Equation (7) computes f_{high}, the cut-off frequency of the rectangular filter whose integrated output power is equivalent to the noise power at the output of the virtual LPF:

$$f_{\mathrm{high}} = \frac{1}{N_W}\int_0^\infty N_W \frac{1}{1+(f/f_H)^2} df = \frac{\pi}{2} f_H, \tag{7}$$

which is a well-known result for first-order low-pass filtering and thermal noise only. The input-referred noise power $\overline{v_{in}^2}$ is then computed by integrating the IRN PSD from 0 to f_{high}, hence the $(\pi/2)f_H$ expression in (6).

When $1/f$ noise and input high-pass filtering are added to the signal chain, the above analysis is no longer sufficient to describe the IRN, such as shown in Fig. 6(b). To describe how noise affects the signal in its useful bandwidth, the authors propose to assume a first-order band-pass filter at the amplifier output, with cut-off frequencies $[f_L; f_H]$ where f_L is the cut-off frequency of the input HPF, determined by the signal bandwidth limits. The noise PSD at the output of this virtual filter becomes

$$\mathrm{PSD}_{\mathrm{filt}}(f) = N_W\left(1+\frac{f_c}{f}\right)\frac{1}{1+(f/f_H)^2}\frac{(f/f_L)^2}{1+(f/f_L)^2}, \tag{8}$$

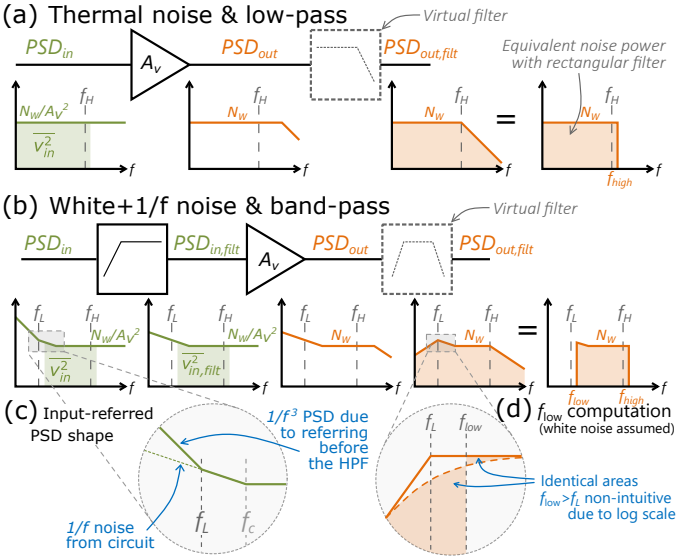

Fig. 6. Representation of the noise asymptotic PSDs and bandwidths (a) with white noise and low-pass filtering at f_H only, and (b) when adding $1/f$ noise and input high-pass filtering at f_L. A white noise PSD of value W is assumed at the amplifier output, as well as an in-band gain of A_v. Green-filled areas indicate the integrals to evaluate the input-referred noise power. (c) and (d) provide details on the shape of the IRN PSD at low frequency and on the computation of f_{low}, respectively.

where f_c is the noise corner frequency at which the thermal and flicker noise PSDs are equal. Assuming $f_H \gg f_L$, the integral of this PSD from $f = 0$ to $f = +\infty$ is equivalent to the integral of the noise PSD at the output of the amplifier from f_{low} to f_{high}, where

$$f_{\text{low}} = \frac{\pi}{2} f_L; \qquad f_{\text{high}} = \frac{\pi}{2} f_H. \tag{9}$$

The expression for f_{low} can be visualized with a non-asymptotic PSD such as in Fig. 6(d), which shows that f_{low} is higher than f_L due to the attenuation in the signal band beyond f_L. In this figure, it is shown for white noise but the same principle holds when adding $1/f$ noise. The input-referred noise power can then be computed by integrating the input-referred PSD over the $[f_{\text{low}}; f_{\text{high}}]$ bandwidth. This work proposes to extend the definition of the NEF to the case of a BPF with the following expression:

$$\text{NEF} \triangleq v_{\text{in,RMS}} \sqrt{\frac{I_{\text{tot}}}{4kTV_T\text{ENBW}}}, \tag{10}$$

where the ENBW is defined with

$$\text{ENBW} \triangleq f_{\text{high}} - f_{\text{low}}, \tag{11}$$

in the case of band-pass filtering. The definition of NEF in (10) will be used in the rest of this paper.

With these analytical tools developed, it is possible to describe how $1/f$ noise affects the total noise power and the NEF. Fig. 7 shows the impact of $1/f$ noise with a sweep on the noise corner frequency f_c at constant thermal noise level. The ratio of $1/f$ noise power over total noise power is shown in Fig. 7(a) and the impact on the NEF can be seen in Fig. 7(b). Three conclusions can be drawn from these graphs. First, the impact of $1/f$ noise is strongly dependent on the useful signal bandwidth. Then, even if f_c is below the signal bandwidth, $1/f$ noise can be non-negligible. Finally, if f_c lies in the signal bandwidth, the NEF is quickly degraded. These conclusions highlight the need to push the noise corner frequency f_c below the signal bandwidth by minimizing the $1/f$ noise, emphasizing the importance of a quantification of the noise-area trade-off.

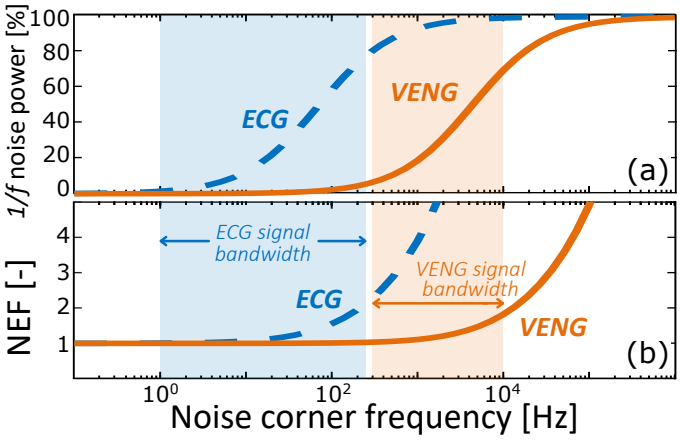

Fig. 7. Impact of $1/f$ noise on (a) the $1/f$ IRN power normalized to the total IRN power, and (b) the resulting NEF. The NEF is supposed to be equal to 1 when no $1/f$ noise is added. Curves for applications with different bandwidths (ECG and VENG) are shown, with shaded areas corresponding to the respective application bandwidths.

IV. Validation on a Current-Reuse Amplifier

This section presents the application of the proposed methodology to a low-noise current-reuse amplifier. Based on the analytical formulation, we obtain the optimal biasing for the circuit leading to the lowest possible NEF that can be reached with this topology. Then, different simulation-based optimizations are performed on the amplifier to compare the analytical results with the simulated Pareto front. The thermal noise derivation is first presented and the results are compared with a numerical optimization with unlimited area. Then, the flicker noise is computed analytically and the results are compared with simulation-based optimizations with different area constraints, highlighting the noise-area trade-off. Finally, the area requirements for low thermal noise are discussed.

A. Amplifier Topology

Among the architectures reaching the lowest NEFs, the principle of CR is often employed [6], [9]. The idea is to duplicate the input voltage to the gate of two differential pairs, doubling the total transconductance of the input branch. If both pairs share the same DC current, this bias current is *used* twice, hence the name of the technique.

Fig. 8 shows a fully differential amplifier implementing current reuse. The differential input voltage is applied on the gates of $\text{N}_\text{L}/\text{N}_\text{R}$ and $\text{P}_\text{L}/\text{P}_\text{R}$ transistors, increasing the total transconductance G_m. Without the $\text{R}_\text{OL}/\text{R}_\text{OR}$ resistors, the gain is given by

$$A_v = G_m R_{\text{out}} = \frac{g_{mN} + g_{mP}}{g_{dN} + g_{dP}}. \tag{12}$$

The CR technique thus approximately doubles the transconductance, but also decreases the output resistance, leaving

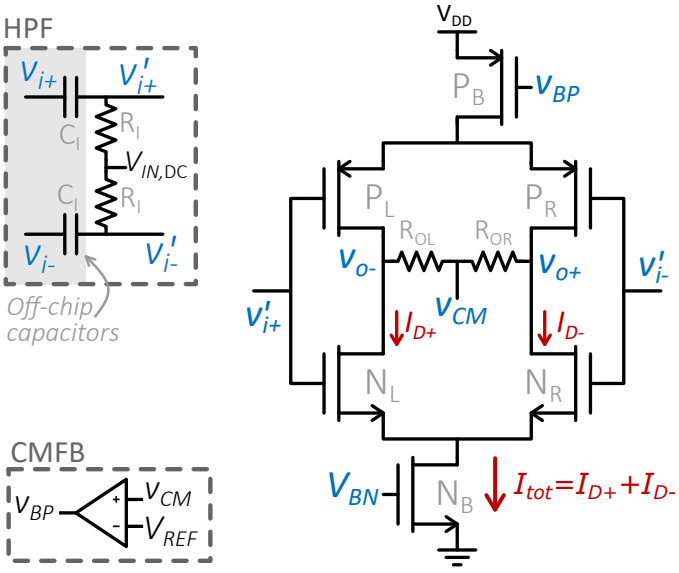

Fig. 8. Schematic of a current-reuse amplifier including an input high-pass filter (HPF) and a common-mode feedback (CMFB) loop. The body terminals of N-channel and P-channel transistors are connected to ground and V_{DD}, respectively.

the voltage gain approximately unchanged compared to architectures with single use of current. However, increasing G_m affects the noise transfer function. Considering a drain current constant noise PSD of S_i for N and P transistors, the input-referred voltage noise PSD $S_{\mathrm{v_{in}}}$ in the amplifier bandwidth becomes

$$S_{\mathrm{v_{in}}} = 2\frac{S_{i,N}+S_{i,P}}{(g_{mN}+g_{mP})^2}. \tag{13}$$

The IRN PSD is thus approximately divided by two compared to conventional topologies with a single differential pair.

Coming back to the schematic of the amplifier in Fig. 8, transistors $\mathrm{N_B}$ and $\mathrm{P_B}$ are used as matched current sources. A common-mode feedback (CMFB) regulates the common-mode output voltage by acting on the gate of $\mathrm{P_B}$. $\mathrm{R_O}$ resistors are used to sense the output voltage, which is compared to a DC reference voltage V_{REF}, set to $V_{\mathrm{DD}}/2$. The difference is amplified by a single-stage operational transconductance amplifier (OTA). The $\mathrm{R_O}$ resistors added for the CMFB loop decrease the output resistance and thus the voltage gain. With R_O in the MΩ range or lower, the in-band gain is given by

$$A_v = \frac{g_{mN}+g_{mP}}{g_{dN}+g_{dP}+1/R_O} \approx R_O\left(g_{mN}+g_{mP}\right). \tag{14}$$

Large resistors can be implemented as such in the amplifier thanks to high-density resistors, benefiting from higher linearity than MOSFET-based pseudo-resistors. Moreover, an input HPF is added to the inputs of the CR amplifier. It is composed of resistors $\mathrm{R_I}$ and off-chip capacitors $\mathrm{C_I}$. The voltage $V_{\mathrm{IN,DC}}$ allows to set the input DC voltage. For all studied cases, a capacitance $C_I = 30$ nF is assumed in this work. The presence of off-chip capacitors in the nF range is not critical as the total system volume is dominated by bulky electrodes for signal sensing, whose volume is in the $\mathrm{mm^3}$ range [35]. This presented topology can be used in a wide range of applications thanks to the easy tuning of bandwidth and gain. In addition, the low number of stacked transistors makes it functional at low supply voltage V_{DD}. Finally, no technology-specific techniques (e.g., back biasing in FD-SOI) are used here, making this amplifier easily portable from one CMOS technology to another.

B. Analytical Thermal Noise - Current Trade-Off

As shown in (5), the $1/f$ noise decreases with the transistor channel area. If a large area is allowed for the total amplifier, flicker noise becomes negligible compared to thermal noise. This section only discusses the impact of thermal noise, while the trade-off between flicker noise and gate area will be taken into account in Section IV-D. In the absence of mismatch, the CR amplifier has the following thermal noise sources which impact its noise at the differential output:

- N and P transistors in the left and right branches,
- output resistors $\mathrm{R_O}$,
- input resistors $\mathrm{R_I}$.

The noise from N and P transistors will be detailed first and resistor noise will be added afterwards. If the electrode impedance is not negligible compared to $\mathrm{R_I}$, it should be considered in the small-signal model and its noise should be computed as well. If its value is known, the value of $\mathrm{R_I}$ can be adapted accordingly. However, as the value of the source impedance varies strongly with the application and the type of electrode used, it is not discussed in this study.

Using (4) for the thermal noise of the transistors, the total IRN PSD due to the transistors is the following

$$S_{\mathrm{v_{in,tr}}} = \frac{8kT}{(g_{mN}+g_{mP})^2}\left(\gamma_N g_{mN}+\gamma_P g_{mP}\right). \tag{15}$$

To emphasize the noise-current trade-off, (15) can be rewritten as

$$S_{\mathrm{v_{in,tr}}} = \frac{16kT}{I_{\mathrm{tot}}}\frac{\left(\gamma_N\left(\frac{g_m}{I_D}\right)_N+\gamma_P\left(\frac{g_m}{I_D}\right)_P\right)}{\left(\left(\frac{g_m}{I_D}\right)_N+\left(\frac{g_m}{I_D}\right)_P\right)^2}, \tag{16}$$

where I_{tot} is the total current drawn from the supply (excluding the current needed by the biasing circuit and the CMFB OTA). Equation (16) highlights the necessity to push transistors towards weak inversion, maximizing both g_m/I_D values and minimizing $S_{\mathrm{v_{in,tr}}}$. Assuming that it is possible to reach the maximum g_m/I_D for each transistor, (1) can be substituted into (16). The IRN PSD then becomes

$$S_{\mathrm{v_{in,tr}}} = \frac{4kTV_T}{I_{\mathrm{tot}}}n_{\mathrm{eq}}^2\left(\frac{\gamma_N}{n_N}+\frac{\gamma_P}{n_P}\right), \tag{17}$$

where n_N and n_P are the values of the body factor in weak inversion extracted from $(g_m/I_D)_{\max}$, as explained in Section III-A. n_{eq} is the equivalent body factor for N and P transistors given by

$$n_{\mathrm{eq}} = \frac{2}{1/n_N+1/n_P}. \tag{18}$$

Equation (17) shows that the thermal noise PSD is inversely proportional to the supply current, which highlights the noise-current trade-off in this amplifier. As all parameters are constant except for I_{tot}, (17) provides the theoretical minimum

thermal noise from the N and P transistors for a given bias current and a given technology node.

Next, the IRN PSD due to the output resistors can be computed as

$$S_{\mathrm{v_{in,R_O}}} = \frac{32kT}{\left(\left(\frac{g_m}{I_D}\right)_N + \left(\frac{g_m}{I_D}\right)_P\right)^2} \frac{1}{R_O I_{\mathrm{tot}}^2}. \quad (19)$$

Assuming maximum g_m/I_D for all transistors, (19) becomes

$$S_{\mathrm{v_{in,R_O}}} = \frac{8kTV_T^2 n_{\mathrm{eq}}^2}{R_O I_{\mathrm{tot}}^2}. \quad (20)$$

Finally, the case of $\mathrm{R_I}$ is more complicated as its noise is modulated by the input HPF. The frequency-dependent IRN PSD from the $\mathrm{R_I}$ thermal noise is

$$S_{\mathrm{v_{in,R_I}}}(f) = \frac{8kTR_I}{(2\pi f R_I C_I)^2}. \quad (21)$$

This equation can be seen in different ways. First, if the filter is only used to remove the DC offset from the electrode, its cut-off frequency does not need to be precisely set as long as it is below the signal bandwidth. In that case, (21) becomes

$$S_{\mathrm{v_{in,R_I}}}(f) = \frac{8kT}{(2\pi f C_I)^2 R_I}. \quad (22)$$

This equation shows that R_I must be maximized to minimize the noise. As a consequence, MOS pseudo-resistors are often used to reach up to the GΩ or TΩ range. In these conditions, on-chip capacitors in the pF range can be used to implement $\mathrm{C_I}$ while keeping a low level of noise from $\mathrm{R_I}$.

However, if the filter cut-off frequency f_L needs an accurate value to filter out interference and to precisely set the signal bandwidth, these conclusions do not hold. Indeed, the cut-frequency then sets R_I and C_I with

$$R_I C_I = 1/(2\pi f_L). \quad (23)$$

As a result, the IRN PSD from $\mathrm{R_I}$ becomes

$$S_{\mathrm{v_{in,R_I}}}(f) = \frac{8kTf_L}{2\pi C_I f^2}. \quad (24)$$

In this case, C_I is the only degree of freedom that can be used to minimize the noise from $\mathrm{R_I}$. Consequently, using on-chip capacitors in the pF range might result in designs where the IRN is dominated by the noise from the high-pass filter. Off-chip capacitors in the nF range are then preferred. This latter case will be considered in the rest of this work.

To easily combine this noise PSD with the other ones without important loss of accuracy, the average PSD over the frequency of interest is used. The considered integration bounds are given by (9). The average IRN PSD for $\mathrm{R_I}$ can be expressed as

$$S_{\mathrm{v_{in,R_I,avg}}} = \frac{16kT}{\pi^3 C_I f_H}. \quad (25)$$

The total IRN PSD $S_{\mathrm{v_{in,tot}}}$ of the CR amplifier can then be obtained by summing the results from (17), (20) and (25). The NEF is computed as

$$\mathrm{NEF} = \sqrt{S_{\mathrm{v_{in,tot}}} \frac{I_{\mathrm{tot}}}{4kTV_T}}, \quad (26)$$

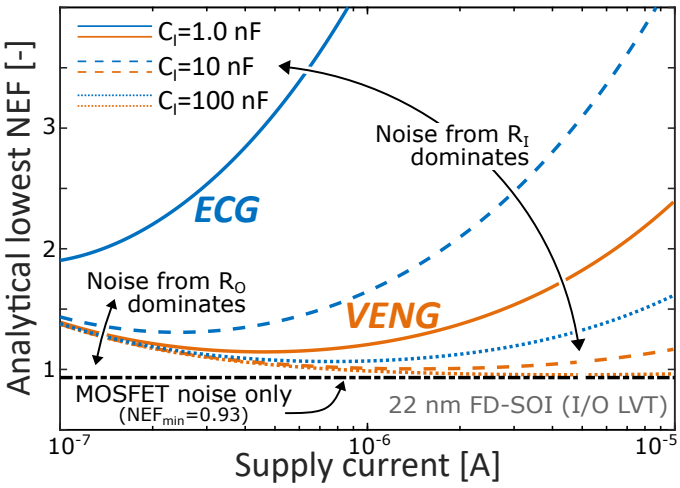

Fig. 9. Analytical optimal NEF that can be reached with the CR amplifier with I/O LVT transistors in 22-nm FD-SOI considering thermal noise only and $R_O = 1$ MΩ. The variations of the NEF due to input and output resistors can be observed. The value of C_I is swept to show the impact of the design of the input HPF. ECG and VENG applications are considered with their different respective bandwidths shown in Table I.

which corresponds to (10) when $\mathrm{S_{v_{in,tot}}}$ is constant in the whole ENBW. Fig. 9 shows the analytical NEF as a function of the supply current for different values of $\mathrm{C_I}$, assuming $\mathrm{R_O} = 1$ MΩ. When considering only MOSFET thermal noise, the NEF is constant. For the technology-dependent parameters, weak-inversion I/O LVT transistors in 22-nm technology are selected and their γ values are extracted at $(g_m/I_D)_{\max}$. At low current, the noise from the output resistor becomes large. At high current, it is the noise from $\mathrm{R_I}$ that dominates as it does not scale down with I_{tot}, as shown by (25). For each value of $\mathrm{C_I}$, $\mathrm{R_I}$ is higher in the ECG case than for VENG due to the bandwidth difference. As a result, the noise from $\mathrm{R_I}$ is higher in the case of ECG. In the rest of this paper, a capacitance value $\mathrm{C_I} = 30$ nF is assumed for both applications. Even though this value is sub-optimal in the ECG case, selecting 30 nF allows to add to the analysis designs for which the noise is not dominated by MOSFETs. In those designs, the IRN is not necessarily inversely proportional to the current, resulting in non-constant NEF over the considered range of supply current. However, in designs targeting a minimization of the NEF, the value of $\mathrm{C_I}$ should be optimized taking into account its impact on the HPF noise.

C. Simulation-Based Optimization

To challenge the analytical noise results of the CR amplifier obtained in Section IV-B, the circuit is implemented in schematic for simulation. The simulator is then integrated in an optimization routine such as the one described in [17]. Table II summarizes the optimization objectives, constraints and variables. The dimensions of the bias transistors and the design of the feedback OTA are fixed. The bias transistors and the feedback OTA respectively occupy 30 µm^2 and 25 µm^2 of gate area and the OTA draws 50 nA from the supply. The total area is not constrained in this study but will be the subject of further discussion in Section IV-D. In 65 nm, V_{DD} is set to 1.2 V and LVT core transistors are used, while V_{DD} is equal

TABLE II
OPTIMIZATION OBJECTIVES, CONSTRAINTS AND VARIABLES

Objective	**Direction**
Supply Current	min.
RMS IRN	min.
Constraint	**Threshold**
In-band gain	$>$ 35 V/V
Lower frequency limit	$<$ 1 Hz (ECG) ; $<$ 300 Hz (VENG)
Upper frequency limit	$>$ 250 Hz (ECG) ; $>$ 10 kHz (VENG)
Variable	**Bounds**
Bias current	[0.1 - 10] µA
R_O value	[0.1 - 10] MΩ
NMOS width W_N	[1.0 - 900] µm
NMOS length L_N	[0.1 - 20] µm
PMOS width W_P	[1.0 - 900] µm
PMOS length L_P	[0.1 - 20] µm

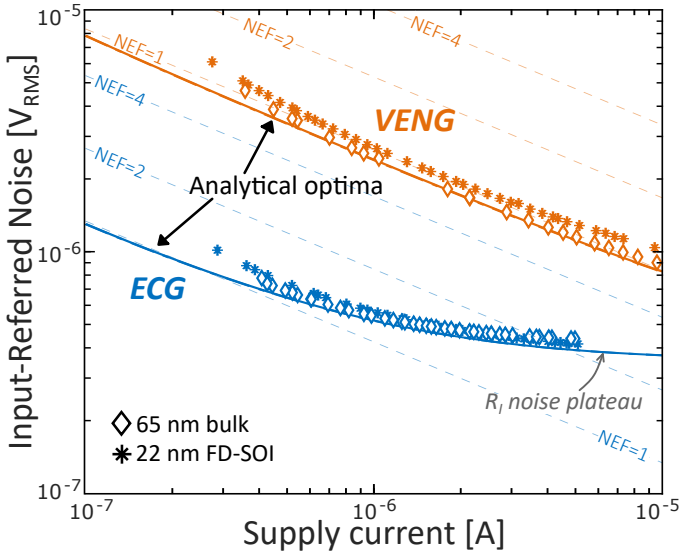

Fig. 10. Optimization results for the CR amplifier without any constraint on the area. Analytical optima are shown as solid curves. The scatter plots indicate the simulation-based Pareto fronts. ECG (blue) and VENG (orange) applications are optimized in 65-nm bulk (diamond) and 22-nm FD-SOI (star). Iso-NEF lines are indicated with light dashes. Flicker noise is included in simulation but not analytically. It is minimized thanks to unconstrained area.

to 1.8 V for the LVT I/O transistors in 22 nm. LVT devices are chosen for lower thermal noise, as indicated in Fig. 5. As the IRN is not directly related to V_{DD}, the difference in the supply voltage does not have an impact on the overall results to first order. To test all the objectives and constraints, DC, AC and NOISE AC simulations are performed, in this order. At the end of each simulation, potential sizings that fail to respect the constraints are discarded to save computation time, as explained in [17]. After DC simulations, sizings for which the transistors are not saturated are also rejected. To further speed up the optimization process, insights from the analytical design can be used to reduce the search space of the optimization algorithm. For instance, as weak inversion is targeted for the transistors, their aspect ratio W/L must be maintained high.

Fig. 10 presents the optimization results for both ECG and VENG applications, in 65 nm and 22 nm. Analytical optima are highlighted for comparison. For each application, the analytical optimum is almost the same in both considered technology nodes, such that they cannot be distinguished in the figure. While the choice of technology node significantly impacts the speed, power and area performance of the digital back end, the noise-current trade-off of the AFE only presents marginal differences between the two studied nodes. Iso-NEF curves, added for comparison, differ from one application to another as those curves are bandwidth-dependent. In the ECG case, as the HPF resistance has a larger value than in the VENG case, the noise from $\mathrm{R_I}$ is more significant. As a result, at high current, the Pareto front cannot follow an iso-NEF curve, such as anticipated analytically in Fig. 9. In Fig. 10, the optimization results tend to saturate at a fixed noise value as the current increases. In the VENG case, this effect is less significant than for ECG as R_I is lower.

Yet, some differences still exist between the analytical optima and the Pareto front. Fig. 11 shows the g_m/I_D of transistors $\mathrm{N_L/N_R}$ and $\mathrm{P_L/P_R}$ in the Pareto-optimal designs for the VENG application in 22 nm. It can first be seen that all designs have $(g_m/I_D) > 20$ for both transistors, meaning that N and P devices are biased in weak inversion, such as predicted analytically from (16). Second, Fig. 11 shows that g_m/I_D decreases as the supply current increases. This can be explained through Fig. 4, which shows that maintaining a constant g_m/I_D level can only be done at constant $I_D/(W/L)$. When the supply current increases, so does the drain current I_D of all transistors. To maintain $(g_m/I_D) \approx (g_m/I_D)_{\max}$, the aspect ratio W/L should increase by the same amount as I_D. As the transistor dimensions are limited during the optimization by the variable bounds and by the bandwidth constraints, W/L is actually bounded. Consequently, g_m/I_D decreases. Among all designs on the Pareto fronts, the channel length is always above 2.6 µm, resulting in widths between 150 and 900 µm.

Several conclusions can be drawn from this simulation-based optimization and its comparison with analytical optima. First, the analytical models developed above allow the accurate prediction of the optimal noise-current trade-offs of the CR amplifier topology. Transposing this analytical study to other topologies could be used to quickly estimate the optimal NEF that can be reached in a certain application, without requiring heavy implementations of simulation-based optimizations. Next, the technology-dependent parameters used in the analytical design have a marginal influence on the overall estimations. Small errors on the value of the thermal noise coefficient are thus not critical for the overall noise estimation, such that raw estimations of γ can lead to accurate results. Finally, as the analytical models are shown to be accurate, analytical insights can be used to limit the search space of an optimization process if one is implemented. For instance, in the case of the CR amplifier, the W/L ratio of N and P transistors can initially be limited to very high values to reach the weak inversion.

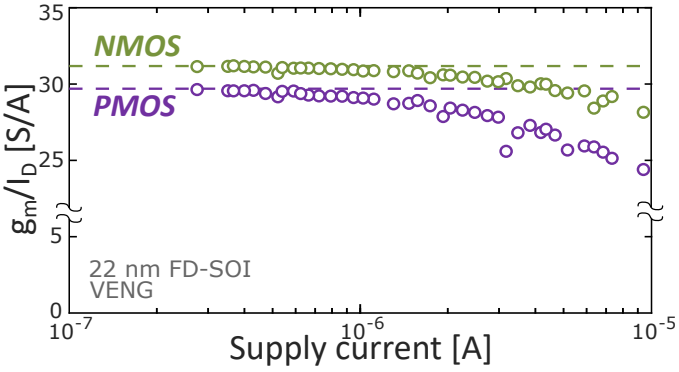

Fig. 11. g_m/I_D values for N (green) and P (purple) I/O transistors in 22-nm FD-SOI. Maximum g_m/I_D obtained from simulations of single transistors (dashed lines) and Pareto-optimal designs (circles) for the VENG application obtained from the optimization summarized in Fig. 10.

D. Analytical Noise - Area Trade-Off

In Section IV-B and in Fig. 10, the flicker noise was neglected in the analytical models and was limited to very low values in simulation thanks to unconstrained amplifier area. As a result, the total gate area reached up to 70,000 µm^2 in 22 nm for a VENG bandwidth. However, in a real application, the chip area is not unlimited. For instance, [10] implements a whole VENG AFE in a silicon area of 77,000 µm^2, the input LNA taking about 25,000 µm^2 in a 22-nm FD-SOI technology. An ECG amplifier presented in [6] and implemented by stacking three CR amplifiers occupies a silicon area of 180,000 µm^2 in 0.18 µm CMOS. Finally, a configurable input amplifier for ECG monitoring presented in [17] has an area of 55,000 µm^2. While no area-based comparison can be made between the gate area extracted from our simulations and the silicon areas reported in these works, it shows that the total area is often constrained. For cost reasons and to obtain an estimation of the area taken by analog parts early in the design phase, it is therefore necessary to study the importance of flicker noise as a function of the available area and to include this analysis to the present work. This section first derives an analytical model for the flicker IRN of the CR amplifier. This analytical model is then compared to simulation-based optimization results for different area constraints. Finally, the area required to keep the transistors in weak inversion is also discussed.

The flicker noise from the bias transistors and from the feedback OTA are considered to be only common-mode signals rejected by the differential output. The flicker noise IRN PSD from the main N and P transistors is computed with (5):

$$S_{\mathrm{v_{in,fl}}}(f) = \frac{\left(\frac{g_m}{I_D}\right)_N^2 \frac{\alpha_N/f^{1+\xi_N}}{(W_N L_N)} + \left(\frac{g_m}{I_D}\right)_P^2 \frac{\alpha_P/f^{1+\xi_P}}{(W_P L_P)}}{\frac{1}{2}\left(\left(\frac{g_m}{I_D}\right)_N + \left(\frac{g_m}{I_D}\right)_P\right)^2}. \quad (27)$$

To first order, no absolute g_m/I_D design choice can be made from (27) to minimize the flicker noise. However, the α parameters are lower in weak inversion and the low thermal noise design from (16) as well as the optimization results in Fig. 11 indicate that high g_m/I_D values are preferred. As a consequence, it is assumed that N and P transistors are biased in weak inversion. Equation (27) can thus be rewritten assuming $(g_m/I_D) = (g_m/I_D)_{\max} = 1/(nV_T)$:

$$S_{\mathrm{v_{in,fl}}}(f) = \frac{n_{\mathrm{eq}}^2}{2}\left(\frac{\alpha_N}{n_N^2(W_N L_N)f^{1+\xi_N}} + \frac{\alpha_P}{n_P^2(W_P L_P)f^{1+\xi_P}}\right). \quad (28)$$

This expression can be integrated analytically in the $[f_{\mathrm{low}}; f_{\mathrm{high}}]$ bandwidth to obtain the flicker noise power

$$P_{\mathrm{v_{in,fl}}} = \frac{n_{\mathrm{eq}}^2}{2}\left(\frac{\alpha_N/\xi_N}{n_N^2(W_N L_N)}\left(\frac{1}{f_{\mathrm{low}}^{\xi_N}} - \frac{1}{f_{\mathrm{high}}^{\xi_N}}\right) + \frac{\alpha_P/\xi_P}{n_P^2(W_P L_P)}\left(\frac{1}{f_{\mathrm{low}}^{\xi_P}} - \frac{1}{f_{\mathrm{high}}^{\xi_P}}\right)\right). \quad (29)$$

The total gate area (N and P transistors only) is given by

$$A_{\mathrm{NP}} = 2(W_N L_N + W_P L_P). \quad (30)$$

Considering (29) and (30), it is possible to analytically optimize the area allocation between N and P transistors. It gives

$$W_N L_N = \frac{\sqrt{\frac{\beta_N}{\beta_P}}}{1+\sqrt{\frac{\beta_N}{\beta_P}}}\frac{A_{\mathrm{NP}}}{2}; \quad (31)$$

$$W_P L_P = \frac{1}{1+\sqrt{\frac{\beta_N}{\beta_P}}}\frac{A_{\mathrm{NP}}}{2}; \quad (32)$$

with β_N and β_P parameters defined as

$$\beta_{\mathrm{N,P}} = \frac{\alpha_{\mathrm{N,P}}/\xi_{\mathrm{N,P}}}{n_{\mathrm{N,P}}^2}\left(\frac{1}{f_{\mathrm{low}}^{\xi_{\mathrm{N,P}}}} - \frac{1}{f_{\mathrm{high}}^{\xi_{\mathrm{N,P}}}}\right). \quad (33)$$

Finally, the noise power integrated from the PSD becomes

$$P_{\mathrm{v_{in,fl}}} = n_{\mathrm{eq}}^2 \frac{\left(\sqrt{\beta_P}+\sqrt{\beta_N}\right)^2}{A_{\mathrm{NP}}}. \quad (34)$$

From (34), it can be observed that the flicker noise power does not depend on the bias current as long as the N and P transistors remain at constant g_m/I_D values. Thus, contrary to thermal noise, increasing the supply current does not result in a reduction of the IRN. As a consequence, there is no flicker noise-current trade-off but rather a flicker noise-area one. On a noise-current curve, flicker noise can lead to a constant-noise plateau. Equation (34) indicates that the noise value of this plateau is inversely proportional to the available active area.

E. Area-Constrainted Pareto Fronts

The CR amplifier is optimized for the VENG application in 22-nm FD-SOI for different area constraints. The area considered for the optimization is the sum of gate areas of the N_L/N_R and P_L/P_R transistors of the amplifier. Fig. 12 shows the resulting Pareto fronts. The analytical flicker noise plateau is indicated for each area threshold value. Flicker noise plateaus for areas larger than 1,000 µm^2 are not indicated as those are outside of the plot bounds, meaning that the flicker noise is not dominant within the considered range of current values.

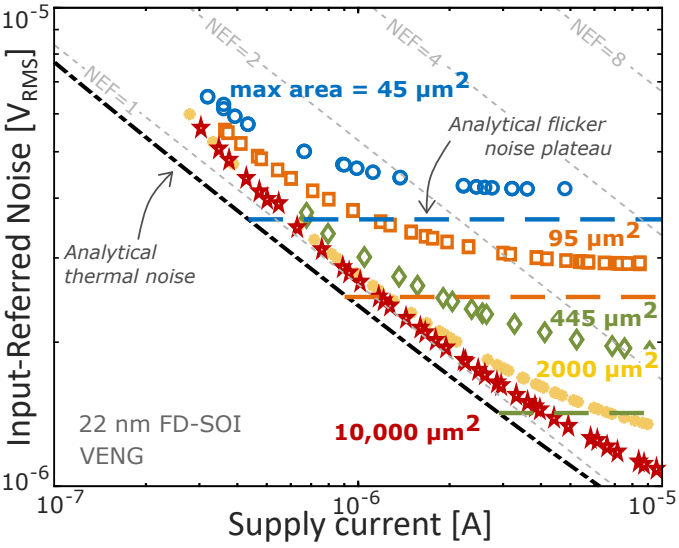

Fig. 12. Pareto fronts resulting from the optimization of the CR amplifier for a VENG bandwidth in 22-nm FD-SOI I/O devices, for different area constraints. The considered area is only the WL product of the four main transistors. Analytical thermal noise (black dashed line) and flicker noise plateau (colored horizontal dashed lines) are indicated for comparison. Iso-NEF curves are added in gray.

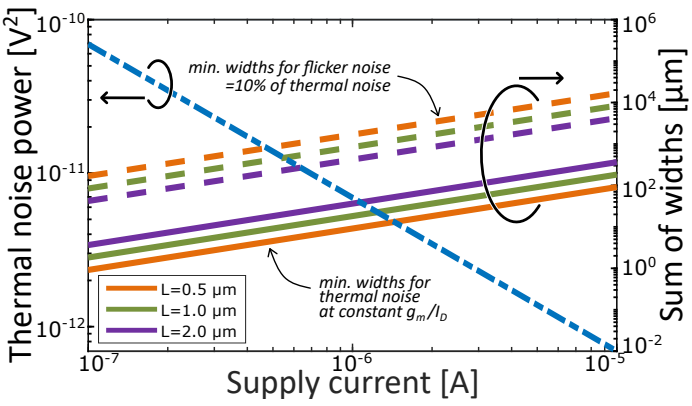

Fig. 13. Analytical evolution of the noise-current-area trade-off for a VENG bandwidth in 22 nm I/O transistors. On the left y-axis (blue dash-dotted line), the evolution of the thermal noise power with the supply current, assuming N and P transistors biased at 80% of their $(g_m/I_D)_{\max}$. On the right y-axis (solid lines), the required sum of widths $W_N + W_P$ to maintain the g_m/I_D values as the current increases, assuming different values of channel length L identical for N and P devices. On the right y-axis (dashed lines), the sum of widths required to reach a flicker noise power ten times lower than the thermal noise power, assuming the same channel lengths.

For the most constrained optimization with a maximum area of 45 µm^2, the optimizer tends to lengths around 0.45 µm and widths from 16 to 30 µm, reaching both good analog performance (not too low length) and weak inversion (high aspect ratio W/L). As the allowed area increases, so do L and W/L.

For the displayed flicker noise plateaus, a comparison between analytical results and simulations can be made. It can be seen that for all cases, the flicker noise plateau obtained in simulation is underestimated by about 30% when computing it analytically. The major sources for those differences are (i) inaccurate modeling of the flicker noise coefficient α, and (ii) limited g_m/I_D of the transistors due to the limited aspect ratio W/L. To reduce that uncertainty, the flicker noise model could be enhanced with g_m/I_D-dependent values of the α coefficient. However, such improvements would require technology-dependent curve fitting and analytical optimizations taking into account thermal and flicker noise combined. These additional layers of complexity are in opposition to our approach that targets simple models. Still, the analytical flicker noise model developed above allows us to determine a lower bound for the flicker noise and its order of magnitude, as function of the available active area. It can also be used the other way around: if a certain level of flicker noise is specified, the required gate area can be computed analytically, giving a first estimate of the minimum area required for the amplifier.

However, beside flicker noise, thermal noise can also be impacted by a reduction in area. As discussed in Section IV-C, maintaining a constant g_m/I_D level (for constant thermal noise-current trade-off) as the current increases can only be done with variations of the aspect ratio W/L, increasing the required gate area. As highlighted from Fig. 4, there exists a plateau in the g_m/I_D curve that allows to sweep the normalized current at almost constant g_m/I_D. But that plateauing trend is not sufficient for the range of currents considered in this work. Fig. 13 analytically quantifies the required area for keeping a constant g_m/I_D. The supply current is swept up to 10 µA with constant g_m/I_D levels for both N and P transistors, fixed at 80% of their maximum g_m/I_D. As the current increases, the thermal noise power decreases as expected but the aspect ratio W/L required for that noise reduction increases to keep the normalized current constant. Fig. 13 shows the corresponding sum of widths $W_N + W_P$ assuming different values of channel lengths. Finally, the figure also shows the sum of widths required to reach a flicker noise power equal to 10% of the thermal noise power, which is a condition to neglect flicker noise compared to thermal noise. Those widths for flicker noise are computed assuming the same channel lengths as for thermal noise. It can be seen that the widths required to minimize the flicker noise are larger than the ones to minimize the thermal noise. It can thus be deduced that, in this case, flicker noise is the bottleneck in the noise-area trade-off. Keeping the flicker noise below 10% of the thermal noise allows to sweep the supply current at almost constant NEF, and to gain robustness against flicker noise modeling inaccuracies. If the area required required to maintain the flicker noise at a negligible level is too large, a chopping structure can also be implemented. In that case, this analytical flicker noise analysis can be used to study the value of the noise corner frequency as a function of the available area and the supply current.

Combining the analytical models for thermal and flicker noise sources developed above can be used to obtain a full model of the noise of an amplifier topology with only a few technology-dependent parameters. The body factor in weak inversion n is required but is often known by the designer. Fig. 10 showcases that the overall noise results only have little dependence on the thermal noise coefficients γ. Finally, the flicker noise model has more variations due to the technology-

dependent and bias-dependent parameter α, but the order of magnitude of the flicker noise plateau can still be obtained from raw estimations of α. As a result, lower and upper bounds of noise coefficients can be used instead of curve fitting of the bias-dependent models. Once the sizing and biasing are found to reach an optimal noise-current-area trade-off, other performance metrics such as gain, matching and common-mode rejection should be evaluated before implementation on silicon.

To generalize the proposed methodology to other amplifier topologies, the IRN PSD must be re-computed analytically. The bias-dependent noise coefficients that are technology-specific can be reused and the noise-current-area trade-off is quickly computed. We have applied the proposed methodology to two published works after reverse-engineering their sizing and bias choices. First, the neural amplifier from [8] results in an analytical NEF of 3.7 according to our methodology, very close to the NEF of 3.8 reported in simulations in the publication. Similarly, applying our methodology to the 65-nm ECG amplifier from [17] gives an NEF of 1.7 compared to the measurement results of 1.93. Finally, the methodology can be applied for circuits used in a wide range of low-noise low-power low-area applications by updating the bandwidth constraints.

V. Conclusion

In this paper, we presented a novel hybrid methodology combining analytical and simulation-based models to quickly estimate the input-referred noise of low-noise and low-current amplifiers. This study takes into account an input high-pass filter, often included in biomedical AFEs, as well as flicker noise and the employed noise models have the benefit of only requiring parameters commonly used by circuit designers. The presented analysis allows us to analytically quantify the noise-current-area trade-off of biomedical amplifiers. When applied to a current-reuse architecture in different application and device flavors, the proposed methodology shows an excellent agreement with simulation-based optimizations. For thermal noise, no significant differences were observed and it was shown that there was only a minor dependence of the results on technology-dependent parameters. Discrepancies up to 30% are observed in the case of flicker noise due to the larger range of variations of the technology-dependent model parameters. The quantified outputs of the methodology can be used to compare amplifier architectures with each other as well as to obtain design insights under the form of required passive components values and g_m/I_D levels. The same methodology can be applied to other topologies, such as stacked structures using current-reuse amplifiers as basic block.

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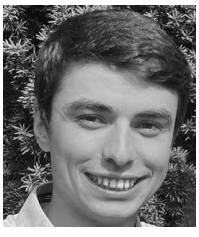

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