A Narrowband RF Front End in 22-nm FD-SOI Featuring a Programmable Low-Noise Amplifier with a Configurable Noise-Power Trade-Off

Marco Gonzalez, Pol Maistriaux, and David Bol
ICTEAM Institute, Université catholique de Louvain, Louvain-la-Neuve, Belgium
Email: {marco.gonzalez, pol.maistriaux, david.bol}@uclouvain.be

***Abstract*—Wireless receivers are usually designed to guarantee a certain performance level in the worst-case operating conditions. However, as these conditions are rarely encountered, the receivers consume more power than necessary to correctly demodulate the incoming signal. This power overhead could be avoided by programmable receivers, which adapt their performance to the conditions of the wireless channel. In this paper, we propose a highly programmable RF front end for narrowband low-power wide-area networks. It trades off a noise figure between 7 and 9 dB for a power consumption between 3.65 and 1.81 mW thanks to a dynamically programmable low-noise amplifier. Integrated into a LoRa receiver, the proposed programmable RF front end can bring up to 46 % of power savings.**

I. Introduction

In the context of the Internet of Things (IoT), where objects are connected to the Internet under very constrained power budgets, low-power wide-area networks (LPWANs) have emerged as solutions for enabling long-range communication between these objects. Even in an LPWAN, wireless communication remains the main contributor to the instantaneous power consumption of the object and among the greatest contributors to its average power consumption. Taking the example of LoRaWAN, one of the LPWAN protocols employing the proprietary LoRa physical layer, the RF transceiver of a class-A device can consume more than 90 % of the instantaneous power consumption and almost 50 % of the average power consumption, assuming the device transmits one 16-byte packet per hour with the highest spreading factor (SF), i.e., SF12 [1]. In LoRaWAN, class-A devices have only two short receive windows for downlink messages scheduled after an uplink packet is transmitted [2], resulting in a high link asymmetry. The contribution of the receiver to the average power in class-B and C devices, which are respectively in receive mode periodically and continuously, can thus increase significantly. These devices are however key to enable downlink capabilities, which could then be leveraged by mesh networks capable of reaching much larger areas.

The high power consumption of the RF transceiver is linked to the high attenuation incurred in communicating through a wireless channel. In the case of the receiver, it must be able to demodulate the incoming low-power signal, targeting sensitivities for LoRa below −120 dBm to reach ranges between hundreds of meters to a few kilometers. Several impairments in the wireless channel can make this task more difficult as they can introduce a stochastic variation of the channel attenuation due to shadowing from obstacles, or dynamic interferences due to the presence or absence of blockers. Because of these stochastic behaviors, receivers are usually designed to guarantee a certain performance, e.g., a packet error rate (PER) of 1 % in the case of LoRa, in the worst-case channel conditions. However, these worst-case conditions are only encountered on rare occasions. In a forest environment, for example, the channel attenuation strongly depends on the season, as depicted in Fig. 1. The presence of foliage on trees could add as much as 5 dB of attenuation [3]. Even during the same season, the channel attenuation still changes significantly due to the other impairments. Therefore, designing a receiver for operation in the rarely present worst-case conditions results in a power penalty because the analog performance of the RF front end such as noise, linearity, and interference immunity must be at their best continuously.

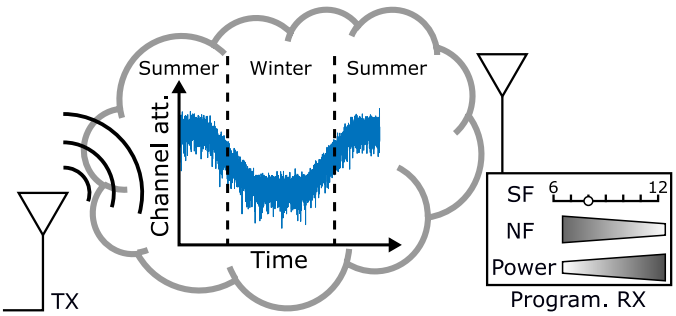

Fig. 1. Wireless channel conditions in a forest environment through the seasons. A programmable receiver (RX) is proposed to adapt to such conditions and avoid power overheads.

This power penalty can be avoided if the receiver adapts its performance to the conditions of the wireless channel, as shown in Fig. 1. An already standard adaptive scheme in wireless communications consists in changing the modulation complexity of the signal to be more energy-efficient when good channel conditions are experienced [5]. LoRa includes such adaptability in the form of the SF, which determines the number of bits sent per symbol, as well as the duration of this symbol. A small SF results in a short symbol which needs a high signal-to-noise ratio (SNR) to be demodulated correctly.

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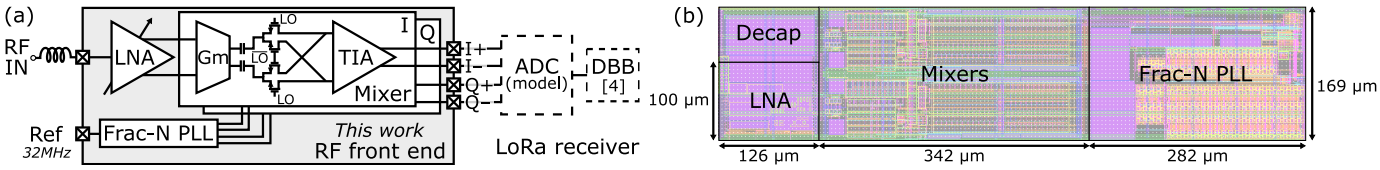

Fig. 2. (a) Schematic, and (b) layout of the proposed programmable RF front end. Models for the power consumption of the ADCs and the digital baseband (DBB) processor from [4] were used to approximate the power consumption of a complete LoRa receiver.

As the SF is incremented, the required SNR is reduced by 2.5 dB [6], but the data rate decreases. By tuning the SF as a function of the received signal power, the transmitted packet energy can be adapted to the channel conditions. However, the power consumption of the receiver remains unchanged, which is especially problematic for devices relying heavily on the receive mode, e.g., class B and C devices. Significant energy savings can only be obtained by reducing this power consumption [7]. Programmable receivers can result in instantaneous power savings of a factor 2× compared to static designs [8], or in average power savings of 30 to 75 % in the case of wake-up receivers [9], i.e., low-power receivers used in channel-sensing mode. With this goal, several programmable receivers or sub-blocks have been proposed, but they have either a power consumption in the tens of milliwatts that is prohibitive for IoT nodes using LPWANs [8], [10], [11], or a limited tuning range of only a few modes of operation [12]. In this paper, we propose a low-power and highly programmable RF front end leveraging the noise-power trade-off of its low-noise amplifier (LNA). This RF front end can be used for the physical layer of several narrowband LPWAN technologies, e.g., NB-IoT, SigFox, and LoRa, and we use the latter to highlight the benefits of the proposed front end with respect to the system-level performance.

The paper is organized as follows. Section II presents the general architecture of the RF front end and its high-level performance. Section III presents the design, optimization, and simulation results of the low-noise amplifier, the main contributor to the programmability of the system. Finally, conclusions are presented in Section IV.

II. Proposed Programmable RF Front End

The schematic and layout of the proposed programmable direct-conversion RF front end are shown in Fig. 2(a) and Fig. 2(b), respectively. It is implemented in GlobalFoundries 22-nm fully depleted silicon-on-insulator (FD-SOI) technology and supplied at 0.8 V. It features a programmable balun noise-canceling LNA, whose noise-power trade-off can be configured dynamically. It also includes a fractional-N phase-locked loop (PLL) consuming 370 µW, and two passive mixers for the in-phase (I) and quadrature (Q) paths. A direct-conversion receiver architecture was chosen because of its simplicity. Band-pass filters are replaced by simpler low-pass filters and there is no need for complex image-rejection filters due to the absence of image frequencies. On the downside, the flicker noise dominates in the band of interest. To mitigate this, a passive current-mode mixer was chosen, and, by AC-coupling the switches, their contribution to the flicker noise

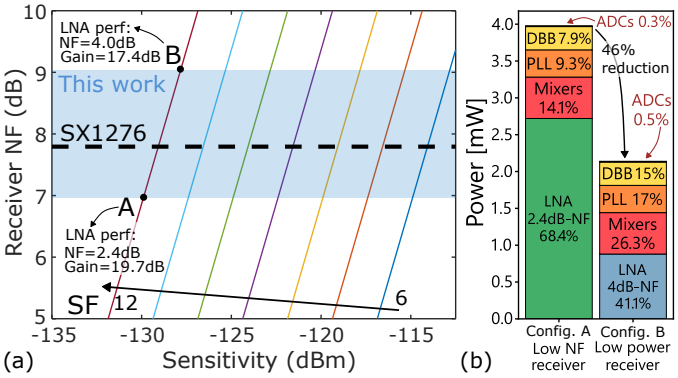

Fig. 3. (a) NF required at the receiver to attain the sensitivity of LoRa as a function of the spreading factor (SF). The dotted line represents the mean NF of the SX1276 chip from Semtech. Two LNA configurations, A and B, are highlighted, exhibiting respectively the best and worst NF. (b) Extrapolated power consumption of a LoRa receiver for configurations A and B of the LNA.

of the system is negligible [13]. Moreover, spread-spectrum techniques, as used in LoRa, perform a despreading operation at the receiver, after which the noise energy is spread over the entire bandwidth [14], thereby limiting the effect of flicker noise on low frequencies. A transconductance stage (Gm) was added to interface the current-mode mixer with the voltage-domain output of the LNA. Finally, a transimpedance amplifier (TIA) converts back the signal into the voltage domain and provides first-order low-pass filtering at 500 kHz, the maximum bandwidth allowed in LoRa [6]. Simulations of the mixer alone give a power consumption of 281 µW, and an integrated double-sideband noise figure (NF) of 24.8 dB, limited by area constraints.

The RF front end is programmable to exploit the trade-off between power consumption and noise, expressed in terms of NF for limiting the power overhead due to varying channel conditions. The LNA usually dominates this trade-off because it is the first block in the chain and its gain reduces the relative impact of the noise added by blocks downstream in the chain. The focus of this work is therefore placed on the programmability of the LNA.

The NF of the receiver directly affects its sensitivity, as it can be calculated using the following expression:

$$\text{Sensitivity} = 10\log(kTB) + NF + SNR_{\text{min}}, \qquad (1)$$

where SNR_{min} is the minimum SNR required to correctly demodulate a LoRa packet at a 1-% error rate, k is Boltzmann's constant, T is the absolute temperature in Kelvin, and B is the bandwidth of the signal of interest. Fig. 3(a) shows the NF required to reach the sensitivity of LoRa at the maximum allowed bandwidth of 500 kHz. The dotted line indicates the mean NF for all SFs of the SX1276 chip [6], one

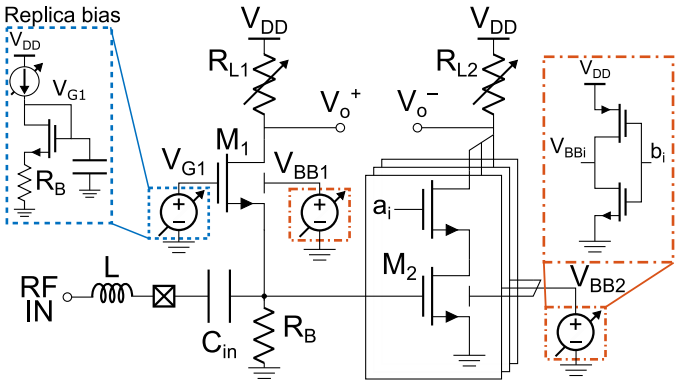

Fig. 4. Schematic of the proposed programmable balun noise-canceling LNA. The M_1 gate voltage is generated by a diode-connected replica, whereas both back-bias voltages are generated by inverters.

of the commercial LoRa transceivers developed by Semtech, the company that owns the LoRa physical layer IP. The NF of the proposed RF front end can be changed dynamically in a range going from point A to point B, saving up to 2× in power consumption. Point A in Fig. 3(a) indicates the design point usually considered for receivers, where the best performance is reached and the signal is correctly demodulated even in the worst-case channel conditions. However, if the SNR of the received signal is, for instance, 2 dB higher (point B), the NF could be degraded by the same amount, thereby maintaining the initial PER and reducing the power consumption at the same time. A non-programmable receiver operating at point A therefore incurs a power overhead for its lower but unnecessary NF, while the SF cannot be decreased yet to benefit from a shorter packet to reduce the TX packet energy.

Overall, the NF of the LNA can be tuned from 2.4 to 4 dB, resulting in a power consumption between 0.88 and 2.72 mW. We can extrapolate this result to estimate the power consumption of a complete LoRa receiver. For the digital baseband (DBB) signal processing, we use the power from [4] which implements a LoRa software-defined radio with an SF of 7 and a bandwidth of 125 kHz. It uses 12-bit I and Q samples acquired at 2 MHz, i.e., with an oversampling factor of 16, and consumes 316 µW. Regarding the analog-to-digital converter (ADC), we use the lower bound of 0.67 fJ/conv−step from [15] obtained empirically, resulting in a power consumption of 10.97 µW for the two required ADCs. Finally, we neglect the power consumption of the analog low-pass filters since they operate in baseband and are not typically a major contributor to the overall power consumption. The resulting power consumption of the detailed receiver for the LNA configuration points A and B are depicted in Fig. 3(b). The entire receiver would consume between 2.14 and 3.98 mW depending on the configuration, resulting in a 46-% power reduction at the expense of a 2-dB sensitivity degradation.

III. Design of the Programmable LNA

A. Architecture

Fig. 4 shows the schematic of the proposed programmable LNA, based on the noise-canceling balun LNA architecture [16]. It is composed of a common-gate branch on the left, which provides the gain on the positive path and the 50-Ω matching to the antenna, and a common-source branch on the right, which provides the gain on the negative path and is designed to cancel out the noise from the common-gate transistor M_1. By combining the LNA and balun functions, we can take full advantage of the suppression of all common-mode signals coming from the use of fully differential blocks, without the insertion losses of a standalone balun needed to interface with single-ended antennas.

A high-Q off-chip inductor offers narrowband input matching. This results in a higher interference immunity, which is important when working on license-free frequency bands as with LoRa. Another advantage of the high-Q inductor is that a relatively low power consumption is needed for input matching and low NF [17].

The programmability of the LNA is implemented through four tuning knobs: the load resistors (R_{L1} and R_{L2}), the gate voltage of transistor M_1, V_{G1}, the width of transistor M_2, and the back-bias voltage of both transistors, a tuning knob enabled by the forward back-biasing of the FD-SOI technology.

A couple of banks of resistors allow tuning the load re-

TABLE I
Ranges of the Optimization Parameters and Performance Constraints Thresholds of the LNA.

Parameter	Range	Constraint	Threshold
R_{L1} & R_{L2} resistance	100 to 1500 Ω	Gain	≥ 15 dB
M_1 gate voltage (V_{G1})	0.3 to 0.8 V	S_{11}	≤ −10 dB
M_2 width	64 to 800 µm	Gain Imb.	≤ 2 dB
M_1 & M_2 back-bias voltage	0 or 0.8 V	Phase Imb.	≤ 10°

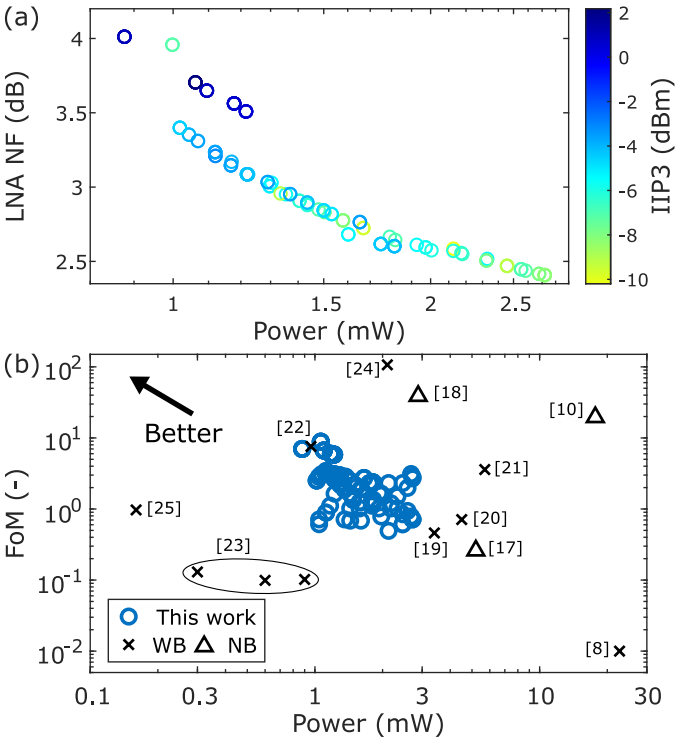

Fig. 5. (a) LNA Pareto front resulting from a genetic optimization based on post-layout simulations. (b) Comparison to state-of-the-art narrowband (NB) and wideband (WB) LNAs in terms of the figure of merit (FoM) and power consumption.

TABLE II
COMPARISON TO STATE-OF-THE-ART SUB-GHZ NARROWBAND LNAS AND SUB-12-GHZ WIDEBAND LNAS.

	Narrowband				Wideband									
Publication	**This work**	[17]	[10]	[18]	[19]	[20]	[21]	[22]	[23]			[24]	[25]	[8]
Year	ISCAS 2024	VLSI 2021	JSSC 2015	TMTT 2015	ISSCC 2022	JSSC 2021	TCAS-I 2020	TCAS-I 2018	ISLPED 2017			S3S 2017	JSSC 2016	TCAS-I 2012
Technology	22 nm FD-SOI	0.13 µm bulk	65 nm bulk	0.13 µm bulk	28 nm bulk	28 nm bulk	65 nm bulk	65 nm bulk	28 nm FD-SOI			28 nm FD-SOI	0.13 µm bulk	0.18 µm bulk
Programmable	✓	✗	✓	✗	✗	✗	✗	✗	✓			✗	✗	✓
Supply [V]	0.8	1.2	1.6/1	1.2	1	1	1	1.2	0.6	0.8	1	1	0.4	1.8
Power [mW]	0.88 to 2.72	5.2	15.8 to 20.2	2.88	3.4	4.5	5.7	0.96	0.3	0.6	0.9	2.1	0.16	18 to 39.6
f_c / BW [GHz]	0.868	0.868	0.2 to 1.6	0.9	2.8	4.5	2.1	2.5	5.6	7.5	9.5	11.1	2.5	1.4
Gain [dB]	17.4 to 19.7	14.21	14 to 24	18	19.6	15.2	27.5	21.2	16.8	18.8	21.5	19.2	13	5 to 12.8
NF [dB]	2.4 to 4	0.92	$\geq$ 3.6	1.94	2.7	2.09	2.3	3	7.3	6.7	6.3	2.2	4.5	1.88†
IIP3 [dBm]	−10.2 to 2.2	−12	14.5	9	−8.5	4.62	−2.2	−2		−16		12.1	−12	−28.9 to −10
FoM	0.49 to 8.84	0.26	19.56*	38.9	0.46	0.71	3.59	7.58	0.13	0.10	0.10	106.78	0.97	0.01†
Area [mm²]	0.0126	0.047	0.2	0.099	0.0078	0.03	0.046	0.05		0.0015		0.00091	0.39	1
I/O	Balun	SE	Balun	FD	SE	SE	Balun	FD		SE		Balun	SE	SE

SE: Single-Ended FD: Fully Differential * Estimated from Table III † Performance of non-programmable LNA

sistances. The gate voltage V_{G1} is controlled by modifying the current flowing through a diode-connected replica of transistor M_1 with a simple current digital-to-analog converter. For tuning the width of transistor M_2, we used several parallel branches composed of common-source transistors of varying widths and switches controlled by the digital signals a_i. Finally, the back-bias voltage of both transistors was restricted to only two values for simplicity of implementation. An inverter connects the back gate either to the supply voltage or to ground.

B. Optimization

The design of LNAs is a complex optimization problem due to the trade-offs in terms of power consumption, impedance matching, noise, and linearity that are involved. Given the difficulty of expressing such trade-offs analytically, numerical optimization methods are preferable to solve this optimization problem. We chose the multi-objective optimization methodology from [26], which relies on a genetic algorithm to extract the optimal design parameters in the form of a Pareto front. The methodology is based on the iterative evolution of a population composed of individuals representing different sets of values for the design parameters. On each iteration, only the individuals who respect all the constraints and have the best optimization objectives are kept to create the next generation.

In the case of the LNA, the optimization objectives are the minimization of the power consumption and the NF, and the maximization of the linearity, measured in terms of the input third-order intercept point (IIP3). Four performance constraints were imposed, as shown in Table I. The gain, gain imbalance, and phase imbalance check for a correct DC point and AC response as well as a correct balun behavior, and the S_{11} checks for a correct impedance matching. As described in [26], these constraints were verified in separate SPICE simulations, ordered from the fastest to the most time-consuming. Directly rejecting sets of parameters that violate one of these constraints helps to reduce significantly the total optimization time.

C. Post-Layout Simulation Results

Fig. 5(a) shows the Pareto front for the proposed LNA resulting from the genetic optimization based on post-layout simulations using the parameter ranges shown in Table I. The implemented programmability allows changing the configuration dynamically to any of the points in the Pareto front with a limited area overhead. These results are compared to sub-GHz narrowband and sub-12-GHz wideband LNAs in Table II. The figure of merit (FoM) used to compare objectively the LNA to the state of the art is the following:

$$\text{FoM} = \frac{\text{Gain}\left[\frac{\text{V}}{\text{V}}\right] \times \text{IIP3}\,[\text{mW}]}{(F-1) \times \text{Power}\,[\text{mW}]}, \tag{2}$$

where F is the noise factor, i.e., the NF in linear scale.

As shown in Fig. 5(b), the proposed LNA is comparable to other state-of-the-art designs and is among the best in terms of the trade-off between the FoM and power consumption. Those achieving a better FoM use architectures focused on improving the IIP3, resulting in either an increased power consumption [10] or in complex feedback structures that make the programmability difficult [18], [24]. Compared to other programmable designs [8], [10], [23], the proposed LNA offers at the same time the low power consumption needed for LPWAN, a large tuning range of the main performance metrics, and a FoM on par with the rest of non-programmable LNAs.

IV. CONCLUSIONS

In this work, we present an RF front end for narrowband LPWAN technologies that is programmable so it can be adapted to the conditions of the wireless channel with the goal of limiting the power overhead due to the sizing for the worst-case channel conditions. The programmability stems from the LNA, which achieves an NF between 2.4 and 4 dB for a corresponding power consumption between 2.72 and 0.88 mW. The IIP3 can also be tuned between −10.2 and 2.2 dBm. The complete RF front end consumes between 1.81 and 3.65 mW in post-layout simulations with an integrated double-sideband NF between 7 and 9 dB. By extrapolation with state-of-the-art ADCs and digital demodulator, power consumption savings of 46 % can be achieved at the receiver level at the expense of a 2-dB sensitivity degradation.

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