Solid-State Electronics 125 (2016) 73–81

Contents lists available at ScienceDirect

Solid-State Electronics

journal homepage: www.elsevier.com/locate/sse

FinFET and UTBB for RF SOI communication systems

Jean-Pierre Raskin

Institute of Information and Communication Technologies, Electronics and Applied Mathematics (ICTEAM), Université catholique de Louvain (UCL), Place du Levant, 3, Maxwell Building, bte L5.03.02, B-1348 Louvain-la-Neuve, Belgium

ARTICLE INFO

Article history:
Available online 25 July 2016

The review of this paper was arranged by Jurriaan Schmitz

Keywords:
Silicon-on-Insulator (SOI)
High-resistivity SOI substrate
Trap-rich SOI substrate
FinFET
Ultra Thin Body and BOX (UTBB)
Analog/RF performance
Cutoff frequency
Fringing capacitance
Self-heating
Mutiple gate MOSFET

ABSTRACT

Performance of RF integrated circuit (IC) is directly linked to the analog and high frequency characteristics of the transistors, the quality of the back-end of line process as well as the electromagnetic properties of the substrate. Thanks to the introduction of the trap-rich high-resistivity Silicon-on-Insulator (SOI) substrate on the market, the ICs requirements in term of linearity are fulfilled. Today partially depleted SOI MOSFET is the mainstream technology for RF SOI systems. Future generations of mobile communication systems will require transistors with better high frequency performance at lower power consumption. The advanced MOS transistors in competition are FinFET and Ultra Thin Body and Buried oxide (UTBB) SOI MOSFETs. Both devices have been intensively studied these last years. Most of the reported data concern their digital performance. In this paper, their analog/RF behavior is described and compared. Both show similar characteristics in terms of transconductance, Early voltage, voltage gain, self-heating issue but UTBB outperforms FinFET in terms of cutoff frequencies thanks to their relatively lower fringing parasitic capacitances.

1. Introduction

The Radio Frequency (RF) performance of an integrated circuit will not only depend on the analog and high frequency characteristics of the active devices, i.e. the transistors, but also the quality of the back-end of line process which defines the losses along the interconnection line and the quality factor of the passive elements such as the inductors and tunable capacitors, as well as the electromagnetic properties of the substrate on which the RF integrated circuit (IC) is lying. Fig. 1 schematically represents the three important levels of optimization for a RF IC.

The parasitic resistances (metal lines and vias) and capacitances (dielectric layers) along the interconnection constitute a low-pass filter which drastically limits the operational frequency of ICs [1]. Advanced back-end of line (BEOL) process provides higher number of metal lines, thicker metal layers, low-k dielectric interlayers and denser vias using carbon nanotubes are investigated for diminishing the parasitic resistances between metal layers [2–6].

The substrate losses and crosstalk remain a challenge for designing high-performance ICs in Si-based technologies for RF applications. In 1997, the RF performance of high-resistivity (HR) Silicon-on-Insulator (SOI) substrate material was presented for the first time [7]. The great potential of HR SOI substrate to reduce RF losses as well as the crosstalk in Si-based substrates was demonstrated. Prior to this work, the scientific community considered the Si-based substrate as the limiting and blocking obstacle for working RF ICs. In 2000s, Prof. Raskin's research team made the fundamental discovery that enables the success of RF-SOI on the market today. The root cause of missing RF performance of standard HR SOI was found by demonstrating the existence of a parasitic surface conduction [8–10] below the buried oxide and the way to disable it by introducing traps. In 2005, the possibility of creating HR SOI substrates characterized with an effective resistivity as high as 10 kΩ cm due to the silicon surface modification below the buried oxide (BOX) of a high resistivity SOI substrate was demonstrated [11]. The surface modification consists of the introduction of a high density of defects called traps at the BOX/HR-Si handle substrate. There are several ways to create those traps [11–13] but the grain boundaries in a thin polysilicon layer have been shown as a quite efficient and robust solution. The latest results obtained with the new generation of trap-rich SOI substrates are presented in Section 7.

Today, partially depleted (PD) Silicon-on-Insulator (SOI) with a channel length of 130 nm is the mainstream technology for RF SOI ICs. New generation of mobile communication systems such as 5G require higher cutoff frequency for the system, better linearity and lower power consumption. Moreover the integration of high

E-mail address: jean-pierre.raskin@uclouvain.be

http://dx.doi.org/10.1016/j.sse.2016.07.004
0038-1101/

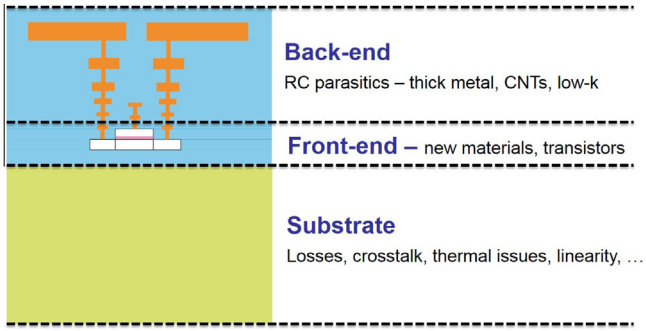

Fig. 1. RF IC quality relies on the back-end and front-end of line processes as well as the substrate electromagnetic properties.

quality passive elements such inductors requires higher number and thicker metal layers. Thus, for getting higher transistor cutoff frequencies and better BEOL, RF SOI must move to shorter nodes. However, further reduction of device dimensions is problematic due to intrinsic physical limitations such as short channel effects, high current leakage through gate dielectrics, high series resistances, low mobility due to interface effects and high doping levels, high current density and thus self-heating and reliability issues, and so on. The most common strategies to address these challenges include the introduction of new materials such as germanium, III-V, high-k gate dielectrics and metal gates, low-k for the back-end dielectrics and gate spacers, SOI technology, strain channel engineering, and alternative device architectures such as multiple gate, i.e. FinFET, planar double-gate, gate-all-around (GAA) nanowires, or tunnel FET, etc.

Fully Depleted (FD) electronic regime is a promising approach to continue scaling of MOSFETs. Scaling the thickness of the silicon body is proposed in the case of FinFET and ultra-thin body and buried oxide (BOX), named as UTBB, technologies in order to control short channel effects (SCE) [14,15]. In order to limit SCE, the channel thickness must be approximately 1/4 and 2/3 of the channel length, respectively, in the case of UTBB and FinFET. Technological aspects, electrostatics, scalability and variability issues in UTBB FD-SOI MOSFETs as well as their perspectives for low power digital applications are widely discussed and shown to be excellent [16–25]. However, lateral coupling of source and drain through the substrate is enhanced in the case of thin-BOX devices. To mitigate this parasitic substrate coupling a highly-doped layer is implanted right underneath the BOX, or so-called Ground Plane (GP), which screens or prevents electric field lines penetration into the substrate. Furthermore, the GP opens a practical way for multi-threshold voltage (V_{th}) and back-gate biasing schemes realization [26].

Good DC figures of merit (FoM) of FinFET and FD planar SOI devices were previously reported in [15,27], respectively. However, analog/RF FoM for both advanced devices have not been widely reported. In this paper, the analog and RF behaviors of FinFET and UTBB are presented and compared. The transconductance, the Early voltage and the voltage gain are presented in Section 3, and the self-heating issue and the cutoff frequencies are described, respectively, in Sections 4 and 5. Finally, the RF performance of standard and trap-rich high-resistivity SOI substrates are compared in Section 7.

2. Experimental devices

UTBB, called also 28 FD-SOI, were fabricated at ST-Microelectronics, Crolles, France, and FinFET at IMEC, Leuven, Belgium.

UTBB presents a BOX, a Si body and an equivalent gate oxide thicknesses of 25 nm, 7 nm and 1.3 nm, respectively. The channel is strained, left undoped and rotated by 45° from the (100) plane. The gate stack is formed by a HfSiON dielectric with the equivalent oxide thickness of 1.3 nm and a TiN electrode. Elevated source-drain structures are employed to reduce parasitic access resistances. The ground-plane implantation introduced under the BOX is well-type. The gate lengths of the measured devices range from 26 nm to 1 μm. More details about the process can be found in [27].

40 nm-long n-channel FinFETs were fabricated on SOI wafers with around 60 nm-thick top Si layer and 145 nm-thick BOX. Fin patterning (resulting in a 60 nm fin height) is followed by gate stack (HfO_2 dielectric + TiN gate) deposition, spacer formation, highly doped drain (HDD) implant, Ni silicidation and Cu Back-End-of-Line (BEOL). The background doping of the silicon fins is 10^{15} cm^{-3}, and no additional fin doping, threshold voltage adjust implants or halo (pocket) implants are used. FinFETs are composed of parallel gate fingers, each finger containing an array of parallel fins in order to design devices with appropriate channel width/length ratios, fin widths varying from 12 to 82 nm, numbers of fins per finger ranging from 5 to 20 and fin spacing between 228 and 528 nm. More details about the FinFET structures and technology can be found in [28–30].

Multi-finger devices are used for both UTBBs and FinFETs and embedded in coplanar waveguide (CPW) access pads for performing on-wafer wideband electrical characterization from a few kHz up to 110 GHz [31].

3. Analog performance

Fig. 2 shows the experimental dependence of Early voltage (V_{EA}) on the fin width (W_{fin}) for 10-μm-long FinFETs at a gate (V_{gs}) and drain (V_{ds}) voltage of 0.5 V and 1.0 V, respectively. In order to be sure that self-heating was not affecting the extraction of V_{EA}, we measured the drain conductance in the 50 kHz–100 MHz frequency range. For large W_{fin}, the devices operate as partially depleted (PD) transistors and the output conductance in saturation can be further deteriorated by the kink effect. As W_{fin} decreases, the devices move toward the FD operation, the kink effect is suppressed, the channel control from the gates is enhanced and, as a result, V_{EA} improves. For the narrowest fins, V_{EA} is strongly increased to values on the order of 100 V/μm of the channel length. According to the literature, such high V_{EA} values have only been experienced in devices operating in volume-inversion (VI), for instance 13 V for 0.2 μm-long FD single-gate (SG) MOSFETs operating in quasi-DG regime [32] or 150 V for 3 μm-long gate-all-around (GAA) DG MOSFETs [33].

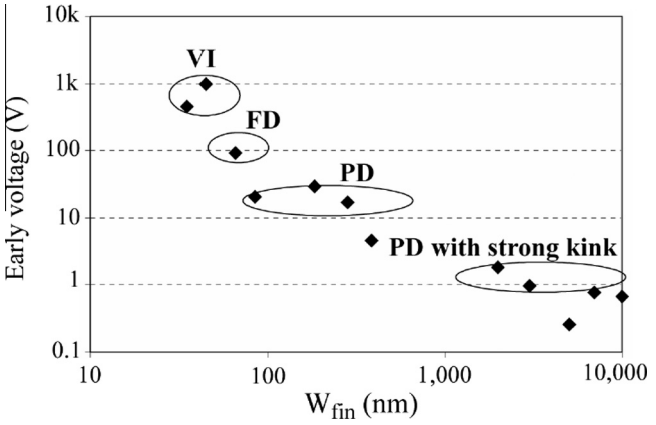

Fig. 2. Early voltage for 10-μm-long FinFETs with different fin widths at V_{gs} = 0.5 V and V_{ds} = 1.0 V [34].

Fig. 3 benchmarks the studied 28 nm node UTBB against other technologies. Selected bias conditions are those that are typically used for analog applications and thus the data for other technologies are available [28,35]. Variation of transconductance g_m with the voltage gain (A_v) is chosen as a figure of merit. The benchmarked technologies include SOI FinFETs [30], planar MOSFETs [30] and UTBB MOSFETs [35]. FD SOI MOSFETs are very close and can even outperform optimized FinFETs particularly if narrow channel devices are used. It would be important to point out that UTBB FD SOI MOSFETs maintain their excellent performance in a wide temperature range, with very limited degradation of main parameters [36]. For instance, only 5 dB reduction of A_{v0} was observed over 200 °C. This makes UTBB FD SOI MOSFETs particularly attractive for high-precision analog circuits. Furthermore, A_v was demonstrated [36] to be maximized in the moderate inversion regime (at $\sim V_{th}$), which is beneficial for low-power applications.

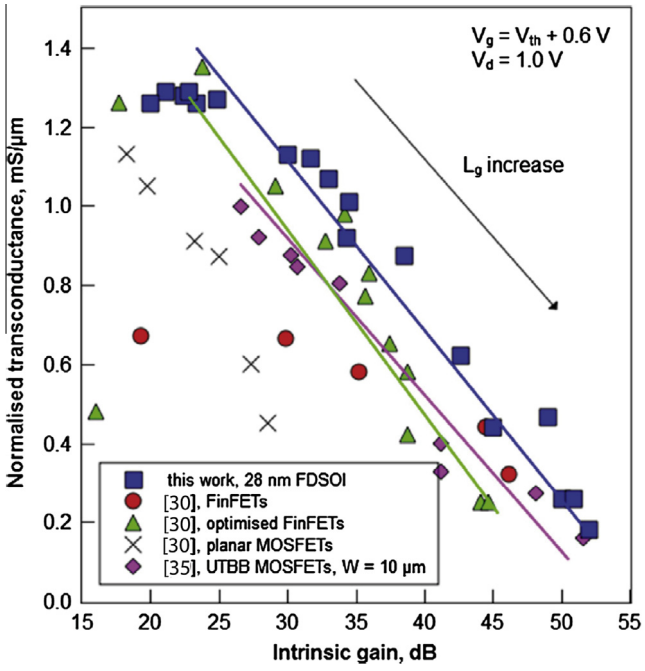

Fig. 3. Transconductance variation as a function of voltage gain for various FD SOI technologies under DC conditions [37].

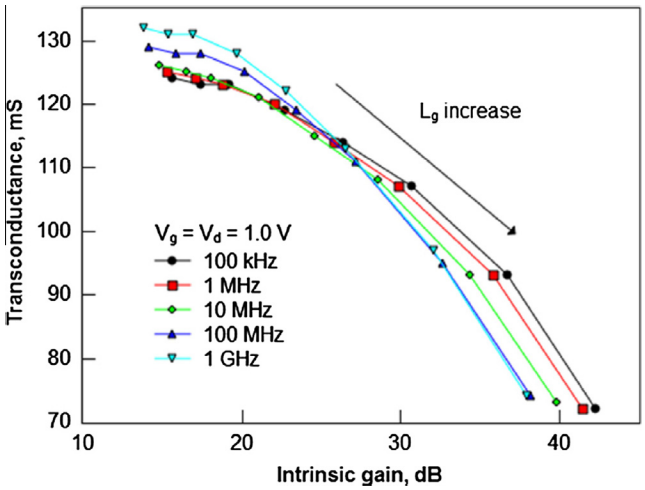

Fig. 4. Variation of g_m with A_v extracted at various frequencies for UTBB at $V_g = V_d = 1$ V [37].

The g_m–A_v analog metric in Fig. 3 is obtained at DC, however, due to frequency dependence of self-heating and substrate effects [36], DC techniques do not provide fair assessment of analog FoM of devices aimed for high frequency operation. Therefore, RF characterization method was used. Fig. 4 shows g_m–A_v in the frequency range from 100 kHz to 1 GHz for UTBB. An increase of g_m and a reduction of A_v with increasing frequency are observed. It is worth noting that the A_v variation with frequency is dominated by strong g_d frequency dependence. Indeed, depending on the gate length, g_d increases by 25–70% due to self-heating and substrate coupling whereas g_m increases only by 1–10%.

Fig. 4 shows the output conductance (g_d) variation in the frequency range from 40 kHz to 4 GHz in devices with various gate lengths at gate (V_g) and drain (V_d) voltage of 1 V. The channel length reduction results in a stronger g_d variation. The increase of g_d in the frequency range up to a few gigahertz in SOI devices can be attributed to self-heating [38,39] and the substrate effect [40].

4. Self-heating issues

Self-heating in semiconductor devices arises because of device scaling which naturally leads to higher current and power densities. Self-heating strongly affects analog device performance. It results in a higher device temperature, which leads to threshold voltage shift [41], mobility reduction, and consequently degradation of the output current. Additionally, self-heating affects the off-current, series resistance, and the carrier saturation velocity [41,42]. It reduces device reliability [43–47], increases electromigration, and introduces a temperature gradient at both, device and chip level, potentially causing timing errors and delayed signals. Due to the finite thermal capacitance of a device, the dynamic self-heating is removed if a device operates above a certain frequency [41]. This frequency can range from a few kHz to few hundreds of MHz, depending on the device geometry. Once the dynamic self-heating is removed, the device temperature does not follow voltage oscillations and the device operates at a constant elevated temperature. The dependence of self-heating on frequency introduces undesirable performance variation with frequency in analog applications, such as the amplifier gain becoming a function of frequency. Quantifying the effect of self-heating is important for device and circuit designers.

Pulsed *I–V* and AC conductance or RF characterization techniques, within the time and the frequency domain, respectively, represent two approaches for evaluating self-heating in solid-state devices. In [38], it was demonstrated that the existing pulsed *I-V* characterization setups do not provide sufficiently short pulses to completely avoid the temperature rise in the channel for advanced MOSFETs. RF thermal characterization is required as the isothermal frequencies of the advanced devices enter the gigahertz region [29,48]. Since the silicon volume of the advanced MOS devices is so much reduced the thermal time constant (of devices today) is in the range of a few tens of ns. Self-heating was then evaluated using the RF extraction method described in [38]. The method relies on proportionality of the thermal resistance to g_d difference at high (isothermal) and low frequencies (Fig. 5).

The temperature rise is a product of the thermal resistance, the drain current and the drain voltage. Fig. 6 presents the temperature rise in the device active region of FinFETs above ambient (fixed at 300 K) for different fin widths. The temperature rise is obtained at a constant power of 50 mW. The temperature rise is smaller in devices with wider fins and a higher number of parallel fins (not shown here) due to the reduced thermal resistance as expected. Fig. 7 shows the variation of average temperature with the gate length (for UTBB) at $V_g = V_d = 1.0$ V. For the same channel length,

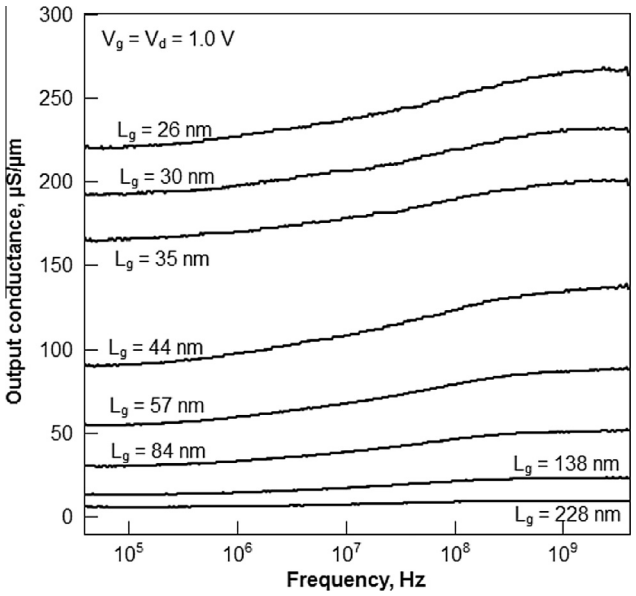

Fig. 5. Output conductance variation with frequency in devices with various gate lengths at $V_g = V_d = 1$ V [37].

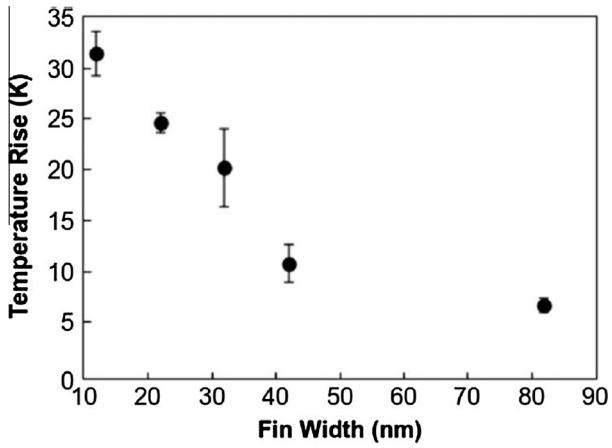

Fig. 6. Temperature rise above ambient in the channel of FinFETs with varying fin widths at constant power (50 mW) [29].

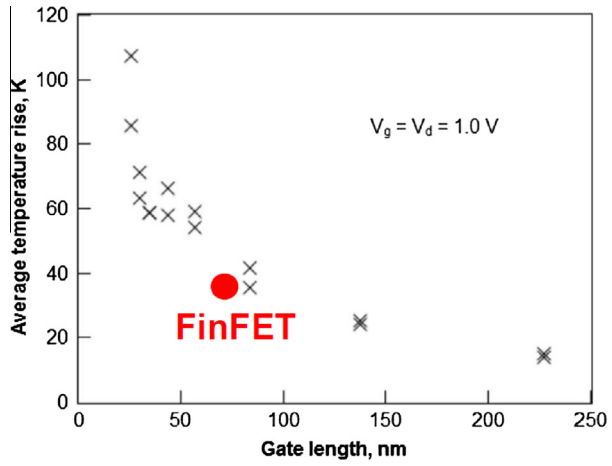

Fig. 7. Average temperature rise due to self-heating in UTBB devices with various gate lengths at $V_g = V_d = 1.0$ V.

UTBB and FinFET present similar self-heating behavior. Both devices are characterized by a quite thin and narrow silicon channel and the main thermal path from the channel is the source and drain contacts to the back-end metallic lines.

5. Cutoff frequency

MOSFET frequency performance is evaluated by two major figures of merit, i.e. the maximum oscillation frequency, f_{max}, and the current gain cutoff frequency, f_T.

Fig. 8 shows the f_T and f_{max} variations versus the channel length L_g for UTBB. Both f_T and f_{max} increase with L_g scaling down but f_T follows a $1/L_g$ trend (and an even weaker one in shortest devices) i.e. attenuated comparing with ideally predicted $1/L_g^2$. This is due to carrier velocity saturation, parasitic source and drain resistances R_s, R_d and extrinsic total gate capacitance C_{gge}. It is important to point out that in case of devices shorter than 90 nm, f_{max} becomes smaller than f_T. This is due to the increase of gate resistance R_g with L_g reduction.

Fig. 9 shows the comparison between the extracted cut-off frequency for FinFETs including the whole parasitic effects (f_{Te}), the cut-off frequency with the extrinsic series resistances removed (f_{TR}) and the intrinsic cut-off frequency, i.e. after withdrawing the parasitic resistances and capacitances (f_{Ti}) as a function of the FinFET channel length. First of all, comparing the current gain cutoff frequency of UTBB (Fig. 8) and FinFET (Fig. 9) of similar channel length we see that UTBB outperforms FinFET by at least 50%. In Fig. 9, we can also observe only a marginal improvement of f_T after the removal of the series resistances for FinFET. On the contrary, after subtracting the total parasitic gate capacitance C_{gge}, intrinsic cut-off frequency reaches nearly 400 GHz for a 60 nm-long FinFET.

Fig. 10 compares the extracted extrinsic and intrinsic total gate capacitances (C_{gge} and C_{ggi}) for the measured L_g-array FinFETs. The capacitances are normalized by the total gate oxide capacitance (C_{ox}). As can be seen, for relatively long channel FinFETs ($L_g = 500$ nm), the extrinsic capacitances are much lower compared with the intrinsic counterparts. However, for short channel devices ($L_g \leqslant 120$ nm) C_{gge} is even greater than C_{ggi}. This effect is more noticeable as the channel length is decreased.

The origin of the additional parasitic capacitance in the case of FinFET (and multiple gate devices in general) is directly related to the metal or polysilicon interconnection between each fin. The parasitic capacitance value depends on the proximity between the gate and S/D electrodes, and it will be more and more important as L_{ext} is comparable or even shorter than S_{fin}. For very short L_{ext},

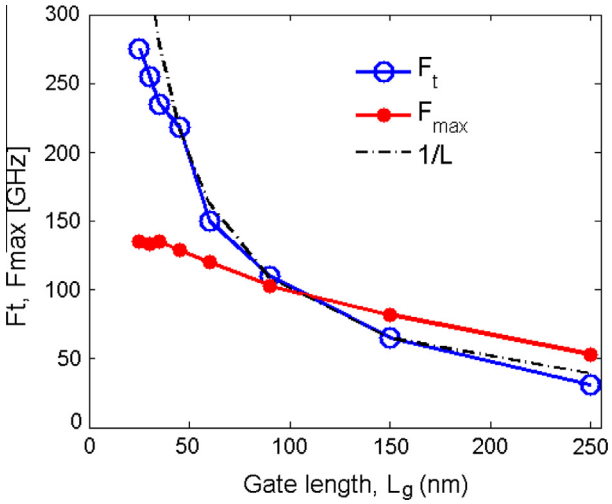

Fig. 8. f_T and f_{max} versus gate lengths (L_g) for UTBB with $W_f = 2$ μm and $N_f = 10$ [49].

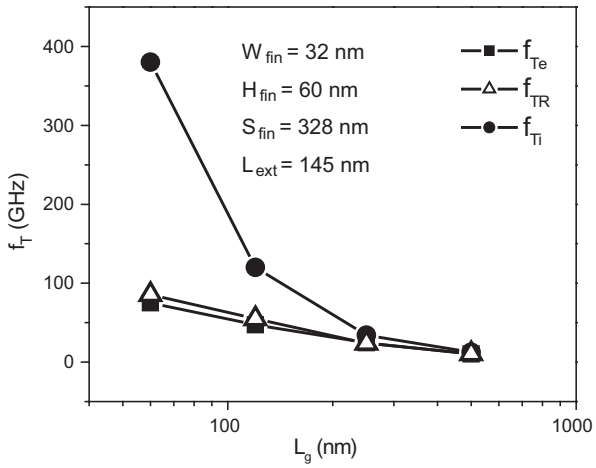

Fig. 9. Measured cut-off frequencies versus FinFET channel length [50].

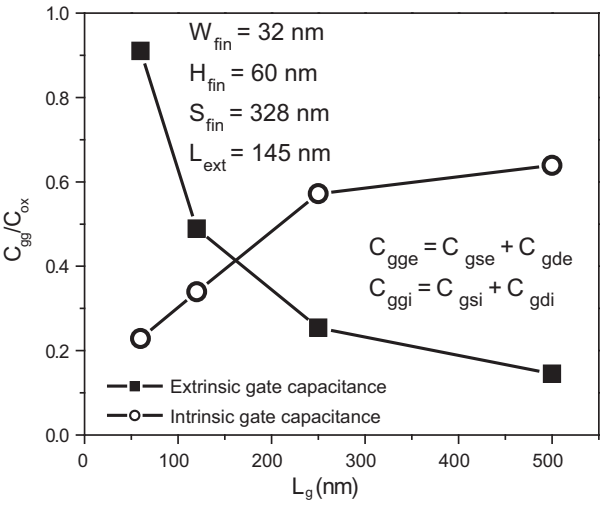

Fig. 10. Comparison between the C_{gge}/C_{ox} and C_{ggi}/C_{ox} ratios for measured FinFETs with different channel lengths. C_{ggi} are extracted at $V_d = 1.1$ V and V_g at maximum gate transconductance [50].

direct electrical coupling exists between both electrodes, and thus a parallel-plate like capacitor (C_{3b}) must be considered between the gate electrode and the S/D electrodes, as presented in Fig. 11. Thus, the C_3 component has to be split into two components: (i) C_{3a} which corresponds to the fringing component as was indicated in the Wu's model [51], and (ii) C_{3b} a parallel-plate like component.

In [50], measurements and numerical 3-D simulations clearly demonstrate the fringing capacitance decrease achieved by reducing the fin spacing, the S/D fin extension as well as by increasing the fin aspect ratio. In [52], the model showed that triple-gate FinFETs suffer from very high parasitic gate capacitances which are larger than the expected projection of the ITRS. It shows that the FinFET 3-D geometry optimization, such as the fin spacing reduction as presented in Fig. 12, is not sufficient to fulfill the ITRS requirements. A total fringing gate capacitance of maximum 0.18 fF/μm for the sub-22-nm technology nodes is targeted, and therefore the use of new materials and process such as the air gap or low-*k* dielectric spacers is of prime importance.

6. Benchmarking with state-of-the art devices

The benchmarking of f_T and g_m for the UTBB and other state-of-the art technologies are shown in Fig. 13. As can be seen, the

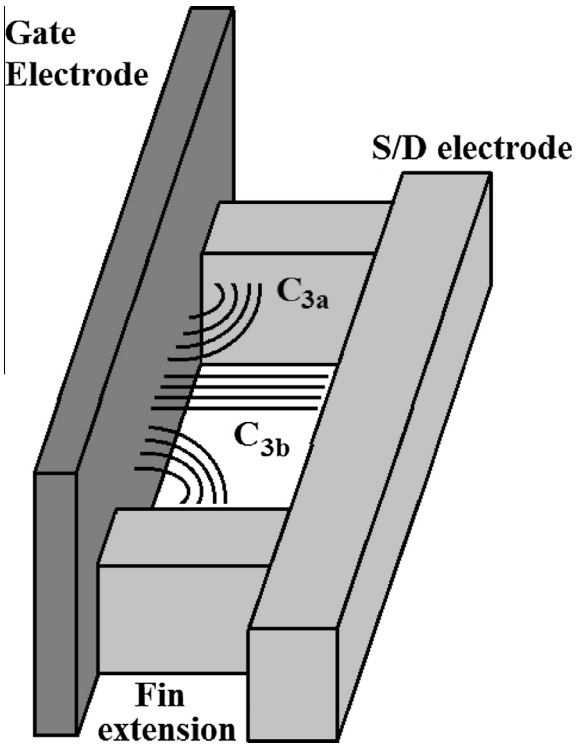

Fig. 11. Three-dimensional view of two fins half-FinFET to highlight the capacitance components C_{3a} and C_{3b} which correspond, respectively, to the fringing component as was indicated in the Wu's model [51] and a parallel-plate like component between the sides of the gate electrode and the S/D contact regions [50].

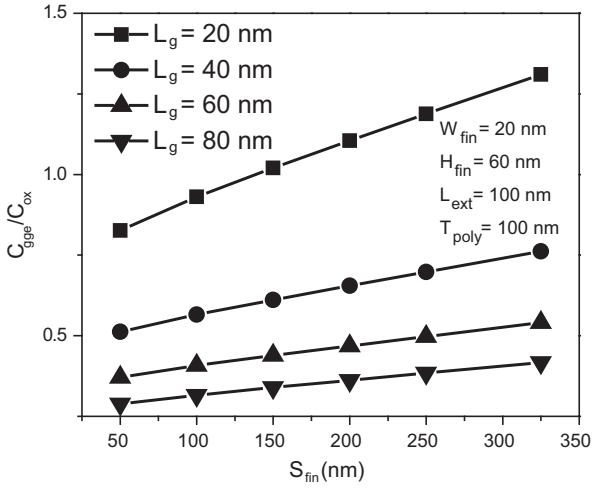

Fig. 12. Simulated extrinsic total gate capacitance versus fin spacing for different channel lengths [52].

highest g_m and f_T of 1800 mS/mm and 480 GHz, respectively, is reported for 45 nm-node CMOS technology based on PD-SOI MOSFET with strained channel [53]. Fig. 13a and b show the direct correlation between $g_{m\text{-}max}$ and f_T. Our benchmarking illustrates that the performance of the studied UTBB 28 FD-SOI is much better than previous reported in [54] and is comparable or better with other technologies reported before i.e. UTB, PD-SOI, FinFET and Bulk for similar gate lengths.

It is worth noting that the value of extrinsic f_T still remains below the ITRS roadmap target. Thus, we consider the intrinsic g_m and f_T. This allows us for benchmarking the "estimated improvement" one could gain with UTBB devices with respect to

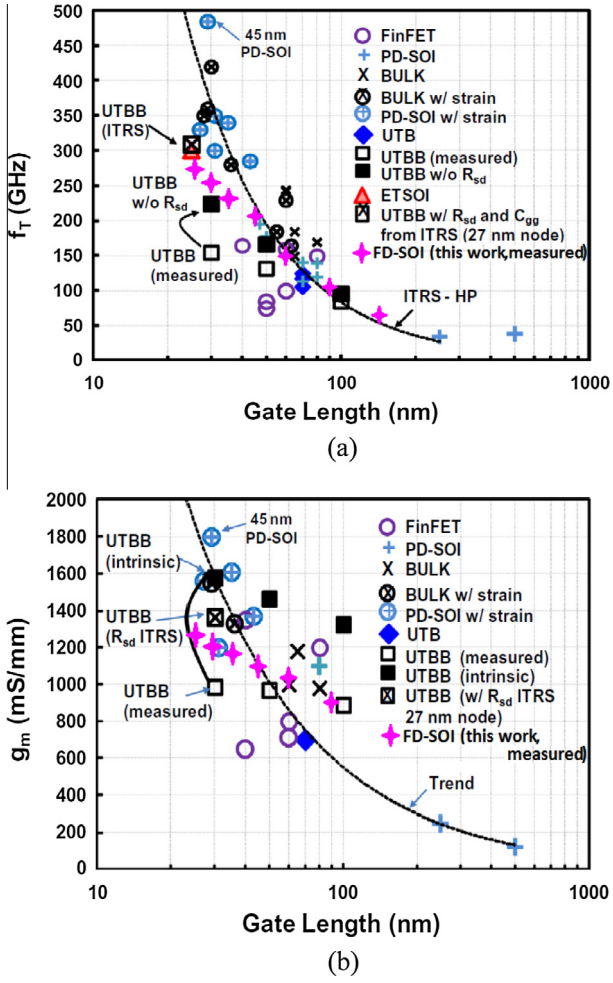

Fig. 13. Benchmarking of (a) f_T and (b) $g_{m\text{-}max}$ of state-of-the art MOSFETs versus gate length, L_g (nm) [54].

other state-of-the-art technologies. One can see that intrinsic g_m (w/o R_{sd}) shown in Fig. 13a is significantly high (as high as ~1600 mS/mm), a value which is comparable with measured g_m obtained from strained technology devices. However, such improvement is not directly translated into significant improvement in f_T (Fig. 13b) and still inadequate to meet ITRS [55] requirements. Next we consider R_{sd} = 300 Ω μm and C_{gg} = 0.7 fF/μm as in ITRS requirement for FD-SOI technology. The result shows that the g_m (R_{sd} from ITRS, Fig. 13a) and f_T (w/ R_{sd} and C_{gg} ITRS, Fig. 13b) as high as ~1350 mS/mm and 310 GHz can be achieved respectively. Such values are comparable with strained silicon technology and extremely thin SOI (ETSOI) with strain implementation.

As presented in [54], the total gate capacitance for PD SOI is about 0.71 fF/μm which is much lower than the extrinsic capacitance observed in multi-channel (i.e. stacked gate-all-around Si nanowires) and FinFET [50] with value of 2.60 fF/μm and 1.0 fF/μm, respectively. In [56–58] the comparison shows that the extrinsic gate capacitance of multi-channel device contributes five-time and FinFET is 40% higher than planar single-gate devices, respectively.

Besides the mobility boosters, an efficient improvement is achievable by optimization of process and architecture targeting reduction of parasitic series resistances and capacitances using (i) silicidation process of the source, drain and gate regions [59], (ii) optimization in device layout and dimension (i.e. gate pitch and width) to reduce the fringing effects at the perimeter, (iii) optimization on the underlap length, i.e. when the effective channel length is longer than physical channel length, which provides a trade-off between g_m (which is related to parasitic resistances) and C_{gg} [60,61], (iv) device architecture and spacer materials: modification of the device architecture such as introduction of faceted source and drain [62–64], low-κ spacer materials [65,66], gate capping layer thickness [66] and gate-height [66] can be used to reduce the fringing parasitic capacitance effect.

7. RF SOI substrates

Since 2009, Prof. Raskin's research team has been collaborating with Soitec to develop a lossless trap-rich SOI substrate for RF applications. Soitec now provides a new type of HR-SOI called eSI™, for enhanced Signal Integrity substrate with a measured effective resistivity as high as 10 kΩ cm. Due to the introduction of eSI, the RF SOI substrate can really be considered as a lossless Si-based substrate. This high-resistivity characteristic, which is conserved after a full CMOS process [67], translates to very low RF insertion loss (<0.15 dB/mm at 1 GHz) along coplanar waveguide (CPW) transmission lines, an effective resistivity close to the nominal silicon substrate resistivity (Fig. 14), a purely capacitive cross-talk similarly to quartz substrate (Fig. 15) [68] and integrated inductors with a high quality factor (Fig. 16) [69].

Besides the insertion loss issue along interconnect lines, the generation of harmonics in the Si-based substrates has been investigated. It has been demonstrated that the harmonic level originating from the substrate is reduced by at least 20 dB by moving from standard resistivity SOI substrates (~10 Ω cm) to high resistivity SOI (~1 kΩ cm), and more importantly, an additional drop of 40 dB is achieved with the innovative trap-rich HR SOI (TR SOI) substrate (Fig. 17). This low harmonic level is comparable with insulating substrates [70].

RF-SOI wafers are mainstream today on cellular and connectivity switch market whereas they were not even in production in 2008, with GaAs being mainstream at the time (Fig. 18). Beyond the RF switch, eSI RF-SOI technology opens the path for further system integration in the Front End Module space as well as even more complex mixed signal System-on-Chip (SoC). As highlighted by several press releases, the demand for the newly developed HR-SOI is booming and it is becoming the major material for high-performance RF applications. All major foundries in the field of RF applications across US, Europe and Asia have adopted the newly developed HR SOI substrates. It is also worth noting that inspired by Prof. Raskin's discovery, since 2009 IBM has been

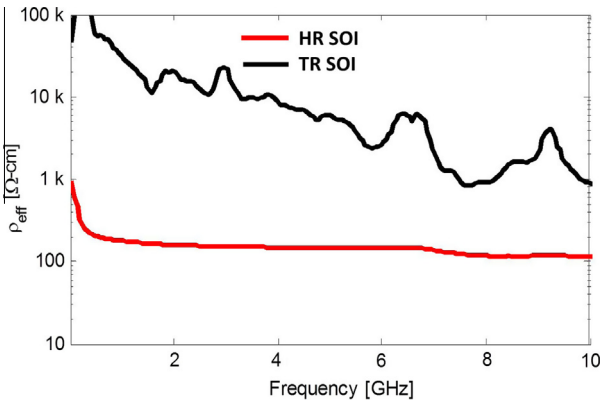

Fig. 14. Measured effective resistivity of a high-resistivity SOI substrate (HR SOI) and a trap-rich (TR SOI, i.e. eSI HR-SOI from Soitec) HR SOI substrate presenting both of them a handle Si substrate characterized by a nominal resistivity of 10 kΩ cm. While TR SOI presents an effective resistivity of around 10 kΩ cm, the value of the HR SOI without traps is actually only of 200 Ω cm.

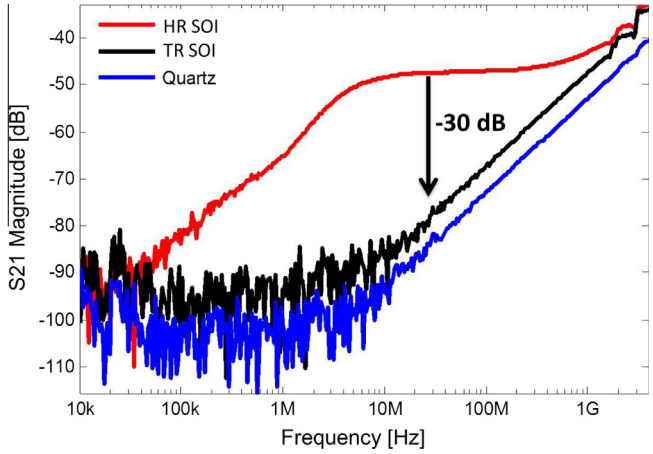

Fig. 15. Measured crosstalk response (S21) for the basic test structure on quartz and HR based-Si substrates with (TR SOI, i.e. eSI HR-SOI from Soitec) and without (HR SOI) 300 nm-thick polysilicon trap-rich layer. The distance *d* between the disturbing input and the output device is 50 μm.

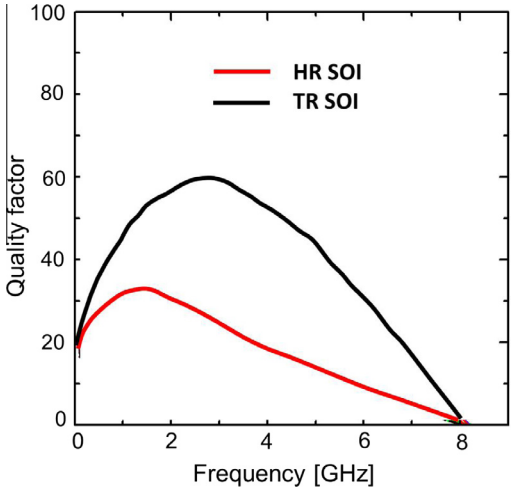

Fig. 16. Measured quality factor of a 2 nH spiral inductor integrated on top of HR SOI and TR SOI (i.e. eSI HR-SOI from Soitec) substrates.

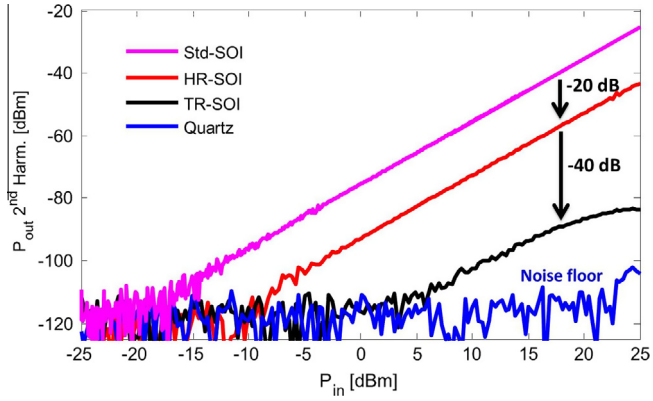

Fig. 17. Measured harmonic distortion along a coplanar waveguide transmission line (CPW) lying on standard SOI (~10 Ω cm) and HR based-Si substrates (~10 kΩ cm) with (TR SOI, i.e. eSI HR-SOI from Soitec) and without (HR SOI) 300 nm-thick polysilicon trap-rich layer. Identical CPW transmission line has been measured on top of a quartz substrate to quantify the harmonic measurement noise floor.

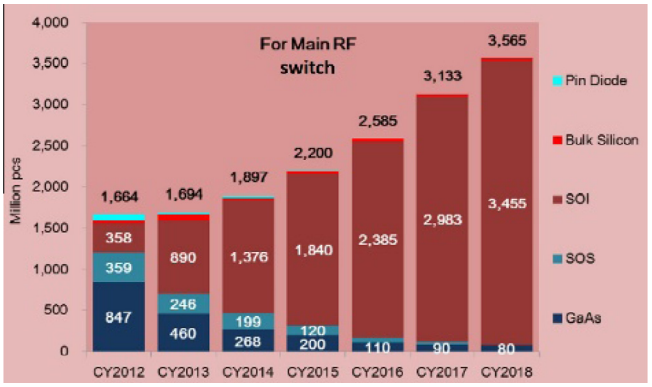

Fig. 18. Rapid adoption of trap-rich SOI substrate for RF switches.

proposing an alternative technology, also based on the introduction of defects into Si underneath the BOX, by pattern ion implants in order to enhance the RF performance of SOI RF integrated circuits [71].

There is a consensus across analysts and RF-SOI players to say that 2016 RF-SOI volume production will exceed one million wafers. Regarding fabless, all Front End Module makers have moved their antenna switches from GaAs to RF-SOI. Skyworks claim that 70% of its module have RF-SOI inside. Twenty billions RF-SOI ICs will be built in 2016, most of them going into FEM market representing 16 billions dollars. Analysts Yole and Navian claim that more than 85% of antenna switches are now on RF-SOI. Since there is average four switches per SmartPhone, we can say that 99% of smartphones have RF-SOI inside. In iPhone6s, based on Soitec estimates, there are 10 modules having RF-SOI inside.

8. Conclusion

FinFET and UTBB SOI MOSFETs are the promising advanced devices to fulfill the ITRS requirements. Efforts must be made on the reduction of the parasitic resistances and capacitances, especially in the case FinFET, to still get high-speed and high-frequency behavior improvements with the transistor channel length downscaling. RF-SOI continues to grow at 20% Compound Annual Growth Rate, driven by switch, power amplifier, low noise amplifier, etc. Present ramping of 300 mm wafers is enabling nodes below 65 nm, targeting 5G, millimeter-waves, and advanced System-on-Chip. The next innovative step will be the integration of advanced SOI MOSFETs such as FinFET or UTBB with trap-rich SOI substrate.

Acknowledgments

All the results presented in this invited paper have been obtained with the active participation of my colleagues Prof. D. Flandre, Dr. V. Kilchytska, Dr. M. K. Md Arshad, Dr. S. Makovejev, Dr. J. C. Tinoco, Dr. M. Emam, Mr. B. Kazemi Esfeh. I would like to thank all of them for their precious work and the inspiring discussions we have together on the topic of RF SOI. I would like also to thank the teams of ST-Microlectronics, CEA-Leti and IMEC for providing us with state-of-the-art MOSFETs and Soitec for our successful collaboration on the trap-rich SOI substrate.

References

[1] Clarke James S, George Christopher, Jezewski Christopher, Caro Arantxa Maestre, Michalak David, Torres Jessica. Process technology scaling in an increasingly interconnect dominated world. In: Symposium on VLSI technology. p. 1–2.

[2] Inoue Naoya. Challenges in low-k integration of advanced Cu BEOL beyond 14 nm node. In: IEEE international electron devices meeting. p. 29.1.1–4.
[3] Tagami M, Yang C-C, Shobha H, Soda E, Madan A, DeHaven P, et al. Improvement of RC performance for advanced ULK/Cu interconnects with CVD hybrid dielectric/metal liner. In: IEEE international interconnect technology conference. p. 1–3.
[4] Kincal S, Abraham MC, Schuegraf K. RC performance evaluation of interconnect architecture options beyond the 10-nm logic node. IEEE Trans Electron Devices June 2014;61(6):1914–9.
[5] Wu Shien-Yang, Lin CY, Chiang MC, Liaw JJ, Cheng JY, Yang SH, et al. An enhanced 16 nm CMOS technology featuring 2nd generation FinFET transistors and advanced Cu/low-k interconnect for low power and high performance applications. In: IEEE international electron devices meeting. p. 3.1.1–4.
[6] Ceyhan A, Naeemi A. Cu interconnect limitations and opportunities for SWNT interconnects at the end of the roadmap. IEEE Trans Electron Dev 2013;60 (1):374–82.
[7] Raskin J-P, Viviani A, Flandre D, Colinge J-P. Substrate Crosstalk reduction using SOI technology. IEEE Trans Electron Dev 1997;44(12):2252–61.
[8] Wu Y, Gamble HS, Armstrong BM, Fusco VF, Stewart JAC. SiO_2 interface layer effects on microwave loss of high-resistivity CPW line. IEEE Microw Guided Wave Lett 1999;9(1):10–2.
[9] Lederer D, Raskin J-P. Substrate loss mechanisms for microstrip and CPW transmission lines on lossy silicon wafers. In: Proc microwave symp dig. p. 685–8.
[10] Lederer D, Desrumeaux C, Brunier F, Raskin J-P. High resistivity SOI substrates: how high should we go? In: Proc IEEE int SOI conf. p. 50–1.
[11] Lederer D, Raskin J-P. New substrate passivation method dedicated to high resistivity SOI wafer fabrication with increase substrate resistivity. IEEE Electron Dev Lett 2005;26(11):805–7.
[12] Gamble H, Armstrong BM, Mitchell SJN, Wu Y, Fusco VF, Stewart JAC. Low-loss CPW lines on surface stabilized high resistivity silicon. IEEE Microw Guided Wave Lett 1999;9(10):395–7.
[13] Wong B, Burghartz JN, Natives LK, Rejaei B, van der Zwan M. Surface-passivated high resistivity silicon substrates Tor RFICs. IEEE Electron Dev Lett 2004;25(4):176–8.
[14] Liu Q, Yagishita A, Loubet N, Khakifirooz A, Kulkarni P, Yamamoto T, et al. Ultra-Thin-Body and BOX (UTBB) fully depleted (FD) device integration for 22 nm node and beyond. In: Symposium on VLSI technology. p. 61–2.
[15] Hisamoto D, Lee W, Kedzierski J, Takeuchi H, Asano K, Kuo C, et al. FinFET—a self-aligned double-gate MOSFET scalable to 20 nm. IEEE Trans Electron Dev 2000;47(12):2320–5.
[16] Fenouillet-Beranger C et al. Efficient multi-VT FD SOI technology with UTBOX for low power circuit design. In: Proceedings of the IEEE symposium on VLSI technology. p. 65–6.
[17] Andrieu F et al. Low leakage and low variability ultra-thin body and buried oxide (UT2B) SOI technology for 20 nm low power CMOS and beyond. In: Proceedings of the IEEE symposium on VLSI technology. p. 57–8.
[18] Fenouillet-Beranger C et al. Impact of a 10 nm ultra-thin BOX (UTBOX) and ground plane on FD SOI devices for 32 nm node and below. Solid-State Electron 2010;54(9):849–54.
[19] Monfray S et al. Thin-film devices for low power applications. Solid-State Electron 2010;54(2):90–6.
[20] Burignat S, Flandre D, Md Arshad MK, Kilchytska V, Andrieux F, Faynot O, et al. Substrate impact on threshold voltage and subthreshold slope of sub-32 nm Ultra Thin SOI MOSFETs with thin Buried Oxide and undoped channel. Solid-State Electron 2010;54:213–9.
[21] Rudenko T, Kilchytska V, Burignat S, Raskin J-P, Andrieu F, Faynot O, et al. Experimental study of transconductance and mobility behaviors in ultrathin SOI MOSFETs with standard and thin buried oxides. Solid-State Electron 2010;54:164–70.
[22] Burignat S, Md Arshad MK, Kilchytska V, Flandre D, Faynot O, Scheiblin P, et al. Drain/substrate coupling impact on DIBL of ultra thin body and BOX SOI MOSFETs with undoped channel. In: 39th European solid-state device research conference – ESSDERC'09, Athens, Greece, September 14–18, 2009. p. 141–4.
[23] Md Arshad MK, Raskin J-P, Kilchytska V, Andrieux F, Scheiblin P, Faynot O, et al. Extended MASTAR modeling of DIBL in UTB and UTBB SOI MOSFETs. IEEE Trans Electron Dev 2012;59(1):247–51.
[24] Rudenko T, Md Arshad MK, Raskin J-P, Nazarov A, Flandre D, Kilchytska V. On the gm/ID-based approaches for threshold voltage extraction in advanced MOSFETs and their application to ultra-thin body SOI MOSFETs. Solid-State Electron 2014;97:52–8.
[25] Makovejev S, Kazemi Esfeh B, Andrieu F, Raskin J-P, Flandre D, Kilchytska V. Assessment of global variability in UTBB MOSFETs in subthreshold regime. J Low Power Electron Appl 2014;4:201–13.
[26] Md Arshad MK, Makovejev S, Olsen SH, Andrieu F, Raskin J-P, Flandre D, et al. UTBB SOI MOSFETs analog figures of merit: effect of ground plane and asymmetric double-gate regime. Solid-State Electron 2013;90 (December):56–64.
[27] Planes N, Weber O, Barral V, Haendler S, Noblet D, Croain D, et al. 28 nm FDSOI technology platform for high-speed low-voltage digital applications. Symposium on VLSI technology, vol. 33(4). p. 133–4.
[28] Subramanian V, Parvais B, Borremans J, Mercha A, Linten D, Wambacq P, et al. Planar bulk MOSFETs versus FinFETs: an analog/RF perspective. IEEE Trans Electron Dev 2006;53(12):3071–9.
[29] Makovejev S, Olsen SH, Raskin J-P. RF extraction of self-heating effects in FinFETs of various geometries. IEEE Trans Electron Dev 2011;58(10):3335–41.
[30] Parvais B, Mercha A, Collaert N, Rooyackers R, Ferain I, Jurczak M, et al. The device architecture dilemma for CMOS technologies: opportunities & challenges of FinFET over planar MOSFET. In: International symposium on VLSI technology, systems and applications. p. 80–1.
[31] Raskin J-P. Wideband characterization of SOI materials and devices. Solid-State Electron 2007;51:1161–71.
[32] Kilchytska V, Chung TM, Torrese G, van Meer H, De Meyer K, Raskin J-P, et al. Investigation of charge control-related performances in double-gate SOI MOSFETs. In: Proc. 203rd meeting electrochem soc-11th int symp SOI technol devices, Paris, France, April 27–May 2, 2003. p. 225–30.
[33] Pavanello MA, Martino JA, Chung TM, Kranti A, Raskin J-P, Flandre D. Impact of the graded-channel architecture on double gate transistors for high-performance analog applications. In: Proc. 203rd meeting electrochem soc-11th int symp SOI technol devices, Paris, France, April 27–May 2, 2003. p. 261–6.
[34] Raskin J-P, Chung TM, Kilchytska V, Lederer D, Flandre D. Analog/RF performance of multiple-gate SOI devices: wideband simulations and characterization. IEEE Trans Electron Dev 2006;53(5):1088–94.
[35] Kilchytska V, Alvarado J, Collaert N, Rooyackers R, Put S, Simoen E, et al. Gate-edge charges related effects and performance degradation in advanced multiple-gate MOSFETs. Solid State Electron 2011;59(1):18–24.
[36] Kilchytska V, Md Arshad MK, Makovejev S, Olsen SH, Andrieu F, Faynot O, et al. Ultra-thin body and BOX SOI analog figures of merit. Solid-State Electron 2012;70(April):50–9.
[37] Makovejev S, Kazemi Esfeh B, Barral V, Planes N, Haond M, Flandre D, et al. Wide frequency band assessment of 28 nm FDSOI technology platform for analogue and RF applications. In: The 15th international conference on ultimate integration on silicon – ULIS'14, Stockholm, Sweden, April 7–9, 2014. p. 53–6.
[38] Makovejev S, Olsen SH, Kilchytska V, Raskin J-P. Time and frequency domain characterization of transistor self-heating. IEEE Trans Electron Dev 2013;60 (6):1844–51.
[39] Jin W, Liu W, Fung SKH, Chan PCH, Hu C. SOI thermal impedance extraction methodology and its significance for circuit simulation. IEEE Trans Electron Dev 2001;48(4):730–6.
[40] Kilchytska V, Levacq D, Lederer D, Raskin J-P, Flandre D. Floating effective back-gate effect on the small-signal output conductance of SOI MOSFETs. IEEE Electron Dev Lett 2003;24(6):414–6.
[41] Tenbroek BM, Lee MSL, Redman-White W, Bunyan RJT, Uren MJ. Self-heating effects in SOI MOSFET's and their measurement by small signal conductance techniques. IEEE Trans Electron Dev 1996;43(12):2240–8.
[42] Adan A, Higashi K. OFF-state leakage current mechanisms in bulk Si and SOI MOSFETs and their impact on CMOS ULSIs standby current. IEEE Trans Electron Dev 2001;48(9):2050–7.
[43] O'Neill A, Agaiby R, Olsen S, Yang Y, Hellstrom P, Ostling M, et al. Reduced selfheating by strained silicon substrate engineering. Appl Surf Sci 2008;254 (19):6182–5.
[44] Semenov O, Vassighi A, Sachdev M. Impact of self-heating effect on long-term reliability and performance degradation in CMOS circuits. IEEE Trans Dev Mater Rel 2006;6(1):17–27.
[45] Liew BK, Cheung NW, Hu C. Effects of self-heating on integrated circuit metallization lifetimes. Proc int electron devices meeting tech dig, vol. 16. p. 323–6.
[46] Kaczer B, Degraeve R, Pangon N, Groeseneken G. The influence of elevated temperature on degradation and lifetime prediction of thin silicon-dioxide films. IEEE Trans Electron Dev 2000;47(7):1514–21.
[47] Kim Y-H, Lee JC. Reliability characteristics of high-k dielectrics. Microelectron Rel 2004;44(2):183–93.
[48] Makovejev S, Raskin J-P, Md Arshad MK, Flandre D, Olsen SH, Andrieu F, et al. Impact of self-heating and substrate effects on small-signal output conductance in UTBB SOI MOSFETs. Solid-State Electron 2012;71:93–100.
[49] Kazemi Esfeh B, Kilchytska V, Barral V, Planes N, Haond M, Flandre D, et al. 28 nm FD SOI technology platform RF FoM. In: IEEE SOI-3D-subthreshold microelectronics technology unified conference – S3S'14, Millbrae, CA, USA, October 6–9, 2014. p. 80–2.
[50] Tinoco JC, Salas S, Martinez-Lopez AG, Alvarado J, Raskin J-P. Impact of extrinsic capacitances on FinFETs RF performance. IEEE Trans Microw Theory Tech 2013;61(2):833–40.
[51] Wu W, Chan M. Analysis of geometry-dependent parasitics in multifin double-gate FinFETs. IEEE Trans Electron Dev 2007;54(4):692–8.
[52] Salas S, Tinoco JC, Martinez-Lopez AG, Alvarado J, Raskin J-P. Parasitic gate capacitance model for triple-gate FinFETs. IEEE Trans Electron Dev 2013;60 (11):3710–7.
[53] Lee S et al. Record RF performance of 45 nm SOI CMOS technology. In: IEEE electron device meeting (IEDM). p. 255–8.
[54] Md Arshad MK, Kilchystka V, Emam M, Andrieu F, Flandre D, Raskin J-P. Effect of parasitic elements on UTBB FD SOI MOSFET RF figures of merit. Solid-State Electron 2014;97:38–44.
[55] The international technology roadmap of semiconductors [Online] <http://www.itrs.net>; 2013.
[56] Lim TC, Bernard E, Rozeau O, Ernst T, Guillaumot B, Vulliet N, et al. Analog/RF performance of multichannel SOI MOSFET. IEEE Trans Electron Dev 2009;56 (7):1473–82.
[57] Lederer D, Parvais B, Mercha A, Collaert N, Jurczak M, Raskin J-P, et al. Dependence of FinFET RF performance on fin width. In: Proc silicon monolitic integrated circuits in RF systems (SiRF). p. 8–11.

[58] Lederer D, Kilchytska V, Rudenko T, Collaert N, Flandre D, Dixit A, et al. FinFET analog characterization from DC to 110 GHz. Solid-State Electron 2005;49:1488–96.
[59] Chen J, Colinge J-P, Flandre D, Gillon R, Raskin J-P, Vanhoenacker D. Comparison of $TiSi_2$, $CoSi_2$ and NiSi for thin-film silicon-on-insulator applications. J Electrochem Soc 1997;144(7):2437–42.
[60] Kranti A, Burignat S, Raskin J-P, Armstrong GA. Underlap channel UTBB MOSFETs for low-power analog/RF applications. In: 10th international conference on ultimate integration of silicon – ULIS 2009, Aachen, Germany, March 18–20, 2009. p. 173–6.
[61] Kranti A, Rashmi S, Burignat J-P, Raskin GA, Armstrong. Analog/RF performance of sub-100 nm SOI MOSFETs with non-classical gate-source/drain underlap channel design. In: The 10th topical meeting on silicon monolithic integrated circuits in RF systems – SiRF'10, New Orleans, LA, USA, January 11–13, 2010. p. 45–8.
[62] Khakifirooz A, Cheng K, Kulkarni P. Challenges and opportunities of extremely thin SOI (ETSOI) CMOS technology for future low power and general purpose system-on-chip applications. In: Proc VLSI technology, system and applications. p. 110–1.
[63] Khakifirooz A, Member S, Cheng K, Reznicek A, Adam T, Loubet N, et al. Scalability of extremely thin SOI (ETSOI) MOSFETs to sub-20-nm gate length. IEEE Electron Dev Lett 2012;33(2):2011–3.
[64] Cheng K, Khakifirooz A, Kulkarni P, Ponoth S, Kuss J, Edge LF, et al. Extremely thin SOI (ETSOI) technology: past, present, and future. In: Proc IEEE international SOI conference. p. 1–4.
[65] Ko C, Kuan T, Zhang K. A novel CVD-SiBCN low-k spacer technology for high-speed applications. In: Symposium on VLSI technology, vol. 39; 2008. p. 3–4.
[66] Niebojewski H, Le Royer C, Morand Y, Jaud M, Rozeau O, Dubois E, et al. Extra-low parasitic gate-to-contacts capacitance architecture for sub-14 nm transistor nodes. In: EuroSOI, Paris; 2013. p. 2–3.
[67] Ben Ali K, Roda Neve C, Gharsallah A, Raskin J-P. RF performance of SOI CMOS technology on commercial 200 mm high resistivity silicon trap-rich wafers. IEEE Trans Electron Dev 2014;61(3):722–8.
[68] Ben Ali K, Roda Neve C, Gharsallah A, Raskin J-P. Ultra wide frequency range crosstalk into standard and trap-rich high resistivity. IEEE Trans Electron Dev 2011;58(12):4258–64.
[69] Shim Yonghyun, Raskin J-P, Roda Neve C, Rais-Zadeh M. RF MEMS passives on high-resistivity silicon substrates. IEEE Microwave Wirel Compon Lett 2013;23(12):632–4.
[70] Roda Neve C, Raskin J-P. RF harmonic distortion of CPW lines on HR-Si and trap-rich HR-Si substrates. IEEE Trans Electron Dev 2012;59(4):924–32.
[71] Botula A, Joseph A, Slinkman J, Wolf R, He Z-X, Ioannou D, et al. A thin-film SOI 180 nm CMOS RF switch technology. In: IEEE topical meeting on silicon monolithic integrated circuits in RF systems – SiRF '09, San Diego, CA, USA, January 19–21; 2009.