Effect of surface states on the electrical properties of Self-Switching Diodes Based on SOI

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Abstract
Self switching devices (SSDs) are new nano-scale active components. These devices are made with Silicon-on-Insulator (SOI) technology and operate at room temperature. In this work, we investigate experimentally their I-V characteristics which show a diode-like behaviour due to electrostatic effects and we were able to reproduce them by Medici simulations. Then, we focus on the effect of surface states density on the electrical properties of the SSDs.

1. Introduction

Future applications in electronics will need devices and circuits with higher performance and with proven fabrication techniques that will allow these designs to be reliable. Major challenges in nanoelectronic research are to develop reliable room-temperature operating devices that are easy and inexpensive to manufacture with high yield. Song et al. [1] have realized a new type of nanometer-scale, rectifying device, called self-switching diode (SSD) by tailoring the boundary of a narrow III-V semiconductor channel to break its longitudinal symmetry. Therefore and as pointed out by Åberg et al. [2], SSDs could be made in Si. More precisely, SOI substrates are used for their high mobility and implicitly for defining the depth of the channel [3]. In this work, diode-like current-voltage (I-V) characteristics and simulations of SOI based SSDs are presented and the effect of surface states density on their electrical properties are discussed.

2. Device Fabrication

The SSDs were fabricated using p-type SOI substrates. The carrier density and mobility at room temperature are 2.45×10^{16} cm^{-3} and 400 cm^2/Vs respectively. The thicknesses of the top silicon layer and the buried oxide (BOX) are, respectively, 205 nm and 400 nm. The key to the fabrication of our SSDs was to etch by a focus ion beam technique the two trenches that define the lateral dimension of the channel. This versatile technique allows us to pattern and etch the devices in only one fabrication step. The upper inset in Fig. 1a shows a typical electron micrograph in which the dark areas were etched down to the buried oxide layer. This fabrication process allows us to obtain a narrow channel confined between the etched trenches in the *xy*-plane and by the oxide which lies under the channel in the *z*-direction (see the upper inset of Fig. 1a). The trenches reach the device boundary forcing the current *I* to flow through the tiny channel. In this paper, we describe the results obtained on a W=230 nm wide SSD. The length of the channel is about L=1.3 µm.

3. Electrical Measurements

I–V characteristics of the SSD obtained at T=300 K are shown in Fig. 1a. When no voltage is applied across the wire, the channel is largely depleted because of the surface states at the etched boundaries [1]. If a positive voltage V is applied between the left and right contacts, the depletion zones are reduced thus leading to an increased effective channel width. If V<0, however, the field effect from the negative bias on both sides of the channel will increase the depletion zones thus reducing the effective channel width and possibly even completely pinching-off the channel, as illustrated in Fig. 1. The above mechanism leads to a preferred direction of carrier flow and gives rise to the diode-like I-V curve and we did not observe any reverse leakage current above 10 nA up to V = -5 V. The temperature dependence of the device's I-V is shown in fig. 1b. The results are given in a semi-log curve to show the effect of the temperature on both direct and reverse current. The current decreases when the temperature decreases. In particular, the reverse current (at constant V) seems to be thermally activated with an energy E_T=0.5 eV. This value is half of the gap band energy in the silicon and can be related to the surfaces energy levels situated around the mi-gap.

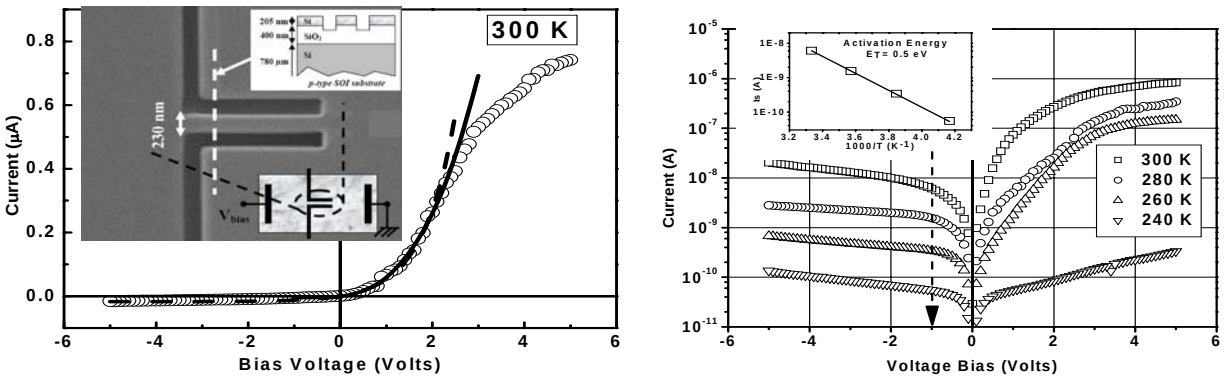

Figure 1: (a) I-V characteristic (circle) of a single p-type SSD shown in the lower inset and its corresponding exponential (dashed line) and polynomial (solid line) fits. (b) Temperature dependence of the SSD's I-V plotted in a semi-log curve. The inset shows the Arrhenius plot of the reverse current at V = -1 V.

4. Simulations Results

We have modeled the SSDs using Taurus-Medici from Synopsys, a finite element semiconductor simulation program. The simulation allows us also to investigate the effect of critical parameters such as the surface states density on the side walls of the trenches Q_{ss} on the electrical characteristics of the SSD. Fig. 2(a) shows the electrical potential in the middle of the channel (along the dotted line in the inset). The simulation results carried out without any DC bias at given geometry and acceptor density show that the increase of the surface states density leads to an abrupt increase in the potential barrier height (Fig.2b). If we assume that the width of the depletion zone in the channel is strongly related to the surface density, we conclude that below $2x10^{11}$ cm^{-2} the depletion zone is always smaller than the channel width.

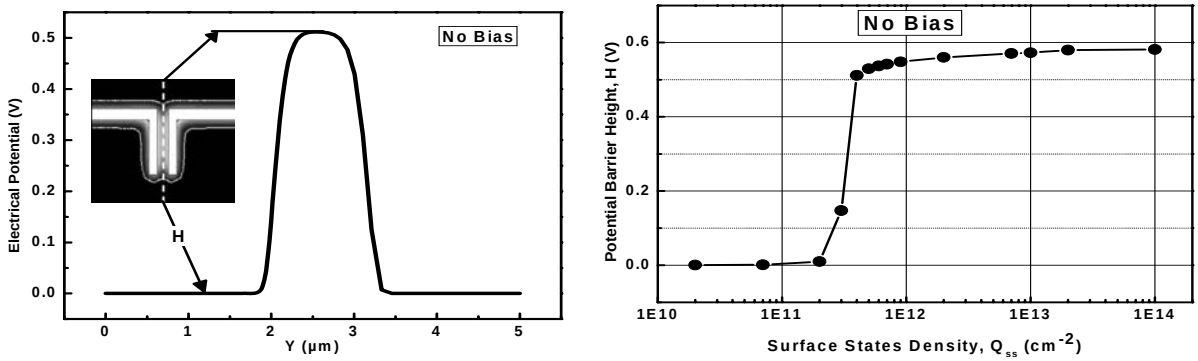

Figure 2: (a) Electric potential along the length of the channel (dashed line in the hole density plot given in the inset) The potential barrier height H is indicated. (b) The dependence of the potential barrier H vs. the surface states density Q_{ss} when no polarisation is applied on the device (W = 230 nm, L = 1.3 μm and $N_a = 2.45x10^{16}$ cm^{-3}).

5. Conclusion

Our work on SOI shows that SSDs can be compatible with advanced CMOS on SOI technologies, which increase the number of potential applications for SSDs. One of the most significant advantages of SSDs is the remarkably simple process requiring only to create trenches in a semiconductor film. The thermally activation of the reverse current allows us to relate the non-linear behaviour of the I-V curves to the surface states. In practice Q_{ss} is difficult to control since it is very sensitive to fabrication conditions. The simulation results suggest also that reproducibility of the device performance might be a concern when Q_{ss} ranges between $2x10^{11}$ cm^{-2} and 10^{12} cm^{-2}.

6. References

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