High linearity and low RF loss GaN-on-Si substrates achieved through interface engineering

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***Abstract*— GaN-on-Si HEMTs are emerging as a leading platform for 5G and FR3 6G RF front-end modules. Conductive losses in the Si substrate, especially at the high resistivity Si and III-N epitaxial layer interface degrade the power amplifier and switch performance. This parasitic conduction also causes harmonic distortion degrading switch linearity. We demonstrate that substrate RF properties such as high effective resistivity and low harmonic distortion can be achieved through interface engineering during III-N layer epitaxy and 2nd harmonic power (H2) lower than -85 dBm can be achieved with a corresponding effective resistivity of >7 kΩ·cm. Furthermore, the evolution of substrate linearity with temperature and bias for samples grown with varied AlN nucleation layer growth conditions was studied and a 2nd harmonic power < -85 dBm is achieved for HEMTs stacks up to 125 °C.**

Keywords*— *GaN HEMTs on Si, Substrate RF losses, Harmonic distortion, temperature dependent substrate linearity

I. INTRODUCTION

GaN-on-Si is emerging as a leading candidate for 5G and FR3 6G in both handset and infrastructure application space [1,2]. A widely reported issue of GaN-on-Si HEMTs is high RF losses even for III-N layers grown on high resistivity (HR) Si substrates, which is detrimental to both HEMT and passive device performance [2-9]. This is analogous to the RF-SOI technology where degraded linearity and passive performance was observed even for HR Si substrates [10-12] and is attributed to a parasitic conduction channel at Si and buried oxide (BOX) interface lowering the *effective substrate resistivity*, ρ_{eff} [10-12]. The ρ_{eff} is used in this work to qualify the substrate losses [8] and is extracted from RLGC parameters of a CPW lines as [10]:

$$\rho_{eff} \equiv \frac{C_{eq}}{\epsilon_{eq}} \cdot \frac{1}{G}, \text{ with}$$

$$C_{eq} \equiv \sqrt{C_{air} \cdot C} \text{ and } \epsilon_{eq} \equiv \epsilon_0 \sqrt{\frac{\epsilon_{r,eff}(\epsilon_{r,eff}-1)}{\epsilon_{r,Si}-1}}$$

C_{air} : air-filled capacitance (modeled)
$\epsilon_{r,eff}$: effective dielectric constant

For RF front-end modules, ρ_{eff} >3 kΩ·cm is required to achieve quasi-lossless substrates [10]. However, generally, the RF losses after HEMT epitaxy using MOCVD are found to be higher than that expected from the starting HR substrate [2-9]. It is understood that the high RF losses are caused by formation of a parasitic surface channel (PSC) at the interface of AlN nucleation layer (NL) and Si substrate. The PSC layer has been attributed to 2DEG formation at the AlN NL/Si interface, formation of acceptor type Si-O-N complexes near the top of Si substrate, diffusion of Al and Ga into the substrate during III-N epitaxy, HEMT processing dependent charges in the buffer layers, and interstitial oxygen double donor formation in the Si substrate [4-8]. In addition to RF losses, owing to a PSC at the AlN/Si interface, harmonic generation in the substrate could be enhanced [8,9] as compared to semi-insulating substrates e.g., SiC. As mentioned above, RF losses and distortion are sensitive to substrate manufacturing, III-N epitaxy, and device processing, with the largest contributor being the epitaxy of AlN NL layer [2,4,5,9,13,14].

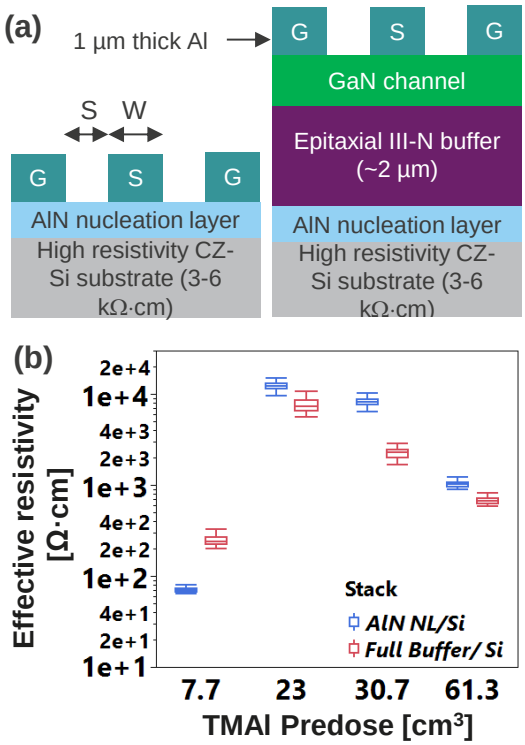

Fig. 1. (a) III-N-on-Si stacks studied in this work. Two types of samples were grown on Si(111) substrates: (i) AlN nucleation layer (NL) (ii) AlN NL followed by a III-N buffer and channel layers. (b) Impact of TMAl pre-flow dose on effective resistivity (ρ_{eff}) for the two stack types. For both the AlN NL/Si and III-N buffer/Si stacks, highest ρ_{eff} is achieved for TMAl predose of 23 cm^3. ρ_{eff} averaged over 0.5-2.5 GHz frequency range is plotted. CPW dimensions used for ρ_{eff} extraction: W/S = 17 µm/10 µm.

In [13] and [14], we demonstrated a procedure to reproducibly achieve high ρ_{eff} for AlN NL/Si templates through interface charge engineering. It was identified that for AlN nucleation layer, the temperature and the predose volume of tri-methyl aluminum (TMAl) are key parameters in determining RF losses [13, 14]. In particular, TMAl preflow volume was varied from 7.7 cm^3 to 61.3 cm^3 range at a fixed substrate temperature. Using detailed material and electrical characterizations, the relationship between TMAl predose and interfacial layer composition was established [14]. It was discovered that with a higher TMAl predose volume, the typically observed SiN_x interfacial layer incorporates more carbon leading to significant changes in the interfacial charges from +5e12 cm^{-2} for predose of 7.7 cm^3 and -1.7e13 cm^{-2} for predose of 61 cm^3. Another key finding was that the interface charges are approximately a linear function of predose volume in the range studied, which can be used to find the optimal dose for a nearly net charge free interface. Thus, a straightforward recipe for reduction of RF losses in AlN/Si stacks was found. In this work, we demonstrate that this technique is also applicable to thick epitaxial HEMT buffers which are grown on top of the AlN NL layer. Furthermore, we study the harmonic distortion performance of the AlN/Si and III-N buffer/ Si stacks as a function of bias and temperature.

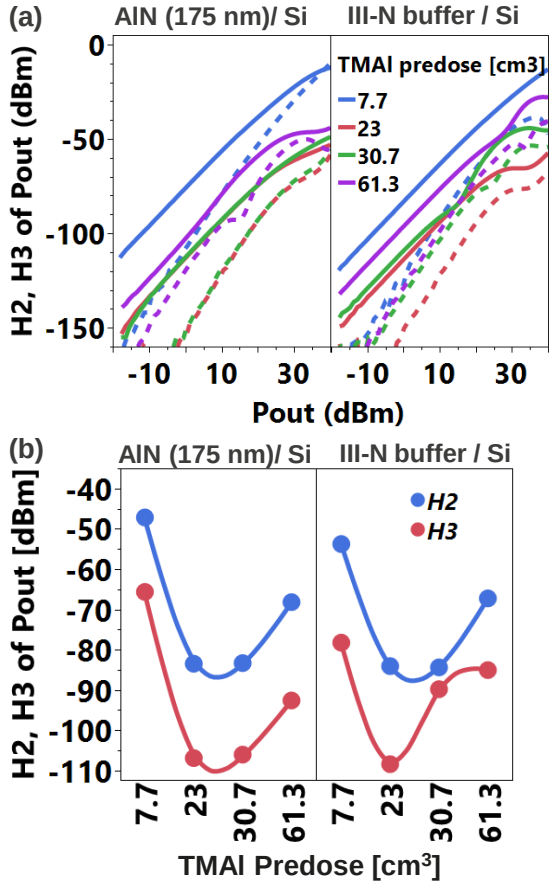

Fig. 2. (a) 2nd (H2) and 3rd (H3) harmonic powers measured at 900 MHz for the AlN NL and III-N buffer stacks for varying TMAl predose. (b) H2 and H3 at P_{out} of 15 dBm. A wide growth window exists where total harmonic power is ≲ -85 dBm. CPW dimensions: W/S/L =23.4 µm/12.5 µm/2 mm. Bias: 0V, T_{chuck}: 25 °C, f_0: 900 MHz.

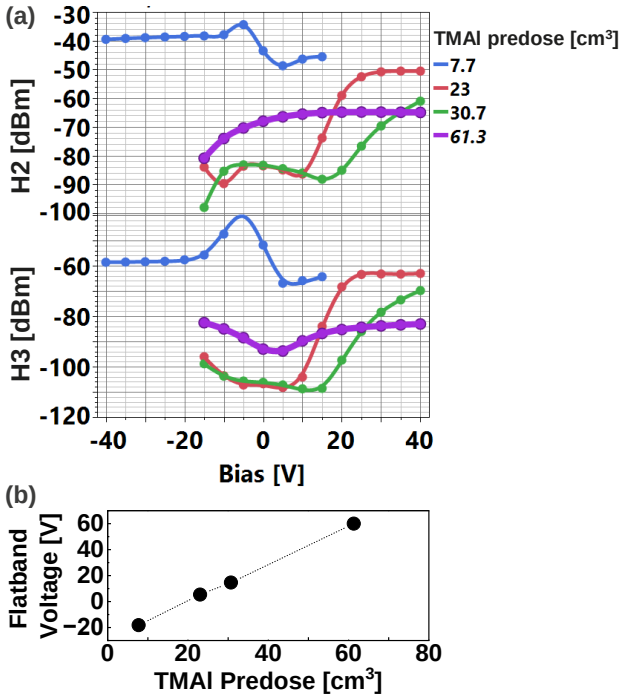

Fig. 3. (a) H2 and H3 for AlN NL/Si stack at P_{out} of 15 dBm as function of DC bias applied to signal line of the CPW. Samples with higher RF loss show weak dependence on bias. Largest modulation in harmonics is observed near flatland voltages shown (b). Flatband voltage is extracted from CV measurements for various TMAl predoses. A linear relation between VFB and TMAl predose is observed. CPW dimensions: W/S/L =23.4 µm/12.5 µm/2 mm. T_{chuck}: 25 °C, f_0: 900 MHz.

II. RF LOSSES

In this work, two material stacks grown using AIXTRON G5+ C Planetary Reactors® on high resistivity (3-6 kΩ·cm), 200 mm mCZ Si(111) are studied: (i) 175 nm AlN nucleation layer, (ii) a HEMT epitaxial buffer and GaN channel stack grown on top of the AlN nucleation layer [Fig. 1(a)]. Co-planar waveguides (CPWs) were fabricated on these stacks by evaporating 1 µm thick Al. ρ_{eff} was extracted from S-parameter measurements and data for various TMAl predose are shown in Fig. 1(b). A very high ρ_{eff} (> 10 kΩ·cm) is achieved for samples with predose of ~23 cm^3. For predose of < 10 cm^3, an electron-based PSC at the AlN/Si interface is expected.

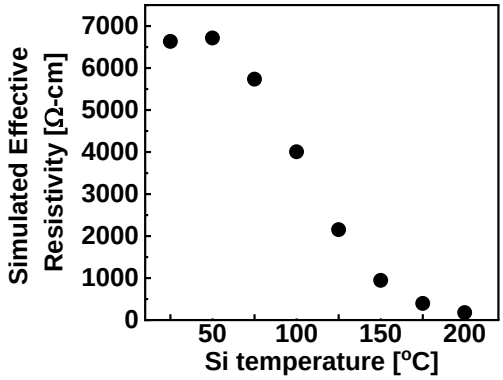

Fig. 4. Modeled effective resistivity for III-N buffer/Si stack with TMAl predose of 23 cm^3 as a function of substrate temperature. ρ_{eff} starts to degrade at ~75 °C. CPW dimensions: W/S =17 µm/10 µm.

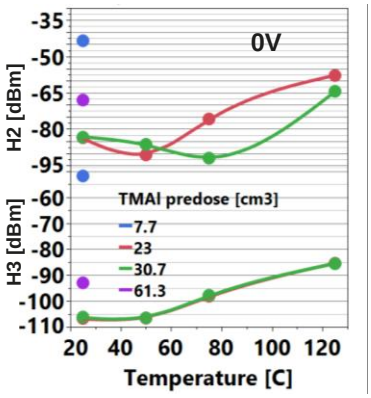

Fig. 5. 0V-bias H2 and H3 for AlN NL/Si stack as a function of temperature for varying predose conditions. H2 starts to degrade at lower temperature for the sample with lowest RF loss at 0-bias i.e. with 15s TMAl predose condition. CPW dimensions: W/S/L =23.4 µm/12.5 µm/2 mm. T_{chuck}: 25 °C, f_0: 900 MHz.

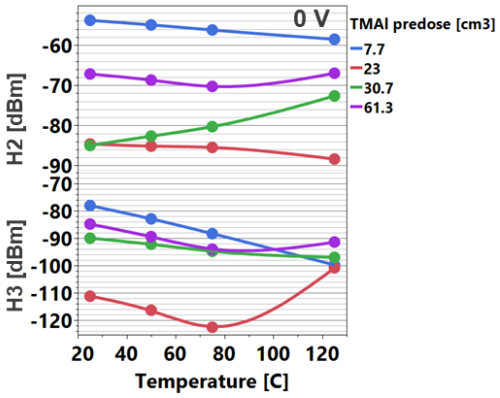

Fig. 6. 0V-bias H2 and H3 as a function of chuck temperature for various TMAl predose conditions for III-N buffer/Si stacks. H2 is maintained below -85 dBm for 15s predose upto 125 °C. CPW dimensions: W/S/L =23.4 µm/12.5 µm/2 mm. T_{chuck}: 25 °C, f_0: 900 MHz.

On the other hand, for predose of >20 cm^3, a hole-based PSC at AlN/Si interface is expected [13]. Furthermore, samples with a III-N buffer and GaN channel on top of the AlN NL layer were also grown [8]. A similar trend in ρ_{eff} as seen for AlN/Si stack is observed confirming the applicability of the proposed approach to the III-N buffer stacks also. There is generally a higher degree of Al/Ga diffusion into Si substrate observed for a thick HEMT buffer as compared to thinner AlN layer due to higher thermal budget [4,8,12]. This explains the lowered ρ_{eff} in buffer/Si stacks as compared to their AlN/Si counterparts for >20 cm^3 TMAl predose i.e. with a hole-based PSC layer. The opposite trend is seen for <8 cm^3 predose sample as a higher Al/Ga diffusion will compensate the electron-based PSC layer.

III. Substrate Linearity and its Bias-Temperature Dependence

Large-signal characterization at fundamental frequency of 900 MHz was carried out on CPW lines at varying chuck temperatures with DC bias applied to the central conductor of the lines [8,11]. As shown in Fig. 2, the 2nd (H2) and 3rd (H3) harmonics of the transmitted power (P_{out}), follow the same trend lines was attributed to modulation of ρ_{eff} with applied bias [8,12,15,16]. The modulation is highest near the flatband voltage. This is clearly observed for AlN/Si stacks in Fig. 3 with lowest H2 and H3 at 0V bias [samples with 23 and 30.7 cm^3 predose], where there is a large change in the H2 and H3 near DC biases close to flatband voltage [13].

Under realistic operating conditions, the temperature of the Si substrate can be >25 °C. This leads to change of resistivity for the bulk Si as well as the PSC layer. Based on spreading resistance profiles (SRP) for doping in the Si substrate and charges at the III-N/Si interface post epitaxy, ρ_{eff} can be modeled as a function of temperature [Fig. 4]. ρ_{eff} degraded above 75 °C, which was also experimentally observed [16,17]. For AlN/Si stacks with TMAl predose volumes of 23 cm^3 and 30.7 cm^3, H2 and H3 were measured at upto 125 °C (Fig. 5). H2 and H3 start to increase in 50-75 °C range for both the samples. At 125 °C, H2 which is the dominant harmonic component, increases by >20 dB as compared to 25 °C. In Fig. 6, H2 and H3 for samples with III-N buffer/Si stack are shown for various TMAl predose conditions. In contrast to AlN/Si stacks, III-N buffer/Si stacks exhibit lower temperature dependence upto 100 °C. The sample with 23 cm^3 predose achieved lowest H2 and H3 across the temperature range. Additionally, III-N buffer/Si stacks show nearly bias independent H2 and H3 at 25 °C [Fig. 7]. At 125 °C, bias dependence for the sample with 23 cm^3 predose is the highest [Fig. 7].

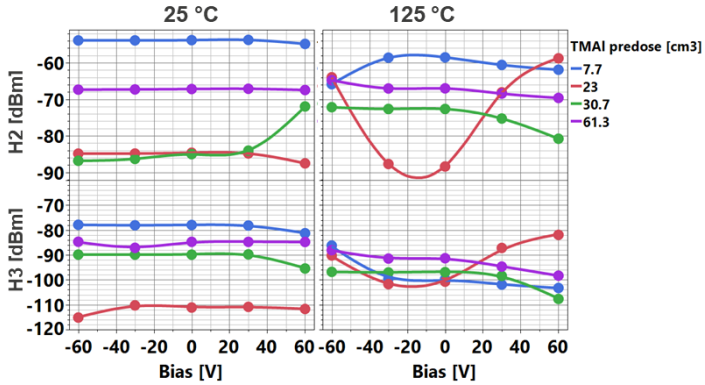

Fig. 7. H2 and H3 as a function of bias for various TMAl predose conditions for III-N buffer/Si stacks. The sample with lowest interface charge [with 15s TMAl predose] exhibits largest sensitivity to bias at high chuck temperature.

Finally, in Fig. 8, H2 at 0V DC bias is benchmarked for samples reported in this work against our prior results and those reported in literature [9]. A strong correlation between harmonic distortion and effective resistivity is seen. For III-N buffer/Si stacks, H2 < -85 dBm (at H1 of 15 dBm) is achieved.

IV. Conclusions

We reported on low RF loss and high linearity GaN-on-Si substrate technology achieved through interface engineering. In particular, using TMAl predose as a control knob, both AlN/Si and III-N buffer/Si stacks with high effective resistivity and low harmonic distortion are achieved. For a TMAl predose of 23 cm^3, effective resistivity of >7 kΩ·cm is achieved. Record low

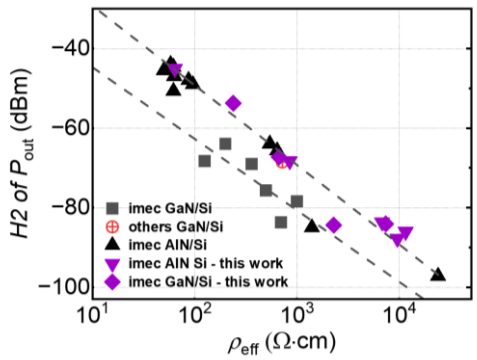

Fig. 8. Trends of H2 vs ρ_{eff} for various AlN/Si and buffer/Si stacks at P_{out} (H1) of 15 dBm. The trends are in line with our previous work. H2 < -85 dBm is achieved for III-N buffer/Si stack with TMAl predose of 23 cm^3. CPW dimensions used: W/S/L =23.4 µm/12.5 µm/2 mm.

H2 levels of -85.4 dBm and -88.4 dBm at 25 °C and 125 °C, respectively, were measured.

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