

Impact of passivation layer on the subthreshold behavior of p-type CuO accumulation-mode thin-film transistors

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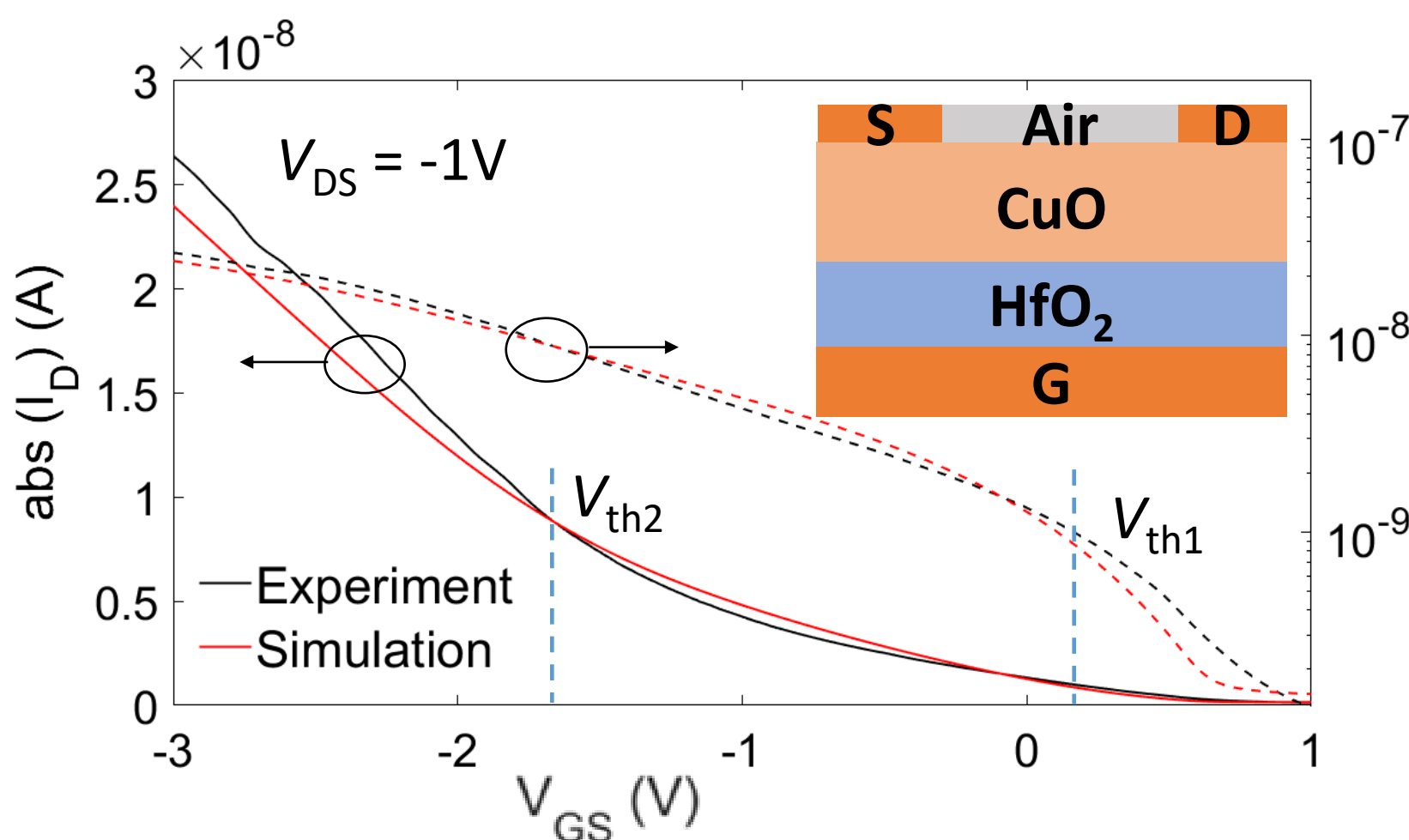
Background and Objectives

- P-type metal oxide (MO) TFTs are less studied and still featuring poor performance compared to their n-type counterparts.
- Passivation layers, such as HfO₂ and Al₂O₃, have been reported to improve the subthreshold operation of p-type MO TFTs.
- Use simulation tools to construct numerical models of p-type CuO TFT and explain the conduction mechanism in subthreshold regime.
- Investigate the impact of HfO₂ passivation layer on the subthreshold behavior of CuO TFT and further optimize the device structure.

Reference structure without passivation

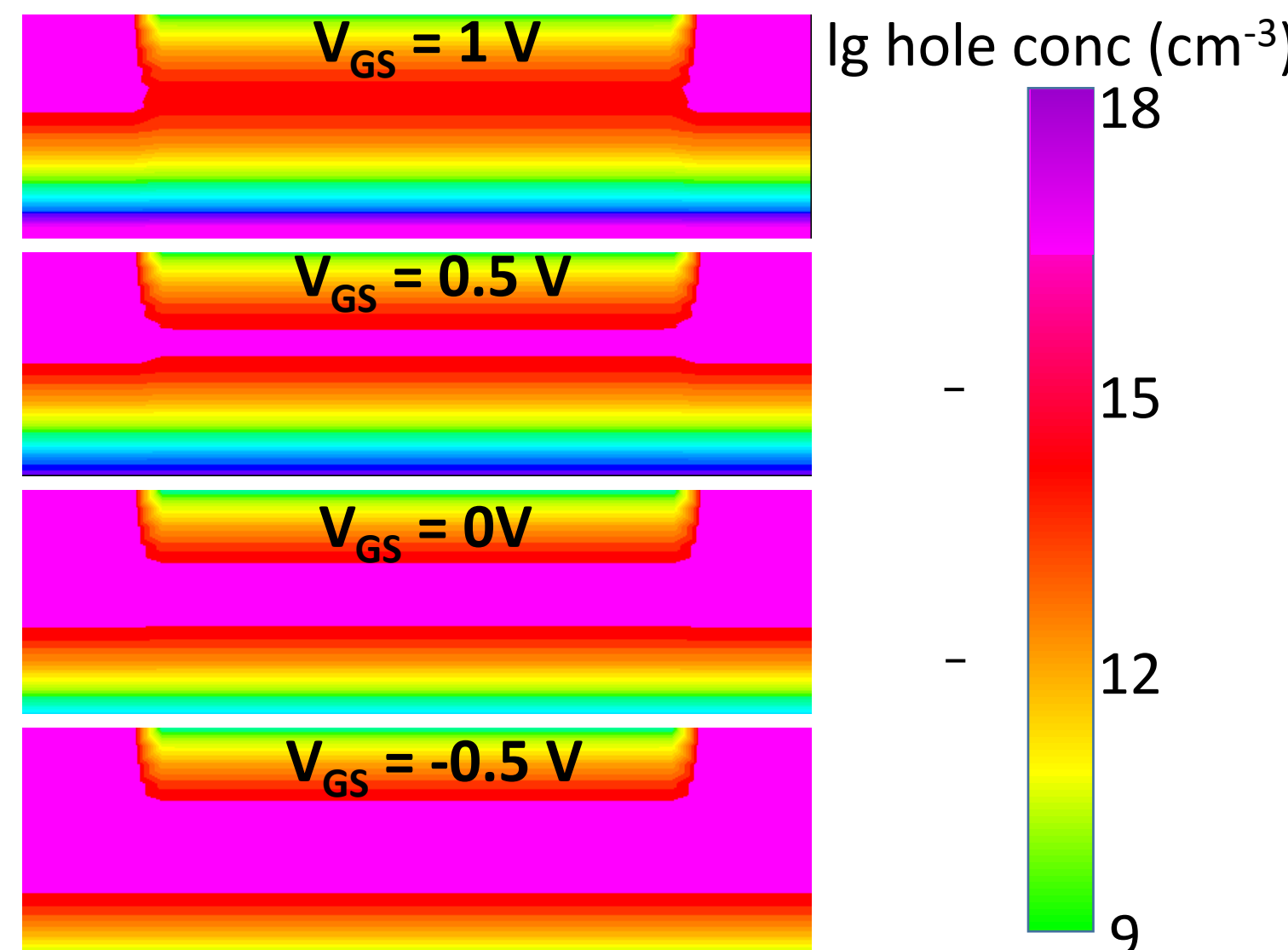
Table I. Process, measured [1] and Fitted device parameters used in simulations

	Band Gap (eV)	Mobility (cm ² V ⁻¹ s ⁻¹)	Doping Density (cm ⁻³)	Interface Defect Density D _{it} (eV ⁻¹ cm ⁻²)	Thickness (nm)	W/L	Fixed Oxide Charges Q _f (cm ⁻²)
Process parameters	—	—	—	—	CuO: 50 S/D: 100 HfO ₂ : 25	27	—
Measured parameters	1.6	6.2×10 ⁻⁴	5×10 ¹⁷	Back (HfO ₂): 6×10 ¹⁰ Front (air): 3.57×10 ¹³	—	—	Back: 9×10 ¹² Front: -
Fitted parameters	1.6	6.2×10 ⁻⁴	5×10 ¹⁷	Back (HfO ₂): 6×10 ¹⁰ Front (air): 3.57×10 ¹³	CuO: 120 S/D: 100 HfO ₂ : 25	27	Back: 9×10 ¹² Front: -



➤ V_{th1} is observed when a buried channel forms in the CuO film.

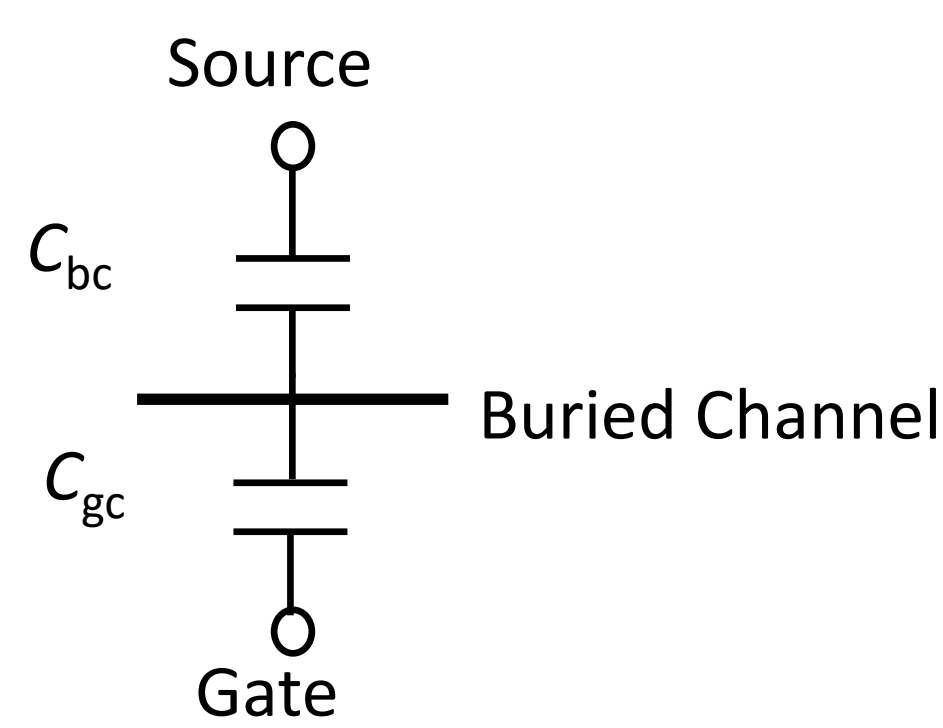
➤ V_{th2} is identified at the flat band voltage.



➤ V_{GS} > V_{th1}: The CuO film is fully depleted, and the current is cut-off.

➤ V_{th2} < V_{GS} < V_{th1}: A partial depletion region occurs in the CuO layer, resulting in a buried channel that enlarges for decreased V_{GS}.

➤ V_{GS} < V_{th2}: Holes are accumulated in the bottom of CuO film and thus forms an accumulation channel



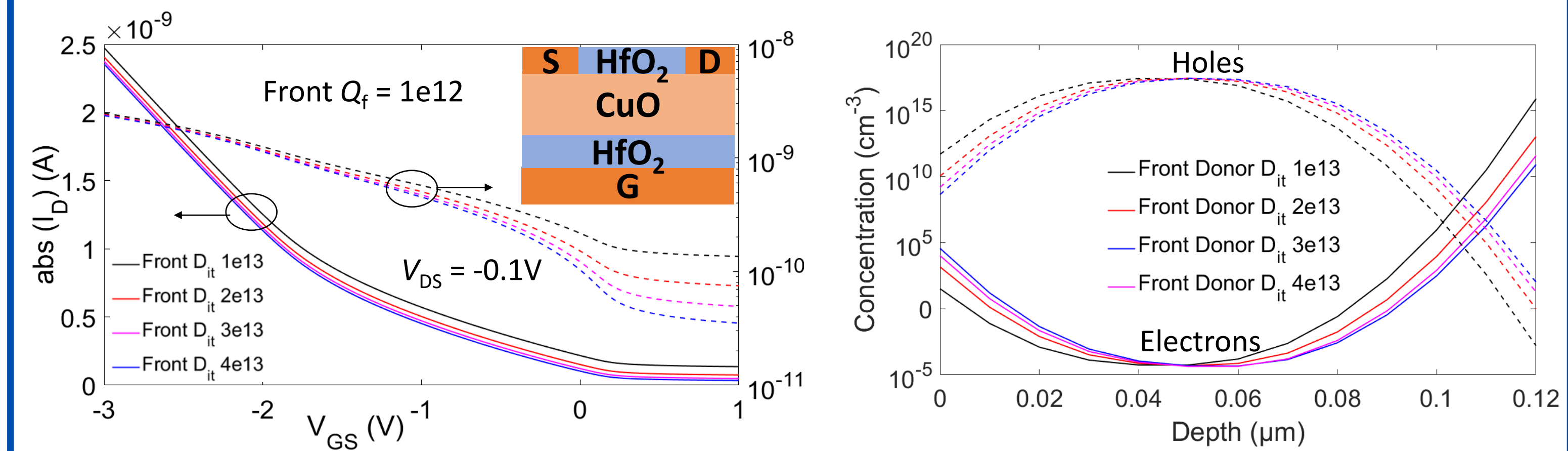
$$SS = \left(\frac{d \log(I_D)}{dV_{GS}} \right)^{-1} \cong \ln(10) \frac{kT}{q} \left(1 + \frac{C_{bc}}{C_{gc}} \right)$$

➤ A simplified capacitance model of the accumulation-mode CuO TFT in subthreshold operation.

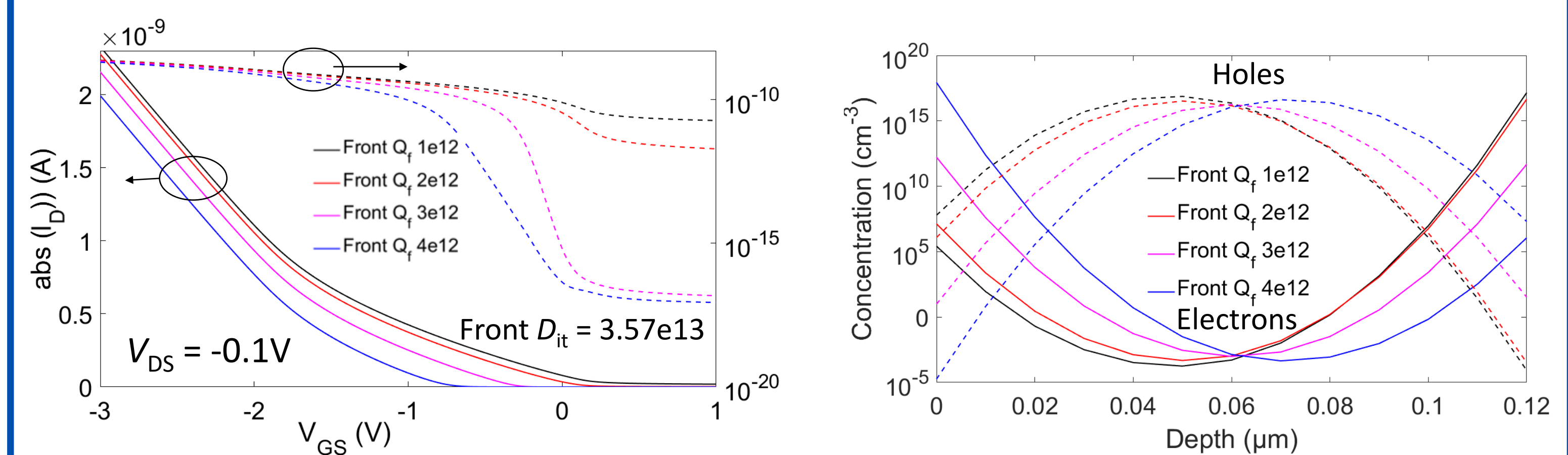
Table I. Device performance varying CuO thickness and front Q_f

Front Q _f (cm ⁻²)	SS (mV/dec)		V _{th1} (V)		I _{on} /I _{off}	
	T _{CuO} = 90 nm	T _{CuO} = 120 nm	T _{CuO} = 90 nm	T _{CuO} = 120 nm	T _{CuO} = 90 nm	T _{CuO} = 120 nm
1×10 ¹²	140	560	-0.89	0.16	1.89×10 ⁷	1.8×10 ¹
2×10 ¹²	110	260	-1.02	0.13	8.45×10 ⁷	1.47×10 ²
3×10 ¹²	61	61	-1.28	-0.29	1.09×10 ⁸	2.28×10 ⁷
4×10 ¹²	97	123	-1.58	-0.75	1.35×10 ⁸	5.67×10 ⁷

Top passivated structure with 100 nm HfO₂ passivation layer



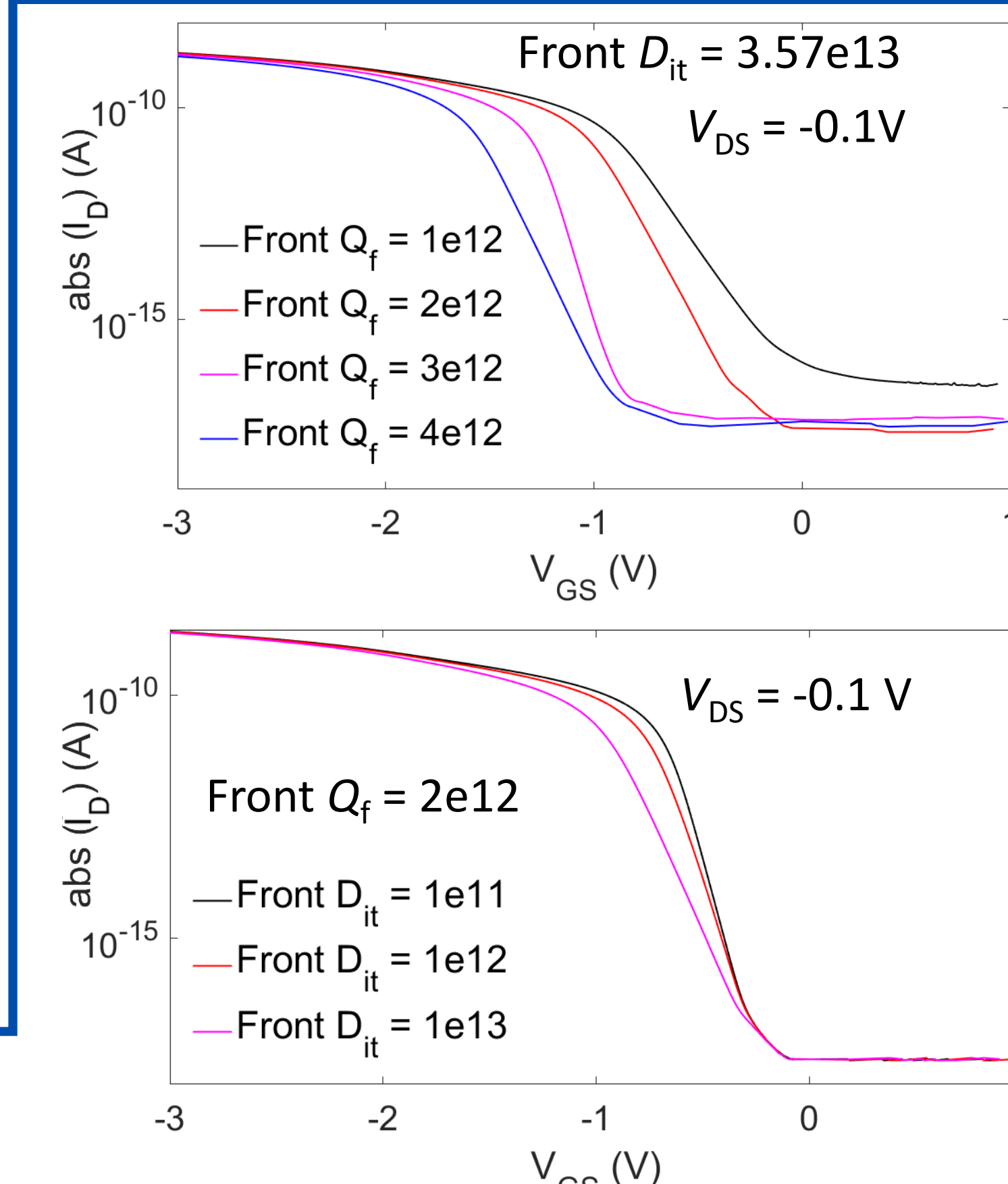
➤ Increased front donor D_{it} enlarges the top depletion region width and pushes the subthreshold buried channel closer to the back gate, leading to a higher C_{gc} and a smaller C_{bc}, which improves SS



➤ The impact of Q_f on subthreshold behavior is similar to that of D_{it}, but more significant.

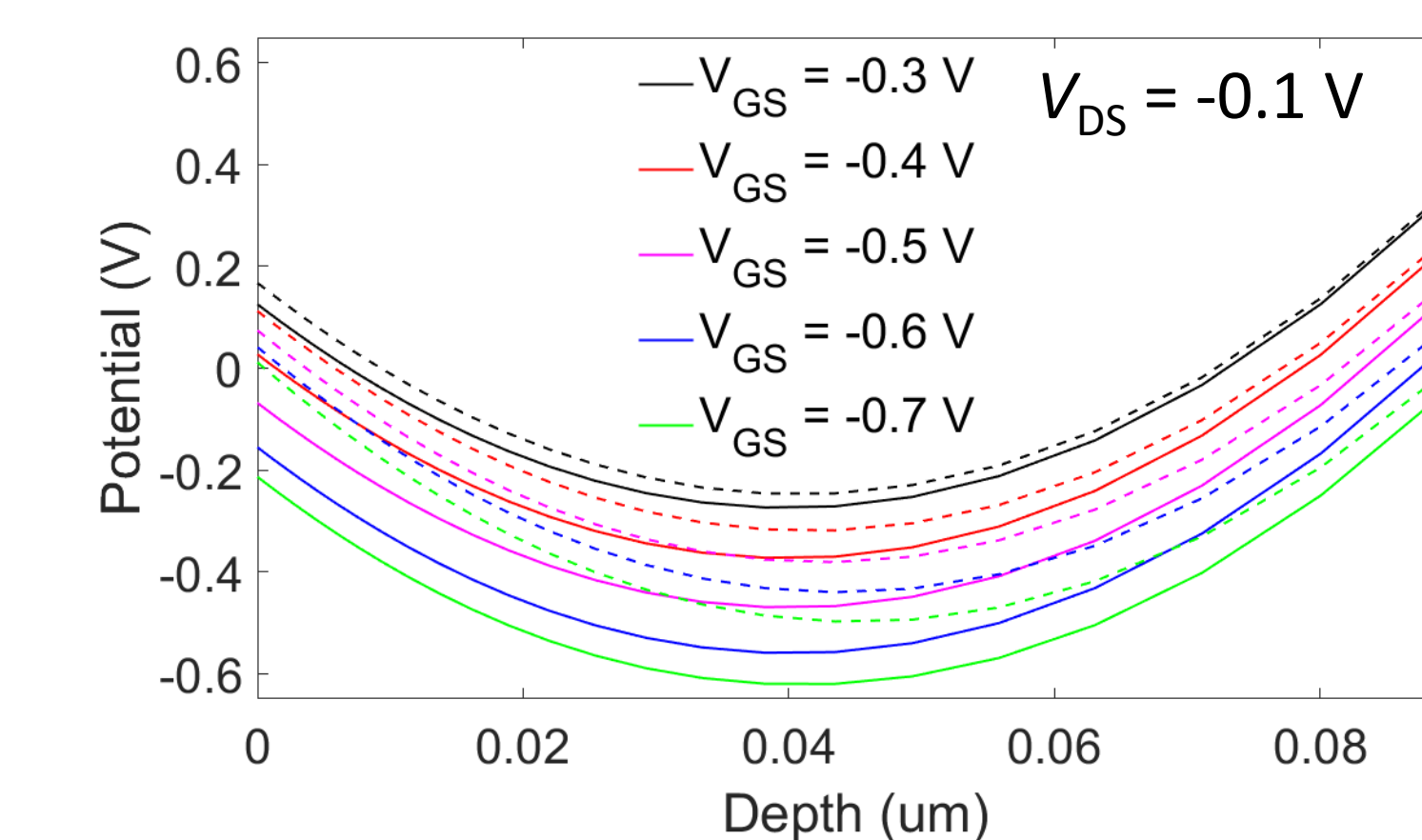
➤ A top inversion layer appears for Q_f larger than 3×10¹² cm⁻², pinning the top surface potential, thus increasing C_{bc} and degrading SS.

Optimized structure with 90 nm CuO film



➤ The effect of Q_f on subthreshold behavior is the same as the 120 nm CuO film case, while much lower off current and SS are obtained due to enhanced depletion in subthreshold regime.

➤ SS degrades with increased D_{it}, which is opposite to the observation in the case of 120 nm CuO film.



➤ With D_{it} increases from 1×10¹¹ (solid lines) to 1×10¹³ eV⁻¹ cm⁻² (dashed lines), reduced control of the gate bias on the film potential occurs and leads to an increase of SS.

Conclusions

- The subthreshold behavior is improved by the HfO₂ passivation layer, as well as by a thinner CuO film.
- This simulation study provides guidelines to improve the p-type TFT performance and could be applied to other MO semiconductors such as Cu₂O and SnO.

References

[1]. Zeng X, Zhukova M, Faniel S, Li G, Flandre D. Room-temperature DC-sputtered p-type CuO accumulation-mode thin-film transistors gated by HfO₂. Appl Phys Lett 2022;121:133503. <https://doi.org/10.1063/5.0098757>.

Acknowledgements

This work is financially supported by China Scholarship Council and Université Catholique de Louvain Co-Funding Fellowship (No. CSC202106130093).