Low-Loss Si-Substrates Enhanced Using Buried PN Junctions for RF Applications

M. Rack, *Member, IEEE*, L. Nyssens, and J.-P. Raskin, *Fellow, IEEE*

***Abstract*— A novel method for increasing the effective resistivity in low-doped silicon substrates is presented. By creating a chain series of p-n depletion junctions beneath the insulator, the parasitic surface conduction channel is interrupted, significantly lowering substrate losses and reducing harmonic distortion in the simulated and measured CPW lines achieving performance close to the widely used trap-rich silicon substrate at RF frequencies.**

***Index Terms*— RF CMOS, substrate losses, oxide charges, harmonic distortion, high-resistivity silicon substrate.**

I. Introduction

SILICON CMOS technology is widespread throughout digital applications, and advanced nodes are now offering competitive characteristics towards radio-frequency (RF) applications for wireless communication circuits and next generations of cellular networks [1]. In this RF-IC field signals propagate in a conductor that is defined atop an insulator-semiconductor multilayer. Fig. 1a shows a CPW line defined atop such a stack of materials. To avoid losses in such lines, and also to avoid coupling between them, it is of importance that the underlying substrate present a high effective resistivity. Furthermore it is required that the substrate be as linear as possible to minimize distortion of the line signals. For these reasons the standard resistivity (∼10 Ωcm) handle silicon substrate (widespread among digital applications) is unsuited to wireless systems, RF devices and power circuits due to its high conductivity, high RF losses and low linearity [2]. Low-doped bulk silicon is then preferred with high nominal resistivity (ρ_{nom}) above 1 kΩcm. However the effective resistivity (ρ_{eff}), which is sensed by overlying circuits, can differ strongly from ρ_{nom}, due to band bending effects at the semiconductor/ insulator interface that severely lower the local resistivity, impacting greatly on the overall ρ_{eff}. The resistivity of semiconductors is by nature dependent on the local electric field. Low-doped high-resistivity (HR) substrates are strongly field-sensitive, and it is typical for the substrate volume beneath the insulator to be in a conductive state due to (even low-level) parasitic fields present in the multilayer. Then, a highly conductive channel-like layer is induced as depicted in Fig. 1a. The most common parasitic fields originate from fixed charges (usually positive in Si/SiO_2 structures) present at the insulator/semiconductor interface. Such charges ("+" symbols in Fig. 1), are inevitable in the IC fabrication process, and attract free carriers to the interface in high concentrations, locally lowering the resistivity beneath the circuits by a factor of 10^3 to 10^6. This in turn lowers the substrate's effective resistivity by a factor of 10 to 10^4, to values as low as 1 Ωcm. This is referred to as the parasitic surface conduction (PSC) effect that renders the use of a HR substrate ineffective for improving the performance of overlying ICs [3]. A breakthrough on this issue was introduced in 1999 with the introduction of a thin polysilicon layer rich in defects (traps) beneath the buried oxide (BOX) in silicon-on-insulator (SOI) technology [4], [5]. This layer effectively combats the PSC by pinning the Fermi-level near mid-gap at the interface in a highly resistive state, achieving ρ_{eff} of over 1 kΩcm. Integrating multiple functionalities (RF alongside digital) on a single chip is a main driving force behind the progress of ICs, and today the trap-rich (TR) substrate is used in front-end modules of virtually all modern-day smartphones in the SOI switching circuits placed in the signal path to and from the antenna [6], [7]. In this letter, we present an alternative novel method for achieving high RF-substrate performance rivalling those of TR wafers that relies on locally interrupting the PSC channel by inducing a chain series of buried depletion junctions at the Si/SiO_2 interface.

II. Sample Fabrication

A total of 11 experimental wafers were processed starting from high-resistivity ($\rho_{\text{nom}} > 5\ k\Omega$cm) Si substrates. First, a thermal oxide of 20 nm is grown atop each wafer in order to prevent channeling effects during implants. Next, a 50 keV Phosphorous N^+ implant is performed over the entire wafer with a dose of 10^{13}, 3×10^{13} and 10^{14} cm^{-2} for the depleted (DP) $-A$, $-B$ and $-C$ samples, respectively. A mask is then patterned by photolithography (Fig. 2) over the top surface, defining resist regions of width W_{N+} separated by a distance of W_{P++}. A 30 keV Boron P^{++} implant is then performed with a dose of 10^{14}, 3×10^{14} and 10^{15} cm^{-2} for the DP $-A$, $-B$ and $-C$ samples, respectively. The photoresist is then removed and the samples are thermally annealed for dopant activation. Finally 180 nm of SiO_2 is deposited by PECVD, and a 1 μm-thick aluminum metallic layer is

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The authors are with the ICTEAM Institute, Université catholique de Louvain, 1348 Louvain-la-Neuve, Belgium (e-mail: martin.rack@uclouvain.be).

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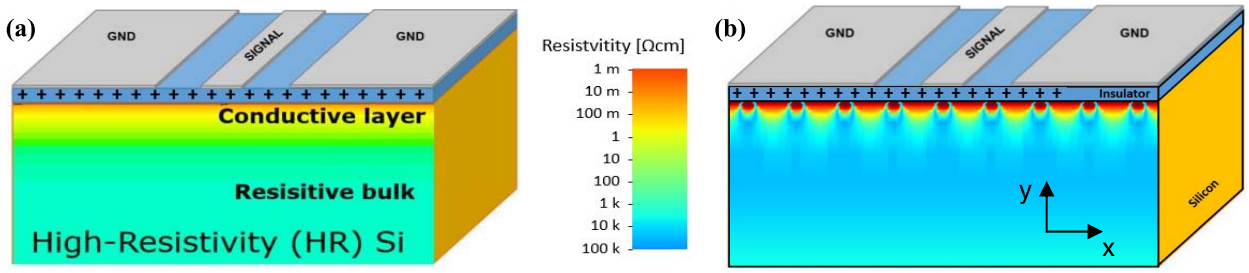

Fig. 1. Representation of the 2D resistivity profile in a HR substrate suffering from PSC (a) and in a DP substrate enhanced with buried PN depletion junctions (b), viewed normal to the PN junctions.

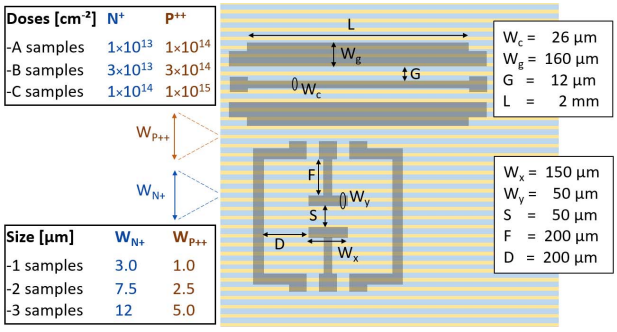

Fig. 2. Pattern and sizing of the P and N doped regions relative to the CPW and crosstalk structures on the DP substrates.

deposited atop by electron-beam physical vapor deposition and patterned defining the RF passive structures over the 200 nm of total oxide thickness. The backside of the wafer is similarly metallized with 1 μm-thick aluminum to provide an Ohmic DC contact. Three doping pattern sizes, W_{N+} and W_{P++}, were considered: 1 μm and 3 μm for -1 samples, 2.5 μm and 7.5 μm for -2 samples, 5 μm and 12 μm for -3 samples. A high-resistivity (HR) and a trap-rich (TR) wafer were also implemented as comparisons to these DP substrates. For the TR sample, 500 nm of poly-silicon is used as trapping layer below the BOX. The considered devices are CPW lines and crosstalk structures defined parallel and at a 90° angle to the doping lines, as shown in Fig. 2.

III. Performance Results

The depletion junctions induced between adjacent P and N regions serve to impede the field propagation in unwanted directions. The conductive PSC path is interrupted which results in an increase of substrate ρ_{eff} in the direction perpendicular to the buried junctions. Furthermore, the strong dopant concentration in these P and N regions are much less field-sensitive, giving rise to an increase in substrate linearity. Fig. 1b presents the resistivity profile in such DP substrates. These profiles were obtained from TCAD Silvaco Athena software by simulations of the full process flow described in Section II. Although the resistivity in the P and N regions is low, they come in series with the depleted junctions characterized by very low free carrier density that are therefore highly resistive. This is highlighted in Fig. 3 which presents the carrier concentrations and local resistivity as a function of the horizontal direction directly beneath the BOX.

A. Small-Signal Performance

On-wafer measurements of CPW lines were performed using a PNA-X vector network analyzer and a pair of GSG

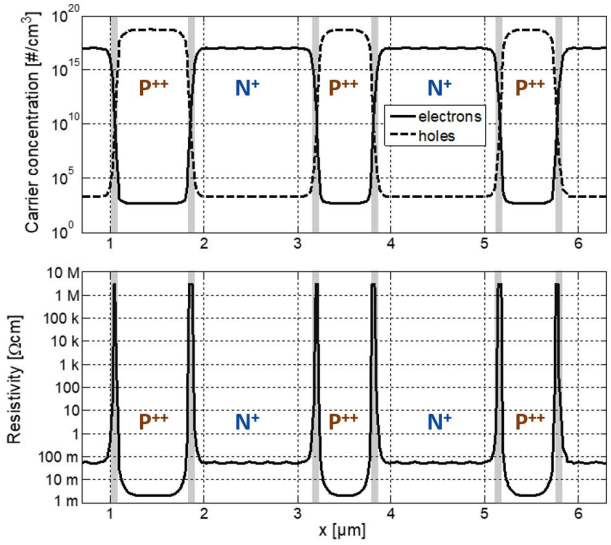

Fig. 3. Electron and hole concentration (top) and local resistivity (bottom) in a DP substrate directly beneath the BOX.

Infinity Probes with an on-wafer SOLT (Short-Open-Load-Thru) calibration based on an Impedance Standard Substrate (ISS). The Si substrate is grounded via the metallic measurement chuck biased to 0 V DC. From the measured S-parameters we extract the effective resistivity ρ_{eff}, effective relative permittivity $\varepsilon_{r,\text{eff}}$, RF line losses α and characteristic line impedance Z_C up to 20 GHz using the method described in [8] and the deembedding proposed in [9]. The layout and dimensions of the CPWs, that were chosen such that $Z_C = 50\ \Omega$ when implemented on a substrate with an $\varepsilon_{r,\text{eff}}$ of 11.7 (that of Si), are given in Fig. 2.

The extraction results pertaining to both the measured and simulated (Silvaco Atlas software) lines are shown in Fig. 4. Due to the PSC effect, the HR substrate presents low ρ_{eff}, high α (mainly shunt substrate losses), and $\varepsilon_{r,\text{eff}}$ and Z_C that converge towards 11.7 and 50 Ω, respectively, as the propagation mode shifts from the slow-wave to the quasi-TEM mode. The TR sample shows high performance with ρ_{eff} above 5 $k\Omega$cm and low α (mainly series metallic losses). The propagation mode in the overlying CPW is then quasi-TEM starting from a few tens of MHz and therefore $\varepsilon_{r,\text{eff}}$ and Z_C are close to 11.7 and 50 Ω over the measured frequency range.

The DP substrates show increased performance compared to the HR wafer. The DP-A1 sample shows the best performance values of all nine DP wafers because it has the highest density of PN junctions between signal and ground lines in the CPW,

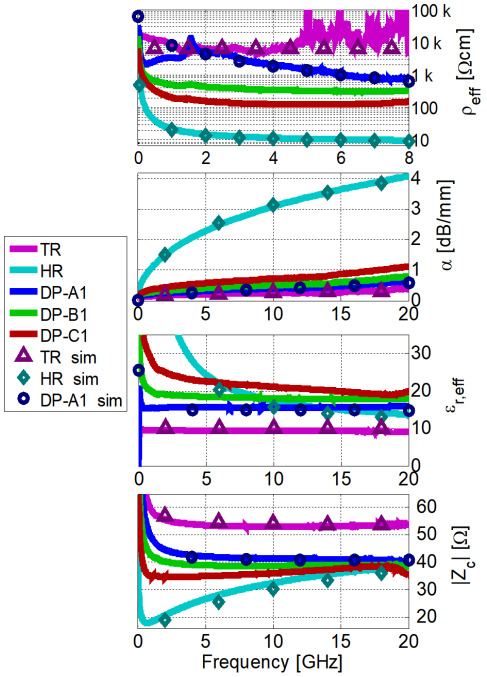

Fig. 4. Effective electrical substrate parameters extracted from RF measurements of CPW-lines.

and because it has the widest depletion junctions due to it using the lowest doping levels. It presents a high ρ_{eff} in the range of 2 $k\Omega$cm at 5 GHz and low RF losses. Though they show lower performance than the DP-A1 substrate, the higher-doped DP-B1 and DP-C1 samples still show significant improvement over the HR wafer. Because the conductivity in the P and N regions is very high, the E-field flattens there and they are seen as local equipotential regions. This has the effect of concentrating the E-field in the small depletion volumes in between them, which translates to a higher $\varepsilon_{r,\text{eff}}$ sensed by the overlying coplanar technology. Though undesired, the increase in $\varepsilon_{r,\text{eff}}$ is acceptable, as the DP-A1 substrate presents a value of 15.6. Although this value is larger than the relative permittivity of silicon (11.7), it is a worthwhile trade-off enabling a 200-fold increase of the ρ_{eff} as compared to HR. For this reason the CPW-line of these DP-substrates are no longer matched to 50 Ω and present Z_C values closer to 40 Ω.

The layout and dimensions of the crosstalk devices are given in Fig. 2. The S_{21} coefficient from these measurements, plotted in Fig. 5 (left), evaluates the amount of coupling facilitated by the substrate between the two pads of the structure [10], [11]. The HR wafer shows high coupling due to the PSC effect, and a characteristic resistive plateau from 200 MHz to 8 GHz, while the TR sample presents a capacitive behavior over the measured frequency range with a 20 dB/decade slope. The DP samples show strong improvement over the HR wafer with over 25 dB increase in isolation at 1 GHz.

It is important to point out that the substrate's effective resistivity is directional using this enhancement scheme and that a co-design between the smart PN implants and the RF device should be performed simultaneously during layout. Indeed, the pattern of the PN implants serves to impede electrical field propagation in unwanted directions according to the needs of substrate loss or coupling mechanisms of the

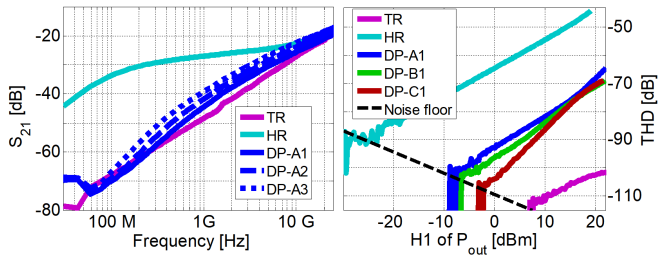

Fig. 5. Left: coupling levels through the substrate between the two pads of the crosstalk on-wafer device for various sample wafers. Right: total harmonic distortion level at the output of a 2 mm CPW line on various substrates.

overlying devices. For example, different PN implant patterns should be used beneath CPW lines, inductors, antennas, RF switches, or between two areas to reduce crosstalk.

B. Large-Signal Performance

Large-signal measurements of the CPWs were performed on-wafer using a dedicated setup [12]. A single tone with fundamental frequency of 900 MHz is injected into one port of the CPWs on each substrate. The power of this input tone H'1, is swept from −30 dBm to +25 dBm, and the output signal's components H1 (fundamental), H2 and H3 (second and third harmonics) are retrieved by a spectrum analyzer. The total harmonic distortion (THD) is plotted in Fig. 5 (right). It is shown that the voltage sensitive HR sample is highly non-linear, whereas the CPW on the TR wafer shows low distortion. The DP substrates present intermediate results, achieving 30 dB total linearity increase over HR. The lower doped DP-A1 sample shows slightly higher THD due to slightly wider and more field sensitive depletion regions, highlighting therefore a slight trade-off between effective resistivity and linearity.

IV. Conclusion

In this work a novel substrate enhancement technique is presented enabling high quality RF performance to be achieved in terms of substrate losses, crosstalk interference levels, and linearity. Using initial prototypes samples alongside TCAD simulations it is shown that CPW lines implemented on these substrates highly outperform those on a high-resistivity wafer by effectively combatting the parasitic surface conduction effect. By careful design of the PN depletion junctions it is shown that the RF performances are close to those of the widely used benchmark trap-rich solution and are promising candidates for integrated RF applications. Just like TR substrates (only compatible with SOI), the presented enhancement technique effectively counters the PSC, using a smart implant scheme that is readily implementable at the foundry level for a variety of process technologies (SOI and also bulk). Industrial level lithography (in the tens of nm) will enable the fabrication of substrates with even higher RF performance to those given in this work (with μm- lithography) by packing a higher density of depleted junctions beneath devices.

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