Effect of temperature on advanced Si-based substrates performance for RF passive integration

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Co-integration of digital and analog systems using off-chip technologies is difficult, onerous, and adds parasitic effects due to additional interconnections and packages for both, multi-chip-module (MCM) and System in Package (SiP) approaches. Two different Si-based solutions, Porous Si (PSi) [1-2] and Trap-Rich Silicon (TR Si) [3-4] appear as enabling technologies for the fabrication smaller, faster and cheaper RF devices. The choice of one technology over another depends on whether we decide to be compatible with bulk or SOI CMOS process.

In the case of SOI, HR-Si substrates can be used as handle wafers to provide high-resistivity capabilities for RF integration. However, for resistivities higher than 1 kΩ-cm the presence of parasitic surface conduction (PSC) effects strongly degrade the RF performance of the substrate, increasing substrate losses, crosstalk and non-linearities [5]. The introduction of a trap-rich layer between the BOX and the handle HR-Si wafer helps recovering the nominal HR properties of the HR-Si substrate [3-5]. Commercial 200 mm trap-rich HR-SOI wafers are already available for the integration of 3G and wireless communication systems into SoCs [6].

For bulk standard-Si substrates only Porous Si (PSi) solution provides high-resistivity properties for on-chip RF integration while being compatible with standard Si CMOS process. The creation of a locally produced thick porous Si layer (PSi layer) on the Si substrate [7], on which the RF devices are fabricated, has already demonstrated results comparable to other classical RF substrate solutions [2]. Additionally, PSi has a permittivity almost 4 times smaller than that of Si [8] that is useful to reduce crosstalk coupling at high frequencies between devices fabricated on the same chip [9].

The performance of trap-rich HR-SOI under small- and large-signal high-frequency operation has been already investigated [5]. However, the nonlinear behaviour of PSi has not been fully addressed yet, neither the effect of temperature on the RF properties of both PSi and TR Si technologies. In this work, we present for the first time a reduction of the substrate resistivity of PSi substrate with increase temperature, from 25 up to 175℃ (Fig. 4), as well as the increase in the nonlinear substrate behaviour for both Si-based solutions. The RF performance for small- and large-signal operation is investigated by means of CPW lines built on PSi and TR Si (Fig. 1), and compared with initial standard and HR-Si substrates, respectively. Measurements confirm the excellent RF lossless and linear performance of both substrates compared with their corresponding initial substrates (Figs. 2, 3). The observed variation with temperature can be explained by an increase of the bulk resistivity for HR-Si substrates that apparently also affect PSi material, regardless of its nano-metric porous structure.

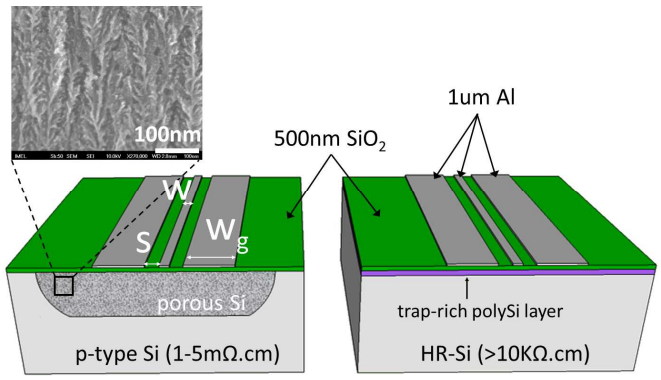

Figure 1. Schematic of a CPW transmission line fabricated on a 200-µm-thick Porous-Si layer (left) and on a Trap-Rich Si substrate (right).The dimensions of the CPW are W=26, W=12, and W_g=208 µm.

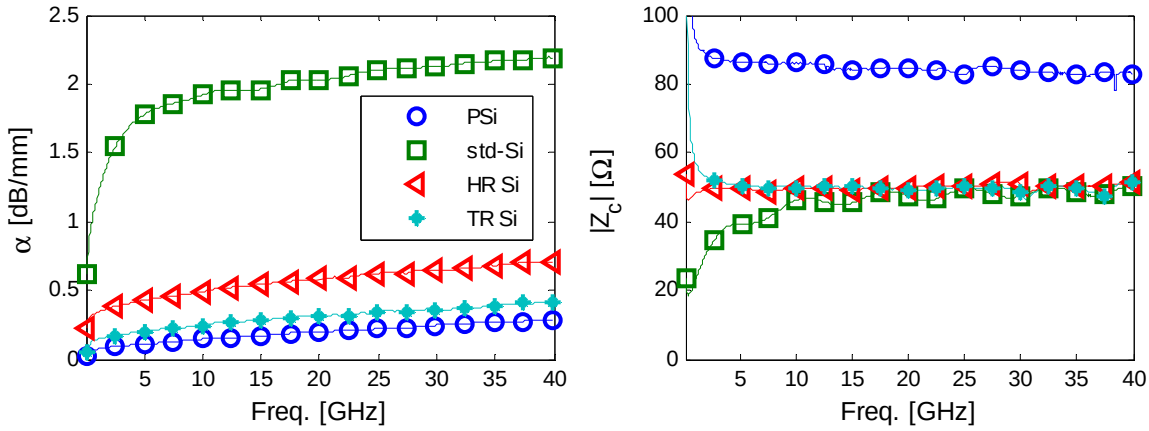

Figure 2. Attenuation (left) and characteristics impedance (right) of CPW lines on the investigated Si-based solutions.

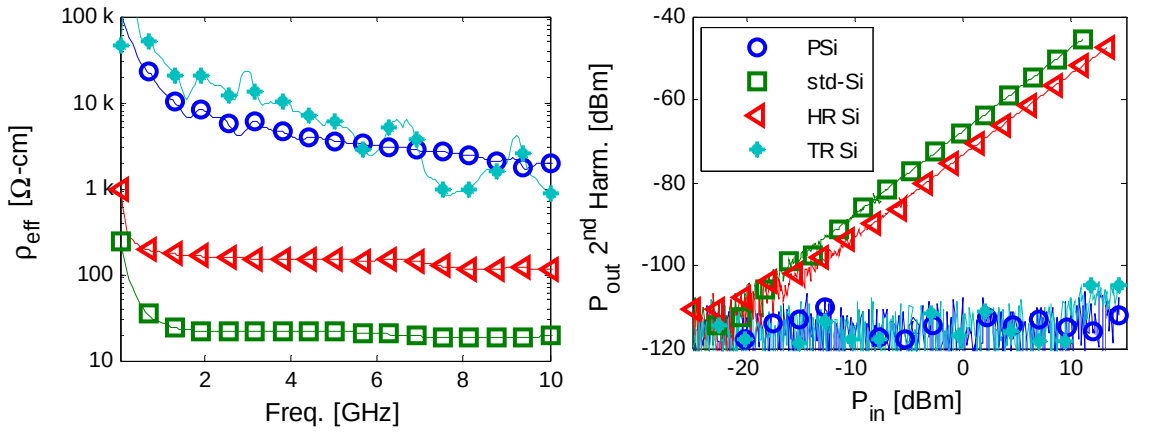

Figure 3. Effective Si resistivity (left) and harmonic distortion (right) for a CPW line on the investigated substrates.

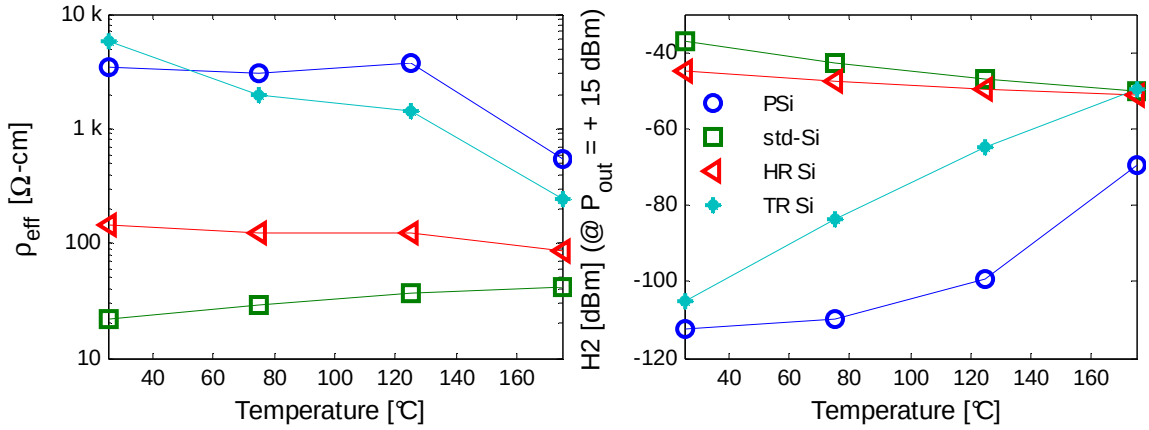

Figure 4. Variation of the effective Si resistivity at 5 GHz (left) and of the harmonic distortion (right) of a 2,146-µm-long CPW line on the investigated substrates.

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