

Development, characterisation and simulation of wafer bonded Si-on-SiC substrates



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ABSTRACT

Novel silicon-on-silicon carbide (Si/SiC) substrates are being developed in order to produce lateral power devices for harsh environment applications. Two methods of producing 100 mm Si/SiC substrates are detailed by wafer bonding silicon-on-insulator (SOI) wafers to semi-insulating 4H-SiC, then removing the SOI handle wafer and buried oxide. The final process includes a radical activation bonding process with low temperature processing, resulting in 97% yield. A uniform oxide layer at the Si/SiC interface of 1.4–1.8 nm is revealed, without voids, which minimises charge density at this interface. Capacitance-voltage (C-V) measurements of lateral metal-oxide-semiconductor capacitors (LMOS-Cs) are carried out on both processes revealing what appears to be an inversion from an n-type to a p-type like response in the 2 μm layers. Thinning the Si layers to 1 μm and making new LMOS-Cs, C-V responses show an improved n-type-like response, though frequency dispersion and incomplete accumulation remain. Finite element simulations showed that this effect could be reproduced by the introduction of interfacial charge at the two interfaces. Finally, while one possible explanation for fully inverting the C-V response of an n-type 2 μm Si layer on SiC was shown, the full understanding for this remains to be further studied.

1. Introduction

Silicon-on-silicon-carbide (Si/SiC) devices are being designed and fabricated for harsh environment applications [1–3] such as space. Designed to be both radiation hard and able to operate in extreme temperatures, devices are being targeted for power conversion applications such as electric propulsion [4] and high voltage transmission [5], where uncooled electronics could increase the overall lifetime, reliability, and science capability of a mission [6].

The Si/SiC substrate and device concept is shown [7–10] in Fig. 1. Lateral power MOSFETs and IGBTs, similar to the state of the art developed within SOI, are being developed to support 600 V within a 1 μm Si device layer. Unlike SOI, these substrates benefit from the high thermal conductivity and radiation hardness of the SiC, which allows for the efficient handling of self-heating effects. The wide bandgap of SiC forms both conduction and valence band offsets to the Si device layer, therefore minimising substrate leakage when using semi-insulating wafers. However, we have shown recently [7,8] that replacing

the buried oxide in SOI with a SiC substrate leads to the loss of the double RESURF effect, and hence an increased series resistance.

Si/SiC substrates are herein formed by wafer bonding 100 mm semi-insulating 4H-SiC wafers to SOI wafers, before grinding down the SOI handle wafer and etching the buried oxide (BOX). Previously, the first groups to look into Si-on-SiC did so with a BOX between the layers, forming SOI wafers with a SiC handle wafer [11,12]. However, this is a methodology that our own modelling [9] proves to only fractionally impact on self-heating compared to conventional SOI. Si as a contact layer to SiC was considered using a SmartCut process [13,14] to transfer 400 nm of Si onto a 75 mm off-axis n-type 4H-SiC wafer, forming a heterojunction diode. Another method [2] involved the direct bonding of 50 mm Si and 6H-SiC wafers, before the Si wafer was ground and polished to approximately 1 μm. Simple lateral Si MOSFETs demonstrated the ability of the substrates to dissipate heat away from the junction region and maintain a high channel mobility at 300 °C. The use of SOI wafers in producing Si/SiC substrates was first proposed in [15], where a 330 nm device layer from a 100 mm SOI wafer was transferred

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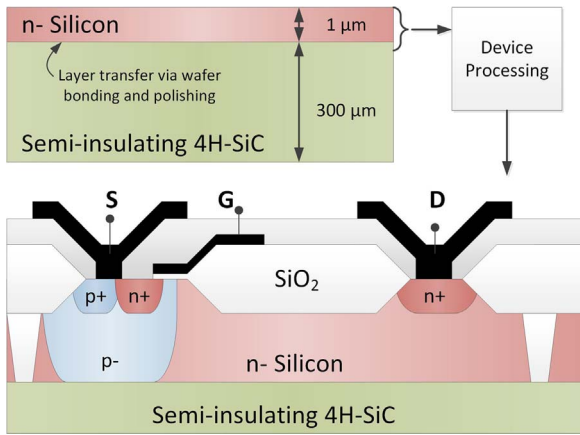


Fig. 1. Top, the Si/SiC material system that has been developed. Bottom, a proposed Si/SiC LD-MOSFET transistor.

onto a 50 mm 4H-SiC wafer, before removing the handle wafer. This was developed into a process [3] whereby a SIMOX SOI wafer with a 5 μm device layer was bonded to a polycrystalline SiC substrate with 800 nm of Si CVD grown on its surface. In this substrate, LD-MOS transistors were produced [3], which had an improved thermal and RF performance compared to SOI.

In this paper, we will discuss the development of 1 and 2 μm Si/SiC substrates that will be used for developing harsh environment LD-MOS devices. Using lateral MOS capacitors and FEM simulation, we will show the impact of interface charge on these layers and reveal how the bonding process was adapted to mitigate against this.

2. Experimental details

100 mm Si/SiC substrates have been produced with a Si device layer thickness of 1 and 2 μm, by two Bonding Processes (BPs). These are described here and illustrated in Fig. 2.

The starting material was common to both processes. A 100 mm Norstel semi-insulating (SI; $\geq 1.10^7 \Omega \text{ cm}$) on-axis 4H-SiC wafer was to be bonded to a 100 mm IceMOS Technology Ltd SOI wafer with a buried oxide 2 μm thick, and a lightly n- doped device layer (5–45 Ω cm). These wafers were first cleaned using standard RCA cleaning solutions.

BP1 was carried out by IceMOS Technology Ltd and is extensively described in [10]. First, a grid of trenches 2 μm deep is etched into the SiC surface prior to bonding. This was designed as an escape route to for outgassing during the annealing process. The SOI device layer is etched to the final device layer thickness of 1 μm, if required. After a proprietary surface plasma treatment, a hydrophobic bonding process was performed to form a bond between the wafers. A 2 h, 1200 °C anneal was then performed to form a permanent bond between the wafers, and to shrink the interfacial oxide. This caused the wafers to bow, but as the Si handle wafer was ground away down to the oxide layer, this strain was released. Finally, the oxide, which had been the buried oxide of the SOI wafer, was removed with hydrofluoric acid.

BP2 was carried out by Tyndall National Institute, in which a radical activation process is used to enable low-temperature bonding. After RCA cleaning, a further cleaning process was performed using an EVG wafer-cleaning tool equipped with a DI megasonic nozzle. The wafers were then loaded in a bonder, in which the surfaces are exposed to nitrogen free radicals by an *in-situ* surface activation tool to improve the hydrophilicity of the surface prior to bonding the two wafers by bringing them into contact. The physical contact of the wafers forms a temporary bond. To enhance the bond strength the bonded pair was annealed *ex-situ* in N₂ ambient at 300 °C for 24 h. As in process 1, the SOI handle wafer was then thinned by grinding, before a HF solution was used to remove the buried oxide. An optional dry etch to reduce the

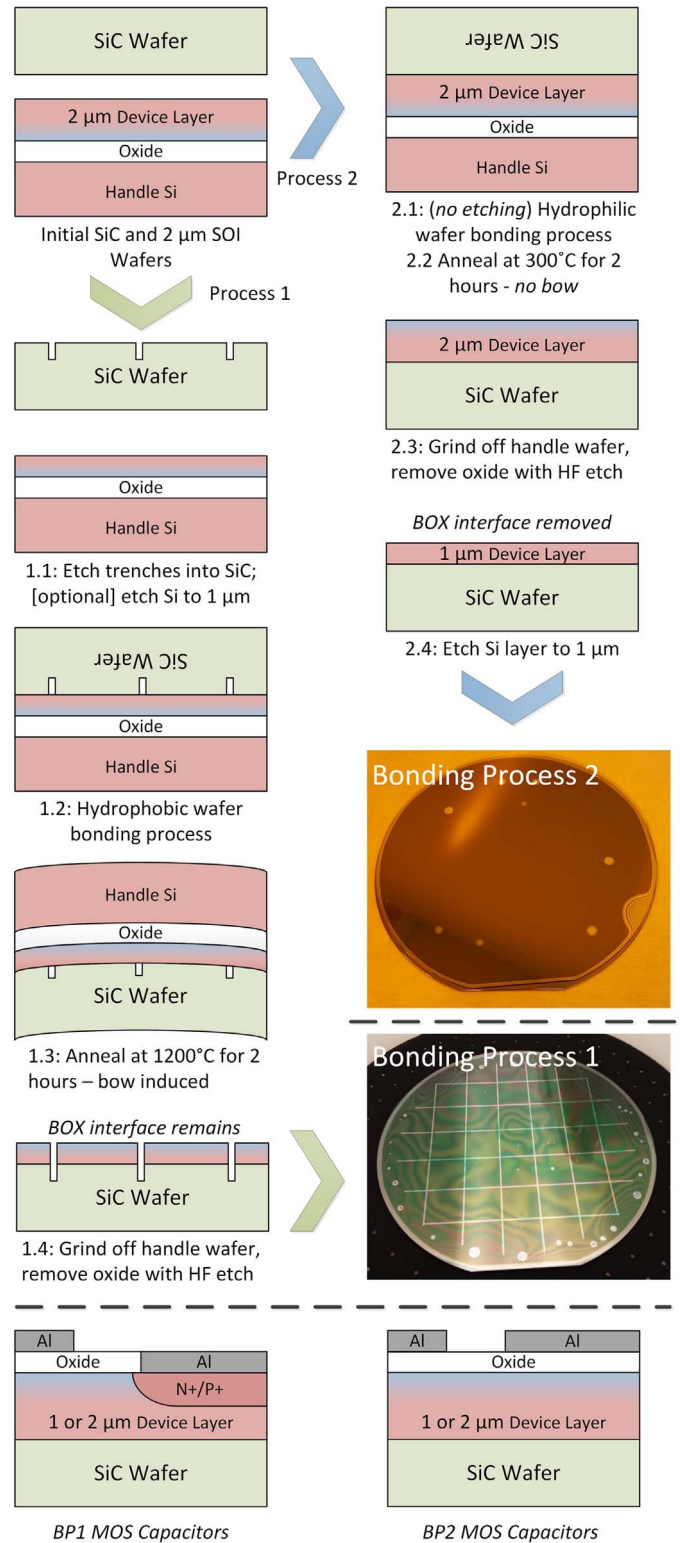


Fig. 2. Top: The two bonding processes described in the text, with images of the final bonded 100 mm Si/SiC substrates. Bottom: the two MOS capacitor structures used throughout.

device layer to 1 μm was then performed at the end of this process.

Laterally-contacted MOS Capacitors (LMOS-Cs) were formed on each Si/SiC substrate. These can be seen in Fig. 2. To fabricate the gate contact, the top Si surface was RCA cleaned before 55 nm of SiO₂ was thermally grown in dry oxygen (5 L/min) for 6 h followed by N₂O (1 L/min) annealing for 2 h, both at 900 °C. 300 nm Al was deposited as the

gate contact with a diameter of 400 μm . As will be discussed, the substrate contact was made by depositing Al onto either an implanted N⁺ or P⁺ contact surrounding the MOS gate, or a second MOS interface $100\times$ the area of the gate was used, to avoid adding further charge into the Si layer. The distance between gate and substrate contact was 120 μm . Finally, the samples were annealed in forming gas ($\text{H}_2:\text{N}_2 = 1:19$) at 450 $^\circ\text{C}$ for 2 h to reduce the MOS interface trap densities.

Identical LMOS-Cs formed on bulk Si, alongside the Si/SiC, showed consistent, frequency independent, responses suggesting that low resistance Ohmic contacts had been formed.

3. Results and discussion

3.1. Physical results

BP1 was developed after trials using a variety of the methods in the literature, previously described. Initial attempts to scale up a SmartCut process [13,14] to transfer 1 μm and 2 μm Si layers, across 100 mm wafers, resulted in poor yield due to inconsistent wafer splitting and unclean surfaces related to the processing prior to bonding. Bonding then grinding bulk Si [2] was not considered due to the fine control required to grind the substrate down to a final thickness of 1 μm . Instead, a SOI to semi-insulating (SI) SiC bonding process similar to [15] was chosen because the use of SOI allows the buried oxide to act as a natural etch stop region. Furthermore, in the decade since [15], the size, quality and price of SI 4H-SiC have all improved to such an extent that this has become a viable and cost-effective choice for 100 mm bonding to SOI, so reducing the cost-benefit of using poly-SiC [3].

LMOS-Cs, such as those seen in Fig. 2, were fabricated with N⁺ ohmic contacts on the 1 μm and 2 μm Si/SiC substrates produced using BP1. We previously reported [10] that C-V and I-V results from both diodes and LMOS-Cs suggested that the Si film after the layer transfer process appeared to be p-type, despite the use of n-type SOI and N⁺ ohmic contacts. These results can be seen in Fig. 3a and b where it appears that accumulation is occurring at a negative bias. Repeating these structures with P⁺ Ohmic contacts, resulted in the C-V characteristics of Fig. 3c and d. The two responses are very similar, with apparently characteristic p-type responses and little frequency dispersion. As such it appears that the original n-type Si response has been inverted.

Given the substrate fabrication methodology used, the cause of this inversion was considered most likely to be a result of interfacial charge at the Si/SiC and/or the Si/SiO₂ interface. TEM images of the Si/SiC interface [10], revealed voids or pits that were likely caused by strain induced by the high temperature anneal. It also showed that an inhomogeneous interfacial oxide was present at the Si/SiC interface, which varied in thickness from 0 to 2 nm across the wafer. Finally, with the Si etch having been performed on the SOI substrate prior to bonding, the Si/SiC top surface in both the 1 μm and 2 μm layers always originated from the Si/BOX interface of the SOI.

As a result of these findings, BP2 was developed, utilizing a 300 $^\circ\text{C}$, 24 h anneal to create a permanent bond between the layers without inducing strain. Despite the low temperature of this anneal, bond pull testing yielded a bond strength greater than 360 N, which was the limit of the equipment. Furthermore, etching the Si back to 1 μm after the wafers were bonded had the dual benefit of eliminating any processing prior to bonding (the etching of trenches in the SiC was also eliminated), and of etching away all the Si that originated from the area above the BOX in the SOI wafer. As a result of these changes, 97% yield was achieved across the 100 mm wafer. These can be seen in Fig. 2. TEM images revealed no voids at the interface and a uniform oxide layer at the Si/SiC interface of 1.4–1.8 nm thick. It has been reported [16] that this thin interfacial oxide can be removed with a high temperature anneal post-bond. Here, trials with an 1150 $^\circ\text{C}$, 4 h anneal resulted in the oxide being shrunk by 7–9%. Given such a marginal gain and a desire to limit the amount of high temperature processing, this

was not included.

LMOS-Cs, seen in Fig. 2, were fabricated in the 1 μm and 2 μm Si/SiC substrates resulting from BP2, and the resulting normalised C-V curves can be seen in Fig. 4. These were formed without P⁺ or N⁺ Ohmic contacts, given that both could potentially form p-n junction depletion regions and skew the C-V response. Instead, the ground contact was another MOS interface that is $> 100\times$ the area of the gate.

Fig. 4a shows that the 2 μm Si/SiC substrate still appears to be p-type with frequency dependent accumulation and depletion regions, just as they did in BP1. However, in Fig. 4b, the 1 μm Si/SiC substrate appears closer to an n-type response. This suggests that the Si material at, or just below, the surface of the 2 μm Si/SiC plays a major role in the inversion of the response of the original n-type Si. This area is represented throughout Fig. 2. Originating from just above the Si/BOX interface in the SOI, this region is present within the BP1 devices and the BP2 2 μm layer. While we cannot be certain of what effect this region has, it is likely that there is a high density of interfacial charge at the Si surface, while bulk charge, low lifetime and/or poor mobility, could all skew the C-V responses. Despite this improvement from the 2 μm to the 1 μm , the results of Fig. 4b still show that C_{OX} is not fully reached, with C_{OX} having been confirmed by bulk Si MOS capacitors produced together with these, with the same device structure. There also remains significant frequency dependence in both accumulation and depletion in nearly all the results. However, it is worth noting that the minima in the depletion capacitance occurs at a negative bias in this and every sample. This can be seen to be very similar to a simulation study performed on SOS [17]. There it is shown that the introduction of significant interfacial charge ($N_{IT} = 1\times 10^{12} \text{ cm}^{-2}$) at the n-Si/Al₂O₃ interface resulted in reduced accumulation values when the layer was fully depleted and that the depletion capacitance minima will still occur at a negative bias in n-type material. As such it is likely that in our Si/SiC devices, the influence of the bonded Si/SiC interface plays a similar role in causing these similar effects, given that the whole Si layer is low doped and thin enough to fully deplete.

A repeat of the BP2 LMOS-Cs with N⁺ ohmic contacts instead of the back-to-back MOS interfaces resulted in near-identical C-V responses.

3.2. Simulation results

The interpretation of C-V characteristics within thin SOI and SOS layers are complicated in the former case by the presence of the BOX [18,19], and in both cases by the presence of interface charge at the top and bottom interfaces [17–19]. Similarly, in the case of the Si/SiC substrate, it is clear from the experimental results that no one single measurable effect is causing the C-V results shown. It was therefore decided to use a finite-element modelling program (SILVACO) in an attempt to investigate some of the competing mechanisms at play. The 2D structure used was a half-cell reproduction of the BP1 1 μm Si/SiC LMOS-C that was produced experimentally, with N⁺ ohmic contacts and the same oxide and terminal dimensions. Initial simulations of this structure without any interfacial charge produced the dotted 100 kHz reference line in Fig. 5a.

Acceptor-like charge was introduced at the Si/SiC and MOS interfaces, where $N_{IT, Si/SiC} = 1\times 10^{13} \text{ cm}^{-2}$ and $N_{IT, MOS} = 6\times 10^{10} \text{ cm}^{-2}$, both at the Si midgap. In the simulation, as in the experimental LMOS-Cs, the gate oxide covers the entire top surface, and the charge is introduced along its length. In this simulation, no other effects, such as bulk charge, low lifetime or low mobility were introduced. The high level of Si/SiC charge employed was similar to that used by [20], which was based on experimental measurements.

The resulting simulation, seen in Fig. 5a, shows several similarities to the experimental results of BP2 in Fig. 4b. Firstly, the frequency dependent accumulation region is dictated by the level of surface charge introduced. Similar effects have been reported before [21,22], in which a high resistance feature (a poor ohmic contact or low-doped Si) is introduced in series with the MOS interface, causing reduced

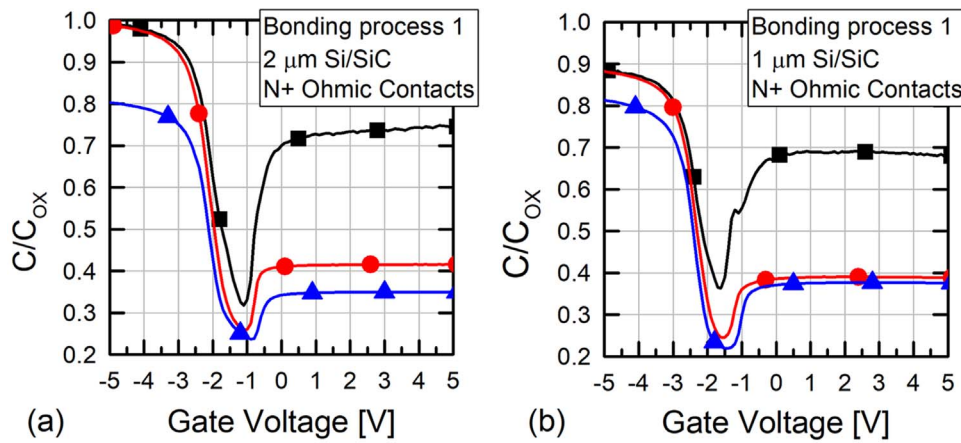


Fig. 3. The results of normalised C-V measurements on Si/SiC LMOS-Cs using BP1 and p-type Ohmic contacts on a) 2 μm and b) 1 μm Si device layers.

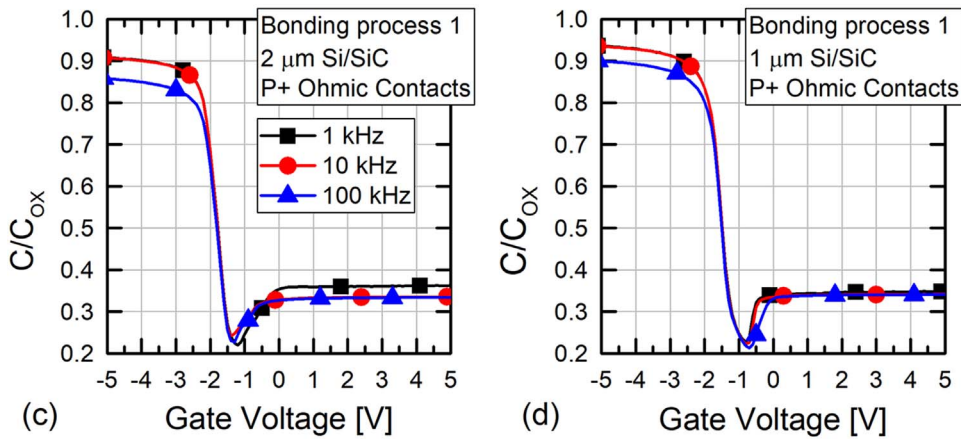
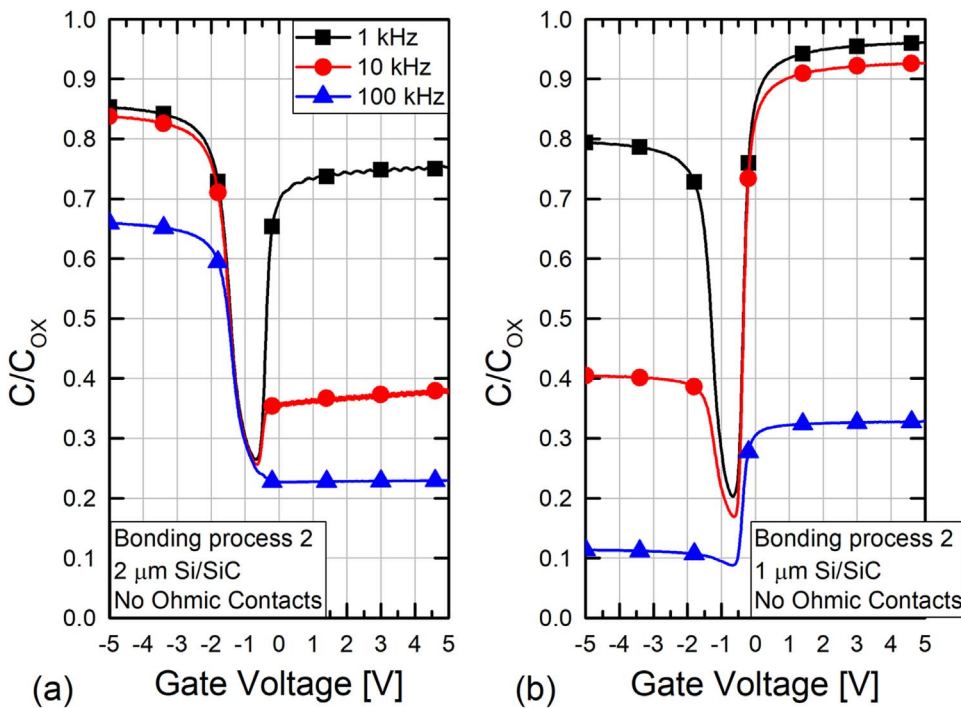


Fig. 4. The results of normalised C-V measurements on Si/SiC LMOS-Cs using BP2 without Ohmic contacts on a) 2 μm and b) 1 μm Si device layers.



accumulation. Here, the ohmic contacts were validated experimentally using bulk Si LMOS-Cs produced at the same time. In simulation, the ohmic contacts add no series resistance. Instead, iterative simulations revealed that the level of charge at the MOS interface had the largest

influence on the frequency dependence of the accumulation region. With the relatively low value of MOS charge, a depletion region forms along the top Si surface. This is then thought to reduce the capacitance and cause the frequency dependence by either adding a series

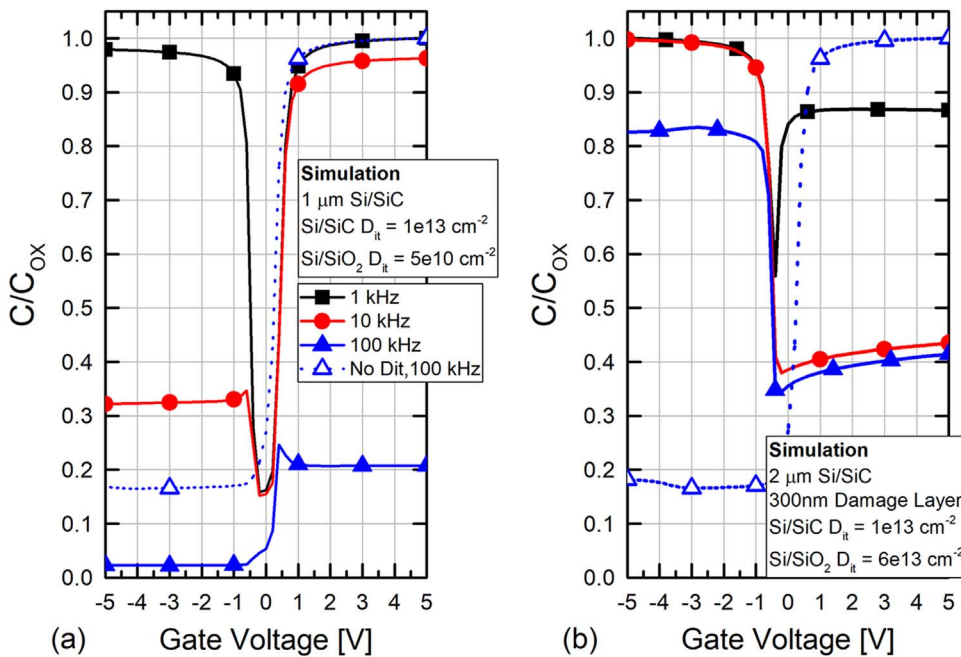


Fig. 5. a) The simulation results of normalised C-V measurements with and without interface charge on a) 1 μm Si/SiC LMOs-Cs, and b) 2 μm Si/SiC LMOs-Cs.

capacitance and/or by increasing the resistance by narrowing the effective width of the low-doped Si layer. The charge at the backside has a similar effect in effectively narrowing the thin Si layer. The simulations confirm that the depletion region reaches the Si/SiC interface as in [17].

In simulation, the degree of frequency dependence of the negative biased depletion region was controlled entirely by the amount of charge at the Si/SiC interface. This is similar to conventional deep depletion/inversion [23] brought about by a widening depletion region beneath the gate. However, the significant charge at the Si/SiC interface introduces a back depletion region in series, which lowers the total capacitance, as can be seen when comparing the 100 kHz signals with and without the Si/SiC charge.

A second simulation was attempted to apparently invert a 2 μm n-Si layer, as in the C-V response of Fig. 4a. This was not possible by simply introducing greater interfacial charge at the two interfaces due to the increased thickness of the Si layer, which prevents its full depletion. It was therefore necessary to introduce other factors, such as bulk charge, low lifetime and/or poor mobility to alter the charge density. This led to multiple degrees of freedom and a number of alternative ways that the response could be reproduced. However, our simulations showed that low lifetime (and hence high generation) was necessary in the Si layer, or at least just beneath the gate to create enough minority charge in depletion/inversion. A high density of acceptor-like MOS interface traps and acceptor-like bulk charge caused the n-type Si layer to be depleted at positive gate biases.

As one example, we proposed a region beneath the MOS interface of 300 nm that might have suffered damage in the processing that might cause the full inversion, such that its removal would result in the previous simulation of Fig. 5a. In this region, the carrier lifetime was reduced to 1 ps and acceptor-like bulk traps were introduced at a density of $1 \times 10^{16} \text{ cm}^{-3}$, at the Si mid-gap. At the MOS interface, deep interfacial charge ($E_C - 0.6 \text{ eV}$) of $N_{i,MOS} = 6 \times 10^{13} \text{ cm}^{-2}$ was introduced. This resulted in a C-V response quite similar to that achieved in Fig. 4a, the experimental results of the 2 μm BP2 Si/SiC layers.

In summary, the simulation allowed a better understanding of the experimental results in this paper. They show that just as in SOS [17], interfacial charge at the two Si interfaces can cause pinching of a thin, low doped Si region, leading to increased series resistance. They also suggest that the experimental results shown could originate from n-type

Si, despite looking as if they are p-type. However, the exact combination of physical mechanisms that determines this remains unknown.

4. Conclusions

Wafer bonded Si-on-SiC substrates have been developed in order to produce lateral power devices for harsh environment applications. 100 mm Si/SiC (1 and 2 μm Si on semi-insulating 4H-SiC) substrates have been produced with 97% yield as a result of a radical activation bonding process and low temperature processing. This improved process had a uniform oxide layer at the Si/SiC interface of 1.4–1.8 nm, without voids, so minimising charge density at this interface. C-V characterisation of these layers showed that the 2 μm layers appeared as if p-type, despite the original SOI being n-type. However, etching this back to 1 μm revealed an n-type-like response, though it still suffered frequency dispersion and incomplete accumulation. Simulations showed that this effect could be reproduced by the introduction of interfacial charge at the two interfaces. Finally, while one method of fully inverting the C-V response of an n-type 2 μm Si layer was shown, the exact reason for this remains unknown. Work continues to reduce the total charge at the Si/SiC interface to prevent high leakage and increased resistance effects when producing full lateral MOSFETs and IGBTs.

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