Improved Split CV Mobility Extraction in 28 nm Fully Depleted Silicon on Insulator Transistors

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***Abstract*— In this work, we assess the applicability of the well-known split CV technique for mobility extraction in 28 nm FDSOI transistors with gate length down to 25 nm using TCAD simulations. We identify the significant bias dependence of the parasitic source/drain resistance and the contribution of the inner fringing capacitance as the main sources of error in the conventional split CV extraction. An improved split CV method, correcting for these parasitics, is demonstrated to accurately extract the effective mobility and its dependence on the gate voltage for devices down to 25 nm gate length. Measurements on 28 FDSOI transistors confirm the insights from the TCAD simulations.**

***Index Terms*— FDSOI, UTBB, split CV, effective mobility.**

I. Introduction

EXTRACTION of the effective mobility μ_{eff} is of major importance to evaluate the performances of advanced transistors. This has become challenging in highly scaled nodes due to the increased relative importance of parasitics, thus requiring adaptations of the well-known methods to properly correct for them. The split current-voltage (CV) method [1] has regained attention for its robustness compared to other simple methods, and several modifications have been proposed to correct it for gate leakage, parasitic capacitances and access resistances [2]–[8]. In this letter, we apply the split CV method to advanced FDSOI devices by identifying and rigorously de-embedding the different parasitics affecting the extraction. We confirm and quantify their impact on the obtained μ_{eff} using TCAD simulations and propose an adapted method to correct for them, not requiring any pre-assumed mobility or inversion charge voltage dependence. It is validated experimentally on 28 FDSOI devices down to 25 nm gate length.

II. Extraction Procedure

The split CV method relies on the expression of the drain current I_D in strong inversion and linear regime, yielding [7]

$$\mu_{eff} = \frac{L_{eff}^2 I_D}{Q_i(V_{DS} - R_{SD} I_D)} \tag{1}$$

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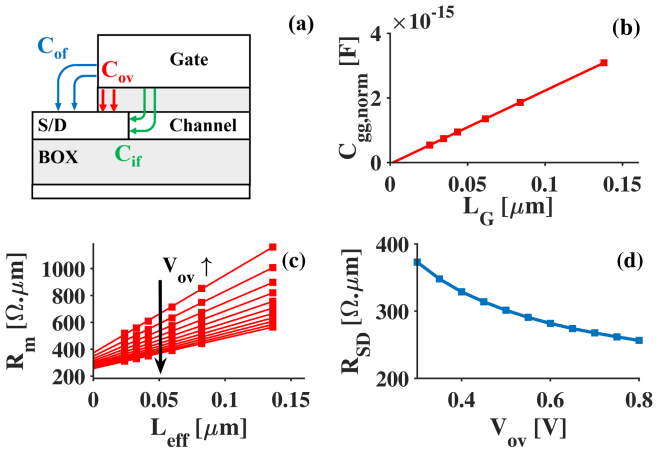

Fig. 1. (a) Parasitic gate capacitances as modeled in [7] (b) L_{eff} extraction by linear interpolation of TCAD $C_{gg,norm}(V_{ov,max} = 0.87\,\text{V}, V_{DS} = 0\,V)$ curves for $L_G = [25, 35, 45, 60, 90, 150]$ nm (c) R_{SD} extraction with the total resistance method for 10 equally spaced voltages in $V_{ov} = [0.3, 0.87]\,V, V_{DS} = 50\,mV$ (d) Extracted $R_{\text{SD}}(V_{ov})$ dependence.

The computation of μ_{eff} therefore requires precise extraction of the effective length L_{eff}, the total series access resistance R_{SD} and the inversion charge Q_i as discussed in the following.

A. Gate Capacitance and L_{eff} Extraction

Figure 1a shows the parasitic capacitances usually considered for advanced MOSFET's. The total gate capacitance writes $C_{gg}(V_{ov}, L_{eff}) = C_{inv}(V_{ov}, L_{eff}) + C_{ov} + C_{of}(L_{eff}) + C_{if}(V_{ov})$ where C_{inv} is the inversion capacitance, C_{ov}, C_{of}, C_{if} respectively the overlap, outer and inner fringing capacitances and $V_{ov} = V_{GS} - V_{TH}$ the overdrive voltage [7]. In order to remove the extrinsic contributions, one classically defines $C_{gg,norm}(V_{ov}) = C_{gg}(V_{ov}) - C_{gg}(V_{ov,min})$ with $V_{ov,min}$ biasing the device in accumulation [7], [9].

In contrast to bulk devices, in FDSOI the inner fringing capacitance is not shielded in accumulation due to the absence of dynamic majority carrier response [10], [11]. One then has

$$C_{gg,norm}(V_{ov}, L_{eff}) \approx C_{inv}(V_{ov}, L_{eff}) + C_{if}(V_{ov}) - C_{if}(V_{ov,min}) \tag{2}$$

which shows a parasitic contribution of the voltage-dependent inner fringing capacitance. Extraction of $L_{eff} = L_G - \Delta L$ is usually performed by interpolating $C_{gg,norm}$ extracted in strong inversion against the gate length L_G [12], [13]. Though the inner fringing capacitance is known to be shielded in strong

inversion [10], [14], it has been noted that the $C_{if}(V_{ov,min})$ term in Eq. (2) could disturb the extraction [11]. This will be assessed in Section III.

B. Bias Dependent R_{SD} Extraction

Correcting for the access resistance R_{SD} is a mandatory step in short transistors, where it can dominate the total device resistance. While several R_{SD} extraction methods are available in literature [15]–[17], they often neglect its bias dependence. However, in [17], [18] a significant dependence of R_{SD} on the gate voltage was reported in FDSOI and linked to the formation of a local inversion layer in the underlaps (i.e. beneath the spacers). This was shown to lead to an artificial degradation of the low-field mobility extracted using the Y function method [18]. Here, R_{SD} is therefore extracted for different overdrive voltages using the total resistance method [15], where R_{SD} is obtained as the linear interpolation at $L_{eff} = 0$ of the total device resistance $R_m(L_{eff}) = \frac{V_{DS}}{I_D}(L_{eff})$ curves (Fig. 1c).

C. Q_i Extraction Correcting for the Inner Fringing Capacitance

The inversion charge Q_i is ideally obtained as

$$Q_i(V_{ov}) = \int_{V_{ov}^*}^{V_{ov}} C_{inv}(V)dV \tag{3}$$

where V_{ov}^* is a bias voltage in accumulation (where C_{inv} is zero). Using $C_{gg,norm}$ as an approximation of C_{inv} in Eq. (3) results in a parasitic charge contribution due to the integration of the inner fringing terms in Eq. (2). In this work, we therefore rather model the total gate capacitance C_{gg} as

$$C_{gg} \approx A(V_{ov})L_{eff} + B(V_{ov}) \tag{4}$$

with $A(V_{ov}) = A_1(V_{ov}) + A_2$, $B(V_{ov}) = B_1(V_{ov}) + B_2$ and perform a linear interpolation of C_{gg} against L_{eff} to extract these coefficients (Fig. 2b). $A_1(V_{ov})$ can be attributed to the inversion capacitance and A_2 to the outer fringing capacitance per unit length. The $B(V_{ov})$ term corresponds to a usual parasitic capacitance plot extracted in a similar manner in [8], [17], [19]. $B_1(V_{ov})$ relates to the inner fringing behaviour, while B_2 is finally attributed to the overlap capacitance.

III. Results and Discussion

In this section, Synopsys Sentaurus TCAD simulations of $I_D(V_G)$ and $C_{gg}(V_G)$ (obtained from the simulated Y_{11} parameter) curves are used to validate the extraction procedure and quantify the impact of the different parasitics on the extracted mobility. The bulk and source contacts are kept to ground. The 2D simulated structure was provided by CEA-Leti and adequately reproduces the 28 nm FDSOI transistor geometry and doping profiles [20].

A gate bias dependent mobility model (including effects of dopant impurity scattering, velocity saturation and surface scattering) was implemented in the simulation.

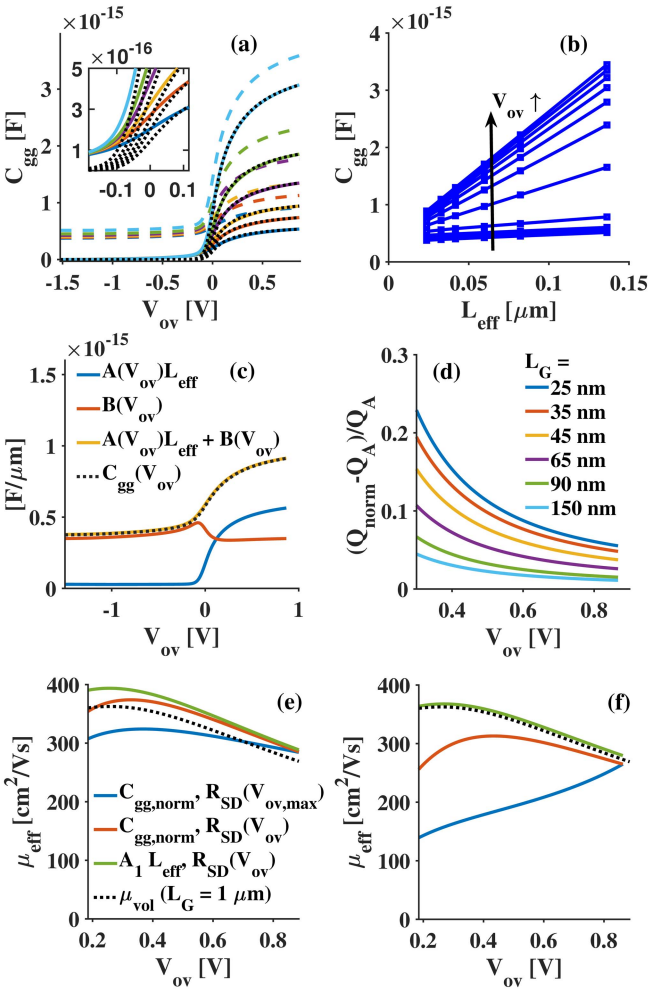

Fig. 2. (a) C_{gg} (dashed), $C_{gg,norm}$ (full) and $A_1 L_{eff}$ (black dots) for L_G = [25, 35, 45, 60, 90, 150] nm (colors correspond to the legend in (d)), V_{DS} = 50 mV, f = 100 kHz. The inset highlights the difference between $C_{gg,norm}$ and $A_1 L_{eff}$ due to the inner fringing terms. (b) Interpolation of C_{gg} against L_{eff} for 20 equally spaced overdrive voltages in V_{ov} = [−1.5, 0.87] V (c) Results from the linear interpolation of C_{gg} for a L_G = 25 nm transistor (d) Relative error between the charge extracted from $C_{gg,norm}$ (Q_{norm}) and from $A_1 L_{eff}$ (Q_A) for gate lengths between L_G = 25 nm and L_G = 150 nm (e),(f) μ_{eff} extraction for transistors with resp. L_G = 150 nm, L_G = 25 nm ($V_{ov,max}$ = 0.87 V). The effective mobility implemented in TCAD is estimated as $\mu_{vol} = \iint_S \mu(x,y)n(x,y)dxdy / \iint_S n(x,y)dxdy$ where S is the effective channel region. A long L_G = 1 μm transistor has been used to minimize the influence of the source and drain doping diffusions (corrected by R_{SD}) in the μ_{vol} estimation.

A. Parameters Extraction

1) Effective Length: Fig. 1b shows the extraction of L_{eff} as described in Section II-A. One obtains ΔL = 1.8 nm. We verified that the obtained $C_{gg,norm}/L_{eff}$ curves are well superimposed (not shown). Therefore, the influence of the $C_{if}(V_{ov,min})$ term (see Section II-A) is considered negligible, validating the obtained ΔL value in our case.

2) Access Resistance: Figure 1c shows the excellent linearity of $R_m(L_{eff})$ curves, validating the use of the total resistance method. A significant bias dependence of R_{SD}, by ≈ 50% from $V_{ov} = 0.3\,V$ to $V_{ov,max} = 0.87\,V$, as reported in [17], [18] is confirmed by our simulations.

3) Inversion Charge: Fig. 2b shows the linear interpolation of C_{gg} to extract the different coefficients described in

Section II-C. Results are shown on Fig. 2c. Eq.(4) is shown able to accurately model C_{gg} for both long and short transistors (with less than 2.5% error obtained for all gate lengths on the entire voltage range). The peak in $B(V_{ov})$ observed below threshold is characteristic of the inner fringing capacitance [8], [17]. From these insights, we can evaluate the impact of the inner fringing capacitance on the extraction of Q_i. The inset in Fig. 2a indeed highlights the difference between $C_{gg,norm}$ and $A_1(V_{ov})L_{eff} \approx C_{inv}$ due to the inner fringing terms in Eq. (2). As shown in Fig. 2d, one then obtains a significant overestimation of Q_i when integrating $C_{gg,norm}$ instead of $A_1(V_{ov})L_{eff}$, reaching 22% at $V_{ov} = 0.3\,V$ for a $L_G = 25\,\text{nm}$ transistor.

B. Impact on Mobility

Fig. 2e,f, quantitatively show the impact of the different parasitic terms on the extracted μ_{eff}. The simple split CV method (i.e. using $C_{gg,norm}$ and a single R_{SD} value extracted at $V_{ov,max}$) is shown unable to extract the implemented mobility behaviour in the short $L_G = 25\,\text{nm}$ transistor, confirming the need for careful de-embedding of the parasitics. Previous articles have discussed the influence of the R_{SD} bias dependence on the low-field mobility μ_0 extracted with the Y-function method, notably showing it generates an erroneous mobility degradation with L_G [17], [18]. However, its impact on split CV extracted mobility values and their behaviour with V_{ov} has to the author's knowledge not been reported up to now. As Fig. 2f shows, it is particularly significant in the short transistor. The obtained unphysical behavior (monotone increase of μ_{eff} with V_{ov}) is corrected when including the significant bias dependence of R_{SD}. The remaining error (when using $C_{gg,norm}$ but correcting for $R_{SD}(V_{ov})$) is most pronounced in the $L_G = 25\,\text{nm}$ transistor and at lower overdrive voltage. This is attributed to the inner fringing contribution in agreement with Fig. 2d. Using $A_1 L_{eff} \approx C_{inv}$ from the proposed modeling, we are then able to accurately extract the mobility behavior with V_{ov}. The extracted μ_{eff} is within less than 10% error of the estimated TCAD value for all gate lengths in the $0.3\,\text{V} < V_{ov} < 0.87\,\text{V}$ range, confirming the robustness of the proposed method.

IV. Validation on 28 FDSOI Measurements

Experimental data were finally used to verify the above insights. The measured devices are 28 FDSOI transistors from ST-Microelectronics [20] with $L_G = 25$, 35, 45, 60, 90 and 150 nm and $W = 120\,\mu m$. The gate capacitance (Fig. 3a) was extracted from the slope of $Im(Y_{11}) = 2\pi f C_{gg}$ by linear interpolation against the frequency over $f = [5, 10]\,\text{GHz}$ (Y parameters were obtained from open-pad de-embedded S parameters [21], bulk and source were kept to ground). Extraction of ΔL is performed as described above and gives $\Delta L = 6.5\,\text{nm}$ (inset in Fig. 3a). Figure 3b shows the extraction of $R_{SD}(V_{ov})$. The obtained bias dependence is in good agreement with the trend from Fig. 1d. The ability to model the total gate capacitance as $C_{gg} = A(V_{ov})L_{eff} + B(V_{ov})$ is then verified in Fig. 3c. The gate capacitance is reconstructed from its linear interpolation coefficients with less than 2.5% relative error for all lengths and overdrive voltages. Finally, Fig. 3d compares the extracted μ_{eff} when correcting for the different parasitics in both a long ($L_G = 150\,\text{nm}$) and short ($L_G = 25\,\text{nm}$) transistor. The results are in good agreement with the simulations presented in Fig. 2e,f.

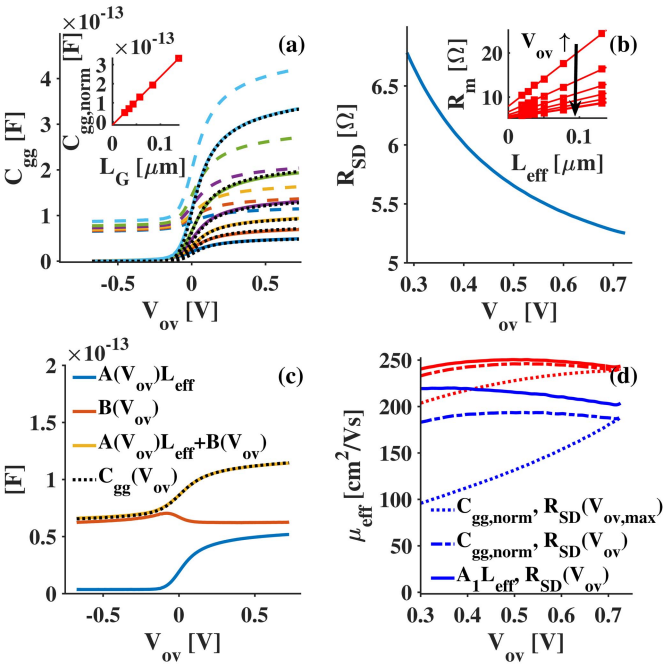

Fig. 3. (a) C_{gg} (dashed), $C_{gg,norm}$ (full) and $A_1 L_{eff}$ (black dots) from 28 FDSOI measurements for $L_G = [25, 35, 45, 60, 90, 150]$ nm (colors correspond to the legend in Fig. 2d) and $V_{DS} = 50$ mV. The inset shows the extraction of L_{eff}. (b) Extraction of bias dependent R_{SD} with the total resistance method. Inset: $R_m = \frac{V_{DS}}{I_D}$ versus L_{eff} for 6 equally spaced overdrive voltages in $V_{ov} = [0.2, 0.7]$ V (c) Results of the linear interpolation of C_{gg} for a $L_G = 25$ nm transistor (d) Extracted μ_{eff} for the $L_G = 150$ nm (red) and $L_G = 25$ nm (blue) transistors.

V. Conclusion

In this letter, we studied the application of the split CV method in 28 FDSOI transistors down to 25 nm gate length. The significant R_{SD} bias dependence related to the underlaps parasitic transistors was shown to have a major impact on the extracted mobility values and their evolution with the gate voltage. We also highlighted the impact of the inner fringing capacitance, whose contribution to the extracted charge was seen significant in short transistors. Correcting for these parasitics, the proposed method was shown able to extract μ_{eff} within 10% error and to accurately reproduce its dependence on the gate voltage for transistors down to 25 nm gate length. The extraction only relies on direct device measurements, not requiring any pre-assumed expression of the inversion charge or mobility dependence on the gate voltage.

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REFERENCES

[1] C. Sodini, T. Ekstedt, and J. Moll, "Charge accumulation and mobility in thin dielectric MOS transistors," *Solid-State Electron.*, vol. 25, no. 9, pp. 833–841, Sep. 1982, doi: 10.1016/0038-1101(82)90170-8.

[2] V. Kilchytska, D. Lederer, N. Collaert, J.-P. Raskin, and D. Flandre, "Accurate effective mobility extraction by split C-V technique in SOI MOSFETs: Suppression of the influence of floating-body effects," *IEEE Electron Device Lett.*, vol. 26, no. 10, pp. 749–751, Oct. 2005, doi: 10.1109/LED.2005.855408.

[3] T. Rudenko, N. Collaert, S. De Gendt, V. Kilchytska, M. Jurczak, and D. Flandre, "Effective mobility in FinFET structures with HfO_2 and SiON gate dielectrics and TaN gate electrode," *Microelectronic Eng.*, vol. 80, pp. 386–389, Jun. 2005, doi: 10.1016/j.mee.2005.04.026.

[4] S.-I. Takagi and M. Takayanagi, "Experimental evidence of inversion-layer mobility lowering in ultrathin gate oxide metal-oxide-semiconductor field-effect-transistors with direct tunneling current," *Jpn. J. Appl. Phys.*, vol. 41, no. 1, pp. 2348–2352, Apr. 2002, doi: 10.1143/JJAP.41.2348.

[5] F. Lime, C. Guiducci, R. Clerc, G. Ghibaudo, C. Leroux, and T. Ernst, "Characterization of effective mobility by split C(V) technique in N-MOSFETs with ultra-thin gate oxides," *Solid-State Electron.*, vol. 47, pp. 1147–1153, Jul. 2003, doi: 10.1016/S0038-1101(03)00049-2.

[6] P. M. Zeitzoff, C. D. Young, G. A. Brown, and Y. Kim, "Correcting effective mobility measurements for the presence of significant gate leakage current," *IEEE Electron Device Lett.*, vol. 24, no. 4, pp. 275–277, Apr. 2003, doi: 10.1109/LED.2003.812140.

[7] K. Romanjek, F. Andrieu, T. Ernst, and G. Ghibaudo, "Improved split CV method for effective mobility extraction in sub-0.1-μm Si MOSFETs," *IEEE Electron Device Lett.*, vol. 25, no. 8, pp. 583–585, Aug. 2004, doi: 10.1109/LED.2004.832786.

[8] L. Trojman, L.-Å. Ragnarsson, and N. Collaert, "Mobility extraction for short channel UTBB-FDSOI MOSFETs under back bias using an accurate inversion charge density model," *Solid-State Electron.*, vol. 154, pp. 24–30, Apr. 2019, doi: 10.1016/j.sse.2019.02.003.

[9] E. San Andres, L. Pantisano, J. Ramos, S. Severi, L. Trojman, S. De Gendt, and G. Groeseneken, "RF split capacitance–voltage measurements of short-channel and leaky MOSFET devices," *IEEE Electron Device Lett.*, vol. 27, no. 9, pp. 772–774, Sep. 2006, doi: 10.1109/LED.2006.881089.

[10] M. Wiatr, P. Seegebrecht, and H. Peters, "Charge based modeling of the inner fringing capacitance of SOI-MOSFETs," *Solid-State Electron.*, vol. 45, no. 4, pp. 585–592, Apr. 2001, doi: 10.1016/S0038-1101(01)00082-X.

[11] I. Ben Akkez, A. Cros, C. Fenouillet-Beranger, P. Perreau, A. Margain, F. Boeuf, F. Balestra, and G. Ghibaudo, "Characterization and modeling of capacitances in FD-SOI devices," in *Proc. Ulis Ultimate Integr. Silicon*, Mar. 2011, pp. 1–4, doi: 10.1109/ULIS.2011.5757984.

[12] M. Mouis and G. Ghibaudo, *Accurate Determination of Transport Parameters in Sub-65 nm MOS Transistors*. Hoboken, NJ, USA: Wiley, ch. 14, pp. 475–544, doi: 10.1002/9781118621523.ch14.

[13] T. S. Hsieh, Y. W. Chang, W. J. Tsai, and T. C. Lu, "A new L_{eff} extraction approach for devices with pocket implants," in *Proc. Int. Conf. Microelectron. Test Struct.*, Feb. 2011, pp. 15–18, doi: 10.1109/ICMTS.2001.928630.

[14] F. Prégaldiny, C. Lallement, and D. Mathiot, "A simple efficient model of parasitic capacitances of deep-submicron LDD MOSFETs," *Solid-State Electron.*, vol. 46, no. 12, pp. 2191–2198, Dec. 2002, doi: 10.1016/S0038-1101(02)00248-4.

[15] D. K. Schroder, Ed., "Series resistance, channel length and width, and threshold voltage," in *Semiconductor Material and Device Characterization*. Hoboken, NJ, USA: Wiley, 2005, doi: 10.1002/0471749095.ch4.

[16] D. Fleury, A. Cros, G. Bidal, J. Rosa, and G. Ghibaudo, "A new technique to extract the source/drain series resistance of MOSFETs," *IEEE Electron Device Lett.*, vol. 30, no. 9, pp. 975–977, Sep. 2009, doi: 10.1109/LED.2009.2026592.

[17] J.-B. Henry, A. Cros, J. Rosa, Q. Rafhay, and G. Ghibaudo, "New access resistance extraction methodology for 14 nm FD-SOI technology," in *Proc. Int. Conf. Microelectron. Test Struct. (ICMTS)*, Mar. 2016, pp. 70–74, doi: 10.1109/ICMTS.2016.7476177.

[18] F. Monsieur, Y. Denis, D. Rideau, V. Quenette, G. Gouget, C. Tavernier, H. Jaouen, G. Ghibaudo, and J. Lacord, "The importance of the spacer region to explain short channels mobility collapse in 28 nm bulk and FDSOI technologies," in *Proc. 44th Eur. Solid State Device Res. Conf. (ESSDERC)*, Sep. 2014, pp. 254–257, doi: 10.1109/ESSDERC.2014.6948808.

[19] S. Severi, G. Curatola, C. Kerner, and K. De Meyer, "Accurate channel length extraction by split C-V measurements on short-channel MOSFETs," *IEEE Electron Device Lett.*, vol. 27, no. 7, pp. 615–618, Jul. 2006, doi: 10.1109/LED.2006.877711.

[20] N. Planes, O. Weber, V. Barral, S. Haendler, D. Noblet, D. Croain, M. Bocat, P.-O. Sassoulas, X. Federspiel, A. Cros, A. Bajolet, E. Richard, B. Dumont, P. Perreau, D. Petit, D. Golanski, C. Fenouillet-Beranger, N. Guillot, M. Rafik, V. Huard, S. Puget, X. Montagner, M.-A. Jaud, O. Rozeau, O. Saxod, F. Wacquant, F. Monsieur, D. Barge, L. Pinzelli, M. Mellier, F. Boeuf, F. Arnaud, and M. Haond, "28nm FDSOI technology platform for high-speed low-voltage digital applications," in *Proc. Symp. VLSI Technol. (VLSIT)*, Jun. 2012, pp. 133–134, doi: 10.1109/VLSIT.2012.6242497.

[21] B. Kazemi Esfeh, V. Kilchytska, V. Barral, N. Planes, M. Haond, D. Flandre, and J.-P. Raskin, "Assessment of 28 nm UTBB FD-SOI technology platform for RF applications: Figures of merit and effect of parasitic elements," *Solid-State Electron.*, vol. 117, pp. 130–137, Mar. 2016, doi: 10.1016/j.sse.2015.11.020.