

High Resistivity SOI wafer for mainstream RF System-on-Chip

Invited paper

Jean-Pierre Raskin¹ and Eric Desbonnets²

¹ Université catholique de Louvain (UCL), Institute of Information and Communication Technologies, Electronics and Applied Mathematics, Place du Levant, 3, B-1348 Louvain-la-Neuve, Belgium
Phone: +32.10.47.23.09, jean-pierre.raskin@uclouvain.be

² Soitec, Parc Technologique des Fontaines, 38190 Bernin, France
eric.desbonnets@soitec.com

Systems-on-Chip (SoC) and Systems-in-Package (SiP) are the most feasible solutions to fulfil the requirements of the new communication systems. Both solutions will lead to a fundamental change in the design of analogue front-end architectures. It requires a high performance technology with devices that provide complex digital functionalities and can easily achieve operating frequencies in the GHz range. Therefore, it appears that only the best submicron CMOS technologies could provide a feasible and cost-effective integration of the communication systems. SOI MOSFET technology has demonstrated its potentialities for high frequency reaching cut-off frequencies close to 500 GHz for nMOSFETs and for harsh environments (high temperature, radiations). Partially depleted (PD) SOI is now massively serving the 45-nm digital market where it is seen as a low-cost – low-power alternative to bulk Si. Fully depleted (FD) devices are also widely spread as they outperform existing semiconductor technologies for extremely low power analogue applications. For RF and SoC applications, SOI also presents the major advantage of providing high resistivity (HR) substrate capabilities, leading to substantially reduced substrate losses. Substrate resistivity values higher than 1 k Ω -cm can easily be achieved and High Resistivity Silicon (HR-Si) is commonly foreseen as a promising substrate for radio frequency integrated circuits (RFIC) and mixed signal applications.

The use of high resistivity substrates is mandatory for the design of high performance RF circuits. HR-Si cannot be introduced in the case of bulk Si MOSFETs due to latch-up problem between devices. In SOI technology, the buried oxide (BOX) isolates the thin top silicon from the Si substrate which can then be turned to high resistivity characteristic without impacting the good behaviour of the MOS ICs.

In collaboration with UCL, Soitec has reached an early milestone in the fast-paced and widespread adoption of its proprietary Enhanced Signal Integrity™ (eSI) substrates. Soitec eSI substrates are the substrate of choice for manufacturing cost effective and high-performance radio-frequency (RF) devices providing a power boost for 4G /LTE applications. eSI offers the best cost performance trade-off, Soitec is seeing very strong and growing market demand from most of the leading RF foundries. These customers are already shipping wireless communication ICs built on eSI substrates. As a result, Soitec is now shipping more eSI products than high-resistivity silicon-on-insulator (HR-SOI) wafers, which are also used in fabricating RF devices.

Experimental results of active and passive RF devices built on eSI substrate will be presented and compared with other Si-based and RF substrates. Potential solutions to still improve the substrate performance will be shortly described.