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Characterization of thin Al_2O_3/SiO_2 dielectric stack for CMOS transistors

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ABSTRACT

This paper systematically investigates the electrical properties of thin Al_2O_3/SiO_2 (with a target equivalent oxide thickness of 4.9 nm) as gate dielectric stack in the metal–oxide–semiconductor (MOS) capacitor. Different deposition techniques, i.e. thermal oxidation, thermal atomic layer deposition, and plasma-enhanced atomic layer deposition, are employed in the fabrication of MOS capacitors. The second derivative, Terman and conductance methods are used to extract the fixed oxide charges and interface trap densities in the MOS capacitors. Our results demonstrate that the Al_2O_3/SiO_2 stack presents better performance in terms of negative fixed oxide charges and low interface trap density compared with the single-layer SiO_2 with the similar equivalent oxide thickness about 3.9 nm. Furthermore, to evaluate the reliability of the Al_2O_3/SiO_2 gate dielectric stack, the leakage current is analyzed. Contributions from Pool-Frenkel emission, trap-assisted tunneling, and Fowler-Nordheim mechanisms to the leakage current are detailed. Our results indicate that Al_2O_3/SiO_2 gate dielectric stacks fabricated by plasma-enhanced atomic layer deposition Al_2O_3 and thermal SiO_2 feature the lowest leakage current.

1. Introduction

The semiconductor industry targets of high performance, high speed, low power consumption and high density of transistors on a wafer have been achieved by reducing the di-mensions of the metal-oxide-semiconductor field-effect transistor (MOSFET). This leads to replacing the silicon dioxide SiO_2 gate dielectric by high-*k* dielectric, considering Al_2O_3, ZrO_2 and eventually HfO_2 as the industrial reference. Suitable gate dielectric material properties must include, concurrently, (i) a high relative dielectric constant (*k*) for high field-effect gate control with the same electrical thickness, (ii) a large energy bandgap for minimizing the gate leakage current, (iii) a low interface trap density (D_{it}) for preventing Fermi level pinning and charge carrier mobility degradation, and (iv) a thermo-dynamic stability close to silicon for reliable transistor fabrica-tion. Moreover, according to the requirement of sustainable development, we should avoid to use scarce metals for high-*k* oxides. Hf-based gate oxides have become the standard for CMOS nodes below the 45 nm, i.e. for equivalent oxide thick-nesses (EOT) ranging from 1.2 to 4.5 nm [1]. Aluminum oxide (Al_2O_3) has been considered in the past for its high *k* value, but too high D_{it} and interface charge scattering, thereby decreasing the channel mobility of transistors have been reported.

Kessel et al. [2] believed that this issue was related to an interfacial SiO_2-like layer SiO_x (~1–2 nm) existing between [1]Al_2O_3 and Si. The reduction of D_{it} can be achieved by inserting a thermally-grown high-quality SiO_2 film between Al_2O_3 and Si [1] to form a gate dielectric stack. Recently, high negative fixed oxide charges (Q_f), sufficiently low D_{it} and sustainable material usage have been investigated in Atomic-layer-deposited (ALD) Al_2O_3 layers for solar cells [3]. Therefore, the questions are: "Could these features be of interest and application for CMOS at the 65 nm node and beyond?" and "Could thicker high- *k* gate oxides be used in advanced nodes for special analog or I/O (input/

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Table 1
Targeted and measured thickness of samples (Targeted EOT = 3.9 nm).

Sample number	Dielectric stack	Targeted thickness (nm)	Measured thickness (nm)*	Calculated EOT (nm)**
1	Thermal SiO_2	3.9	3.9 ± 0.1	3.9
2	PE-ALD Al_2O_3/ thermal SiO_2	3.5/2	2.8 ± 0.1/2.5	4.9
3	T-ALD Al_2O_3/ thermal SiO_2	3.5/2	3.2 ± 0.2/2.5	5.0
4	PE-ALD Al_2O_3/ PE-ALD SiO_2	3.5/2	3.7 ± 0.2/2.5	5.8
5	T-ALD Al_2O_3/ PE-ALD SiO_2	3.5/2	3.5 ± 0.2/2.5	5.6

* Measured thickness in nm is the average value of 16 points on one sample.
** Calculated EOT is calculated with the measured thickness of each layer and theoretical permittivity.

output) functions?" Negative Q_f indeed results in a shift of threshold voltage (V_{th}) towards more positive values in nMOS devices. This could be exploited to decrease the doping concentration in the channel for compensating V_{th} change, simultaneously increasing channel mobility [4] and potentially decreasing variability.

In this article, we fabricate and characterize MOS capacitors based on Al_2O_3/SiO_2 gate dielectric stacks with a target equivalent oxide thickness (EOT) of 4.9 nm. In Section II, the device fabrication and electrical characterization techniques are introduced. Section III details different extraction methodologies (including an equivalent circuit model) of Q_f, flatband voltage (V_{fb}), and D_{it}. In Section IV, leakage currents and tunneling mechanisms through the different gate dielectric stacks are investigated. Finally, conclusions are drawn from the analysis of gate-dielectric-stack MOS capacitors in Section V.

2. Fabrication and characterization techniques

2.1. Sample fabrication

Before describing the fabrication of MOS capacitors, we define the EOT of the gate dielectric stack according to the combined capacitance of two dielectrics in series:

$$t_{EOT} = t_{SiO_2} + \left(k_{SiO_2}/k_{Al_2O_3}\right)t_{Al_2O_3} \quad (1)$$

where t_{SiO_2} and $t_{Al_2O_3}$are the thicknesses of interfacial layer SiO_2 and Al_2O_3, respectively, with relative dielectric constant $k_{SiO_2} = 3.9$ and $k_{Al_2O_3} = 9$.

In this work, we prepare four kinds of gate dielectric stacks. Prior the gate stack formation, 3-in. Si substrates (⟨100⟩, *p*-type, 10 Ω·cm, single-side polished) were cleaned by Piranha solution (3:1: H_2SO_4:H_2O_2 for a duration of 20 min at 110 °C). After the Piranha cleaning, all the wafers were dipped in dilute HF solution (1:50: HF:Deionized water) to remove the native oxide. Then the substrates were immediately put into a Fiji F200 ALD machine or Koyo Thermal system for, respectively, depositing Al_2O_3 or oxidizing Si to thermal SiO_2.

Table 1 gives an overview of the different gate stacks studied in this work. Sample 1, 3.9-nm-thick thermal SiO_2 grown on Si substrate at 900 °C in an ultra-dry oxygen atmosphere for 30 min, is used as a reference sample. For samples 2 and 3, the same fabrication process was used to grow 2-nm-thick thermal SiO_2 by reducing growth time. Otherwise, for samples 4 and 5, 2-nm-thick SiO_2 was deposited by plasma enhanced atomic layer deposition (PE-ALD), using tris(dimethylamino) silane and O_2 radical as, respectively, Si and O sources at 250 °C. In Table 1, 3.5-nm-thick Al_2O_3 layers were deposited by thermal atomic layer deposition (T-ALD) or PE-ALD at 200 °C, respect-tively. In both cases, trimethylaluminum precursor (TMA) from Sigma-Aldrich was used as aluminum source. Deionized water pulses and oxygen flows were used for T-ALD and PE-ALD, respectively. In T-ALD, TMA and H_2O pulses duration was 0.06 s and purge time was 10 s. In PE-ALD, TMA pulse duration and purge time of, respectively, 0.06 and 10 s were used. The pulse duration and purge time of the O_2 plasma were 20 s and 5 s, respectively. An O_2 flow of 30 sccm and a plasma power of 300 W were used. The growth rate of Al_2O_3 was 1 Å per cycle for both PE-ALD and T-ALD. After deposition, the thicknesses were mapped by ellipsometry over the wafer.

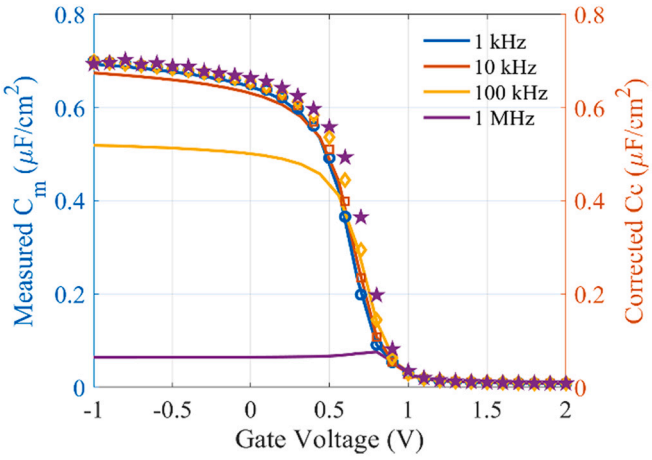

Fig. 1. Measured capacitance (lines) versus gate voltage at different frequencies for sample 2, showing frequency dependence in accumulation. Corrected curves (symbols) after removing effect of series resistance R_s.

In order to measure MOS capacitor characteristics (*C*—*V*, *G*-*V*, and *I*-*V*) with Mercury Probe Station, a 300-nm-thick Al layer was deposited on the backside of the Si wafer using E-gun evaporation. Before the evaporation, the backside of the Si wafers was dipped in BHF to remove the native oxide for ensuring an ohmic contact. Finally, all the samples were annealed in forming gas (N_2: H_2 = 9: 1) at 432 °C for 30 min.

2.2. C—V, G-V and I-V techniques

Capacitance-voltage (*C*—*V*) and conductance-voltage (*G*-*V*) measurements were performed using Mercury Probe Station and HP 4284A LCR meter at different frequencies from 1 kHz to 1 MHz. The use of mercury probe allows to avoid the deposition of metal electrodes on top of the stacks, which simplifies the fabrication process of the MOS capacitors. In order to obtain accurate and reliable measurement results, the following factors are important: (i) before starting *C*—*V* measurements, the electrical equilibrium and the initial state of the device must be ensured. For this purpose, we used sufficient hold time (5 s) and delay time (2 s) for each sweep step and each bias point, respectively; (ii) the series resistances coming from the substrate and dielectric leakage in the *C*-*G* equivalent circuit must be de-embedded; (iii) the parasitic capacitance coming from interconnect cables of instruments must be withdrawn. Tunneling current-voltage (*I*-*V*) measurements were carried out by B1500 Semiconductor Device Analyzer. All the measurements were carried out at room temperature.

In this work, Terman [5] and Conductance [6] methods are used and compared to extract D_{it} at the gate dielectric/Si interface. Conductance method was shown to yield more accurate and reliable results, particularly when the D_{it} is low. Applying both methods makes the analysis more robust.

3. Results and discussion

3.1. Series resistance extraction

Fig. 1 shows an example of *C*—*V* curves measured on MOS capacitors at various frequencies. A large dispersion in strong accumulation region

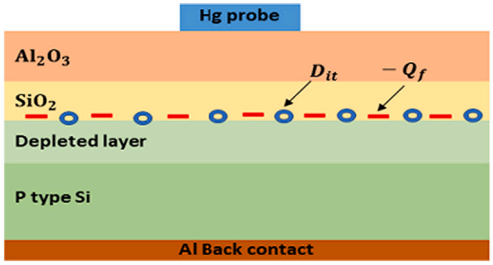

Fig. 2. Cross-section of a MOS capacitor with the Al_2O_3/SiO_2 stack.

is observed due to the large existing series resistance (R_s) originating from the Si substrate. Therefore, to correctly interpret the data, R_s needs to be de-embedded from the measurement data. This requires a small-signal equivalent circuit modeling of the MOS capacitor.

The cross-section of a MOS capacitor with the Al_2O_3/SiO_2 gate stack is illustrated in Fig. 2. In order to model the MOS capacitor with multi-layer gate dielectric stack, C_{Al2O3} is defined as the capacitance of Al_2O_3, C_{il} and G_{il} are the capacitance and conductance of interfacial layer (IL) SiO_2, C_{ox} is the total capacitance of the Al_2O_3/SiO_2 dielectric stack, C_d and G_{it} are the capacitance of depletion layer and the conductance of interface traps between gate dielectric stack and Si substrate, and R_s is the total series resistance. *Hg* probe acts as the top electrode.

Fig. 3a depicts the equivalent circuit of a MOS capacitor with the Al_2O_3/SiO_2 gate stack. As shown in Fig. 3b, for simplification purposes, G_{Al2O3} and C_{Al2O3} elements are replaced by C_{r1} and R_{r1} in series, G_{il} and C_{il} elements are replaced by C_{r2} and R_{r2} in series as given by:

$$C_{r1} = \frac{G_{Al2O3}{}^2 + \omega^2 C_{Al2O3}{}^2}{\omega^2 C_{Al2O3}} \text{ and } G_{r1} = \frac{G_{Al2O3}}{G_{Al2O3}{}^2 + \omega^2 C_{Al2O3}{}^2} \tag{2}$$

$$C_{r2} = \frac{G_{il}{}^2 + \omega^2 C_{il}{}^2}{\omega^2 C_{il}} \text{ and } G_{r2} = \frac{1}{R_{r2}} = \frac{G_{il}}{G_{il}{}^2 + \omega^2 C_{il}{}^2} \tag{3}$$

Where $\omega = 2\pi f$. The total impedance of the simplified circuit in Fig. 3b is:

$$Z_m = \frac{1}{G_m + j\omega C_m} \tag{4}$$

Here G_m and C_m denote, respectively, the conductance and capacitance values measured in the experiments. In strong accumulation region, C_d and G_{it} can be neglected and the equivalent circuit in Fig. 3b is further simplified to that in Fig. 3c, in which R_s' is the total series resistance:

$$R_s' = R_s + R_r \tag{5}$$

where $R_r = R_{r1} + R_{r2}$. In this case, the measured accumulation impedance Z_{ma} can be expressed as:

$$Z_{ma} = \frac{1}{G_{ma} + j\omega C_{ma}} \tag{6}$$

or

$$Z_{ma} = R_s' - j\frac{C_{r1} + C_{r2}}{\omega C_{r1} C_{r2}} \tag{7}$$

where C_{ma} and G_{ma} are the measured accumulation capacitance and conductance, respectively. Comparing the real and imaginary parts of Eqs. (6) and (7), we obtain:

$$R_s' = \frac{G_{ma}}{G_{ma}^2 + \omega^2 C_{ma}^2} \tag{8}$$

$$C_{r2} = \frac{-C_{r1}\left(G_{ma}^2 + \omega^2 C_{ma}^2\right)}{\omega^2\left(C_{ma}^2 - C_{ma}G_{ma}\right) + G_{ma}^2} \tag{9}$$

$$Z_c = \frac{1}{G_c + j\omega C_c} = Z_m - Z_s \tag{10}$$

$$Z_s = R_s' + \frac{1}{j\omega Cr2} \tag{11}$$

Finally, C_c and G_c are the corrected capacitance and conductance of the Al_2O_3/SiO_2 dielectric stack after removing R_s, respectively. The total stack capacitance C_{ox} is obtained from the plateau of C_c in strong accumulation. By substituting Eqs. (4) and (11) into Eq. (10), we obtain

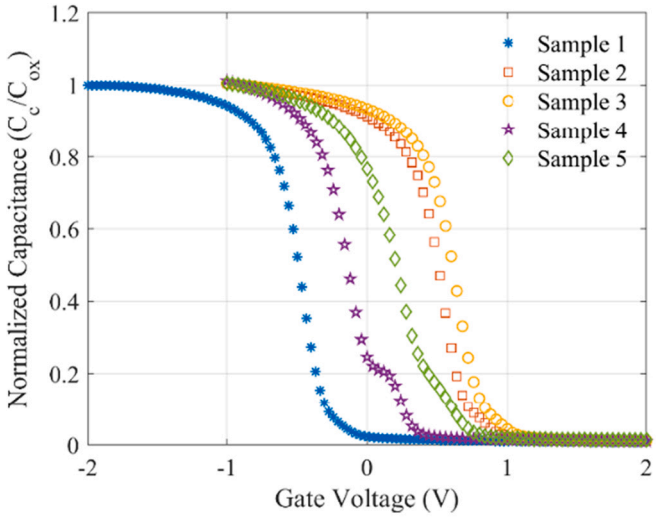

Fig. 4. Normalized corrected C_c-V characteristics for different dielectric stacks at 1 kHz after removing series resistance.

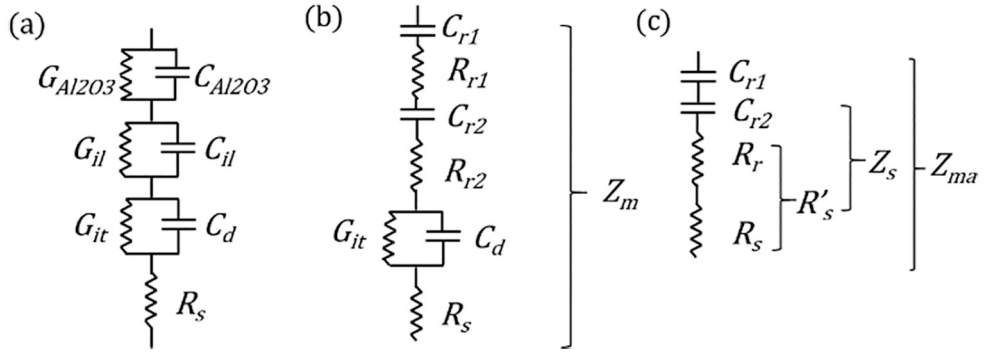

Fig. 3. (a) Equivalent circuit of a MOS capacitor with Al_2O_3/SiO_2 gate stack. (b) Simplified circuit of (a). (c) Simplified circuit in strong accumulation regime.

Table 2
Summary of the extracted values including fiatband voltages (V_{fb}), ffxed oxide charges (Q_f), interface trap density (D_{it}), and leakage current (J_{leak}).

Sample number	Dielectric stack	Calculated EOT (nm)	Gate stack C_{ox} (F/cm^2)	V_{fb} (V)	D_{it} (cm^{-2} eV^{-1}) (Terman method)	D_{it} (cm^{-2} eV^{-1}) (Conductance method)	Q_f (cm^{-2})	J_{leak} (A/cm^2@1 V)
1	Thermal SiO2	3.9	1.0×10^{-6}	- 0.72	2.31×10^{10}	2.00×10^{10}	$+ 1.89 \times 10^{12}$	5.56×10^{-8}
2	PE-ALD Al_2O_3/ thermal SiO_2	4.9	7.0×10^{-7}	+ 0.61	5.60×10^{10}	5.20×10^{10}	$- 4.57 \times 10^{12}$	5.06×10^{-9}
3	T-ALD Al_2O_3/ thermal SiO_2	5.0	6.9×10^{-7}	+ 0.69	6.86×10^{10}	6.21×10^{10}	$- 4.92 \times 10^{12}$	6.87×10^{-9}
4	PE-ALD Al_2O_3/PE-ALD SiO_2	5.8	6.0×10^{-7}	- 0.06	2.82×10^{11}	2.61×10^{11}	$- 1.45 \times 10^{12}$	1.52×10^{-7}
5	T-ALD Al_2O_3/PE-ALD SiO_2	5.6	6.2×10^{-7}	+ 0.31	1.95×10^{11}	1.88×10^{11}	$- 2.79 \times 10^{12}$	6.24×10^{-8}

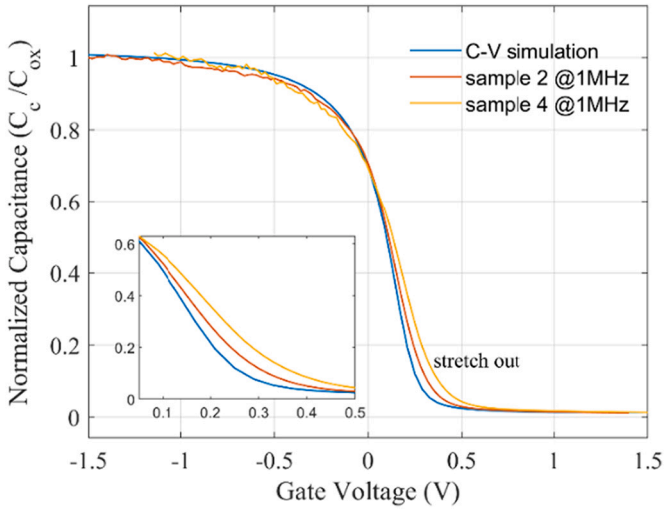

Fig. 5. Corrected (red and orange) and simulated (blue) C_c-V charac-teristics after subtracting V_{fb} at 1 MHz for samples 2 and 4, in which the inset shows the stretch-out in depletion region due to the existing of D_{it}. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

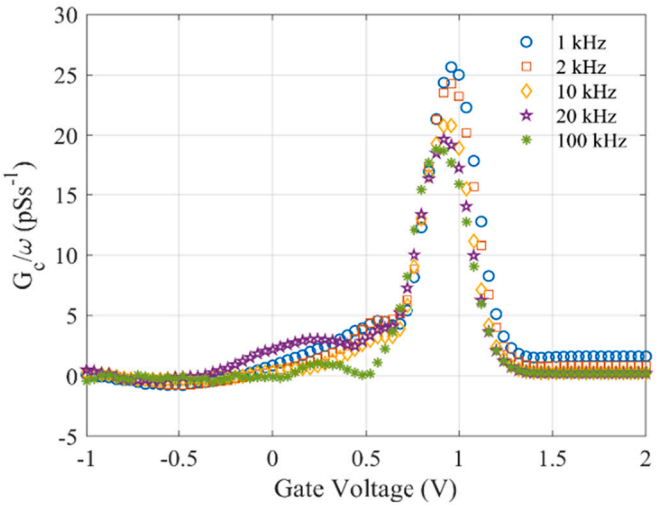

Fig. 6. Corrected G_c-V characteristics for sample 2 at different fre-quencies, in which D_{it} can be extracted by using the conduction method.

the corrected C_c and G_c without frequency dispersion [7]:

$$C_c = \frac{\left(\omega^2 C_m C_{r2} - G_m^2 - \omega^2 C_m^2\right)\left(G_m^2 + \omega^2 C_m^2\right) C_{r2}}{\left(\omega^2 C_{r2}^2\right)\left[G_m\left(1 - R_s' G_m\right) - \omega^2 R_s' C_m^2\right]^2 + \left(G_m^2 + \omega^2 C_m^2 - \omega^2 C_m C_{r2}\right)^2} \tag{12}$$

$$G_c = \frac{\left[G_m\left(1 - R_s' G_m\right) - \omega^2 R_s' C_m^2\right]\left(G_m^2 + \omega^2 C_m^2\right)\left(w^2 C_{r2}^2\right)}{\left(\omega^2 C_{r2}^2\right)\left[G_m\left(1 - R_s' G_m\right) - \omega^2 R_s' C_m^2\right]^2 + \left(G_m^2 + \omega^2 C_m^2 - \omega^2 C_m C_{r2}\right)^2} \tag{13}$$

Using Eq. (12), the corrected C_c values are obtained and represented in Fig. 1. One can see that after the elimination of R_s, no frequency dispersion is observed.

3.2. Fixed oxide charge density (Q_f) and interface trap density (D_{it}) extraction methodology

Fig. 4 shows the corrected C_c-V curves for different dielectric stacks measured at 1 kHz. From the C_c-V curves, the density of Q_f can be calculated as follows:

$$Q_f = \frac{\left(\phi_{MS} - V_{fb}\right) C_{ox}}{q} \tag{14}$$

where ϕ_{MS} is the work function difference between mercury and silicon (− 0.435 V). C_{ox} is a total gate dielectric capacitance including Al_2O_3 and SiO_2, V_{fb} is the flatband voltage and q is the electron charge (1.6×10^{-19} C). For instance, for sample 2, $C_{ox} = 7.0 \times 10^{-7}$ A/cm^2, $V_{fb} = +$ 0.61 V, calculated by the second derivative technique [8]. Therefore, we obtain a negative oxide charge ($Q_f = - 4.57 \times 10^{12}$ cm^{-2}). Table 2 summarizes the related values extracted for the four gate stacks and the reference thermal oxide sample (sample 1).

Fig. 5 shows the corrected C_c-V characteristics after subtracting V_{fb} at 1 MHz for samples 2 and 4. The ideal C—V curve simulated by Silvaco software (with zero V_{fb} and D_{it}) is also shown. A stretch-out in the depletion region is observed. This is due to the fact that carriers captured and emitted in the interface traps follow slowly varying DC voltage, rather than high frequency excitation. Based on Terman method [5], D_{it} are extracted to be 5.60×10^{10} cm^{-2} eV^{-1} and 2.82×10^{11} cm^{-2} eV^{-1} by comparing the measured and simulated C—V curves for samples 2 and 4. The small and large stretch-outs imply the lowest and high D_{it} of samples 2 and 4, respectively.

The conductance method aims at probing the variation of occupancy of interface trap levels located in the Si bandgap around the Fermi level, following the variation of gate voltage.

The capture and emission of majority carriers by interface traps cause an energy loss mechanism observed at all the frequencies except at the lowest frequencies (no energy loss occurs) and at the highest frequencies (no interface traps response occurs).

This energy loss is measured as an equivalent parallel conductance G_p (in our work) as a function of frequency. G_p can be extracted from G_c and calculated below [9]:

$$\frac{G_p}{\omega} = \frac{\omega C_{ox}^2 G_c}{G_c^2 + \omega^2 \left(C_{ox} - C_c\right)^2} \tag{15}$$

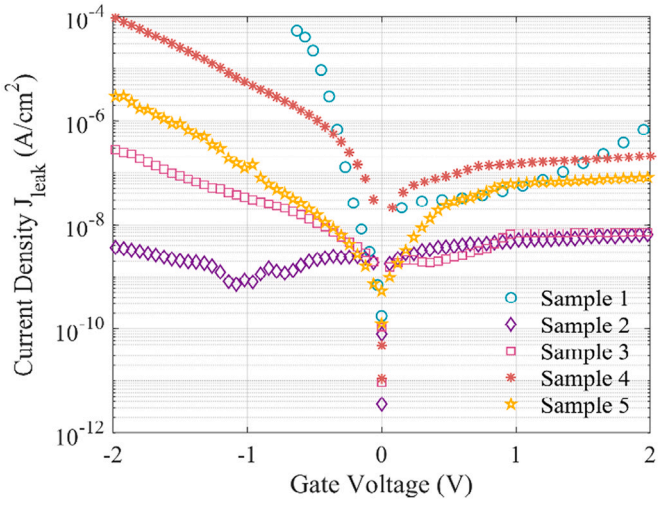

Fig. 7. Leakage current density vs gate voltage for four dielectric stacks and a single-layer SiO_2 dielectric (sample 1) with the similar EOT.

Table 3
Summary of leakage mechanisms.

Mechanism	Expression	*E*-field dependence
Poole-Frenkel [10,12,15]	$J = A_{PF}E_{ox}exp\left[-\frac{q\phi_T - \beta\sqrt{E_{ox}}}{2kT}\right]$	$\ln(\frac{J}{E}) \propto E^{1/2}$
Trap-assisted tunneling [12]	$J = A_{TAT}exp\left[-\frac{8\pi\sqrt{2qm_{ox}}}{3hE_{ox}}\phi_T^{3/2}\right]$	$\ln(J) \propto E^{-1}$
Fowler-Nordheim [16]	$J = \frac{q^3}{8\pi h\phi_B}E_{ox}^2 exp\left(-\frac{8\sqrt{2m_{ox}}}{3hqE_{ox}}\phi_B^{3/2}\right)$	$\ln(\frac{J}{E^2}) \propto E^{-1}$

An approximate expression giving the interface trap density in terms of the measured maximum conductance is [5,9].

$$D_{it} \approx \frac{2.5}{qA}\left(\frac{G_p}{\omega}\right)_{max} \tag{16}$$

where $\omega = 2\pi f$, q = 1.6 × 10^{-19}C and the mercury probe contact area A = 0.0065 cm^2. Fig. 6 represents corrected G_c/ω as a function of gate voltage using conductance method for sample 2 measured at different frequencies. According to the highest peak of G_p/ω as a function of ω, we can calculate D_{it} by Eq. (16). D_{it} being equal to 5.2 × 10^{10} cm^{-2} eV^{-1} indicates a low interface trap density ($C_{it} = qD_{it} << C_{ox}$) [10]. For other samples, values are reported in Table 2. It is worth pointing out that the values extracted by conductance method agree well with the values extracted by Terman method.

3.3. Leakage current characteristics

Fig. 7 presents the leakage current density (J_{leak}) through the gate stack as a function of gate voltage for the different dielectric stacks and single-layer SiO_2 counterpart dielectric, measured at room temperature. It can be seen that J_{leak} of the dielectric stacks is several orders of magnitude lower than that through the single-layer SiO_2 dielectric with similar EOT. Particularly, the PE-ALD Al_2O_3/thermal SiO_2 stack (sample 2) has the lowest leakage current. As shown in the figure, J_{leak} is not symmetric for positive and negative V_g. This phenomenon is caused by different transport mechanisms for the type and number of carriers. The leakage current through the dielectrics may be caused by different mechanisms [11]. Table 3 lists the main mechanisms in our case, namely Poole-Frenkel (PF) emission, trap-assisted tunneling (TAT), and Fowler-Nordheim tunneling (FN). In Table 3, J is the current density, E_{ox} is the electric field calculated as follows:

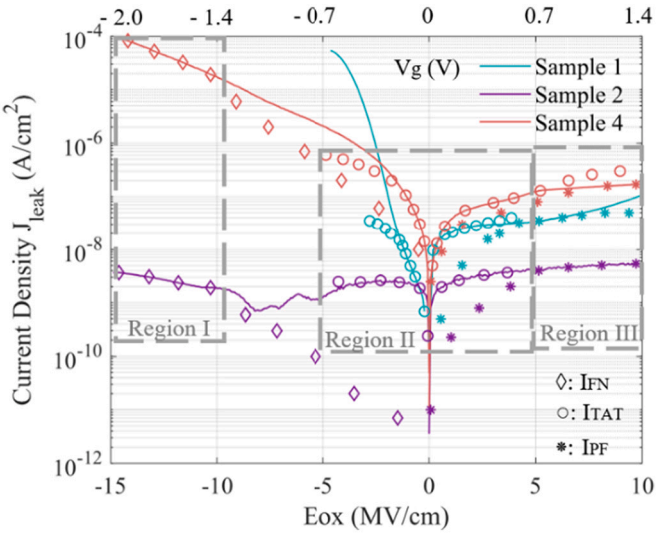

Fig. 8. Different components of the total leakage current (lines for measurements and symbols for FN, TAT and PF models) as a function of E_{ox} (bottom axis) and V_g (top axis) for samples 1, 2 and 4. Samples 3 and 5 are not plotted as they show similar trends to samples 2 and 4, resp.

$$E_{ox} = \frac{V_g - V_{fb}}{t_{SiO_2}}\left(\frac{\epsilon_{SiO_2}t_{Al_2O_3}}{\epsilon_{Al_2O_3}t_{SiO_2}} + 1\right)^{-1} \tag{17}$$

β is the Poole-Frenkel constant (β/kT = 0.01486), A_{PF} is a proportionality constant varying from 1.3× 10^{-13} to 4 × 10^{-13} [12], A_{TAT} is a technology constant from 1× 10^{-6} to 1× 10^{-5} in agreement with experiment data. m_{ox} is the electron effective mass in Al_2O_3 0.28m_0 [13], $q\phi_T$ is the energy position of the electron traps with respect to the conduction band edge of the dielectric in the range of 1.2–3 eV, ϕ_B is the barrier height from 3.85 to 4.6 eV between the dielectric and silicon [14], k is Boltzmann's constant, T is the absolute temperature, and, finally, h is the Planck's constant.

Fig. 8 shows different current components (as a function of E_{ox} and V_g) contributing to the total leakage current J_{leak} for the MOS capacitors of samples 1, 2, and 4. As shown in Fig. 7, the curves of samples 2 and 3 show similar trends whereas samples 4 and 5 behave differently. To make the plot clear, we do not plot the current of samples 3 and 5 here. The leakage mechanisms in different regions are analyzed hereafter.

Region I (Fowler-Nordheim tunneling): the leakage is observed to increase rapidly with increased bias. It is suggested that FN tunneling is prominent in the higher voltage range of -2 V < V_g < -1.4 V for samples 2, 3, 4, and 5. Sample 1 featured very high currents already at -0.7 V so that compliance was triggered and we could not analyze this sample at very negative biases. FN mechanism is a one-step process: when a higher negative voltage is applied to the metal with respect to the substrate, electrons directly tunnel from the interface of metal and dielectric into the conduction band of silicon, through an approximately triangular potential barrier.

Region II (Trap-assisted tunneling): TAT current dominates the measured data in the range of -0.7 to 0.7 V for all samples. Instead of one-step FN tunneling through the potential barrier directly, the electron transport process of TAT tunneling considers that electrons first tunnel into the traps in the dielectric from silicon or metal, and subsequently tunnel into metal or silicon under a low bias. The presence of traps inside the dielectric splits the energy barrier in several parts, thus allowing the consecutive tunneling through thinner energy barriers, thereby increasing the tunneling probability.

Region III (Poole-Frenkel emission): The PF current yields a fair agreement with the measurement data for the region of V_g = 0.7–1.4 V. It is shown that leakage mechanism follows PF emission in this region for

Table 4
Comparison of High-K candidates and conventional SiO_2.

Materials	EOT (nm)	Dielectric constant k	Q_f (cm^{-2})	D_{it} ($cm^{-2}\ eV^{-1}$)	J_{leak} (A/cm^2)	Technology nodes	References
SiO_2	2.9	3.9	$+1.00 \times 10^{12}$	2.00×10^{10}	10^{-5} @ 1 V	180 nm	[20]
SiO_xN_y/SiO_2	2.0	7.0	$+6.21 \times 10^{11}$	7.00×10^{11}	10^{-6} @ 1 V	>45 nm	[1,21]
HfO_2/SiO_2	1.7	20	-1.80×10^{12}	5.21×10^{12}	8.95×10^{-7} @ 1 V	< 28 nm	[11,21–24]
ZrO_2/SiO_2	1.3	25.0	-2.51×10^{12}	3.00×10^{11}	1.00×10^{-5} @ -1 V	< 20 nm (DRAM)	[20,25,26,28]
Al_2O_3/SiO_2 (sample 2)	4.9	9	-4.57×10^{12}	5.20×10^{10}	5.06×10^{-9} @ 1 V	≥ 65 nm	This work

all samples. Therefore, the PF transport process considers that electrons are emitted from traps into the conduction band of dielectric stack by PF mechanism and flow from the dielectric across the metal-dielectric interface into the metal with a higher bias than TAT.

The three leakage currents appear in all Al_2O_3/SiO_2 stacks. The results indicate that the Al_2O_3/SiO_2 stacks are less leaky than the single-layer SiO_2 and that the deposition conditions of the thin Al_2O_3/SiO_2 stacks are important. As long as the deposition process is well optimized, the Al_2O_3/SiO_2 stack could be a good candidate to replace SiO_2 in CMOS applications beyond 65 nm node.

3.4. Comparison and discussion

Table 2 summarizes the V_{fb}, Q_f, D_{it} and J_{leak} for the four Al_2O_3/SiO_2 samples and SiO_2 reference sample. The PE-ALD Al_2O_3/thermal SiO_2 and T-ALD Al_2O_3/thermal SiO_2 samples show higher negative fixed oxide charge density, compared with the PE-ALD Al_2O_3/PE-ALD SiO_2 and T-ALD Al_2O_3/PE-ALD SiO_2 samples. The high negative Q_f would cause a positive shift of the V_{th} in a n-MOSFET as following [17]:

$$V_{th} = \phi_{ms} - Q_f/C_{ox} + V_{it} + 2\phi_F + \frac{\sqrt{4q\epsilon_{si}N_a\phi_F}}{C_{ox}} \quad (21)$$

V_{th} can then be tuned to its desired (or target) value by changing the channel doping concentration (N_a). When Q_f is negative, V_{th} increases. Lowering N_a can compensate for the increase of V_{th}. Simultaneously, low N_a is beneficial for the enhancement of the electron mobility [18] and reduction of the variability.

Next to that, we can see that the D_{it} values calculated by Terman and Conductance methods are rather similar. This confirms the reliability of our extracted results. Moreover, the D_{it} values in the PE-ALD Al_2O_3/thermal SiO_2 and T-ALD Al_2O_3/thermal SiO_2 samples are 2 to 3 times lower than in the PE-ALD Al_2O_3/PE-ALD SiO_2 and T-ALD Al_2O_3/PE-ALD SiO_2 samples. This indicates that the thermal SiO_2 is required as the interfacial layer for improving the interface quality of the gate stack. The reason may be due to the fact that plasma slightly damages the silicon surface, which creates more interface traps. It was reported [1] that the D_{it} ideal value is $\sim 10^{10}\ cm^{-2}\ eV^{-1}$ for advanced MOSFETs, but a value of ($\sim 10^{11}\ cm^{-2}\ eV^{-1}$) giving the interface trap capacitance C_{it} ($= qD_{it}$) to be much lower than C_{ox} is acceptable for thin oxides. In our case, the C_{it} of all dielectric stacks is one to two orders of magnitudes lower than C_{ox}. When the D_{it} value becomes much larger than this value, the subthreshold slope and the mobility of the channel carriers degrade. In this case, the high-k dielectric materials will lose their benefits.

The ALD Al_2O_3/thermal SiO_2 samples present low leakage current of $5–7 \times 10^{-9}\ A/cm^2$ (at $V_g = 1$ V), about an order of magnitude lower than the SiO_2 reference sample, while the PE-ALD SiO_2 samples lie above the ALD Al_2O_3/thermal SiO_2 ones (but still lower than reference SiO_2). This correlates with our conclusion on the best stack from the interface quality point of view and appears related to the interface traps that play a crucial role in the leakage current (PF and TAT) of the stacks. The improvement of the leakage current can then be achieved by proper choice of deposition methods or post annealing of the dielectric stack to reduce the interface trap density [19].

According to the literature survey, we summarize in Table 4, the published important parameters of conventional SiO_2 layer and high-k dielectric stacks we could find with an EOT close to 3 nm. To ease the comparison, our best sample is also cited in the table. Among all the stacks in the table, our stack (PE-ALD Al_2O_3/thermal SiO_2) presents the lowest D_{it}, highest negative Q_f and lowest leakage current density at 1 V.

Low D_{it} value does not only decrease the trap-assisted tunneling current but also prevents from the degradation of the carrier mobility and subthreshold slope as well as reliability issues in MOSFETs. A high negative Q_f value allows a lower doping concentration of channel to increase the carrier mobility and reduce variability at constant V_{th}. The low J_{leak} assures a good insulator property and lower power consumption. Although the dielectric constant of Al_2O_3 is lower than HfO_2 and ZrO_2 and similar to SiO_xN_y, the stack of PE-ALD Al_2O_3/thermal SiO_2 shows overall better dielectric properties than the other stacks for our targeted thickness. Our result reveals that the ultra-thin, high-quality SiO_2 interfacial layer plays a crucial role in the Al_2O_3/SiO_2 stack. Therefore, Al_2O_3 could be a trade-off between SiO_2 and the high-k dielectric materials with re-lative dielectric constants larger than 10 (larger band gap) [18].

4. Conclusion

In this paper, we systematically investigate four kinds of thin Al_2O_3/SiO_2 MOS capacitors with an equivalent oxide thickness (EOT) of ~4.9 nm, prepared by different processes. Compared with the conventional SiO_2 MOS counterpart, Al_2O_3/SiO_2 MOS capacitors show better dielectric performance. It has the lowest interface trap density ($D_{it} = 5.20 \times 10^{10}\ cm^{-2}\ eV^{-1}$) and the lowest leakage current density ($J_{leak} = 5.06 \times 10^{-9}\ A/cm^2$). Its fixed oxide charges (Q_f), approximately $\sim 10^{12}\ cm^{-2}$, is on the same level as Q_f in SiO_2 but negative. Although popular dielectrics cited in Table 4 (such as HfO_2 and ZrO_2) have higher dielectric constant k than Al_2O_3, the Al_2O_3/SiO_2 stack exhibits lower D_{it}, reasonable Q_f, and particularly, several orders of magnitude lower J_{leak}. Our results indicate that the Al_2O_3/SiO_2 stack could be a good candidate to replace the conventional SiO_2 in CMOS technology node 65 nm and beyond. Its more negative Q_f would allow to keep fixed threshold voltage while lowering the channel doping and hence improving mobility and variability. Moreover, Al_2O_3 does not belong to rare-earth metal oxides, which is suitable for sustainable development goals.

Credit author statement

Yiyi Yan, Denis Flandre and Jean-Pierre conceived and designed the study. Yiyi Yan, Sébastien Faniel fabricated the samples. Yiyi Yan characterized all the samples. Yiyi Yan and Bin Wang analyzed the data and prepared the figures and tables. Yiyi Yan, Valeriya Kilchytska, Denis Flandre and Jean-Pierre wrote the manuscript, and all coauthors revised and approved it.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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