

A 2.5-nA Area-Efficient Temperature-Independent 176- / 82-ppm/°C CMOS-Only Current Reference in 0.11- μm Bulk and 22-nm FD-SOI

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Abstract—Internet-of-Things (IoT) applications require nW-power current references that are robust to process, voltage and temperature (PVT) variations, to maintain the performance of IoT sensor nodes in a wide range of operating conditions. However, nA-range current references are rarely area-efficient due to the use of large gate-leakage transistors or resistors, which occupy a significant silicon area at this current level. In this paper, we introduce a nA-range constant-with-temperature (CWT) current reference, relying on a self-cascode MOSFET (SCM) biased by a four-transistor ultra-low-power voltage reference through a single-transistor buffer. The proposed reference includes a temperature coefficient (TC) calibration mechanism to maintain performance across process corners. In addition, as the proposed design relies on the body effect, it has been fabricated and measured in 0.11- μm bulk and 22-nm fully-depleted silicon-on-insulator (FD-SOI) to demonstrate feasibility in both technology types. On the one hand, the 0.11- μm design consumes a power of 16.8 nW at 1.2 V and achieves a 2.3-nA current with a line sensitivity (LS) of 2.23 %/V at 25°C and a TC of 176 ppm/°C at 1.2 V from -40 to 85°C. On the other hand, the 22-nm design consumes a power of 16.3 nW at 1.5 V and achieves a 2.5-nA current with a 1.53-%/V LS at 25°C and an 82-ppm/°C TC at 1.5 V from -40 to 85°C. Thanks to their simple architecture, the proposed references achieve a silicon area of 0.0106 mm² in 0.11 μm and 0.0026 mm² in 22 nm without compromising other figures of merit, and are thus competitive with state-of-the-art CWT references operating in the same current range.

Index Terms—Current reference, voltage reference, self-cascode MOSFET (SCM), temperature coefficient (TC), temperature-independent, constant-with-temperature (CWT), ultra-low-power (ULP).

I. INTRODUCTION

IN the last decade, the expected growth of the Internet of Things (IoT) has fostered the development of ultra-low-power (ULP) smart sensor nodes, combining sensing and processing capabilities at the edge. As most integrated circuits, the analog blocks constituting these sensor nodes must be biased by current references, whose specifications can be derived from the requirements of IoT applications. First, sensor nodes

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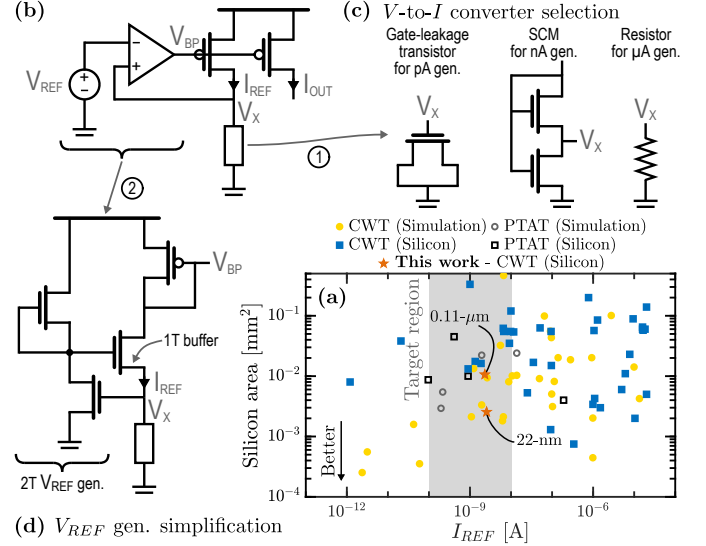


Fig. 1. The area efficiency of nA-range CWT current references can be improved by using an SCM as V-to-I converter, and by simplifying the V_{REF} generation and buffering. (a) Tradeoff between silicon area and reference current, featuring the scarcity of measured area-efficient solutions in the nA range. (b) Conventional CWT current references are based on a reference voltage applied to a V-to-I converter, which can either be (c) a gate-leakage transistor, an SCM, or a resistor, respectively well suited to the generation of pA-, nA-, or μA -range reference current. (d) Voltage reference implemented with a 2T structure and a 1T buffer [1], [2].

are usually supplied by limited-capacity batteries or energy harvesting, constraining the average power consumption to the 0.1-to-100- μW range [3]. A bias current in the order of nA is thus required to cope with the stringent power constraints of always-on blocks in sleep mode while maintaining a satisfying performance in active mode. Moreover, sensor nodes must be able to operate in a wide range of deployment scenarios. The sensitivity of current references to process, voltage and temperature (PVT) variations should therefore be mitigated, as it can profoundly undermine the performance of common analog building blocks such as real-time clock generators [4], [5], temperature sensors [6], [7], and capacitive sensor interfaces [8]. Finally, silicon area must be limited to reduce the production cost and direct environmental footprint of each sensor, especially given the expected massive production volume of the IoT [9]. The same trend should be followed by current references. However, Fig. 1(a) highlights that nA-range current references that are simultaneously robust to PVT variations and area-efficient are scarce in the literature, or have never been demonstrated in measurement.

One of the conventional ways of generating a reference

current is to bias a voltage-to-current (V -to- I) converter with a reference voltage through an op-amp-based feedback loop [Fig. 1(b)]. On the one hand, the choice of V -to- I converter ① strongly impacts the area efficiency of the reference. For example, gate-leakage transistors and resistors are not well suited to the generation of a nA-range current as they occupy a significant area at this current level [Figs. 1(a) and (c)]. Previous works have shown that self-cascode MOSFETs (SCMs) are more appropriate to generate a nA-range current [10], [11], but need to be biased by a proportional-to-absolute-temperature (PTAT) voltage with a constant-with-temperature (CWT) offset to make the current CWT [12]. A temperature coefficient (TC) calibration mechanism is also necessary to maintain performance across process corners, but is difficult to integrate in the β -multiplier architecture proposed in [12]. In addition, the value of the CWT offset in [12] depends solely on technological parameters and cannot be tuned through transistor sizes. This makes the attainable performance heavily reliant on technology, potentially leading to some degradation when the CWT offset is not adapted. On the other hand, the last decade has seen ULP voltage references composed of only a few transistors ② arising as simple and area-efficient alternatives to more complex architectures, with only a marginal deterioration in robustness [13], [14], [15], [16]. Such voltage references, coupled with a single-transistor (1T) buffer [Fig. 1(d)], have already been successfully applied to the generation of a wide range of reference currents [1], [17], [2], but never to a CWT nA-range current.

In this work, we propose to fix the two critical issues of [12] mentioned hereabove by generating the SCM bias voltage with a four-transistor (4T) voltage reference. This structure includes a calibration mechanism to tune the TC in process corners, makes the CWT offset dependent on transistor sizes, and removes the need for a startup circuit. This new building block is the key innovation of this work, as it allows to reliably attain a good performance in terms of LS, TC, and variability in any technology, while minimizing area and power consumption. This leads to an area-efficient CWT current reference generating a current in the nA range and relying on an SCM biased by this 4T voltage reference through a 1T buffer. Note that the proposed architecture can also be used in applications requiring a bias current with a specific temperature dependence, by using a different sizing of the reference or by leveraging the TC calibration mechanism to configure the TC. Two prototypes have been fabricated in United Microelectronics Corporation (UMC) 0.11- μm bulk and GlobalFoundries (GF) 22-nm fully-depleted silicon-on-insulator (FD-SOI) CMOS technologies. The 0.11- μm (resp. 22-nm) design show a measured TC of 176 ppm/ $^{\circ}\text{C}$ (resp. 82 ppm/ $^{\circ}\text{C}$) from -40 to 85 $^{\circ}\text{C}$, while occupying a silicon area of only 0.0106 mm ^{2} (resp. 0.0026 mm ^{2}). The rest of this work is structured as follows. Section II details the governing equations of the reference and presents its operation principle. Next, Section III discusses the design and sizing methodology, while Section IV examines the simulation and measurement results. Finally, Section V compares this work to the literature while Section VI delivers concluding remarks.

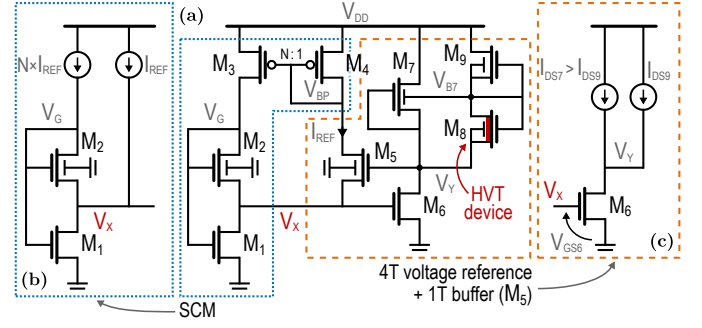


Fig. 2. (a) Basic schematic of the proposed current reference, which consists of (b) an SCM (M_{1-2}) biased by a pMOS current mirror (M_{3-4}), and (c) a 4T voltage reference (M_{6-9}) generating a PTAT voltage with a CWT offset, biasing the SCM through a 1T buffer (M_5).

II. GOVERNING EQUATIONS AND OPERATING PRINCIPLE

This section presents the equations governing the behavior of the two constitutive blocks of the proposed current reference, namely an SCM and a 4T voltage reference, depicted in Fig. 2(a) in its basic form, i.e., without calibration circuit. It also details the operation principle of the reference, and explains how the limitations of the SCM-based β -multiplier current reference in [12] have been overcome in Section II-C.

In what follows, the line sensitivity (LS) and TC are computed using the box method, i.e.,

$$LS = \frac{(I_{REF,max} - I_{REF,min})}{I_{REF,avg}(V_{DD,max} - V_{DD,min})} \times 100 \% / V, \quad (1)$$

$$TC = \frac{(I_{REF,max} - I_{REF,min})}{I_{REF,avg}(T_{max} - T_{min})} \times 10^6 \text{ ppm}/^{\circ}\text{C}, \quad (2)$$

where $I_{REF,min/avg/max}$ respectively stand for the minimum, average, and maximum reference current among the considered range. $V_{DD,min/max}$ (resp. $T_{min/max}$) refer to the lower and upper bounds of the voltage (resp. temperature) range.

A. Self-Cascode MOSFET

First, the SCM depicted in Fig. 2(b) relies on long-channel transistors in moderate inversion, for which a simplified model such as the analog compact MOSFET (ACM) model [18] is adequate to describe the transistor current-voltage (I - V) characteristics. In this model, the drain current is given by

$$I_D = I_{SQ} S (i_f - i_r), \quad (3)$$

where $I_{SQ} = \frac{1}{2} \mu C'_{ox} n U_T^2$ is the specific sheet current, μ is the carrier mobility, C'_{ox} is the gate oxide capacitance per unit area, n is the subthreshold slope factor, U_T is the thermal voltage, $S = W/L$ is the transistor aspect ratio, and i_f , i_r are the forward and reverse inversion levels. The transistor I - V curve is captured by

$$V_P - V_S = U_T \left[\sqrt{1 + i_f} - 2 + \log \left(\sqrt{1 + i_f} - 1 \right) \right], \quad (4)$$

where $V_P = (V_G - V_{T0})/n$ is the pinch-off voltage, V_{T0} is the threshold voltage at zero V_{BS} , and all voltages are referred to the transistor's body, thus accounting for the body effect. i_r is found by replacing V_S by V_D in (4), but is only relevant when the transistor is not saturated. It should be noted that, in what follows, the obtained expressions only slightly differ from the ones obtained in [12] due to the body connection of M_2 to ground. We have nonetheless chosen to detail them

here to avoid any mistake and to provide all the necessary tools for implementing the proposed reference. Applying the ACM equations to transistors M_{1-2} leads to the following equation, which expresses voltage V_X as

$$V_X = U_T \left[\left(\sqrt{1 + \alpha i_{f2}} - \sqrt{1 + i_{f2}} \right) + \log \left(\frac{\sqrt{1 + \alpha i_{f2}} - 1}{\sqrt{1 + i_{f2}} - 1} \right) \right] \quad (5)$$

by defining $\alpha \triangleq i_{f1}/i_{f2} > 1$. Then, based on (3) applied to M_{1-2} , the ratio of the aspect ratios S_1/S_2 must comply with

$$\frac{S_1}{S_2} = \frac{I_{SQ2}}{I_{SQ1}} \frac{1 + N}{N} \frac{1}{\alpha - 1} \quad (6)$$

to ensure that Kirchhoff's current law is respected [11], N being the current ratio between M_3 and M_4 . Besides, applying (3) to M_2 gives the expression of the reference current

$$I_{REF}(T) = I_{SQ2}(T) i_{f2}(T) (S_2/N), \quad (7)$$

where $I_{SQ2}(T) \propto U_T^2 \mu(T) \propto T^{2-m}$, with $\mu(T) = \mu(T_0) (T/T_0)^{-m}$, and m is the temperature exponent of the carrier mobility whose value is comprised between 1.2 and 2 in bulk CMOS [19]. An important quantity which remains to be defined is the sensitivity of the reference current to V_X , computed with I_{REF} expressed by (7) and di_{f2}/dV_X calculated from (5) as $(dV_X/di_{f2})^{-1}$, consequently yielding

$$S_{I_{REF}} = \frac{2}{i_{f2} U_T} \left[\frac{\alpha}{\sqrt{1 + \alpha i_{f2}} - 1} - \frac{1}{\sqrt{1 + i_{f2}} - 1} \right]^{-1}. \quad (8)$$

In existing SCM-based PTAT current references [10], [11], [2], the SCM is biased by a purely PTAT voltage V_X [Fig. 3(a)] and M_{1-2} operate at a fixed inversion level [Fig. 3(b)], thus making I_{REF} proportional to the specific sheet current I_{SQ} (7). Therefore, I_{REF} presents a PTAT behavior dictated by T^{2-m} [Fig. 3(c)]. Nevertheless, to obtain an SCM-based CWT current reference such as [12], the SCM must be biased by

$$V_X = V_{off} + n U_T \log(K_{PTAT}), \quad (9)$$

i.e., a PTAT voltage with a CWT offset as shown in Fig. 3(a), with which solving (5) gives an inversion level i_{f2} that decreases with temperature [Fig. 3(b)]. Eq. (7) indicates that, with a proper sizing of the SCM, the PTAT behavior of I_{SQ} and the CTAT one of i_{f2} can cancel each other out, eventually leading to a CWT reference current [Fig. 3(c)]. Therefore, the key principle leveraged in the proposed reference is that an SCM biased by a PTAT voltage with a CWT offset generates a temperature-independent reference current. A previous study [12] reveals that an I_{REF} TC valley is obtained for a linear relationship between parameters K_{PTAT} and α , and that $S_{I_{REF}}$ is improved at higher V_{off} as M_1 is biased closer to strong inversion.

B. 4T Ultra-Low-Power Voltage Reference

To generate the PTAT voltage with a CWT offset required by the SCM, the proposed reference employs a novel 4T voltage reference architecture, inspired by decades of advances in 2T voltage references [13], [14], [15], [16], and sharing

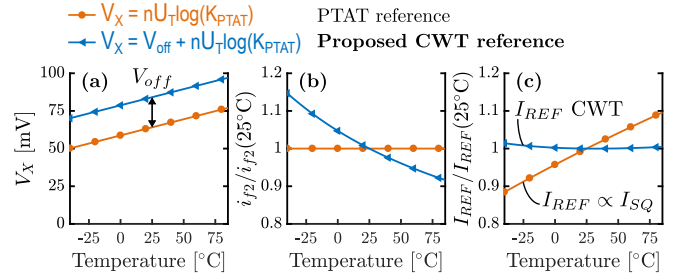


Fig. 3. Operation principle of PTAT references proposed in prior art [10], [11] (in orange) and of the proposed CWT reference (in blue). Analytical expression of (a) the voltage V_X applied to the SCM, (b) the inversion level of M_2 , denoted as i_{f2} , and (c) the reference current I_{REF} , as a function of temperature and for $V_{off} = 20$ mV. Generic technological parameters $n = 1.2$ and $m = 1.5$ are selected. (b) and (c) are normalized to their value at 25°C . For the proposed CWT reference, the parameters leading to a minimum I_{REF} TC are $K_{PTAT} = 8$ and $\alpha = 1.5$.

similarities with 4T structures introduced in [14], [20]. The transistors constituting this 4T voltage reference [Fig. 2(c)] operate in deep subthreshold, in which the drain-to-source current of an nMOS transistor can be described by

$$I_{DS} = I_{SQ} S \exp \left(\frac{V_{GS} - V_T}{n U_T} \right), \quad (10)$$

for $V_{DS} > 4U_T$, where $I_{SQ} = \mu C'_{ox} (n-1) U_T^2$ is another definition of the specific sheet current, and V_T is the threshold voltage at any V_{BS} . In addition, the proposed reference makes extensive use of the body effect, i.e., the change of threshold voltage due to a non-zero V_{BS} voltage, which is captured by

$$\Delta V_T = V_T - V_{T0} = \gamma_b \left(\sqrt{2\phi_{fp} - V_{BS}} - \sqrt{2\phi_{fp}} \right), \quad (11)$$

$$\approx -\gamma_b^* V_{BS}.$$

in a bulk technology, with γ_b the body factor, γ_b^* its linearization around $V_{BS} = 0$, and ϕ_{fp} Fermi's potential, or by

$$\Delta V_T = V_T - V_{T0} = -\gamma_b^* V_{BS} \quad (12)$$

in an FD-SOI technology, for which $\gamma_b^* = C_d/C_{ox}$ is temperature-independent at first order [21] as C_d is the capacitance between the back-gate and channel due to the buried oxide. In addition, it should be noted that in subthreshold, a common expression relating γ_b^* to the subthreshold slope factor n is given by

$$\gamma_b^* = n - 1. \quad (13)$$

A simple way to understand the proposed 4T voltage reference [Fig. 2(c)] is to see it as two drain-to-source leakage current sources, corresponding to transistors M_7 and M_9 connected with a zero V_{GS} , biasing M_6 to generate a reference voltage $V_X = V_{GS6}$. It should be noted that $I_{DS7} > I_{DS9}$ due to the 2T voltage reference formed by M_{8-9} , which leads to $V_{BS7} > 0$ and thus to a forward body biasing (FBB) of M_7 , ultimately resulting in a reduction of V_{T7} . Applying Kirchhoff's current law at node V_Y gives $I_{DS6} = I_{DS7} + I_{DS9}$. Using the expression of the subthreshold current in (10), and assuming that M_{6-7-9} have the same I_{SQ} and V_{T0} , voltage V_X can consequently be expressed as

$$V_X(T) = n U_T \log \left(\frac{S_9}{S_6} + \frac{S_7}{S_6} \exp \left(\frac{-\Delta V_{T7}}{n U_T} \right) \right), \quad (14)$$

where the decrease in threshold voltage $\Delta V_{T7} < 0$ results in a positive CWT offset V_{off} . Moreover, ΔV_{T7} can be related to

M_7 's body-to-source voltage through (11) or (12), with V_{BS7} found by equating the subthreshold currents $I_{DS8} = I_{DS9}$ in the 2T voltage reference formed by M_{8-9} as in [14], giving

$$V_{BS7} = \left(\frac{n_8}{n_9} V_{T08} - V_{T09} \right) + n_8 U_T \log \left(\frac{I_{SQ9} S_9}{I_{SQ8} S_8} \right). \quad (15)$$

It should be noted that this FBB technique can be applied in bulk and FD-SOI technologies, with a more limited voltage range in bulk. Different subthreshold factors are used for M_8 and M_9 as they can be of different V_T types. Next, the nonlinear expression of V_X given by (14) can be expressed as a voltage of the form (9) using a first-order Taylor series approximation of V_X around a temperature T_0 , provided by

$$V_X(T) \approx V_X(T_0) + \frac{dV_X(T_0)}{dT} (T - T_0), \quad (16)$$

$$\approx V_{X0} + \delta_{V_X} T,$$

with V_{X0} the voltage at zero absolute temperature and δ_{V_X} the PTAT slope of V_X . In practice, we find it more convenient to define quantities which can be extracted from simulation results. In what follows, the CWT offset of V_X , denoted as V_{off} , is thus defined as the difference between (14) and a purely PTAT reference voltage constituted solely of M_6 and M_9 , at $T_0 = 25^\circ\text{C}$, and expressed as

$$V_{off} \triangleq V_X(T_0) - nU_{T0} \log \left(\frac{S_9}{S_6} \right),$$

$$= nU_{T0} \log \left(1 + \frac{S_7}{S_9} \exp \left(\frac{-\Delta V_{T7}}{nU_{T0}} \right) \right). \quad (17)$$

It is important to note that $V_{off} \neq V_{X0}$, even though they both represent an offset voltage. Besides, the PTAT slope of V_X is simply estimated as $\Delta V_X / \Delta T \simeq \delta_{V_X}$. Next, Fig. 4 illustrates the impact of changes of S_7/S_6 and S_9/S_6 on voltage V_X . First, an increase in S_7/S_6 for a fixed value of S_9/S_6 [Fig. 4(a)] results in an increased V_{off} ranging from 5 to 55 mV [Fig. 4(b)], while only slightly impacting the PTAT slope [Fig. 4(c)]. Next, an increase in S_9/S_7 for a fixed value of S_7/S_6 [Fig. 4(d)] strongly impacts the PTAT slope, with a variation from 0.1 to 0.3 mV/ $^\circ\text{C}$. Changing the ratios S_7/S_6 and S_9/S_6 therefore allows to tune the CWT offset and PTAT slope of V_X with a relative independence, even though a perfectly independent control cannot be achieved.

C. Proposed Temperature-Independent Current Reference

The proposed temperature-independent current reference combines two key ideas. Firstly, the idea of biasing an SCM using a PTAT voltage with a CWT offset to generate a CWT current, introduced in [12]. This concept shares some similarities with [22], in which the temperature dependence of the current in a deep-triode transistor is compensated with a temperature-dependent bias voltage. Then, the idea of using a ULP voltage reference whose output is buffered on a V-to-I converter, here an SCM, by a single transistor [1], [17], [2]. The main contributions of this work are thus to combine these two concepts and to propose a novel 4T voltage reference architecture to generate the PTAT voltage with a CWT offset required by the SCM. In addition, the proposed design corrects several limitations of [12], which was using a modified subthreshold β -multiplier to generate the SCM bias

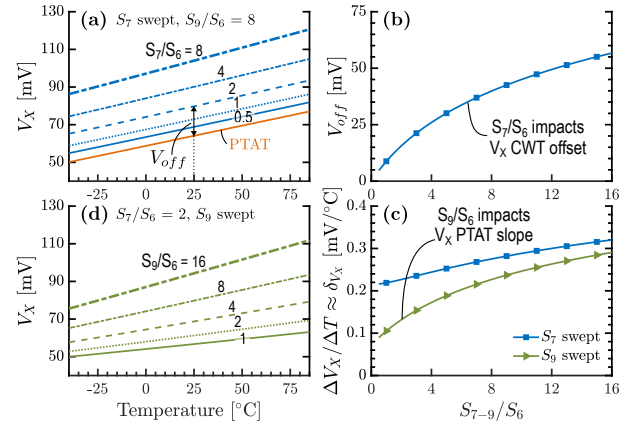


Fig. 4. All figures correspond to generic technological parameters $n = 1.2$, $\gamma_b^* = 0.15$, and $V_{BS7} = 0.2$ V, and rely on a body effect model corresponding to an FD-SOI technology. Temperature dependence of V_X for (a) a sweep of S_7 and a fixed $S_9/S_6 = 8$, and (d) a sweep of S_9 and a fixed $S_7/S_6 = 2$. (b) V_X CWT offset for the S_7 sweep in (a), and (c) V_X PTAT slope for the sweeps shown in (a) and (d), estimated as the variations of V_X across the temperature range divided by the temperature range.

voltage. The four following limitations have been corrected:

(i) A β -multiplier has two stable operating points and requires a startup circuit to ensure that it is biased around the non-zero one. On the contrary, the proposed reference has a single non-zero operating point, eliminating the need for such a circuit. When I_{REF} is equal to zero, V_X and V_Y are ≈ 0 , but this operating point is unstable as M_7 and M_9 have a V_{DS} close to V_{DD} and are biasing M_6 with a non-zero current leading to $V_{GS6} = V_X > 0$;

(ii) The body connection of M_2 to V_X in [12] degrades I_{REF} TC due to the leakage through the parasitic p-well/n-well diode at node V_X . The proposed design solves this issue by connecting the body of M_2 to ground, thus deleting this parasitic diode while slightly changing the SCM's equations;

(iii) An I_{REF} TC calibration circuit, necessary to maintain an acceptable TC in all process corners, can only be integrated in the previous reference as a binary-weighted current mirror at the cost of significant silicon area to achieve a sufficient resolution, but is rather straightforward to add to the proposed reference with a reasonable area overhead by tuning the effective width of either M_7 or M_9 through a digital code. A complete explanation of this calibration is provided in Section IV-A. This feature of the 4T voltage reference is what allows to reduce the measured TC from 565 down to 82 ppm/ $^\circ\text{C}$ for the proposed design in 22-nm FD-SOI;

(iv) The previous reference can only generate a fixed technology-dependent CWT offset related to the body factor and the ΔV_T between two transistors of different V_T types. There is consequently no degree of freedom to tune V_{off} apart from the transistor type. This issue is crucial as a too-low V_{off} leads to a large sensitivity $S_{I_{REF}}$ and thereby, to a degraded performance in terms of LS and variability of I_{REF} necessitating power and area overheads to mitigate it. Four performance metrics are thus negatively impacted by this lack of tunability. Yet, the proposed circuit allows to adjust V_{off} by simply changing the ratio S_7/S_6 , as illustrated in Figs. 4(a) and (b), making it possible to optimize V_{off} and to reliably reach acceptable performance in any technology.

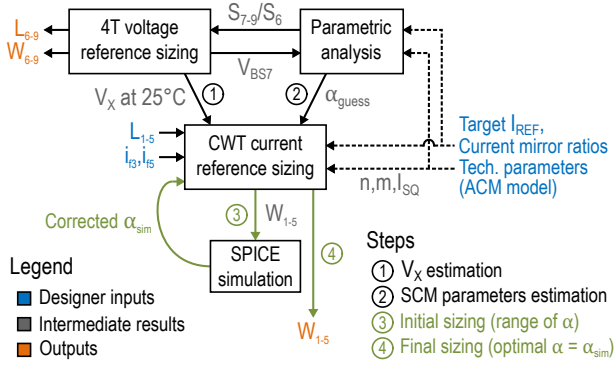


Fig. 5. Four-step flowchart of the design and sizing methodology.

Solving limitations (iii) and (iv), which are particularly critical regarding the overall performance achieved by the current reference in terms of LS, TC, silicon area, and variability, is only possible because of the proposed 4T voltage reference. This circuit is thus a key enabler of the high level of performance achieved in this work and a significant improvement compared to [12], which cannot be considered as a mere implementation detail. Nonetheless, the drawback of the proposed current reference is that the power consumption of the 4T voltage reference scales with the subthreshold I_{DS} leakage, and thus increases exponentially with temperature, leading to a larger power consumption than the β -multiplier-based reference at high temperature.

III. DESIGN AND SIZING METHODOLOGY

A. Overview of the Methodology

A flowchart of the sizing methodology is presented in Fig. 5. It is based on designer inputs such as the target reference current, the ratio of current mirrors, transistor lengths and inversion levels, as well as technological parameters estimated by fitting the ACM model to g_m/I_D curves extracted from SPICE simulations, following the procedure described in [23]. This methodology outputs transistor dimensions and can be divided into four main steps, with steps 1) and 2) being more iterative than sequential.

Step 1) sizes the 4T voltage reference and provides an estimate of V_{BS7} after sizing W_{8-9} to make it CWT.

Step 2) provides an educated guess for the value of α that minimizes I_{REF} TC, denoted as α_{guess} , for a fixed S_7/S_6 and a given S_9/S_6 .

Step 3) takes the estimated V_X at 25°C from step 1) and α_{guess} from step 2) to compute initial sizings of the current reference for a range of α values and fixed S_{7-9}/S_6 ratios in the TT process corner. These sizings, characterized by different W_{1-2} values, are used to run pre-layout SPICE simulations to extract the correct optimal value of α , denoted as α_{sim} , taking into account the exact transistors' behavior.

Step 4) simply consists in running the sizing algorithm with $\alpha = \alpha_{sim}$, thereby generating the final current reference sizing.

B. 4T Ultra-Low-Power Voltage Reference

The objectives of sizing the voltage reference, corresponding to step 1), are twofold. First, it aims at selecting a transistor

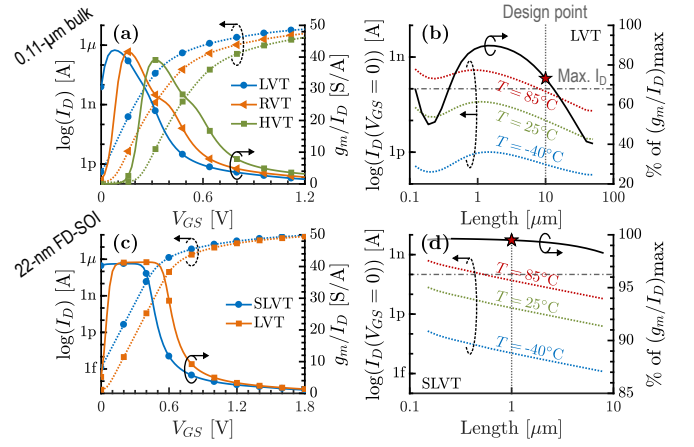


Fig. 6. All figures correspond to the SS process corner with a fixed $V_{DS} = V_{GS,max}/2$. $\log(I_D)$, g_m/I_D vs. V_{GS} curves at $T = -40^\circ\text{C}$ (a) in 0.11 μm for core LVT, RVT and HVT nMOS with $W = 0.5 \mu\text{m}$ and $L = 10.45 \mu\text{m}$, and (b) in 22 nm for I/O SLVT and LVT nMOS with $W = 2 \mu\text{m}$ and $L = 8 \mu\text{m}$. $\log(I_D)$ at $V_{GS} = 0$ and at -40, 25 and 85°C , and g_m/I_D at $V_{GS} = 0$ as a percentage of $(g_m/I_D)_{max}$ (b) in 0.11 μm for a core LVT nMOS with $W = 0.5 \mu\text{m}$ and L ranging from 0.12 to 50 μm , and (d) in 22 nm for an I/O SLVT nMOS with $W = 2 \mu\text{m}$ and L ranging from 0.15 to 8 μm .

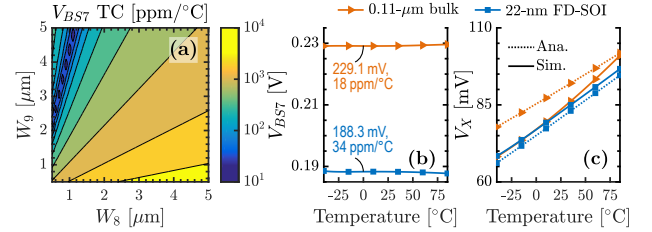


Fig. 7. V_{BS7} is made CWT by tuning the ratio S_9/S_8 in (15). All figures correspond to the TT process corner. (a) V_{BS7} TC from -40 to 85°C in 22 nm at 1.8 V, for W_{8-9} swept from 0.5 to 5 μm and $L_{8-9} = 1 \mu\text{m}$. Temperature dependence of (b) V_{BS7} (simulated), in 0.11 μm at 1.2 V with $S_7/S_6 = 4$ and $S_9/S_6 = 4$, and in 22 nm at 1.8 V with $S_7/S_6 = 2$ and $S_9/S_6 = 8$.

type and length that limit the nonidealities of the voltage reference while minimizing power consumption. Second, it strives to make V_{BS7} CWT by properly sizing W_{8-9} .

First, the 4T voltage reference can deviate from its ideal behavior at low temperature in the slow nMOS process corners. This behavior is explained by the fact that the subthreshold leakage ceases to decrease exponentially with temperature, either because of gate leakage becoming of the same order of magnitude as the I_{DS} one, or due to gate-induced drain leakage (GIDL), i.e., the increase of I_{DS} leakage at low V_{GS} and large V_{DS} [2]. The second explanation is the most likely for the two technologies presented in this work as their gate leakage is negligible. Indeed, 0.11- μm core devices still have a relatively thick oxide, while the devices used in 22 nm are I/O ones with high- κ gates. Both of these effects are nevertheless captured by a reduced g_m/I_D compared to $(g_m/I_D)_{max} = 1/(nU_T)$ at $V_{GS} = 0$. Note that g_m/I_D is simply the slope of the $\log(I_D)$ vs. V_{GS} curve.

On the one hand, Figs. 6(a) and (c) depict the $\log(I_D)$ vs. V_{GS} curves in the SS process corner for different transistor types in 0.11 μm and 22 nm, together with the corresponding g_m/I_D vs. V_{GS} curves. On the other hand, Figs. 6(b) and (d) illustrate the tradeoff between an ideal reference voltage behavior, coinciding with a g_m/I_D at $V_{GS} = 0$ close to

TABLE I
SIZING OF THE PROPOSED NA-RANGE CWT CURRENT REFERENCES.

		UMC 0.11- μm bulk*				GF 22-nm FD-SOI			
		w/o I_{REF} TC calib.		w/ I_{REF} TC calib.		w/o I_{REF} TC calib.		w/ I_{REF} TC calib.	
Type*		W [μm]	L [μm]	i_f	W [μm]	L [μm]	i_f	W [μm]	L [μm]
M_1	HS	0.915 [†]	40 $\times$ 30 $^\circ$	250.60	0.915 [†]	40 $\times$ 30 $^\circ$	SLVT	0.44 [†]	64 $\times$ 8 $^\circ$
M_2	HS	0.36 [†]	40 $\times$ 30 $^\circ$	164.33	0.36 [†]	40 $\times$ 30 $^\circ$	SLVT	0.215 [†]	64 $\times$ 8 $^\circ$
M_3	HS	6 $\times$ 1.25	5 $\times$ 10 $^\circ$	1.43	6 $\times$ 1.25	5 $\times$ 10 $^\circ$	LVT	6 $\times$ 5	5 $\times$ 1 $^\circ$
M_4	HS	2 $\times$ 1.25	5 $\times$ 10 $^\circ$	1.43	2 $\times$ 1.25	5 $\times$ 10 $^\circ$	LVT	2 $\times$ 5	5 $\times$ 1 $^\circ$
M_5	HS	1.2	10	0.10	1.2	10	SLVT	10	0.5
M_6	HS	2 $\times$ 2	10	-	4 $\times$ 2	20	SLVT	2 $\times$ 5.47	1
M_7	HS	8 $\times$ 2	10	-	16 $\times$ 2	20	SLVT	4 $\times$ 5.47	1
M_{7B}	HS	-	-	-	0.16	25	SLVT	4 $\times$ 5.47	1
M_8	LL	8 $\times$ 2	10	-	2 $\times$ 2	20	LVT	16 $\times$ 1.25	1
M_9	HS	8 $\times$ 2	10	-	2 $\times$ 2	20	SLVT	16 $\times$ 5.47	1
M_{SWi}	HS	-	-	-	0.16	25	ULL	-	5 $\times$ 8 $^\circ$
M_{7Vi}	-	-	-	-	-	-	SLVT	-	1
M_{9Vi}	HS	-	-	-	1 to 16 $\times$ 2	20	-	-	-

* Dimensions reported for UMC 0.11- μm bulk are pre-shrink ones, and must be scaled by a factor 0.9 $\times$ to obtain silicon dimensions.
* In 0.11 μm , HS refers to high-speed, i.e., LVT, and LL to low-leakage, i.e., HVT. In 22 nm, SLVT refers to super-low- V_T , LVT to low- V_T , and ULL to ultra-low-leakage, i.e., HVT. [†] Widths fine-tuned based on the outputs of the sizing algorithm to obtain the target I_{REF} . [°] $n \times L$ corresponds to a composite transistor, implemented with n transistors of length L μm connected in series.

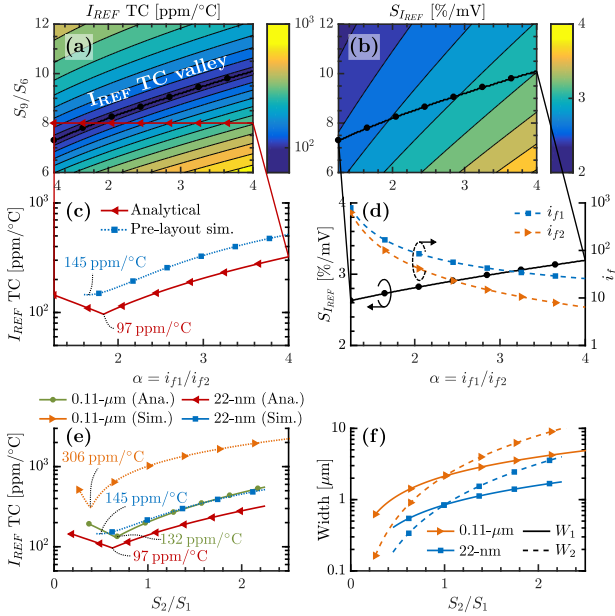


Fig. 8. I_{REF} is made CWT by properly selecting S_9/S_6 and α , for a fixed S_7/S_6 corresponding to a given CWT offset V_{off} . In 22 nm, (a) I_{REF} TC and (b) $S_{I_{REF}}$ for different values of $(S_9/S_6; \alpha)$, with $m = 1.63$, $n = 1.21$, and $S_7/S_6 = 2$, corresponding to $V_{off} = 17.3$ mV. (c) I_{REF} TC, (d) $S_{I_{REF}}$, and i_{f1-2} , as a function of α and computed from the analytical model and pre-layout simulations. In 0.11 μm and 22 nm and as a function of S_2/S_1 , (e) I_{REF} TC for the analytical model and pre-layout simulations and (f) W_{1-2} .

$(g_m/I_D)_{\max}$, and a low power consumption, proportional to I_D at $V_{GS} = 0$. Here, we set a maximum leakage of 100 pA at 85°C for a unitary transistor, but harsher power constraints could be imposed. It should also be observed that the I_{DS} leakage current, and consequently the power consumption, grow exponentially with temperature. In 0.11 μm , core low- V_T (LVT) devices are preferred to regular- or high- V_T (RVT or HVT) ones as they are the only transistor type to have an acceptable g_m/I_D drop at $V_{GS} = 0$ [Fig. 6(a)]. A length of 10 μm is selected, leading to a g_m/I_D at $V_{GS} = 0$ and -40°C worth 73.2 % of $(g_m/I_D)_{\max}$, and a 10.1-pA I_D at 25°C [Fig. 6(b)]. In addition, short-channel effects are visible for small transistor lengths. In 22 nm, I/O super-low- V_T (SLVT) devices are picked as they present a perfect behavior at $V_{GS} = 0$, contrary to LVT ones [Fig. 6(c)]. A length of 1 μm is chosen, reaching a g_m/I_D at $V_{GS} = 0$ and -40°C of 99.5 %

of $(g_m/I_D)_{\max}$ and a 2.08-pA I_D at 25°C [Fig. 6(d)].

Next, widths W_{8-9} are determined by a simple sweep, as exemplified in Fig. 7(a) for a 22-nm technology. This figure shows that an S_9/S_8 ratio of 4.38 leads to a CWT V_{BS7} , by having the TC of the second term in (15), which is proportional to U_T , compensate that of the difference of V_{T0} 's between M_{8-9} . The resulting pre-layout SPICE simulation results of V_{BS7} and V_X are shown in Figs. 7(b) and (c), together with analytical expression (14) for V_X . In 0.11 μm , M_8 and M_9 are respectively implemented with core HVT and LVT nMOS, yielding a 229-mV V_{BS7} with an 18-ppm/°C TC. Regarding V_X , the simulation presents a slightly larger PTAT slope than the analytical expression because of the temperature dependence of the body effect in bulk (11) leading to a non-zero ΔV_{T7} TC. In addition, the body factor γ_b^* is approximated using (13), thus leading to some discrepancies between the analytical expression and simulation. In 22 nm, M_8 and M_9 are respectively implemented with I/O LVT and SLVT nMOS, and a 188-mV V_{BS7} with a 34-ppm/°C TC is obtained. V_X 's simulated behavior is close to the analytical expression, mostly because γ_b^* in FD-SOI is temperature-independent at first order [21], thus making ΔV_{T7} approximately CWT. The simulation only differs from the analytical expression by a 1.9-mV offset.

C. Self-Cascode MOSFET

The parametric analysis of step 2) yields Figs. 8(a) and (b). In Fig. 8(a), the I_{REF} TC valley corresponds to a quasi-linear relationship between S_9/S_6 and α . However, Fig. 8(b) illustrates that this valley is not an iso- $S_{I_{REF}}$ curve as the sizing is performed in the $(S_9/S_6; \alpha)$ space instead of the $(K_{PTAT}; \alpha)$ one. Furthermore, the sizing of the current reference shares similarities with the sizing methodologies proposed in [10], [12]. It consists of four main steps:

- Compute voltage V_X at 25°C using (14) or use the pre-layout simulation value obtained from step 1);
- Solve (5) for i_{f2} , then calculate $i_{f1} = \alpha i_{f2}$, $S_{I_{REF}}$ from (8), S_2 from (3), and S_1 from (6);
- Compute the aspect ratio of transistors M_{3-4} forming the pMOS current mirror using (3) while ensuring that $V_{SG4} > 4U_T$;
- Compute the aspect ratio of M_5 using (3) while ensuring that $V_Y = V_X + V_{GS5} > 4U_T$.

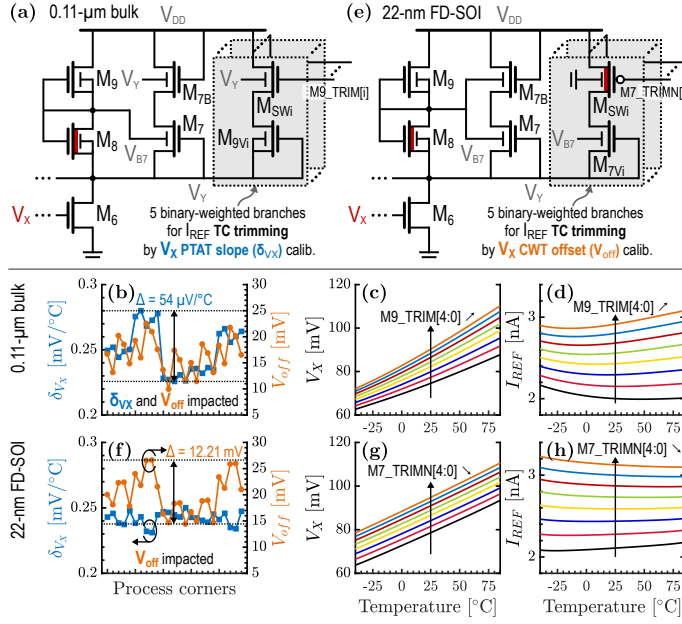


Fig. 9. I_{REF} 's temperature independence can be maintained across process corners by tuning V_X PTAT slope (δV_X) in 0.11- μm bulk or V_X CWT offset (V_{off}) in 22-nm FD-SOI. Schematic of the 4T voltage reference with I_{REF} TC calibration circuit in (a) 0.11 μm and (b) 22 nm. δV_X and V_{off} in process corners (considering skewed process corners of the nMOS of different V_T types used for M_{8-9}) in (b) 0.11 μm and (f) 22 nm. Temperature dependence of V_X and I_{REF} for different 5-bit calibration codes in (c)(d) 0.11 μm and (g)(h) 22 nm, in the TT process corner.

TABLE II

SUMMARY OF THE SIMULATED AND MEASURED PERFORMANCE OF THE PROPOSED NA-RANGE CWT REFERENCES.

	UMC 0.11- μm bulk				GF 22-nm FD-SOI			
	w/o TC calib.	w/ TC calib.	w/o TC calib.	w/ TC calib.	w/o TC calib.	w/ TC calib.	w/o TC calib.	w/ TC calib.
I_{REF} [nA]	2.49	2.74	2.40	2.30	2.48	2.32	2.50	2.54
Power [nW]	17.03	19.37	16.65	16.82	15.43	14.44	15.49	16.30
Area [μm^2]	@1.2V	@1.2V	@1.2V	@1.2V	@1.5V	@1.5V	@1.5V	@1.5V
	0.00657		0.01061		0.00222		0.00255	
Supply range [V]	0.8 – 1.2		0.8 – 1.2		1 – 1.8		1 – 1.8	
LS [%/V]	2.94	2.60	2.07	2.23	0.21	1.47	0.26	1.53
Temp. range [$^{\circ}\text{C}$]	-40 – 85		-40 – 85		-40 – 85		-40 – 85	
TC [ppm/ $^{\circ}\text{C}$]	330.7	529.5	290.6	176.0	137.5	360.6	101.5	81.5
I_{REF} var. (process) [%]	6.00		7.53		3.16		4.18	
I_{REF} var. (mismatch) [%]	1.32	2.11	1.74	3.47	2.68	2.48	2.41	2.55
t_{start} [ms]	15.25	17.53	16.21	18.22	3.29	11.56	3.26	11.20

Let us now have a closer look at the results of the sizing algorithm shown in Figs. 8(c) to (f). First, Fig. 8(d) illustrates that there is an interest in choosing small values of α as they result in a lower $S_{I_{REF}}$. This trend stems from the fact that M_{1-2} are biased in moderate ($i_f \in [1; 100]$) or strong ($i_f > 100$) inversion, at the cost of a larger minimum supply voltage. They will remain close to this inversion level in process corners thanks to the SCM structure, and in temperature corners thanks to the relatively limited variations of i_f with temperature [Fig. 3(b)]. A design point corresponding to $(S_9/S_6; \alpha_{guess}) = (8; 1.825)$ is selected based on Figs. 8(a) and (c), yielding an I_{REF} TC = 96.7 ppm/ $^{\circ}\text{C}$ and $S_{I_{REF}} = 2.77\%/\text{V}$. Pre-layout SPICE simulations in steps 3) and 4) reveal that a 145-ppm/ $^{\circ}\text{C}$ I_{REF} TC is eventually reached for $\alpha_{sim} = 1.65$, also corresponding to $S_{I_{REF}} = 2.73\%/\text{V}$. Fig. 8(e) depicts the same kind of results as Fig. 8(c), but as a function of S_2/S_1 , used as a proxy for α and calculated from (6). In 0.11 μm ,

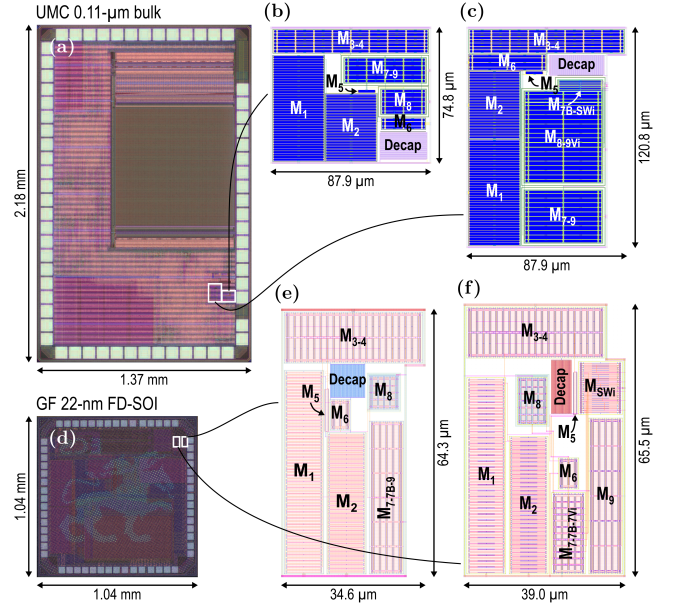


Fig. 10. Chip microphotographs with overlaid layout in (a) UMC 0.11- μm bulk and (d) GF 22-nm FD-SOI. Layouts of the proposed nA-range CWT current references (b)(e) without and (c)(f) with I_{REF} TC calibration.

the difference between the 131.5-ppm/ $^{\circ}\text{C}$ analytical optimum located at $S_2/S_1 = 0.66$ and the 306-ppm/ $^{\circ}\text{C}$ pre-layout one obtained for $S_2/S_1 = 0.39$ originates from the temperature dependence of the body effect, which was not accounted for in the analytical model, as detailed in Section III-B. In 22 nm, the 96.7-ppm/ $^{\circ}\text{C}$ analytical optimum located at $S_2/S_1 = 0.62$ and the 145-ppm/ $^{\circ}\text{C}$ pre-layout one obtained for $S_2/S_1 = 0.49$ are closer to each other but still differ due to inaccuracies of the ACM model, and more specifically, of the fitting of the temperature exponent of carrier mobility m . Finally, Fig. 8(f) demonstrates that W_{1-2} decrease with α as M_{1-2} are biased in stronger inversion while keeping L_{1-2} and I_{D1-2} fixed. In addition, the transistor widths are larger in 0.11 μm because M_{1-2} are $\approx 2\times$ longer in this technology ($L = 40\times 30\ \mu\text{m} = 1.2\ \text{mm}$) than in 22 nm ($L = 64\times 8\ \mu\text{m} = 512\ \mu\text{m}$).

IV. SIMULATION AND MEASUREMENT RESULTS

In this section, we present the I_{REF} TC calibration circuit implemented in the proposed reference, and provide an overview of the implemented current references and the measurement setup. Then, we discuss into details the post-layout simulations and measurements of the designs in 0.11- μm bulk and 22-nm FD-SOI, whose summary is provided in Table II.

A. I_{REF} TC Calibration and Overview of the Designs

Fig. 9 shows the I_{REF} TC calibration mechanism implemented in the proposed current references. First, in 0.11- μm bulk, process variations (including skewed process corners of M_{8-9}) impact V_X PTAT slope (δV_X) and CWT offset (V_{off}) [Fig. 9(b)], with total variations of 54 $\mu\text{V}/^{\circ}\text{C}$ and 12.57 mV, respectively. When both quantities are impacted, we observe that calibrating δV_X is more effective than calibrating V_{off} in terms of number of components. Tuning the number of transistors placed in parallel to implement M_9 using a calibration code [Fig. 9(a)] modifies δV_X by changing the ratio S_9/S_6 in (14)

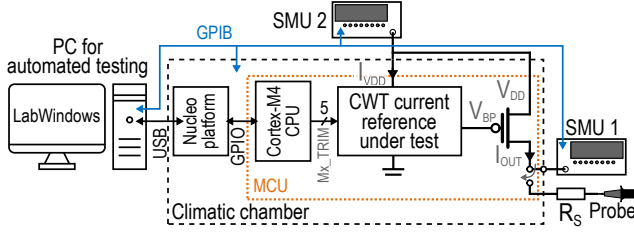


Fig. 11. Conceptual measurement testbench for startup time, supply voltage and temperature dependence characterization.

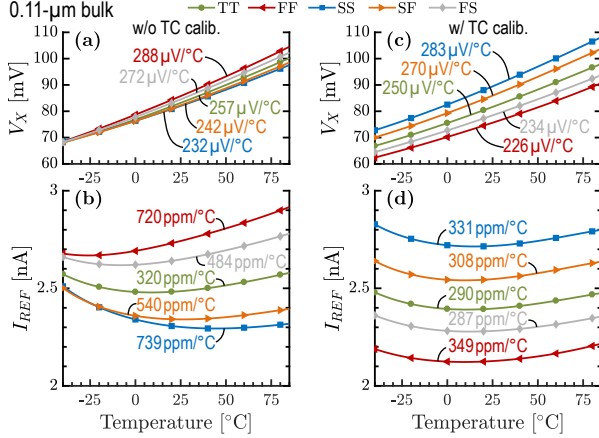


Fig. 12. In UMC 0.11- μm bulk, post-layout simulation of the temperature dependence of V_X and I_{REF} , in all process corners and at 1.2 V, without [(a) and (b)] and with I_{REF} TC calibration [(c) and (d)].

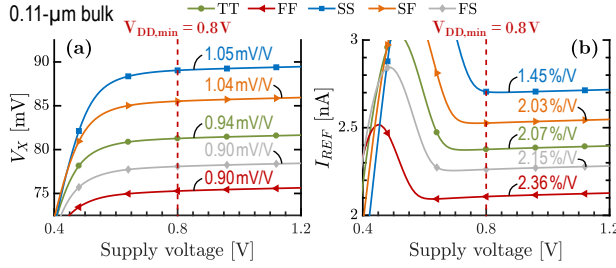


Fig. 13. In UMC 0.11- μm bulk, post-layout simulation of the supply voltage dependence of (a) V_X and (b) I_{REF} in all process corners and at 25°C, with I_{REF} TC calibration.

[Fig. 9(c)], thus allowing to adjust the I_{REF} TC [Fig. 9(d)]. Then, in 22-nm FD-SOI, process variations mostly impact V_X CWT offset (V_{off}) with a total variation of 12.21 mV, and have a lesser influence on δV_X than in 0.11 μm , as it only changes by 19 $\mu\text{V}/^\circ\text{C}$ [Fig. 9(f)]. It is then more effective to calibrate V_{off} . Tuning the number of transistors placed in parallel to implement M_7 using a calibration code [Fig. 9(e)] impacts V_{off} by changing the ratio S_7/S_6 in (14) [Fig. 9(g)], thus providing another way to calibrate the I_{REF} TC [Fig. 9(h)]. Besides, for both technologies, the TC calibration range can be extended to provide a design margin against inaccurate device models. In addition, the impact of junction leakage, gate leakage, or parasitic diode leakage on the 4T voltage reference remains below 1 % of the total current in all PVT corners, preventing nonidealities and avoiding the need for any circuit adjustment. Two current references, respectively without and with I_{REF} TC calibration, have been fabricated in each of the UMC 0.11- μm bulk and GF 22-nm FD-SOI technology nodes. Chip microphotographs, layouts and final

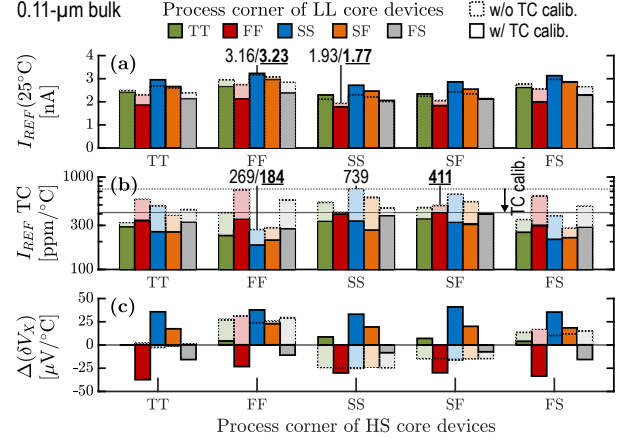


Fig. 14. In UMC 0.11- μm bulk and at 1.2 V, post-layout simulation of (a) I_{REF} at 25°C, (b) I_{REF} TC from -40 to 85°C, and (c) the change in PTAT slope of V_X with respect to its nominal value, without and with TC calibration. Skewed process corners of LL and HS core devices are considered.

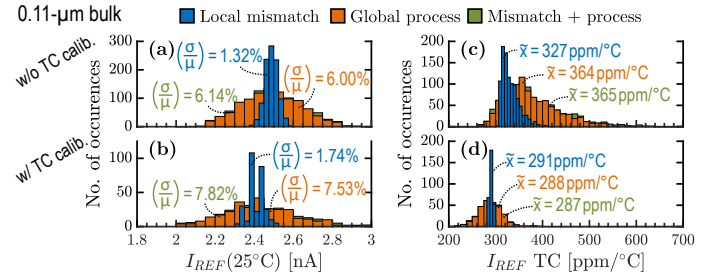


Fig. 15. In UMC 0.11- μm bulk, for $10^3 / 3 \times 10^2$ post-layout MC simulations in TT at 1.2 V, histograms of I_{REF} at 25°C [(a) and (b)] and of I_{REF} TC from -40 to 85°C [(c) and (d)], without [(a) and (c)] and with I_{REF} TC calibration [(b) and (d)]. $\tilde{x}$ denotes the median of a statistical distribution.

dimensions of these four current references can be found in Fig. 10 and Table I, respectively. Based on these references, the area overhead of the the TC calibration circuit is estimated to be 61.5 % compared to the design without calibration in 0.11 μm , and 14.9 % in 22 nm. This gap in area overhead originates from the much-longer transistors used in the TC calibration circuit in 0.11 μm . Only the power consumption of the 4T voltage reference is affected by the calibration, and the power overhead is thus dependent on the calibration code.

B. Measurement Testbench

The measurement setup is schematized in Fig. 11. The proposed current references are integrated in microcontroller units (MCUs), called (i) MANTIS in 0.11- μm bulk, intended for near-sensor image processing applications, and (ii) CERBERUS in 22-nm FD-SOI, intended for edge machine-learning applications and low-power wide-area network communication. Eleven dies have been measured in each technology node. Furthermore, the testing is controlled by a host PC controlling an Espec SH-261 climatic chamber for the temperature sweep, and two Keithley K2450 source measure units (SMUs) for the supply voltage sweep. Note that the stabilization time at each temperature step is sufficiently long to ensure that the die reaches the same temperature as the chamber. Besides, SMU 1 measures the output current I_{OUT} with $V_{SD} = V_{DD,max}/2$, respectively equal to $4\times$ and $8\times I_{REF}$ in 0.11 μm and 22 nm, and SMU 2, the sum of I_{OUT} and the supply current

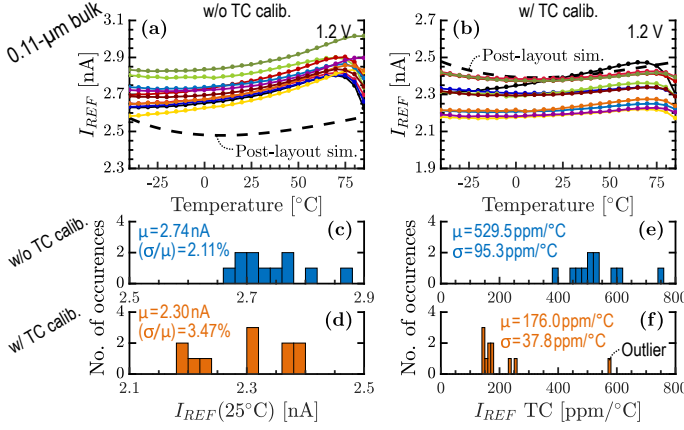


Fig. 16. In UMC 0.11- μm bulk and at 1.2 V, measured temperature dependence of I_{REF} (a) without and (b) with I_{REF} TC calibration. Measured histograms of I_{REF} at 25°C [(c) and (d)] and of I_{REF} TC from -40 to 85°C [(e) and (f)], without and with I_{REF} TC calibration.

I_{VDD} . The pMOS current mirror generating I_{OUT} employs a common-centroid layout to accurately replicate I_{REF} , and only marginally augments I_{REF} (σ/μ) by 0.03 and 0.06 % in 0.11 μm and 22 nm, respectively. In addition, the host PC controls the TC calibration code through a Nucleo platform interacting with the on-chip Cortex-M4 central processing unit (CPU). At last, startup measurements are performed by replacing SMU 1 with an 82-/47-M Ω resistor R_S in series with the 1-M Ω input resistance of the oscilloscope probe.

C. Designs in 0.11- μm Bulk CMOS Technology

First, we discuss the post-layout simulation results of the references. Fig. 12(a) reveals that, without TC calibration, δV_X spans from 232 to 288 $\mu\text{V}/^\circ\text{C}$ due to process variations of the subthreshold slope factor n . This results in a 739-ppm/°C CTAT to 720-ppm/°C PTAT I_{REF} TC in Fig. 12(b). With TC calibration, δV_X is adapted to each process corner [Fig. 12(c)], leading to an I_{REF} TC between 287 and 349 ppm/°C with a residual second order temperature dependence [Fig. 12(d)]. Then, Fig. 13 presents the supply voltage dependence of the reference with TC calibration, whose TC has been calibrated in each process corner. Fig. 13(a) shows that V_X LS lies between 0.9 and 1.05 mV/V from 0.8 to 1.2 V. The analytical expression of the minimum supply voltage is given by

$$V_{DD,min} = 4U_T + \max(V_G, V_X + V_{SG4}, V_X + V_{GS5} + V_{GS8}), \quad (18)$$

and $V_{DD,min} = 0.8 \text{ V}$ is here limited by voltage V_G in the SCM. This translates into an LS of I_{REF} between 1.45 and 2.36 %/V in Fig. 13(b). Next, we consider skewed process corners of high-speed (HS), i.e., LVT, and low-leakage (LL), i.e., HVT, core devices in Fig. 14. We thus consider independent process variations for transistors of different V_T types. The TC calibration moderately raises I_{REF} process variations from +26.4 % / -22.8 % to +29.2 % / -29.2 % in the (FF, SS) and (SS, FF) corners, respectively. This behavior stems from tuning δV_X , which affects the value of V_X itself [Fig. 14(a)]. Meanwhile, the calibration shifts the TC from 289 to 739 ppm/°C, down to 184 to 411 ppm/°C [Fig. 14(b)]. The calibration mechanism tends to harmonize δV_X for a given LL process corner, while δV_X was initially quite uniform in a given

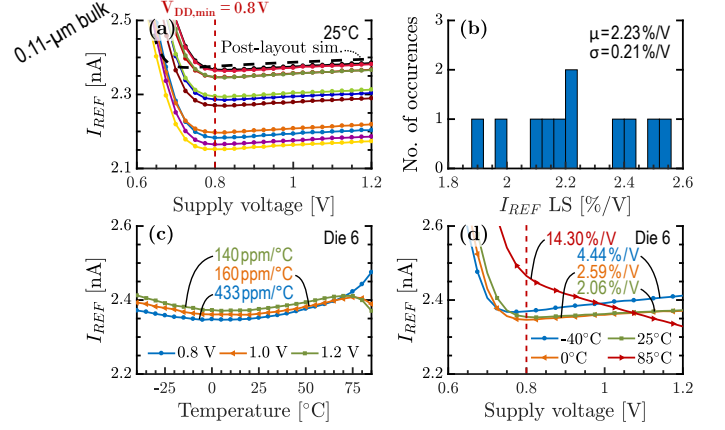


Fig. 17. In UMC 0.11- μm bulk and for the design with I_{REF} TC calibration, (a) measured supply voltage dependence at 25°C and (b) histogram of LS from 0.8 to 1.2 V. For die 6, measured (c) temperature dependence at different supply voltages and (d) supply voltage dependence at different temperatures.

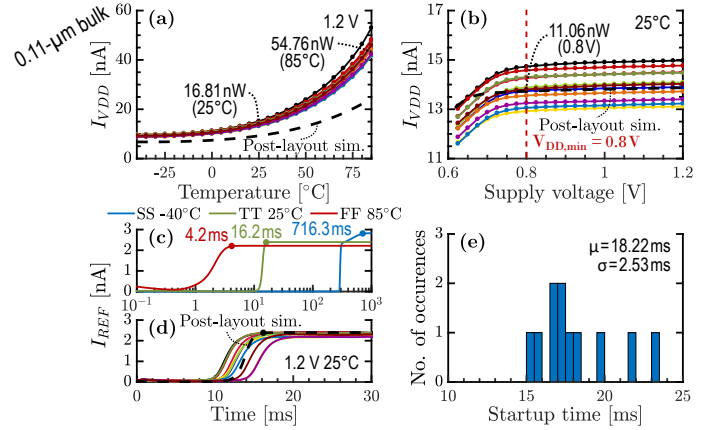


Fig. 18. In UMC 0.11- μm bulk, measured dependence of the supply current (a) to temperature at 1.2 V, and (b) to supply voltage at 25°C. (c) Post-layout-simulated RCC startup waveforms in extreme corners, and (d) measured startup waveforms and (e) histogram of 99-% startup time, at 1.2 V 25°C.

HS process corner [Fig. 14(c)]. Finally, Fig. 15(a) emphasizes that, without TC calibration, I_{REF} varies more significantly due to global process variations, with a 6-% (σ/μ), than from local mismatch, with a 1.32-% (σ/μ). The same conclusion can be drawn with TC calibration [Fig. 15(b)], with slightly larger (σ/μ)'s of 7.53 % and 1.74 % for process and mismatch, due to a different sizing of the 4T voltage reference for the TC calibration circuit, coupled with the tendency of the calibration to accentuate I_{REF} variations. Regarding I_{REF} TC, calibration improves the median value $\bar{x}$ by 40 to 80 ppm/°C, but most notably shortens the tail of the distribution, with a 99th percentile for combined process and mismatch reduced from 576 to 364 ppm/°C [Figs. 15(c) and (d)].

Then, we present the measurement results of the 11 dies. The temperature dependence without and with TC calibration is shown in Figs. 16(a) and (b). We notice a drop of I_{REF} at high temperature which is due to the leakage of the electrostatic discharge (ESD) protection diodes in the I/O pad connected to SMU 1. In Figs. 16(c) and (d), average values of 2.74 and 2.30 nA are obtained, with (σ/μ)'s of 2.11 and 3.47 %. This variability is above the simulated one for local mismatch, suggesting that the measured dies originate from different process batches. It should be noted that, if required by

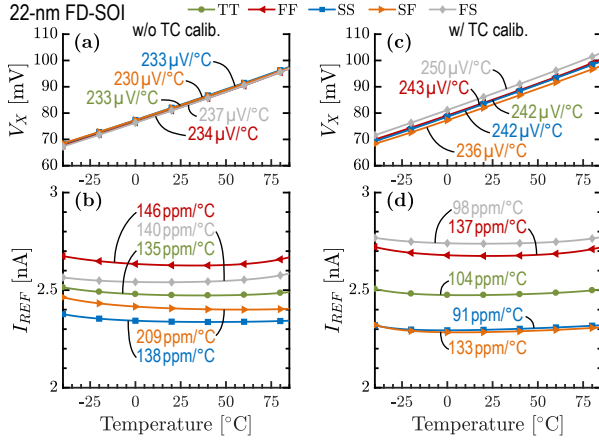


Fig. 19. In GF 22-nm FD-SOI, post-layout simulation of the temperature dependence of V_X and I_{REF} , in all process corners and at 1.8 V, without [(a) and (b)] and with I_{REF} TC calibration [(c) and (d)].

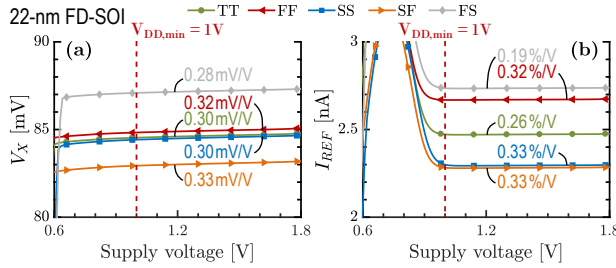


Fig. 20. In GF 22-nm FD-SOI, post-layout simulation of the supply voltage dependence of (a) V_X and (b) I_{REF} in all process corners and at 25°C, with I_{REF} TC calibration.

the applicative context, a calibration of I_{REF} could readily be implemented using a binary-weighted current mirror. Finally, the calibration improves the TC from 530 to 176 ppm/°C, and also reduces σ from 95 to 38 ppm/°C [Figs. 16(e) and (f)]. It should be noted that the 575-ppm/°C outlier in Fig. 16(f), corresponding to the black curve in Fig. 16(b), is not accounted for in the mean. These results are obtained with a complete knowledge of the temperature profile between -40 and 85°C, but a two-point calibration at -25 and 85°C yields similar results, with a mean TC marginally increased to 182 ppm/°C. Moving on to the supply voltage dependence, the details of the 11 dies are shown in Fig. 17(a), and an average LS of 2.23 %/V is achieved in Fig. 17(b). This value is close to the 2.07 %/V obtained in TT post-layout simulation, which is not surprising given the good agreement between simulation and measurement in Fig. 17(a). Then, Fig. 17(c) highlights that the I_{REF} drop at high temperature transforms into an I_{REF} surge as supply voltage decreases. This behavior arises from the fact that, at 85°C, I_{REF} decreases with V_{DD} while it presents a normal supply voltage dependence at all other temperatures [Fig. 17(d)]. For a 0.8-V supply, the leakage of the ESD diodes between the pad and the supply voltages (core and I/O) dominates and increases the measured I_{OUT} , while at 1.2 V, the leakage of the diodes between the pad and ground is prevalent and decreases the measured I_{OUT} . Next, in Fig. 18(a), the supply current is around 10 nA at low temperature as it is dominated by the SCM which draws a current equal to $(N + 1)I_{REF}$ with a current ratio $N = 3$, while at high temperature, it scales exponentially as the power

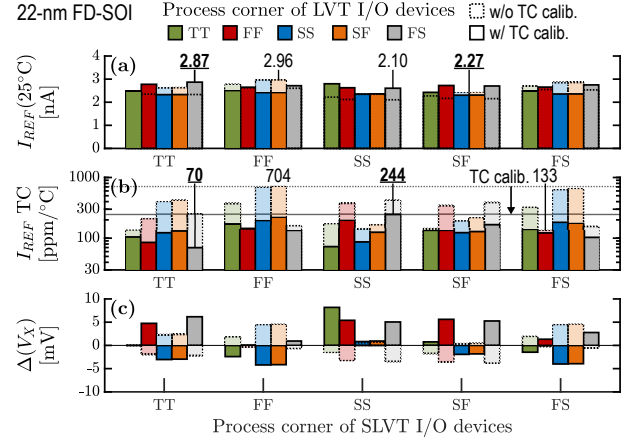


Fig. 21. In GF 22-nm FD-SOI and at 1.8 V, post-layout simulation of (a) I_{REF} at 25°C, (b) I_{REF} TC from -40 to 85°C, and (c) the change in PTAT slope of V_X with respect to its nominal value, without and with TC calibration. Skewed process corners of SLVT and LVT I/O devices are considered.

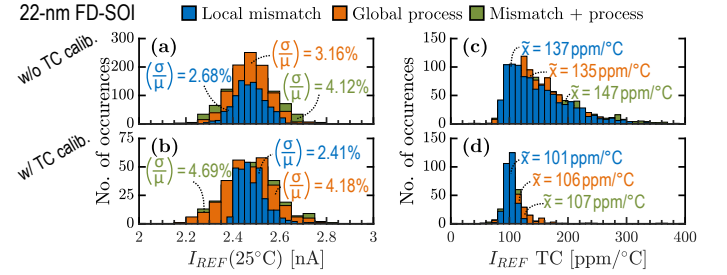


Fig. 22. In GF 22-nm FD-SOI, for $10^3 / 3 \times 10^2$ post-layout MC simulations in TT at 1.8 V, histograms of I_{REF} at 25°C [(a) and (b)] and of I_{REF} TC from -40 to 85°C [(c) and (d)], without [(a) and (c)] and with I_{REF} TC calibration [(b) and (d)]. $\tilde{x}$ denotes the median of a statistical distribution.

consumption of the 4T voltage reference is proportional to the I_{DS} leakage. At 1.2 V, average power consumptions of 16.8 and 54.8 nW are reached at 25 and 85°C, respectively. The steeper supply current increase in measurement compared to the TT simulation indicates that the dies might be from a fast nMOS process corner. Fig. 18(b) shows that the drawn current does not substantially increase with the supply voltage, and that a minimum average power consumption of 11.1 nW is achieved at 0.8 V. Finally, the x-% startup time is computed as the time at which I_{REF} remains within (100-x) % of its steady-state value. The 99-% startup time has a simulated nominal value of 16.2 ms and a worst-case one of 716.3 ms in the SS -40°C corner [Fig. 18(c)]. At 1.2 V and 25°C, the measured startup time is 18.2 ms on average [Figs. 18(d) and (e)], and confirms the inutility of a startup circuit.

D. Designs in 22-nm FD-SOI CMOS Technology

Similarly to the results in 0.11 μm , we first discuss the post-layout simulations results. Fig. 19(a) shows that, without TC calibration, δV_X is less process-dependent than in 0.11 μm , and takes lower values between 230 and 237 $\mu\text{V}/^\circ\text{C}$. These two observations are linked to the subthreshold slope factor, which can be defined as $n = 1 + C_d/C_{ox}$. In bulk, C_d is the depletion layer capacitance, while in FD-SOI, C_d is the capacitance between the back-gate and the channel due to the buried oxide. This capacitance is process-invariant at first order, and smaller than the depletion layer capacitance,

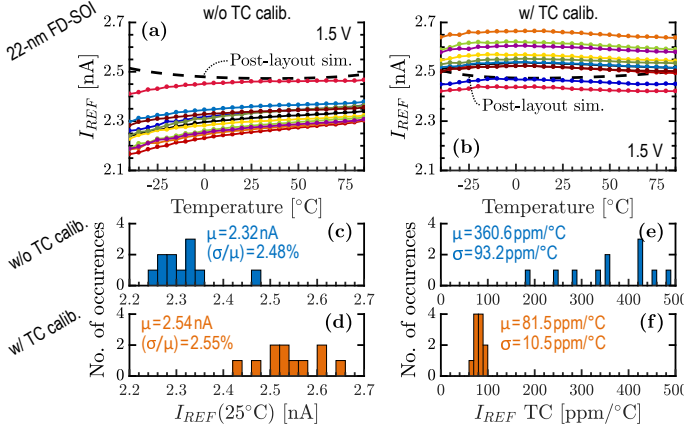


Fig. 23. In GF 22-nm FD-SOI and at 1.5 V, measured temperature dependence of I_{REF} (a) without and (b) with I_{REF} TC calibration. Measured histograms of I_{REF} at 25°C [(c) and (d)] and of I_{REF} TC from -40 to 85°C [(e) and (f)], without and with I_{REF} TC calibration.

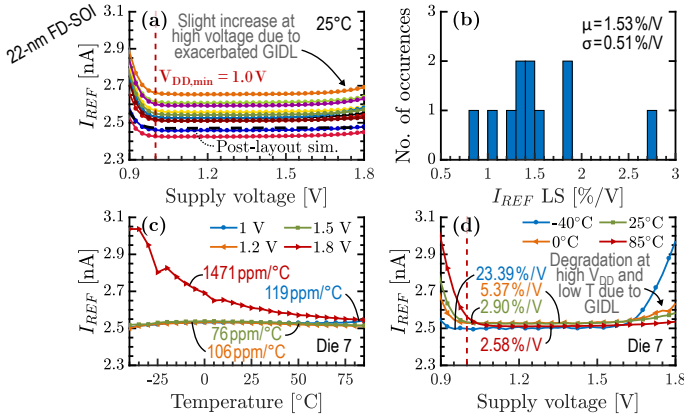


Fig. 24. In GF 22-nm FD-SOI and for the design with I_{REF} TC calibration, (a) measured supply voltage dependence at 25°C and (b) histogram of LS from 1 to 1.8 V. For die 7, measured (c) temperature dependence at different supply voltages and (d) supply voltage dependence at different temperatures.

thus explaining our observations. The resulting I_{REF} TC is comprised between 138 and 209 ppm/°C [Fig. 19(b)]. In 22 nm, the TC calibration changes V_{off} [Fig. 19(c)] and reduces I_{REF} TC between 91 to 137 ppm/°C [Fig. 19(d)]. The necessity of the TC calibration might not be obvious from the analysis of conventional process corners, but will become clear when discussing skewed process corners herebelow. Besides, Fig. 20 shows that, for the reference with TC calibration, V_X LS is around 0.28 to 0.32 mV/V [Fig. 20(a)], which is more than $3\times$ lower than in 0.11 μm thanks to the large intrinsic gain (g_m/g_d) in FD-SOI [24], thereby improving the LS, as it is usually proportional to (g_d/g_m) . This translates into an I_{REF} LS between 0.19 and 0.33 %/V from 1 to 1.8 V, with $V_{DD,min} = 1$ V also limited by V_G in the SCM. The larger $V_{DD,min}$ compared to 0.11 μm stems from a larger V_G , likely due to a different value of I_{SQ} and/or V_{T0} for transistors M_{1-2} implementing the SCM. Next, we consider skewed process variations of SLVT and LVT I/O devices in Fig. 21. Contrary to the 0.11- μm design, the TC calibration somewhat reduces I_{REF} process variations from +18.4 % / -16 % to +14.8 % / -9.2 % [Fig. 21(a)]. The max./min. values are however not attained in the same corners without and with TC calibration. I_{REF} TC is reduced from the 133-to-704-

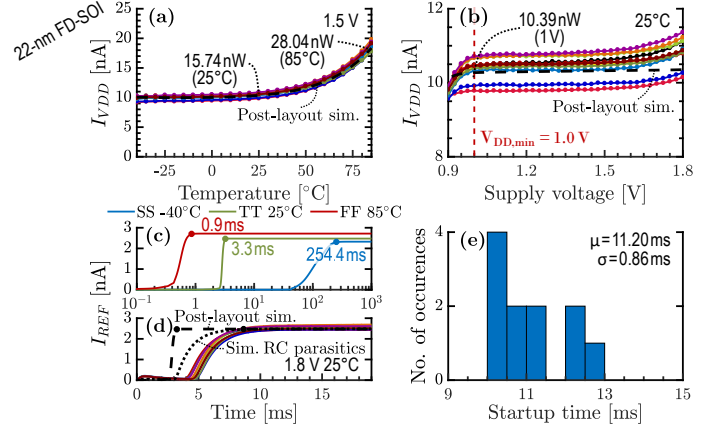


Fig. 25. In GF 22-nm FD-SOI, measured dependence of the supply current (a) to temperature at 1.5 V, and (b) to supply voltage at 25°C. (c) Post-layout-simulated RCC startup waveforms in extreme corners, and (d) measured startup waveforms and (e) histogram of 99-% startup time, at 1.8 V 25°C.

ppm/°C range down to the 70-to-204-ppm/°C one, pointing out the importance of this calibration to maintain performance across process corners [Fig. 21(b)]. We notice that the effect of the TC calibration is to slightly increase V_{off} in fast LVT nMOS corners, and to decrease it in slow LVT nMOS corners [Fig. 21(c)]. Regarding I_{REF} variability at 25°C, similarly to the 0.11- μm references, the impact of local mismatch is more limited than that of global process variations, but with values that are nonetheless closer from each other, with a 2.68-% and 3.16-% (σ/μ)'s for mismatch and process variations without TC calibration [Fig. 22(a)]. With TC calibration, the impact of mismatch is reduced to a 2.41-% (σ/μ), while the impact of process is a bit more significant due to the TC calibration itself, with a value of 4.18 % [Fig. 22(b)]. The median TC improves by roughly 40 ppm/°C when the TC is calibrated, and the tail of the distribution is also reduced, with the 99th percentile for combined variations diminished from 333 to 239 ppm/°C [Figs. 22(c) and (d)].

Continuing with the measurement results, Figs. 23(a) and (b) depict the temperature dependence without and with TC calibration for a supply voltage of 1.5 V, instead of 1.8 V in post-layout simulation results. This choice is related to nonidealities in the 4T voltage reference and will be explained later in this paragraph. Figs. 23(c) and (d) present 2.32- and 2.54-nA average values of I_{REF} without and with TC calibration, with (σ/μ)'s of 2.48 and 2.55 %. These results are in line with post-layout simulations and suggest that the measured dies come from the same process batch, as the variability has the same magnitude as the one due to local mismatch in simulation. The TC calibration mechanism cuts the TC from 361 to 82 ppm/°C, with a sharp reduction of σ from 93 to 11 ppm/°C. In addition, it is interesting to note that all measured dies present a TC lower than 100 ppm/°C. Similarly to the 0.11- μm design, these results correspond to a calibration based on the complete temperature profile between -40 and 85°C, but a two-point calibration at -40 and 80°C gives comparable results and only slightly increases the mean TC to 82.7 ppm/°C. Furthermore, Fig. 24(a) reveals a modest rise of I_{REF} at high supply voltage, due to the exacerbated GIDL at high V_{DS} in the zero- V_{GS} transistors

TABLE III
COMPARISON TABLE OF TEMPERATURE-INDEPENDENT nA-RANGE CURRENT REFERENCES.

Type of work	Simulations										Silicon measurements										
	Far [25]	Cordova [26]	Santamaria [27]	Agarwal [28]	Aminzadeh [29]	Mahmoudi [30]	Bruni [31]	Huang [20]	Yang [32]	De Vita [33]	Kayahan [34]	Ji [35]	Wang [36]	Wang [37]	Huang [38]	Lee [39]	Chang [40]	Shetty [41]	Lefebvre [12]	Lefebvre This work	
Publication Year	ROPEC 2015	ISCAS 2017	ISCAS 2019	TCAS-II 2022	AEU 2022	2022	CAE 2023	AEU 2023	AEU 2023	ISCAS 2007	TCAS-I 2013	ISSCC 2017	VLSI-DAT 2019	TCAS-I 2019	TCAS-II 2020	JSSC 2020	JJAP 2020	TCAS-I 2022	JSSC 2023	JSSC 2024	
Samples	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	20	90	10	10	16	10	10	3	10	20	11 11	
Technology	0.18μm	0.18μm	0.18μm	0.18μm	0.18μm	0.13μm	0.18μm	0.18μm	0.18μm	0.35μm	0.35μm	0.18μm	0.18μm	0.18μm	0.18μm	0.18μm	90nm	0.13μm	22nm	0.11μm 22nm	
I _{REF} [nA]	14	10.9	2.7	5.6	6.7	6.6	6.3	8.9	1.96	9.1	25	6.7	6.5	9.8	11.6	1	1.3	1.9	1.25/0.9*	2.4/2.3* 2.5/2.5*	
Power [nW]	150	30.5	26	9.5	51	3.7	3.3	0.05	9.2	109.7	28500	9.3	15.8	28	48.6	4.5/14	8.6	30	7.8/5.8*	16.7/16.8* 15.5/16.3*	
	@1V	@0.9V	@2V	@0.55V	@1V	@0.4V	@0.6V	@0.8V	@0.55V	@3V	@5V	@N/A	@0.85V	@0.7V	@0.8V	@1.5V	@0.75V	@2.5V	@0.9V	@1.2V @1.5V	
Area [mm ²]	0.0102	0.01	0.0093	0.032	0.46	0.0021	0.0018	0.008	0.0033	0.035	0.0053	0.055	0.062	0.055	0.054	0.332	0.0175	0.0163	0.0132	0.0106 0.00255	
Supply range [V]	1 – 3.3	0.9 – 1.8	2 – 3.63 [†]	0.55 – 1.9	1.1 – 1.8	0.4 – 1.6	0.6 – 1.8	0.8 – 1.8	0.55 – 1.8	1.5 – 4	N/A	1.3 – 1.8	0.85 – 2	0.7 – 1.2	0.8 – 2	1.5 – 2	0.75 – 1.55	0.85 – 2	0.9 – 1.8	0.8 – 1.2 1 – 1.8	
LS [%/V]	0.1	0.54	8.9 [°]	0.022	0.03	2.7	12.1	1.39	0.2	0.57	150	1.16	4.15	0.6	1.08	1.4	0.15	4	0.26/0.39*	2.07/2.23* 0.26/1.53*	
Temp. range [°C]	0 – 70	-20 – 120	-40 – 125	-30 – 70	-40 – 120	-40 – 120	-40 – 120	-40 – 120	0 – 100	0 – 80	0 – 80	0 – 110	-10 – 100	-40 – 125	-40 – 120	-20 – 80	0 – 120	-40 – 120	-40 – 85	-40 – 85 -40 – 85	
TC [ppm/°C]	20	108	309	256	40.3	308	219	139	96.8	44	128/250*	680/283 [†]	157	150	169	289/265 [‡]	53/394*	530/822*	203/565*	290/176* 101/82*	
TC type	Typ.	μ	μ	μ	μ	μ	Typ.	μ	μ	μ	N/A	μ	μ	μ	μ	μ	μ	μ	μ	μ	
I _{REF} var. (process) [%]	N/A	15.8 / 11.6 [†]	N/A	+55.4 / -28.5 [°]	N/A	N/A	+129.1 / -61.8 [°]	+2.8 / -13.9 [°]	8.7	2.16	8/1.22*	N/A	N/A	+11.7 / -8.7 [°]	+17.6 / -10.3 [°]	N/A	21.1	N/A	+9.9 / -9.5	+34.8 / -25.9	
I _{REF} var. (mismatch) [%]	5.8	N/A	20.3	10.4	0.7	6.1	N/A	2.6	1.7	1.4	4.07/1.19*	3.33	1.6	4.3	1.26/0.25 [†]		15.6	6.39/9.20*	1.74/3.47* 2.41/2.55*		
Trimming	No	Yes	No	No	No	Yes	No	No	No	No	No	Yes	No	Yes	Yes	Yes	Yes	Yes	No	Yes	
Spec. components	No	Yes	ZVT	No	Res.	Res., BJT	Yes	No	No	No	No	Res., BJT	No	Yes	Yes	No	No	Yes	No	Yes	
FoM [ppm/°C ² × mm ²]	0.0029	0.0077	0.0174	0.0819	0.1159	0.0040	0.0025	0.0089	0.0032	0.0193	0.0166	0.1415	0.0887	0.0499	0.0570	0.9595	0.0575	0.0835	0.0597	0.0149 0.0017	

* Simulated and measured values. † Before and after trimming. ° Estimated from figures. ‡ For 25 and 2.5 minutes between two calibrations.

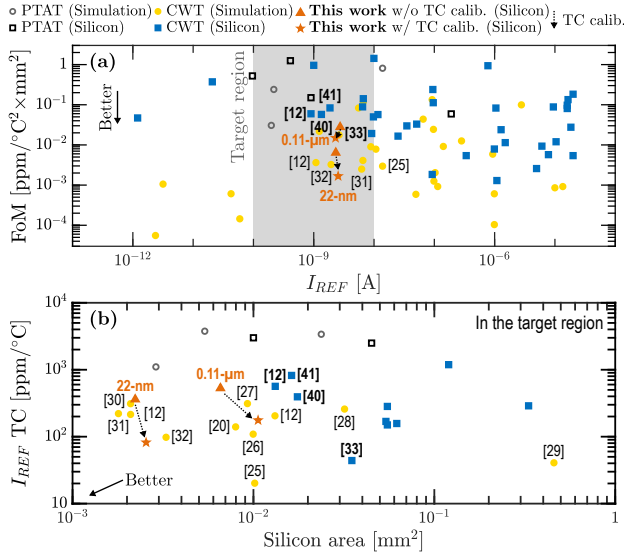


Fig. 26. (a) Figure of merit (19) combining temperature dependence and silicon area as a function of I_{REF} , and (b) tradeoff between TC and area in the nA target region, based on the state of the art of current references.

used as current sources in the 4T voltage reference. This results in an average LS of 1.53 %/V larger than the 0.26-%/V simulated value [Fig. 24(b)]. Besides, Fig. 24(c) illustrates that the TC is consistent across the supply voltage range, except at 1.8 V, for which I_{REF} soars due to the exacerbated GIDL of the zero- V_{GS} transistors, made worse by the increased V_{T0} at low temperature. This interpretation is supported by the measurements in Fig. 24(d), in which the distortion at high supply voltage is aggravated by the temperature reduction, and hints that nMOS devices might be in a slow process corner. Nevertheless, this problem could be solved by placing diode transistors in series with the zero- V_{GS} transistors M_{TVi} to reduce their V_{DS} , without potentially impacting $V_{DD,min}$ as it is currently limited by voltage V_G in the SCM. Then, the supply current temperature dependence [Fig. 25(a)] is similar to the 0.11- μ m design, with a prevalence of the SCM current equal to $4I_{REF} \approx 10$ nA at low temperature, and an increased share due to the 4T voltage reference as temperature rises. Average power consumptions of 15.8 and 28.0 nW are

respectively attained at 25 and 85°C. Moreover, the supply voltage dependence of I_{VDD} is similar to that of I_{REF} [Fig. 25(b)], as the power consumption at 25°C is dominated by the SCM, and a minimum power consumption of 10.4 nW is obtained for $V_{DD,min} = 1$ V. At last, the simulated 99-% startup time is 3.3 ms in typical conditions and 254.4 ms in the worst case [Fig. 25(c)], while the measured value is 11.2 ms on average [Figs. 25(d) and (e)]. On the one hand, this difference is explained by an nMOS process corner slightly slower than the typical one, which causes the shift to the right in Fig. 25(d) and corroborates the observations related to the temperature and supply voltage dependences. On the other hand, it is due to the RC time constant caused by the series resistance R_S and the 25-pF PCB parasitic capacitance, as illustrated in Fig. 25(d). These results again prove that the proposed reference does not require a startup circuit.

V. COMPARISON TO THE STATE OF THE ART

In this section, we compare our work to the state of the art of simulated and fabricated nA-range CWT current references. Table III summarizes the performance of each reference, while Fig. 26 provides a graphical representation of the TC and silicon area across different current levels, using a new figure of merit combining these two characteristics that we propose.

$$\text{FoM} = \frac{\text{TC}}{(T_{\max} - T_{\min})} \times \text{Area} [\text{ppm}/^\circ\text{C}^2 \times \text{mm}^2] \quad (19)$$

This FoM shares some similarities with the one in [15], introduced in the context of voltage references and later applied to current references [41]. However, the proposed FoM must be minimized, and removes the square on the temperature range as we do not believe it is relevant to put so much emphasis on this characteristic. Power consumption normalized to the reference current could also be integrated to this FoM as

$$\text{FoM}_2 = \text{FoM} \times \frac{\text{Power}}{(1 \text{ V} \times I_{REF})} [\text{ppm}/^\circ\text{C}^2 \times \text{mm}^2]. \quad (20)$$

First, the proposed designs uses more scaled technologies than the state of the art, predominantly featuring 0.18 μ m. Nonetheless, we did not normalize the silicon area to the technology node for several reasons:

- a) Analog circuits do not benefit from technology scaling as much as digital ones, as they have to cope with exacerbated analog nonidealities in advanced nodes [42];
- b) An alternative scaling, whose idea is to maintain the same variability σ_{V_T} in any technology, could rely on Pelgrom's mismatch parameter A_{V_T} . Using Pelgrom's law with a constant σ_{V_T} , we observe that silicon area is proportional to $A_{V_T}^2$. Based on values of A_{V_T} of $4.5 \text{ mV} \times \mu\text{m}$ and $3 \text{ mV} \times \mu\text{m}$ in 0.18 and $0.11 \mu\text{m}$ [42], and $2.4 \text{ mV} \times \mu\text{m}$ in 28 nm [24] (close to 22 nm used in this work), the scaling factor with respect to $0.18 \mu\text{m}$ would be $2.3\times$ for $0.11 \mu\text{m}$ and $3.5\times$ for 28 nm , as opposed to $2.7\times$ and $41.3\times$ for a conventional scaling based on the feature size. The latter thus disproportionately penalizes advanced technologies. Although this alternative scaling based on A_{V_T} might seem attractive, it is not conventionally done in the literature and difficult to apply in a fair and rigorous way, as a circuit consists of several transistors of different types and lengths and A_{V_T} is precisely impacted by these two parameters;
- c) The area of some current references [35], [37], [38] is dominated by the resistor used as V -to- I converter, for which the scaling factor to be used is not obvious;
- d) In 22 nm , we used I/O devices whose $0.15\text{-}\mu\text{m}$ L_{min} is comparable to $0.18 \mu\text{m}$ and whose A_{V_T} exceeds that of core devices due to the increased oxide thickness [43].

Besides, Fig. 26(a) highlights that calibrating I_{REF} TC improves the FoM of the proposed $0.11\text{-}\mu\text{m}$ and 22-nm designs by $1.9\times$ and $3.8\times$, respectively, by reducing the TC while slightly increasing the silicon area [Fig. 26(b)]. Therefore, in what follows, we will focus on the designs with I_{REF} TC calibration as they present a better FoM value.

Next, compared to fabricated references in the literature, we obtain a $1.3\times/11.4\times$ FoM reduction for the $0.11\text{-}\mu\text{m}$ and 22-nm designs compared to the closest measured competitor [33], achieving a $44\text{-ppm}/^\circ\text{C}$ TC within a 0.035-mm^2 area. For both designs, the FoM improvement compared to [33] stems from the lower limit of the temperature range, decreased from 0 to -40°C , and the area reduction, as [33] relies on a somewhat-complex β -multiplier variant. Furthermore, [36], [37], [38] feature a TC around $150 \text{ ppm}/^\circ\text{C}$ that is competitive with the proposed designs, but exhibit a larger area above 0.05 mm^2 , due to the use of resistors [37], [38] or massive transistors in deep subthreshold [36] as V -to- I converters. Finally, [12], [40], [41] occupy a silicon area between 0.01 and 0.02 mm^2 which is close to the proposed designs, as [12] relies on an SCM biased by a modified β -multiplier, [40] on a gate-leakage transistor biased by a 6T voltage reference, and [41] on the weighted sum of PTAT and CTAT currents generated by BJT-based β -multipliers. Despite the area efficiency of these techniques, the I_{REF} TC is worse than in the proposed designs as these architectures do not embed any TC calibration circuit, whose addition would inevitably increase the area they occupy.

VI. CONCLUSION

In this work, we demonstrated a nA-range CWT current reference based on an SCM biased by a PTAT voltage with

a CWT offset. This bias voltage is generated by a 4T ULP voltage reference which is the key innovation of this work as (i) it can integrate two types of simple and area-efficient I_{REF} TC calibration circuits, which are key to maintain performance across process corners and to obtain a measured TC comparable with post-layout simulations, (ii) it makes it possible to tune the CWT offset based on transistor sizes, allowing to reliably attain a good performance in terms of LS and variability, in any technology and within a limited area, and (iii) it does not require any startup circuit. Moreover, the proposed current reference architecture can also be used to generate a current with a specific temperature dependence by employing a different sizing or by exploiting the TC calibration circuit. Then, we presented a methodology for sizing the proposed reference based on the ACM model and supported by post-layout simulations. Lastly, we validated the proposed reference based on designs without and with I_{REF} TC calibration, fabricated in $0.11\text{-}\mu\text{m}$ bulk and 22-nm FD-SOI technologies, to prove that the body/back-gate effect can indeed be leveraged in these two technology types. The designs with I_{REF} TC calibration achieve a 2.3-nA current with a $176\text{-ppm}/^\circ\text{C}$ TC and a $2.23\text{-}\%/V$ LS in $0.11 \mu\text{m}$, and a 2.5-nA current with a $82\text{-ppm}/^\circ\text{C}$ TC and a $1.53\text{-}\%/V$ LS in 22 nm . They demonstrate the high level of performance achieved by the proposed reference, as well as its portability to different technologies. In addition, the simplicity of the proposed architecture renders its sizing and implementation quite straightforward. Further work should however focus on reducing the power consumption of the 4T voltage reference at high temperature.

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