A 2.5-GHz Clock Recovery Circuit Based on a Back-Bias-Controlled Oscillator in 28-nm FDSOI

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***Abstract*—A 2.5-GHz clock recovery (CR) unit is proposed within an efficient 2.5-Gb/s ultrawideband (UWB) transceiver fabricated in 28-nm FDSOI for low-power chip-to-chip communications over short distances. The CR circuit is made of two complementary phase-locked loops (PLLs), one for fast frequency locking and the other for high-bandwidth phase tracking. Forward body-biasing (FBB) is used to control a back-bias-controlled oscillator (BBCO) and recover a 2.5-GHz clock frequency. This feature allows to reduce both the supply voltage and the power consumption, while preserving the CR functionality over a wide range of process-voltage-temperature (PVT) variations, including skewed process corners. The CR occupies a silicon area of 0.043 mm^2, locks in less than 1.1 μs, generates an RMS long-term jitter of 6.5 ps, and consumes 1.034 mW while in-lock. This results in an energy value of 0.414 pJ/cycle and a jitter FoM of −224 dB.**

***Index Terms*—Back-bias-control, body-biasing, chip-to-chip communication, clock recovery (CR), FDSOI, low power, oscillator, phase-locked loop (PLL), ultrawideband (UWB).**

I. Introduction

High-performance chip-to-chip communications mostly rely on wireline serial links for the interconnection of different components in modern computers, data centers, or multicore processors. Their success comes from many advantages they have over parallel alternatives, such as lower pin count, simpler routing, lower noise, and lower power. At high data rates, however, the energy efficiency of wireline protocols becomes limited by the RC characteristics of copper interconnects [1]. Wireless schemes thus appear as good alternatives to overcome this challenge, as they can provide better energy efficiency, lower latency, and lower system complexity [2], [3].

In this context, we introduce a highly energy-efficient 2.5-Gb/s ultrawideband (UWB) radio transceiver in 28-nm FDSOI, with a particular focus on the design of its clock recovery (CR) circuit. The proposed transceiver is intended for integration into processor/memory systems-on-chip (SoCs), with chip-to-chip wireless communications over short-distances, as illustrated in Fig. 1. In-chassis server-to-server communication (bypass of the layer-2 switch) or die-to-die communication in 3-D integrated circuits (avoidance of through-silicon vias) are two applicative examples. Section II presents the general architecture. Section III dives into the CR design. Measurement results follow in Section IV.

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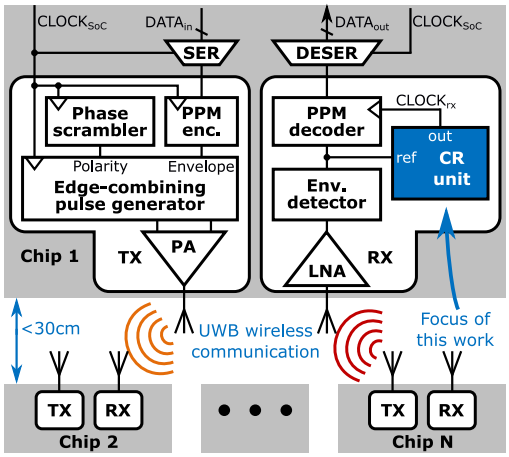

Fig. 1. Proposed UWB transceiver architecture.

II. Proposed UWB Transceiver Architecture

The proposed transceiver contains a transmitter (TX) and a receiver (RX) with CR unit, as depicted in Fig. 1. The chip is designed in 28-nm FDSOI from STMicroelectronics. Low-Vt (LVT) flipped-well devices are used to benefit from forward body-biasing (FBB) [4], [5]. This unique feature is used to decrease the threshold voltage of the transistors, which allows to operate at lower supply voltage and consequently lower power, for the same performance target. Binary pulse position modulation (PPM) is used to transmit the data, as specified in [2]. Fig. 2 shows an example of a UWB PPM-modulated signal together with its envelope, the corresponding bit sequence, and associated clock.

The TX generates the PPM-modulated signal from the 2.5-Gb/s input bit sequence and the 2.5-GHz generic SoC clock, to avoid the need of an external crystal. This is achieved with a pulse generator followed by a power amplifier (PA). A phase scrambler attenuates spectral lines in the frequency domain.

The RX receives the UWB signal and has to recover the corresponding bit sequence. Its architecture is similar to the implementation demonstrated in [3], with the addition of the CR unit which is thus the focus of this letter. As reference, the CR takes the envelope of the incident UWB PPM signal, obtained by the RF front-end (RFFE). The PPM decoder uses the CR recovered clock to properly demodulate and sample the data. As the SoC clock can suffer from high jitter and is used as time reference at the TX side, the CR unit performs high-bandwidth phase tracking at the RX side. For synchronization purposes, it needs a preamble made of all-zeros symbols before receiving the data payload.

III. Proposed Clock Recovery Design

Recovering a clock often relies on phase-locked loops (PLLs), which usually need to achieve fast locking and consume low in-lock

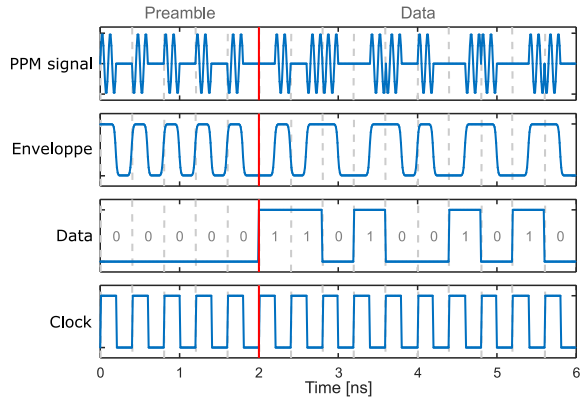

Fig. 2. Example of 2.5-Gb/s UWB PPM modulation with 10 GHz of carrier frequency, divided into a preamble and a data payload.

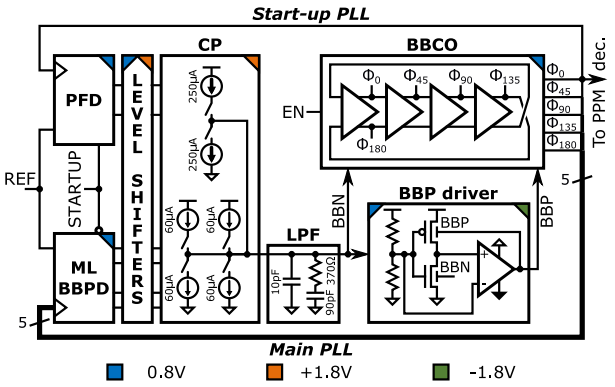

Fig. 3. Proposed dual-loop CR architecture. The PLL selection is externally controlled with the STARTUP signal.

power. These are two conflicting requirements. To avoid this tradeoff and as done in previous works [6], [7], the CR block presented here is made of two complementary feedback loops. A start-up PLL is first needed for fast start-up and frequency acquisition during the preamble. A second PLL (main PLL) is used for high-bandwidth low-jitter phase tracking during the data payload. Fig. 3 presents this dual-loop architecture. The CR is supplied at 0.8 V, except for FBB generation which also needs $+1.8$ V and -1.8 V.

As can be seen in Fig. 3, the two PLLs share an oscillator, a low-pass filter (LPF), and a BBP driver, but differ by the type of phase detector (PD) they use and by the strength of their respective charge-pumps (CPs). As a reminder, the envelope of the UWB PPM signal is used as reference. During the preamble, this reference is a periodic 2.5-GHz signal and a conventional phase-frequency detector (PFD) can be used as detector in the start-up PLL. However, during the UWB data portion, the envelope signal is data-dependent due to the PPM modulation, and looks like 5-Gb/s data (see Fig. 2). The PFD cannot keep the lock in these conditions. For this reason, a half-rate (HR) PD is needed in the main PLL, to accurately track the data phase. A bang–bang PD (BBPD) is chosen for its simplicity, high-speed operation, and better phase alignment compared to a linear counterpart [7]. Due to its highly nonlinear nature [8], this kind of PD exhibits a large gain for small phase errors. This large gain greatly enlarges the main PLL bandwidth to better track the input phase, but can also lead to marginal stability and excessive power consumption. To avoid these two drawbacks, we lowered the CP current by $2\times$ in the main PLL (compared to the start-up PLL). In addition, the BBPD is replaced by a multilevel BBPD (ML-BBPD) version as in [9], which allows to further reduce the CP branch current by $2\times$ while keeping the same CP current range. Altogether, the resulting $4\times$ smaller CP branch current leads to $\sim$70% CP power savings and a $\sim$75% reduction of RMS period jitter. The ML-BBPD needs five clock phases (0°, 45°, 90°, 135°, and 180°).

The start-up and main PLLs are complementary, as the former cannot track the phase within the data payload, while the latter cannot acquire the frequency, even within the preamble. For testing purposes, the PLL selection is externally controlled by the STARTUP signal. In the full application [2], the switch can be automated by detecting the locking of the PFD-based start-up PLL using the most significant output bits of the ML-BBPD, whose absence of activity indicates the main PLL is in range for phase locking. The preamble length is fixed to 1.5 μs, to cover circuit variability and limit latency/power overheads.

Low-power PLLs conventionally use current-starved ring-oscillators (CSROs) [6], [10], but we rely on a back-bias-controlled

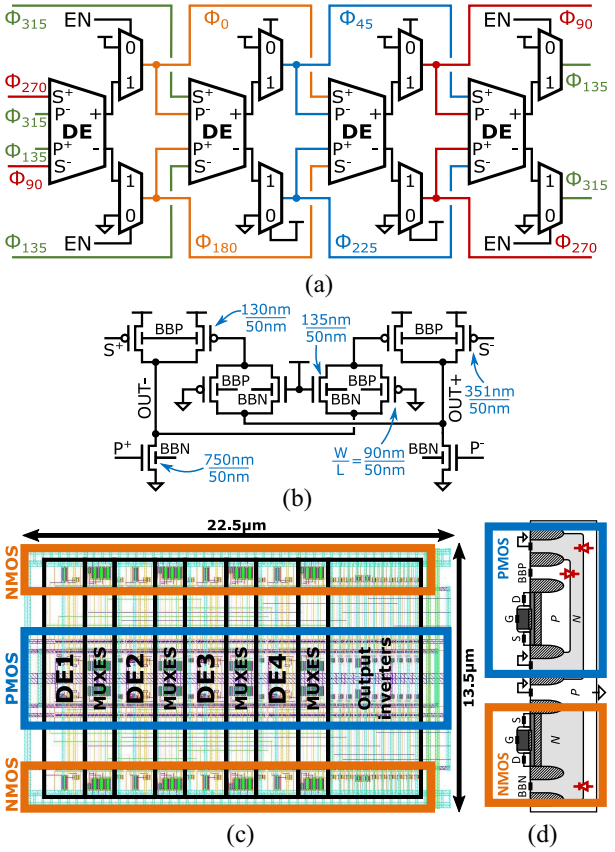

Fig. 4. Details about the BBCO: (a) 4-stages differential architecture, (b) transistor-level schematic of one delay element, (c) abstract layout without sharing of the deep n-well between nMOS and pMOS transistors, and (d) corresponding transistor cross sections.

oscillator (BBCO) instead [11], [12]. A BBCO stacks less transistors and exploits the FBB capability offered by FDSOI technology. This gives the ability to generate 2.5 GHz with a lower supply voltage, and thus lower power. We estimated that 250 mV of supply voltage scaling can be achieved (200 mV thanks to FBB, 50 mV when moving from CSRO to BBCO). The multipath BBCO architecture is represented in Fig. 4(a). Four feed-forward differential stages allow the generation of the five required clock phases. They are similar to the ones used in [11] and proved to be excellent for limited jitter at low power. Their transistor-level schematic is depicted in Fig. 4(b). A nonminimal length of 50-nm is used, leading to $\sim$8% power reduction without any penalty. Multiplexers are used to correctly kick-start the oscillator.

TABLE I
PERFORMANCE COMPARISON OF LOW-ENERGY (<5.5 PJ/CYCLE) CR CIRCUITS FOR SUB-4 GHZ EMBEDDED-CLOCK SYSTEMS

Metric	Units	Shu, 2014 [6]	Ju, 2016 [10]	Lee, 2016 [13]	Gimeno, 2018 [7]	This work
Status	-	Silicon	Silicon	Silicon	Pre-layout sim.	Silicon
Technology	-	90-nm Bulk	65-nm Bulk	65-nm Bulk	28-nm FDSOI	28-nm FDSOI
Supplies	V	1.0/1.3	0.9	1.2	1.0/1.8	0.8/+1.8/-1.8
Area	mm²	0.62	0.25^{+}	0.018	N-A	0.043
Clock frequency	GHz	2.5	0.8	3.25	2.5	2.5
Settling time	μs	N-A	N-A	N-A	< 0.5	< 1.1
In-lock power	mW	13.1	0.268	15.6	1.43	1.034
Energy	pJ/cycle	5.24	0.335	4.8	0.572	0.414
RMS long-term jitter	ps	5	N-A	4.04	N-A	6.5
Jitter FoM†	dB	-215	N-A	-216	N-A	-224
Topology	-	FLL+PLL CSRO in PRPLL FD+BBPD	PLL CSRO PFD	CFD+DPTL ILO+DCDL BBPD	FLL/PLL BBCO FD/ML-BBPD	PLL BBCO PFD/ML-BBPD

$^{+}$Estimated from layout. $^{\dagger}\text{FoM}_{\text{jitter}} = 10\log_{10}\left[(\sigma^2_{\text{lt-jitter}} \cdot \text{P})/(1\text{s}^2 \cdot 1\text{mW})\right]$. **Notations:** FLL: frequency-locked loop – PLL: phase-locked loop - PRPLL: phase-rotating PLL - CFD: coarse frequency detector - DPTL: digital phase tracking loop - CSRO: current-starved ring-oscillator – ILO: injection-locked oscillator – DCDL: digitally-controlled delay-line – BBCO: back-biased-controlled oscillator – FD: frequency detector – BBPD: bang-bang phase detector – PFD: phase frequency detector – ML: multi-level.

The BBCO oscillation frequency is controlled by BBN and BBP (respectively, the nMOS and pMOS body voltages). The CPs regulate BBN through the lead-lag LPF and are externally supplied at +1.8 V. They are made of thick-oxide I/O transistors to withstand this higher voltage. The BBP driver generates the negative BBP voltage from an external supply of −1.8 V. It uses a back-gate driven RC Miller amplifier to continuously match nMOS and pMOS effective currents, as done in [11]. The amplifier also uses I/O transistors, as it is supplied at −1.8 V. The proposed independent FBB generation allows the CR to be tolerant to a wide range of process-voltage-temperature (PVT) conditions, including skewed process corners (fast nMOS/slow pMOS or slow nMOS/fast pMOS). However, the stability of locked-loops based on such differential BBN/BBP voltage generation is threatened by the parasitic coupling capacitance existing between these two nodes [12]. To prevent this, the sharing of the deep n-well between nMOS and pMOS transistors is completely avoided in the BBCO. This costs 50% BBCO area overhead (<0.3% at transceiver level), as illustrated in Fig. 4(c) and (d). The PLL stability can also be degraded by the inherent delay existing between the actuation on BBP and the generation of BBN. The back-gate driven amplifier is properly sized in order to have enough bandwidth compared to the dual-loop PLL so as to avoid this issue.

Complete CR start-up sequences are shown in Fig. 5, simulated under nominal (TT +25°C) and extreme process-temperature (PT) corners. Instead of typical nMOS/typical pMOS (TT), slow nMOS/slow pMOS (SS), and fast nMOS/fast pMOS (FF) process corners are considered here, with temperatures going from −40°C to +85°C. The reported in-lock power and RMS period/long-term jitter numbers are for the nominal case. The start-up is composed of three phases. The CR first acquires the frequency in <1.0 μs with its start-up PLL (STARTUP = 1), thanks to the preamble. It is then switched to the main PLL (STARTUP = 0) and stays phase-locked with the reference signal [see Fig. 5(b)]. Finally, the data starts and the CR stays locked once again [see Fig. 5(c)]. Functionality is preserved over all PT corners (with 0.75 V instead of 0.80 V for FF +85°C case). The CR functionality is also successfully validated under skewed process corners. While the bandwidth of the start-up PLL is around 12 MHz, the main PLL reaches >100 MHz, which improves phase tracking capability and TX jitter tolerance coming from the noisy SoC clock. The jitter levels generated by our CR satisfy the system-level specification of 12 ps RMS period jitter provided in [2].

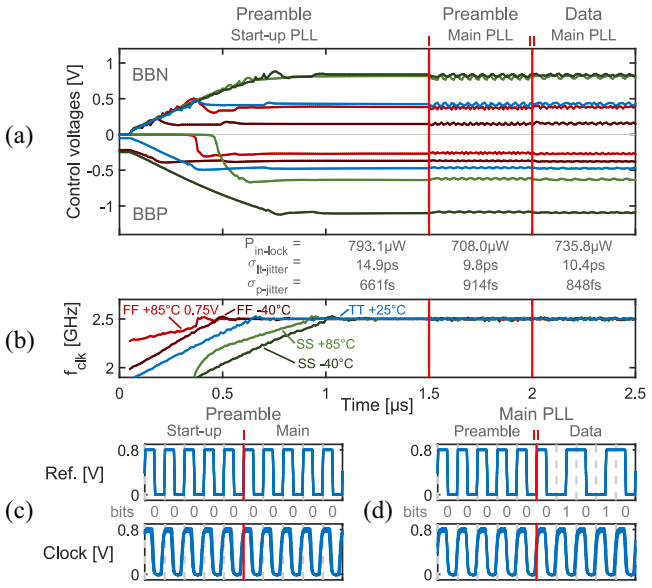

Fig. 5. Post-layout simulations of the proposed CR unit: (a) and (b) complete start-up sequences under nominal and extreme PVT conditions, (c) zoom-in on the transition from start-up to main PLL within the preamble, and (d) zoom-in on the transition from preamble to data payload.

IV. PROTOTYPING AND MEASUREMENTS

The entire UWB transceiver is fabricated in 28-nm FDSOI and occupies an effective silicon area of 0.066 mm^2. Fig. 6 shows a die photograph and highlights its constituting parts. The CR occupies less than 0.043 mm^2 (85% due to the LPF).

The CR functionality and performance are verified in measurements in Fig. 7, with a testing setup similar to [3]. The frequency acquisition is performed in less than 1.1 μs. The main PLL consumption within the data payload is 1.034 mW, which corresponds to 0.414 pJ/cycle. The corresponding experimental RMS jitter is 902 fs (period)/6.5 ps (long-term), which fully meets the specification. The higher power results (compared to simulations, see Fig. 5) can be caused in practice by a slow corner or IR drops, which can both force the CR to lock at higher BBN/lower BBP values and thus consume more. Nonetheless, the results stay competitive and help the full UWB transceiver achieving a measured energy of 2.36 pJ/bit (0.70 pJ/bit for the TX, 1.66 pJ/bit for the full RX).

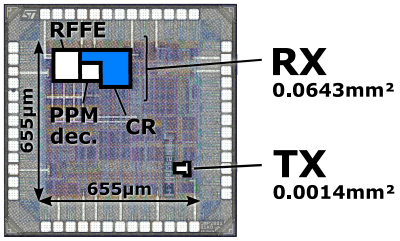

Fig. 6. Die microphotograph.

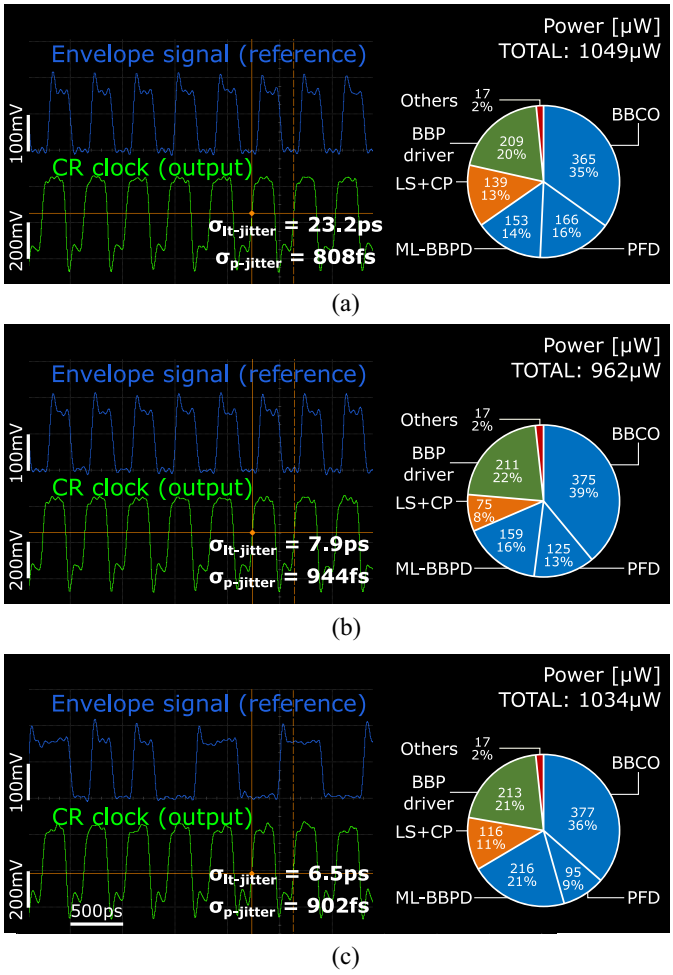

Fig. 7. Measurement results of the proposed CR unit in its three modes. (a) Preamble with start-up PLL. (b) Preamble with main-PLL. (c) Data with main PLL. The power breakdowns of each supply domain are estimated from post-layout simulations.

When compared to other works from the literature in Table I, the proposed CR appears very competitive in terms of energy and area, and achieves the best power-jitter tradeoff. However, we need a negative supply voltage. Solutions exist to efficiently generate it on-chip [11]. The best energy number is achieved by [10], explained by the use of a constant-frequency PPM modulation scheme, which allows to recover the sub-GHz clock with a simple PFD-based low-bandwidth PLL.

V. Conclusion

This letter proposes an efficient CR unit within a 2.5-Gb/s UWB transceiver. The CR uses a PFD-based start-up PLL to acquire the frequency thanks to a preamble. It is then switched to its main PLL based on an ML-BBPD, which is needed within the data-modulated payload signal. Thanks to these two complementary PLLs, the low-power CR achieves fast locking and high-bandwidth phase tracking. The FBB capability of FDSOI technology is exploited to generate the output frequency using a BBCO and operate at a low supply voltage to save power. This FBB feature allows also to maintain the CR functionality over a wide range of PVT conditions, including skewed process corners. A competitive energy value of 0.414 pJ/cycle and an excellent jitter FoM of −224 dB are achieved thanks to these innovations.

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