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Review

A comprehensive review on microwave FinFET modeling for progressing beyond the state of art

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ABSTRACT

FinFET is a multiple-gate silicon transistor structure that nowadays is attracting an extensive attention to progress further into the nanometer era by going beyond the downscaling limit of the conventional planar CMOS technology. Although the interest for this architecture has been mainly devoted to digital applications, the analysis at high frequency is crucial for targeting a successful mixed integration of analog and digital circuits. In view of that, the purpose of this review paper is to provide a clear and exhaustive understanding of the state of art, challenges, and future trends of the FinFET technology from a microwave modeling perspective. Inspired by the traditional modeling techniques for conventional MOSFETs, different strategies have been proposed over the last years to model the FinFET behavior at high frequencies. With the aim to support the development of this technology, a comparative study of the achieved results is carried out to gain both a useful feedback to investigate the microwave FinFET performance as well as a valuable modeling know-how. To accomplish a comprehensive review, all aspects of microwave modeling going from linear (also noise) to non-linear high-frequency models are addressed.

Contents

1. Introduction

The electronics semiconductor industry is perpetually pushing the CMOS downscaling towards its limit to meet application requirements getting incessantly more and more demanding and challenging. Due to the short-channel effects, the conventional CMOS technology is approaching its inherent downscaling limit. With the aim of pushing further this limit into the nanometer era, a plethora of innovative multiple-gate architectures have been proposed in the last three decades [1–7]. In contrast to the conventional planar MOSFET, where the gate oxide stays on one plane, corresponding to the wafer plane, in the multiple-gate field effect transistors (MuGFETs) the thin gate oxide is on more than one plane to achieve gate control from more than one side of the active channel. Depending on the number of sides, MuGFETs are referred to as double- or dual-gate, triple- or tri-gate, quadruple- or surrounding-gate or gate-all-around [7]. These multiple-gate structures reduce

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the short-channel effects through a better electrostatic control of the gate over the conducting channel. Consequently, a lower threshold voltage roll-off and a lower subthreshold slope with associated larger I_{on}/I_{off} ratio can be achieved. Typically, the multiple-gate transistors are controlled by a single gate electrode. Nevertheless, in the case of the multiple independent gate FETs (MIGFETs) the multiple-gate transistors are controlled by separate gate electrodes, which may be independently biased with different voltages. An outstanding example of MuGFET is represented by the FinFET [6–69], originally referred to as folded-channel FET [8]. The name FinFET derives from its shape resembling a fish's dorsal fin in three dimensions [9]. Already from its infancy, this innovative active solid-state device has attracted worldwide attention of the research community, especially because of the advantage of being compatible with the conventional planar CMOS technology. The attention for this emerging transistor has been rapidly increasing over the years. The official launch in Spring 2012 on the market of the latest generation of Intel processors called "Ivy Bridge", which is based on using 22 nm FinFET [70], is a recent evidence of the growing interest for this technology by the microelectronics industry. Although most of the investigations published in the literature have been devoted to technological issues and digital applications, several pioneering studies published by the microwave research community have investigated the FinFETs from a high-frequency standpoint [24–69]. The improvement of the FinFET high-frequency performance is of first importance to bring up viable and competitive solutions for mixed-mode, analog/RF and digital, applications. Most of the efforts have been concentrated on the extraction of microwave models, since accurate and complete high-frequency transistor modeling plays a central role especially for emerging technologies such as FinFET. Indeed, the extracted microwave models can provide useful feedback to technologists for improving device fabrication and further enable a fast and reliable optimization of circuit design. For all those reasons, this manuscript is aimed at synthesizing the results published so far on the high-frequency modeling approaches for FinFET in order to propose a coherent and critical overview that serves as road map for future development. In particular, the paper targets a comprehensive review by covering all aspects of microwave modeling, namely both linear (also noise) and non-linear high-frequency models. It should be pointed-out that the determination of non-linear models is crucial for predicting the transistor behavior under realistic microwave operating conditions [71,72].

The remainder of this paper is structured as follows. Section 2 consists of a brief description of the FinFET architecture. Section 3 is devoted to the basics in microwave measurements, both small- and large-signal conditions. Section 4 is intended to introduce the fundamental principles of microwave modeling and its importance to accelerate the development of the latest advanced transistor technologies. The subsequent three sections are focused on the achievements within the field of FinFET modeling at high-frequencies [39–69], which has been mostly based on the equivalent circuit representation. In particular, Section 5 is aimed at investigating the extraction of the small-signal model for FinFET, while Sections 6 and 7 are, respectively, dedicated to its application for determining noise and large-signal models. Afterwards, Section 8 provides guidelines to improve the FinFET architecture by investigating the impact of its technological peculiarities on the associated microwave performance. Finally, Section 9 presents the main conclusive remarks of this comprehensive study.

2. Basic concept of FinFET architecture

Fig. 1a shows a scanning electron microscope (SEM) image of a FinFET. To gain a basic understanding of the structure and operating principle of this three-dimensional (3D) architecture, Fig. 1b presents a schematic sketch as illustrative example of a Silicon-on-Insulator (SOI) FinFET, where the gate electrode is wrapped around three sides of the thin silicon body of each fin. The conduction width of each triple-gate fin can be calculated as twice the fin height H_{fin} plus the fin width W_{fin}. This triple-gate device can turn into a double-gate structure by making the top insulating layer sufficiently thick to electrically isolate the top gate and, hence, the conduction width is reduced to twice the fin height. FinFET is referred to as quasi-planar structures because, although the channel side-walls are formed perpendicular to the wafer plane in the vertical direction, the drain current flows in both top-Si channel surface and side-walls parallel to the top wafer plane [12,16]. As illustrated in Fig. 1c, multi-finger and multi-fin structures allow achieving wider conducting channel. In particular, the total gate width W of a triple gate FinFET is proportional to the number of fingers N_{finger} and the number of fins per finger N_{fin}:

$$W = N_{finger} N_{fin} (2H_{fin} + W_{fin}) \quad (1)$$

Since H_{fin} is fixed by the process and W_{fin} is limited by the fact that the increase of the ratio W_{fin}/H_{fin} leads to the degradation of the gate control over the channel for a fixed gate length, more fins should be placed in parallel to obtain transistors with wider conducting channel on the same wafer. Hence, the total gate width can be scaled only by integer factor representing the total amount of fins, by changing N_{finger} and/or N_{fin}. However, this discretization of W is not a serious restriction for the transistor scalability, since the sum of W_{fin} and twice H_{fin} is relatively small (e.g., 150 nm [51]).

As illustrated in Fig. 1b, the fin pitch P_{fin} represents the center-to-center distance between two adjacent fins and is given by the sum of S_{fin} and W_{fin}, where S_{fin} represents the minimum edge-to-edge distance between two adjacent fins. Since a high integration level is a mandatory requirement, the appropriate P_{fin} should be fixed to ensure that the total active area of FinFET is equal or even larger than planar MOSFETs for a same footprint, namely consuming the same chip area (see Fig. 1c). Consequently, an aggressive reduction of S_{fin} is required to enhance the integration density. By considering a double-gate FinFET as example, P_{fin} should be smaller than twice H_{fin} to achieve more area efficiency than planar MOSFETs. Furthermore, other two important geometrical dimensions are illustrated in Fig. 1b: T_{ox} denoting the gate-oxide thickness on the side-walls and the source/drain extension length L_{ext}, which represents the distance between the source or drain contact regions and the border of the gate electrode.

It should be noticed that a key advantage of using interdigitated finger lay-out consists of reducing the extrinsic gate resistance R_g, which can significantly affect the RF noise performance and the maximum frequency of oscillation f_{max} of the transistor. By placing more fingers in parallel, R_g is reduced by the increased gate current path width. On the other hand, the use of a longer finger for increasing N_{fin} leads to an increased gate current path length causing a larger R_g. Hence, although the total gate width can be enlarged by increasing the number of both fingers and fins for each finger, only a higher N_{finger} allows reducing R_g. This observation is confirmed by the achieved experimental results showing that R_g decreases with the number of fingers (i.e., R_g is equal to 102.1, 36.4, 23.0, 10.6 Ω for FinFETs with 10, 30, 50, 80 fingers), while its value increases by increasing the number of fins for each finger (i.e., R_g is equal to 19.8, 23.0, 24.3 Ω for FinFETs with 3, 6, 9 fins) [51]. In first approximation, these results can be easily explained by using the conventional scaling rule of the gate resistance for interdigitated transistors, which assumes that the distributed resistive contribution should be proportional to W_0/N_{finger} where W_0 represents the length of each gate finger [73]. In case of the FinFET lay-out, the finger length is made longer when N_{fin} is increased and thereby the distributed resistive contribution is directly proportional to the ra-

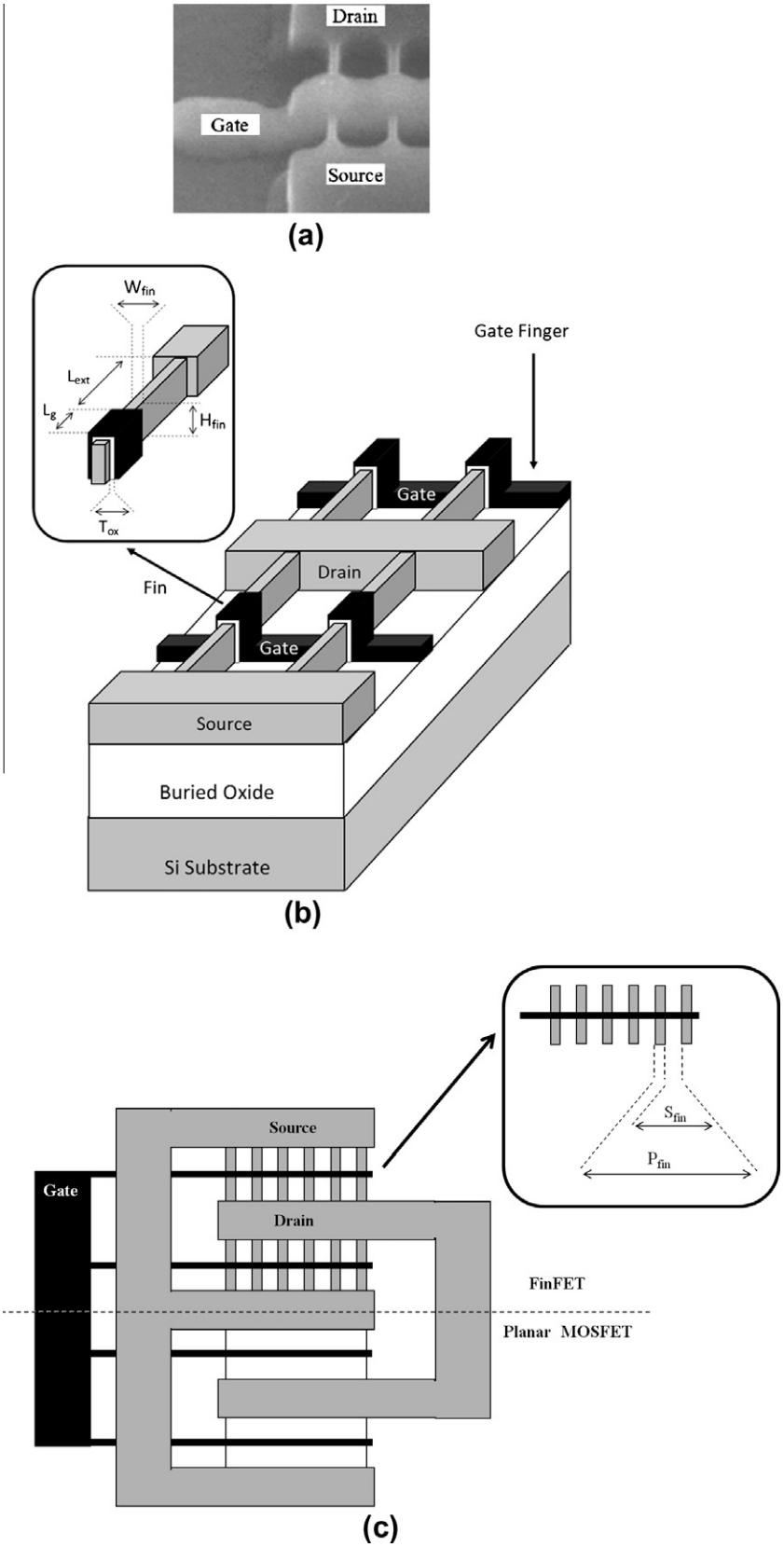


Fig. 1. (a) SEM image showing a gate finger covering two fins in parallel. (b) Illustrative 3D schematic view of a SOI FinFET architecture composed of two gate fingers, each controlling the current flowing along two fins. (c) Illustrative schematic top view of two-gate finger lay-out of both planar MOSFET (lower) and FinFET with six fins for each finger (upper) occupying the same footprint.

tio N_{fin}/N_{finger}. Although this simplified formula expresses straightforwardly the benefit of using multi-finger layout, a more complex analysis of this 3D architecture is required to account for different contributions arising from the top-channel surface, the side-walls, and the fin spacing. Furthermore, the formulation of the gate resistance strongly depends on the specific device lay-out. Wu et al. developed a modeling technique suitable for the gate topology based on filling completely the gaps between the neighboring fins with gate material, as illustrated in Fig. 1a [27,37]. The obtained relationship between the gate resistance and the gate geometrical parameters has been investigated in detail to establish design guidelines, like the optimal fin spacing. Subsequently, Scholten et al. proposed a compact expression to represent the gate resistance for the case in which the gate connection is not present in the gaps between the neighboring fins [74], as depicted in Fig 1b. An important advantage of using this gate topology consists of reducing the extrinsic capacitive contributions [74].

So far, most of the FinFETs are fabricated starting with a SOI substrate, which offers high resistivity characteristics to significantly reduce substrate losses [75–78]. Nevertheless, bulk or body-tied FinFETs are attracting also a remarkable attention since the use of bulk CMOS substrate allows achieving attractive advantages such as lower wafer cost, better heat dissipation, lower defect density, negligible floating body effect, and the possibility to apply a bias voltage to the fin body contact [21,79–83]. Although the microwave modeling studies have been mostly devoted to the SOI FinFETs, Jung et al. focused their analysis on the impact of the substrate resistance for bulk FinFETs [47,48]. In particular, a technique has been developed to extract the substrate resistance for highly scaled multi-finger bulk FinFET by exploiting tied source–drain configuration. It should be pointed out that the bulk resistance plays a crucial role especially in highly scaled bulk FETs, since its impact tends to be strengthened by reducing the device size.

3. Basics in microwave measurements

The microwave characterization of a transistor can be distinguished into two main cases: small- (also noise) and large-signal operations.

The small-signal behavior of a transistor can be represented with the scattering (*S*-) parameters, which can be accurately measured with a vector network analyzer (VNA) and subsequently, simple conversion equations allow obtaining the other equivalent representations, like impedance (*Z*-), admittance (*Y*-), and hybrid (*H*-) parameters [84]. From the extracted *Y*-matrix the equivalent conductances (real part) and capacitances (imaginary part) of the transistor between its different nodes can be explored over a wide frequency band. Having access to the output dynamic characteristics of the transistor, self-heating phenomena can be easily analyzed. FinFETs are prone to self-heating effects due to confinement and increased phonon boundary scattering. In SOI technology the self-heating effects are aggravated by the presence of a thick buried oxide with low thermal conductivity which prevents effective heat removal from the device active region to the Si substrate. Due to shrinking of dimensions in the nanometer scale, devices present a low thermal capacitance and thus a low thermal time constant characterizing the dynamic self-heating which applies the need for high-frequency extraction techniques [85]. The dynamic self-heating effect is characterized in n-channel SOI FinFETs and the dependence of thermal resistance on FinFET geometry is discussed in [86]. It is confirmed experimentally, over a wide frequency band (from 40 kHz to 10 GHz), that fin width and number of parallel fins are the most important parameters for thermal management in FinFETs whereas fin spacing plays less significant role.

As far as the noise characterization is concerned, the noise behavior of a linear noisy two-port network can be completely characterized with four real quantities: the minimum noise factor F_{min}, the noise resistance R_n, magnitude and phase of the optimum source reflection coefficient Γ_{opt}. These noise parameters are used to represent how the noise factor *F*, which is called noise figure NF when expressed in dB, varies with the source reflection coefficient Γ_s:

$$F(\Gamma_s) = F_{min} + \frac{4\frac{R_n}{Z_0}|\Gamma_s - \Gamma_{opt}|^2}{|1+\Gamma_{opt}|^2(1-|\Gamma_s|^2)} \quad (2)$$

where the characteristic impedance Z_0 is typically 50 Ω. The four noise parameters are typically determined with numerical procedures applied to noise figure measurements performed with a noise figure meter (NFM) as a function of at least four different source impedances synthesized by a source tuner [87,88]. Nevertheless, this approach necessitates the use of an expensive automatic tuner system with an associated complex calibration technique. Consequently, several techniques have been developed to obtain the noise parameters from a single measurement of the noise factor with a 50 Ω source impedance, which is indicated as F_{50} [89,90].

To target a complete characterization of microwave transistors, non-linear measurements are required to determine the device behavior under realistic microwave operating conditions, namely when harmonics are generated from the device nonlinearities. This key task can be accomplished with a large-signal network analyzer (LSNA) set-up that allows measuring the magnitude and phase of all harmonics of the incident and scattered traveling voltage waves at the input and output ports [71,72].

To address the needs of electronics and telecommunications applications requiring incessantly higher operating frequency, the accuracy and repeatability of the calibration and measurement become more critical [91,92]. In case of on-wafer characterization, the impact of variations in positioning the probes is significantly enhanced as the frequency increases [91,92]. In light of that, the correct orientation and alignment of the probes should be guaranteed especially at very high-frequencies. In particular, submicron precision probe positioners and dedicated alignment structures should be used [92,93]. From a modeling point of view, various studies have been conducted to analyze the sensitivity of the inherent measurement inaccuracy on the circuit element extraction [94–96].

4. Fundamental principles of microwave modeling

A great consideration is given to the high-frequency modeling of transistors, since the extracted models can be used as helpful feedback to improve the transistor fabrication processes and also as valuable tool to optimize microwave circuit design. The models for transistors can be broken up into three main categories: physical models, equivalent circuit models, and black-box models. Although the best choice among these models depends on the particular application, the equivalent circuit typically offers a valuable compromise. This is because its extraction is based on experimental measurements, while maintaining the link with the physical operating mechanisms. Compared to the black-box model, the equivalent circuit model provides better feedback to the device fabrication processes, since the circuit elements are physically meaningful. Compared to the physical model, the equivalent circuit model provides a solution for faster simulations, which are essential for circuit design. It should be pointed-out that the equivalent circuit modeling of microwave transistors is a complex research activity requiring an interdisciplinary know-how: semiconductor device physics, microwave measurement techniques, circuit network theory, and circuit simulation software packages. Although

several modeling procedures have been proposed and successfully validated in the last decades, the motivation of the research activity in the microwave modeling field originates from the fact that the existing modeling techniques are often insufficient to account for the rapid evolution of transistor technologies. Hence, transistor modeling is continuously object of intensive research, since innovative methods are essentially required to model the latest transistor generation. In such a context, the present work is aimed at providing a bird's eye view of the development and the experimental validation of microwave models for FinFETs with emphasis on equivalent circuit modeling.

In general, the first step of microwave transistor modeling consists of representing the small-signal behavior. Special attention is given to the extraction of the small-signal equivalent circuit, since this model can be used as cornerstone to build both noise and large-signal models. In general, the small-signal equivalent circuit is determined from *S*-parameter measurements. This is an ill-conditioned problem as there are too many unknowns and not enough equations (i.e., eight equations representing the four complex *S*-parameters in terms of the circuit elements at each frequency point). To make this problem simpler, the small-signal equivalent circuit is commonly divided into two main sections: the extrinsic or parasitic part, whose elements are assumed to be bias-independent, and the intrinsic section, whose elements are bias dependent. Based on this assumption, the analytical procedures start by extracting the extrinsic elements and then removing their contributions from the measurements allows determining the intrinsic elements. The two main techniques to determine the extrinsic element contributions are based on *S*-parameter measurements performed on the transistor under "cold" condition (i.e., $V_{ds} = 0$ V, passive device) [97–100] and/or on dedicated test structures (e.g., "open", "short", and "thru") adopting the de-embedding concept [101–105]. The "cold" condition leads to a significant simplification of the equivalent circuit, which allows extracting the extrinsic circuit elements. It should be pointed out that, contrary to the Schottky gate transistors exhibiting high gate current under forward condition, the gate capacitance contributions cannot be disregarded even at relatively high gate voltage in the case of DC insulated gate devices like FinFETs [52]. On the other hand, the de-embedding techniques allow removing straightforwardly the extrinsic effects from the data by using simple matrix manipulations, even without the explicit determination of the associated circuit network. This is the reason why these de-embedding procedures are widely used in the case of silicon transistor technologies like FinFETs, where the determination of the extrinsic circuit elements can be quite challenging, due to the substrate losses [52]. In the case of on-wafer silicon transistors, the de-embedding concept enables removing the parasitic contributions arising mostly from the contact pads, the metal interconnections, and the substrate.

After removing the extrinsic effects from the data, the intrinsic section of the equivalent circuit is identified. Different topologies have been proposed to model the intrinsic non-quasi-static (NQS) effects accounting for the inertia of the intrinsic transistor in responding to rapid signal changes [106–110]. The choice of the most appropriate intrinsic section reflects the specific transistor technology, besides the studied frequency range.

The following three sections will focus on the extraction of the small-signal equivalent circuit for FinFET and its utility for determining both noise and large-signal models. Several papers have been published in the literature to propose accurate modeling procedures for extracting equivalent circuits of microwave transistors in MOSFET technology [111–128]. Inspired by these previous studies, different strategies have been developed to stretch these modeling techniques to represent FinFET devices, since this innovative transistor structure is roughly based on the same operating principle as the conventional MOSFET. The differences in the proposed strategies reflect the physical and technological differences observed in the behavior of the specific FinFET under test, beyond the investigated operating conditions. As will be shown, also the approach based on artificial neural networks (ANNs) has been successfully exploited for extracting the equivalent circuit model of FinFETs.

Nevertheless, although the equivalent circuits should maintain the connection with the device physics, a much deeper insight into the physical structure of the FinFET is mandatory for physical models. This is because their extraction is strongly based on a detailed study of the physical operating mechanisms of the complex 3D nature of the FinFET structure, as addressed in [129–132].

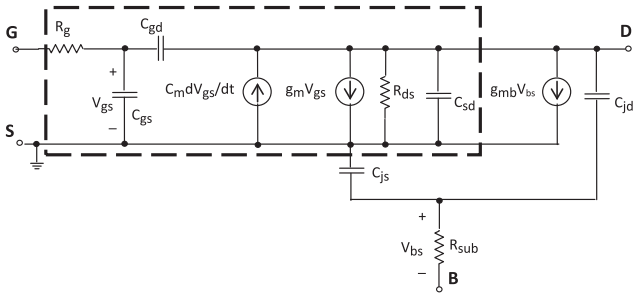
The accuracy of a microwave transistor model can be affected by process variations, which can lead to statistical variations of the device parameters, especially in case of less mature technologies [133,134]. To account for that, statistical variations should be included in the microwave model before its release to the designers [134]. It should be highlighted that the FinFET architecture is particularly prone to process variations, since the aggressive shrinking and the complex nature of its 3D structure lead to a limited process controllability [135–138]. As a consequence, several studies have been dedicated to investigate the sensitivity of the FinFET technology to process variations and their effect on both digital and analog performance and thermal properties [135–140]. Lakshmi et al. investigated the impact of the process variations on the unity current-gain cut-off frequency f_T [139]. In particular, the impact of changing nine different process parameters on f_T has been analyzed by exploiting extensive TCAD simulations. It resulted that f_T is mostly sensitive to the following five parameters: gate length, underlap, gate-oxide thickness, channel doping, and source/drain doping. Recently, by using an RF equivalent circuit representation, Baek et al. observed that the transconductance predominantly affects both f_T and f_{max} [138].

5. Small-signal modeling

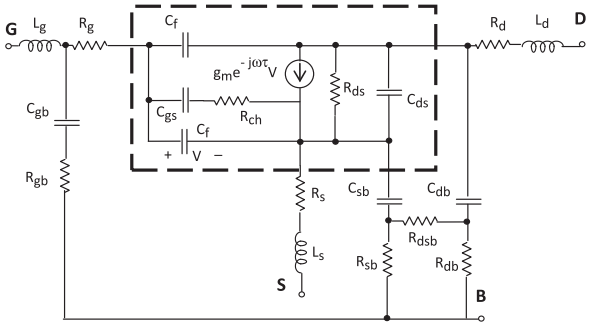
Fig. 2 shows different topologies of small-signal equivalent circuit proposed in literature to model devices fabricated with FinFET technology. Although the distinction between extrinsic and intrinsic sections can be often questionable, due to the bias dependence of certain elements, we used dashed boxes to identify the intrinsic parts of the reported circuits.

Tak et al. presented the four-terminal circuit in Fig. 2a to reproduce 3D device simulation of bulk FinFETs up to 20 GHz [39]. This small-signal equivalent circuit topology includes the transcapacitance C_m taking care of the different effects of the gate and the drain on each other in terms of charging currents (i.e., $C_m = C_{dg} - C_{gd}$), R_g consisting of the distributed channel resistance and the gate electrode resistance [119], and the capacitance C_{sd} accounting for the short channel effect. It should be pointed out that the modeling results presented in the following part of this section and the subsequent two sections are based on SOI FinFETs. This is because so far the SOI substrate is typically used to fabricate FinFETs and, furthermore, SOI is attractive especially for high-frequency applications. Nevertheless, the achieved modeling background can be extremely useful to model also body-tied FinFETs by accounting for the contributions arising from the bulk substrate.

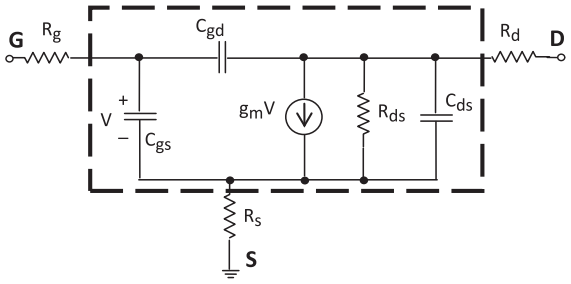
Fig. 2b illustrates another example of four-terminal circuit, which has been proposed by Wang et al. to capture the SOI FinFETs behavior up to 10 GHz [40,41]. After extracting the extrinsic resistances and inductances from *S*-parameter measurements under zero bias (i.e., $V_{ds} = 0$ V and $V_{gs} = 0$ V), the intrinsic elements are calculated and, finally, the substrate network elements are determined by fitting with measurements at high frequencies. However, contrary to these two studies, the body terminal is generally omit-



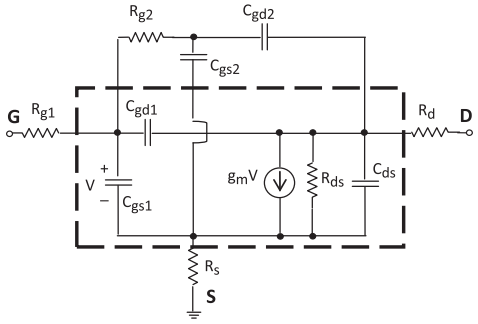
(a) Four-terminal small-signal equivalent circuit including substrate network for bulk FinFET [39]



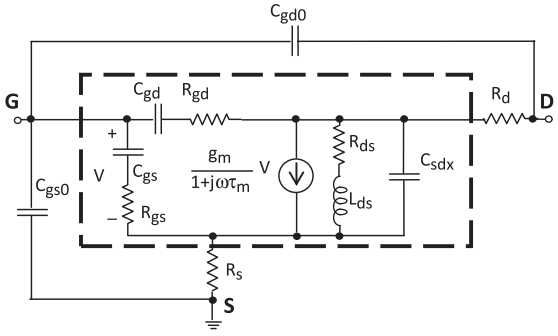
(b) Four-terminal small-signal equivalent circuit including substrate network for SOI FinFET [40, 41]



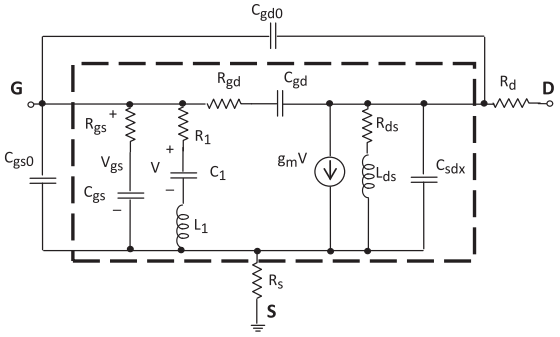
(c) Conventional basic equivalent circuit for modeling single-gate device [42]



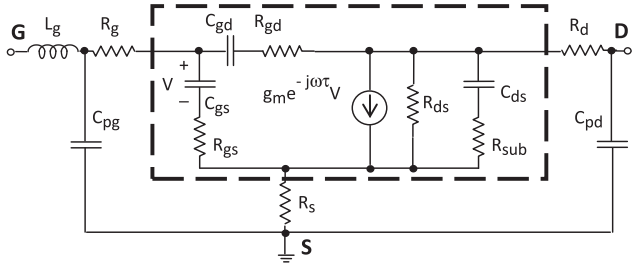
(d) Expansion of the circuit in Fig. 3(c) with a parasitic RC network (i.e., R_{g2}, C_{gs2}, C_{gd2}) to improve high-frequency fitting for FinFET [42]



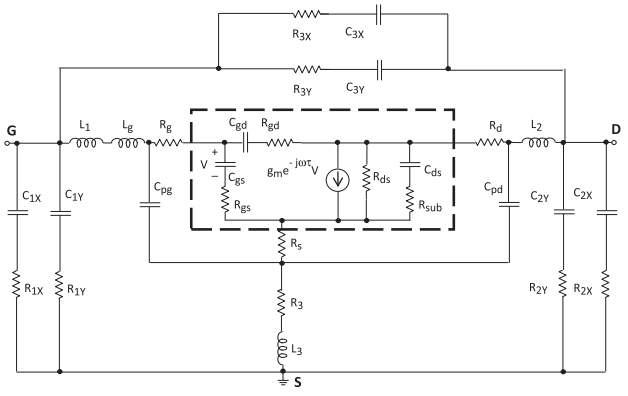
(e) Small-signal equivalent circuit including L_{sd} to account for the time delay of R_{ds} and C_{sdx} to account for the drain induced barrier lowering effect [45]



(f) Modified version of the circuit in Fig. 3(e) by placing R_s and R_d outside the overlap capacitances and adding the second order term in the voltage controlled current source [46]



(g) Small-signal equivalent circuit including the intrinsic resistance R_{sub} to account for the lossy substrate [51]



(h) Extension of the circuit in Fig. 2(g) with the extrinsic network modeling "open" and "short" test structures [54]

Fig. 2. Small-signal equivalent circuit topologies proposed in literature for FinFET technology in silicon bulk (a) and SOI (b–h) technology. The intrinsic sections are highlighted within dashed boxes.

ted as the FinFET is treated as a three-terminal device in microwave analog circuit design. This means that the corresponding DC and high-frequency measurements are performed with both the body/substrate and the source connected to the ground.

Lederer et al. showed that the conventional basic equivalent circuit in Fig. 2c can be used to model single-gate devices up to 110 GHz but such simple topology fails to accurately represent the FinFET behavior [42]. The parasitic capacitances and inductances related to the interconnects (metallic pads and coplanar waveguide feed lines) are omitted in this circuit since their contributions have been removed from the measured raw data with the de-embedding procedure. As reported in Fig. 2d, a parasitic RC network (i.e., R_{g2}, C_{gs2}, C_{gd2}) has been added to improve the agreement between measured and simulated behavior up to 110 GHz. The physical origin of this RC network accounting for the observed higher resistive and capacitive gate contributions has been ascribed to lines of residual polysilicon along the silicon fins. In particular, the polysilicon residuals origin from an incomplete polysilicon etch in the buried oxide (BOX) recess when the polysilicon gate is patterned by resist trimming [42]. Subsequently, by solving these technological problems, f_T and f_{max} higher than 100 GHz have been achieved for 60-nm gate length FinFETs [43].

Kang et al. insist on the importance of modeling accurately the NQS effects to reproduce the FinFET simulated behavior up to 700 GHz [45]. In particular, the model in Fig 2e is expanded with the inductance L_{sd} in series to R_{ds}, to account for its time delay, and the capacitance C_{sdx} in parallel to the branch $R_{ds}L_{ds}$, to account for the drain induced barrier lowering (DIBL) effect of short-channel devices. It should be noticed that the extrinsic gate resistance is omitted since 3D simulation results were used. Subsequently, Kang proposed to improve this model by placing R_s and R_d outside the overlap capacitance and adding the second order term in the voltage controlled current source. These modifications have been included in the model as illustrated in Fig 2f [46].

Crupi et al. proposed an equivalent circuit topology including the resistance R_{sub} to take into account for the substrate losses (see Fig 2g) [51]. By adding this resistance, simulation improvements are obtained for both real and imaginary parts of Y_{22} of the intrinsic section. Nevertheless, the main reason of including R_{sub} is due to the fact that the feedback gate–drain resistance R_{gd} is not enough to mimic the observed increase of the real part of the intrinsic Y_{22} at higher frequencies:

$$\mathrm{Re}(Y_{22}) = \frac{1}{R_{ds}} + \frac{\omega^2 R_{gd} C_{gd}^2}{1 + (\omega R_{gd} C_{gd})^2} + \frac{\omega^2 R_{sub} C_{ds}^2}{1 + (\omega R_{sub} C_{ds})^2} \quad (3)$$

where R_{ds} is the intrinsic output resistance, while C_{gd} and C_{ds} represent, respectively, the intrinsic feedback and output capacitances.

Regarding the extrinsic section of the circuit in Fig. 2g, the drain and source inductances L_d and L_s are disregarded since their effects have been completely removed with the de-embedding procedure based on "open" and "short" structures. On the other hand, six extrinsic elements L_g, C_{pg}, C_{pd}, R_g, R_s, R_d, are included to account for the residual parasitic contributions after the de-embedding procedure.

As can be noticed from Fig 2g, four time constants have been used in the model to account for the intrinsic NQS effects: τ_{gs} representing the time constant of the input RC branch (i.e., $R_{gs}C_{gs}$), τ_{gd} representing the time constant of the feedback RC branch (i.e., $R_{gd}C_{gd}$), τ_{sub} representing the time constant of the output RC branch (i.e., $R_{sub}C_{ds}$), and τ (known also as τ_m) representing the time constant of the transconductance (i.e., $g_m^{-1} C_m$). It has been observed that the QS approximation can be adopted at a few GHz for the tested FinFETs in [51] but its validity is gracefully degraded by increasing the operating frequency. In particular, the time constant of the output RC network resulted to be the dominant effect in determining the onset frequency of the NQS effects (e.g., $(2\pi\tau\mathrm{sub})^{-1}$ is 43 GHz for a FinFET with a gate length of 60 nm and a gate width of 45.6 μm) [53].

To obtain a representation of the whole transistor without any shift of the measurement reference plane, Crupi et al. proposed a lumped equivalent circuit network for modeling both "open" and "short" test structures and included its contribution in the FinFET model (see Fig. 2h) [54]. In particular, the three input, output, and feedback RC branches (i.e., $R_{ix} - C_{ix}$ and $R_{iy} - C_{iy}$, "i" being 1, 2 or 3) are determined to reproduce the measured S-parameters of the "open" structure over the full analyzed frequency range including the low-frequency kinks associated to the lossy substrate (see Fig. 3). By using a standard lossless circuit based on a purely capacitive network modeling the capacitive coupling between the pads, the simulated reflection coefficients S_{11} and S_{22} move from the ideal open condition along the outer edge of the Smith

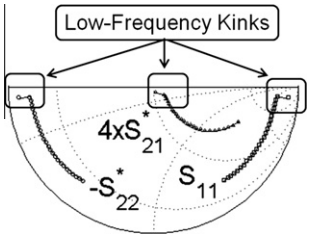


Fig. 3. Measured (symbols) and simulated (lines) S-parameters from 0.3 GHz to 50 GHz for "open" structure: S_{11} (squares), $4 \times S_{21}^*$ (triangles), and $-S_{22}^*$ (circles) [54]. The low-frequency kinks are highlighted within boxes.

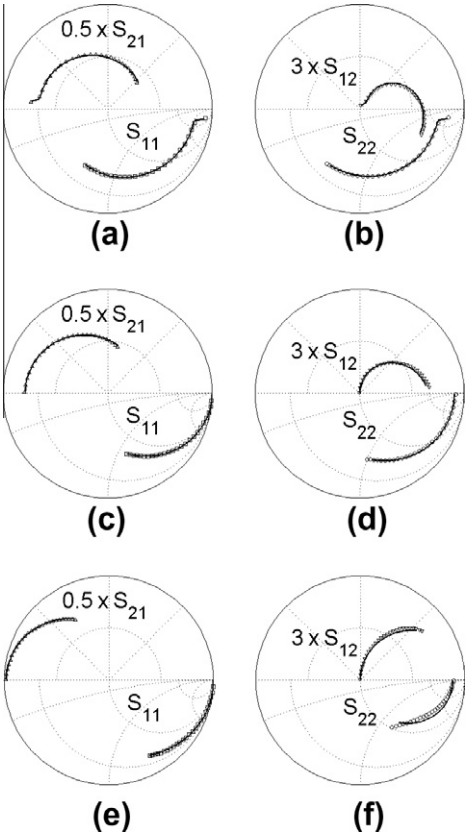


Fig. 4. Measured (symbols) and simulated (lines) S-parameters from 0.3 GHz to 50 GHz for a SOI FinFET with $W = 45.6$ μm and $L_g = 60$ nm at $V_{ds} = 1.2$ V and $V_{gs} = 0.8$ V for (a and b) whole, (c and d) actual, (e and f) and intrinsic device: S_{11} (squares), $0.5 \times S_{21}$ (up triangles), $3 \times S_{21}$ (down triangles), and S_{22} (circles).

chart as the frequency increases. In contrast with that, Fig. 3 clearly shows that the resistive effects have a significant impact on the measured *S*-parameters over the full investigated frequency range, as can be detected by their marked deviations from the ideal capacitive behavior. Hence, resistive contributions have to be included to mimic the measured *S*-parameters of the "open" structure. Roughly speaking, the proposed RC network allows reproducing the observed kinks by passing from a dominant R_xC_x series network to a dominant R_xC_y parallel network at around 2 GHz, while R_y is added only to enhance the fitting at high frequencies. The presence of this extrinsic RC network in the FinFET model allows reproducing the low-frequency kinks observed in the *S*-parameters of the transistor before applying the "open/short" de-embedding. As reported in Fig. 4, the comprehensive small-signal model in Fig. 2h can reproduce accurately the measured *S*-parameters for the whole device at the calibration plane corresponding to the probe tips, for the actual device after applying "open/short" de-embedding procedure, and for the intrinsic device after removing the residual extrinsic contributions associated to L_g, C_{pg}, C_{pd}, R_g, R_s, R_d. Small but noticeable difference between the measured and simulated S_{22} of the intrinsic device can be observed in Fig. 4f. This deviation could be attributed to the intrinsic element values, which are inevitably affected by their sensitivity to the uncertainties in both *S*-parameter measurements and extrinsic element extraction, or to a limitation of the intrinsic circuit topology. To make clearer the impact of the resistive effects (i.e., R_{ix} and R_{iy}, "*i*" being 1, 2 or 3) on the *S*-parameters at low frequencies, Fig. 5 highlights the kink effects by reporting the model simulations for the whole device in the frequency range going from 10 MHz to 4 GHz. The appearance of the kinks in *S*-parameters of microwave transistors has been extensively questioned and debated over years, since it physical origin, shape and frequency range strongly depend on the specific technology [54,141–146]. In the present case, the disappearance of the kink effects after using the "open" structure for the de-embedding allows ruling out that their origin is due to the intrinsic section of the transistor [142–146]. The physical origin should be found in the extrinsic contributions present in the "open" structure. As a consequence, the transistor kinks should be ascribed to the counterbalance between resistive losses in the silicon substrate and the capacitive coupling between pads. To account for the losses in the transistor substrate, various topologies of RC network have been proposed in the literature [117,118,147–149]. Fig. 6 shows the comparison between measured and simulated short-circuit current gain H_{21} for the whole, actual, and intrinsic device. This microwave figure of merit is increased by removing the extrinsic contributions. As a consequence, the shift of the reference plane closer to the intrinsic device implies also a higher f_T. By using the method based on −20 dB/dec extrapolation, f_T is equal to 109 GHz and 69 GHz, respectively, for the intrinsic and actual device. This result of the tested device clearly indicates that a reduction of the extrinsic contributions is essential

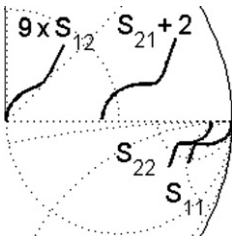


Fig. 5. Simulated *S*-parameters from 10 MHz to 4 GHz for a SOI FinFET with $W = 45.6\ \mu m$ and $L_g = 60$ nm at $V_{ds} = 1.2$ V and $V_{gs} = 0.8$ V. The simulations are achieved by exploiting the extracted model for the whole device.

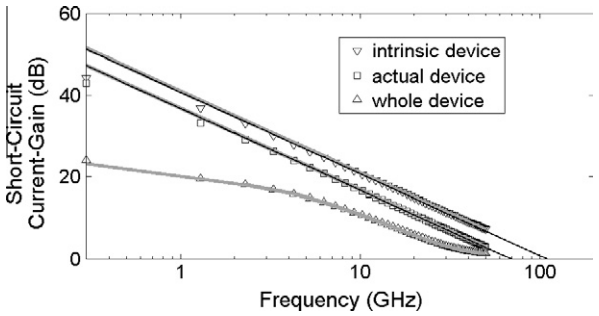


Fig. 6. Measured (symbols) and simulated (gray lines) H_{21} from 0.3 GHz to 50 GHz for an SOI FinFET with $W = 45.6\ \mu m$ and $L_g = 60$ nm at $V_{ds} = 1.2$ V and $V_{gs} = 0.8$ V: whole device (up triangles), actual device (squares), and intrinsic device (down triangles). Using the method based on −20 dB/dec extrapolation (black lines), f_T is equal to 109 GHz and 69 GHz, respectively, for the intrinsic and actual device.

to enable the development of the FinFET architecture for high-frequency applications.

Tinoco et al. focused on developing an improved extraction procedure to determine the extrinsic resistances for FinFET [50]. Basically, the classical extraction methodology presented by Bracale et al. for MOSFETs [115] is adapted to advanced deep-submicron devices by accounting for carrier mobility degradation with the vertical electric field and the transistor asymmetry.

The black-box modeling approach has also been adopted to model the FinFET microwave performance. In particular, Deschrijver et al. exploited a multi-parameter rational fitting technique, called multivariate orthonormal vector fitting, to reproduce the *S*-parameter measurements for FinFET after having applied the "open/short" de-embedding procedure [55]. This approach originally developed for modeling linear passive devices has been successfully applied to transistors.

Marinković et al. developed a procedure based on ANNs to successfully model both the actual and the whole devices [56,57], namely after and before applying the "open/short" de-embedding. The *S*-parameters of the whole device exhibit kink effects at low frequencies, demonstrating a stronger impact on the real parts rather than the imaginary parts. Consequently, the model complexity is increased in the case of modeling the *S*-parameters of the whole device. As illustrated in Fig. 7, the real parts are modeled by a two-step hierarchical neural model consisting of two ANNs, which are trained to model the real parts in the lower frequency range and over the full frequency range. Subsequently, the ANN approach has been adopted to directly model also the *Y*-parameters, which offer the most convenient representation as cornerstone for building a large-signal model [58].

The following two sections will show how the achieved results in the field of the small-signal modeling have been used over the years as cornerstone for building noise and large-signal models for FinFETs built on SOI substrate.

6. RF noise modeling

Raskin et al. published the first paper focused on the investigation on high-frequency noise performance of FinFETs [60]. Based on the modeling strategy developed by Dambrine et al. [150], the small-signal equivalent circuit has been expanded with two uncorrelated noise sources, namely an input-voltage noise source e_{in} and an output-current noise source i_{out} with the equivalent temperatures T_{in} and T_{out} (see Fig. 8a). The extracted model has been used to successfully reproduce the measured noise parameters up to 20 GHz. Although the extrinsic fringing capacitive contributions arising from the 3D nature of this architecture impact negatively the noise performance, a minimum noise figure of 1.35 dB with

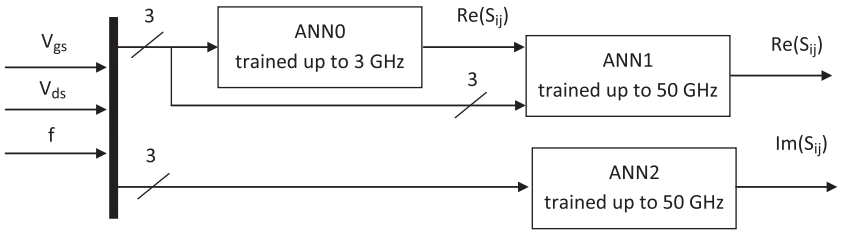
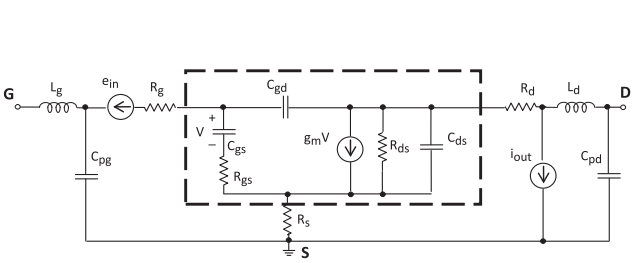
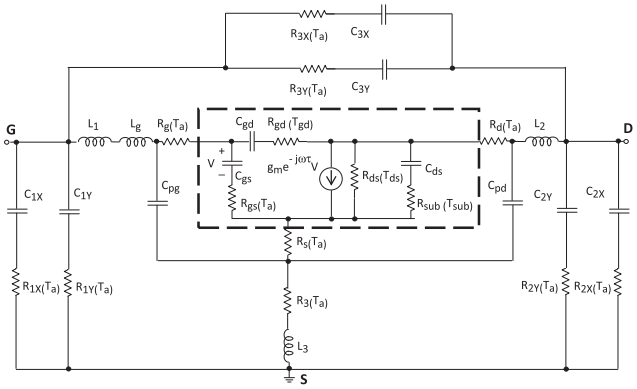


Fig. 7. ANN model for SOI FinFET technology. The input parameters are the two bias voltages and frequency, while the outputs are the measured real and imaginary parts of the *S*-parameters. The real part of the *S*-parameters for the whole device is modeled by a two-step hierarchical neural model consisting of two ANNs: ANN0 and ANN1, which are trained to model the behavior in the lower frequency range and over the full frequency range [56].



(a) Noise model based on expanding the small-signal equivalent circuit by adding two uncorrelated noise sources e_{in} and i_{out} [60]



(b) Noise model based on expanding the small-signal equivalent circuit by assigning an equivalent temperature to each resistor [61]

Fig. 8. Noise equivalent circuit topologies proposed in literature for SOI FinFET technology. The intrinsic sections are highlighted within dashed boxes.

an associated available gain of 13.5 dB are achieved at 10 GHz with V_{dd} = 0.5 V. Hence, the high-frequency noise performance of the FinFET technology still needs to be improved but these preliminary results are quite promising. It should be pointed out that, to access the noise performance of the actual transistor, the "open/short" de-embedding procedure was applied.

As alternative modeling approach, Crupi et al. proposed to assign an equivalent temperature to each resistor of the small-signal equivalent circuit (see Fig. 8b) [61]. The temperatures associated to the intrinsic resistances R_{gd}, R_{ds}, and R_{sub} are obtained by minimizing the difference between measured and simulated F_{50} up to 26.5 GHz, while the other temperatures are selected to be equal to the room temperature. The temperature values are determined based on the fact that the main contribution of increasing the temperature of the QS resistance R_{ds} consists in increasing the simulated F_{50} at low frequencies, while the main contribution in increasing the temperature of the NQS resistances R_{gd} and R_{sub} consists of increasing the simulated F_{50} at high frequencies. The model simulation results have been analyzed with and without the contributions of the lumped element network for "open" and "short" dummy structures to exploit their contributions in the noise performance. The extrinsic network contributions significantly affect the simulated noise characteristics as confirmed by the fact that the absence of this extrinsic network allows lowering NF_{min} and removing the low-frequency kink in Γ_{opt} (see Fig. 9).

A combination of the methods developed in the two previous studies has been proposed by Wiatr et al. to determine the noise performance of the actual device [62]. In this case, the noise characteristics of the actual device have been determined from the measured noise parameters of the whole device by peeling out with a commercial circuit simulator the contributions of each lumped element of the equivalent circuit network associated to the "open" and "short" structures. In particular, the measurements of the four noise parameters have been carried out up to 8 GHz by using the latest noise measurement facilities based on the PNA-X with the noise measurement option [151].

7. Large-signal modeling

To represent the FinFET behavior under realistic microwave operating conditions, research efforts have been devoted to extract large-signal models suitable for this advanced transistor structure. The first study on the large-signal modeling of FinFET was reported by Crupi et al. [63]. As illustrated in Fig. 10a, the intrinsic core of the equivalent circuit consists of four non-linear sources: two charge sources and two current sources (i.e., Q_{gs}, Q_{ds}, I_{gs}, I_{ds}) representing, respectively, the displacement and the conduction intrinsic current contributions as a function of the intrinsic gate and drain voltages. Nevertheless, the gate current source can be disregarded because of its negligible role in case of DC insulated gate devices. This model using the QS approximation has been validated with a fundamental frequency f_0 in the lower GHz range. Based on the earlier study of Vandamme et al. [103], a de-embedding procedure has been applied to remove part of the extrinsic contributions from the large-signal measurements used for the model validation. Subsequently, this model has been extended with the extrinsic element network to shift the reference plane to the probe tips and with the NQS contributions to extend the model validity towards higher frequencies (see Fig. 10b). The inclusion of the extrinsic network modeling the "open" and "short" structures allows mimicking the large-signal measurements also without the need to apply the "open/short" de-embedding [54]. As illustrative example, Fig. 11 shows that this expanded model can account for the input current contributions arising from the presence of the input and feedback extrinsic RC networks (i.e., $R_{ix} - C_{ix}$ and $R_{iy} - C_{iy}$, "*i*" being

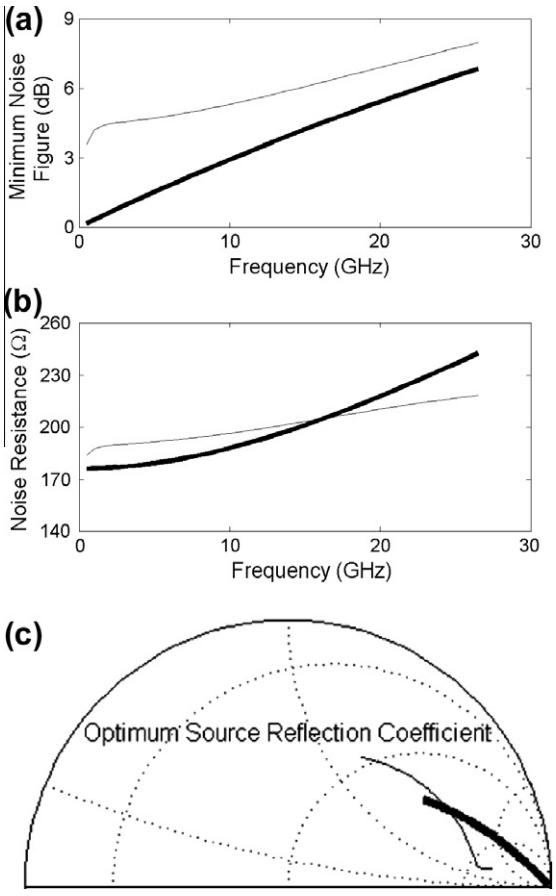


Fig. 9. Model simulations of the noise parameters (a) NF_{min}, (b) R_n, (c) Γ_{opt} from 0.5 GHz to 26.5 GHz for a SOI FinFET with $W = 45.6$ μm and $L_g = 60$ nm at $V_{ds} = 1$ V and $V_{gs} = 0.8$ V: with (thin lines) and without (thick lines) the contributions of the external part of the equivalent circuit determined from *S*-parameter measurements of "open" and "short" structures [61].

1 and 3). In particular, the comparison of the input loci before and after the de-embedding procedure shows that the gate current of the whole device exhibits much higher values and is almost in phase rather than in quadrature with the gate voltage. As far as the NQS effects are concerned, their modeling implies an increased model complexity leading to considerably improved model simulations at higher frequencies but at the same also to a sizeable slower simulation convergence and speed [65]. The latter drawback becomes more critical especially under two-tone excitation [66]. Hence, although the NQS effects become more pronounced as the frequency increases, the QS model in Fig. 10a has a use in the lower RF frequency range because of its simpler formulation implying a faster simulation.

As an alternative approach for implementing the NQS effect in the non-linear model, Homayouni et al. proposed to extend the number of the charge and current non-linear sources [67,68]. Although theoretically a combination of zero order sources and infinite number of higher order sources should be used, the model has been truncated to two charge sources and two current sources at the output port and to two charge sources and one current source at the input port, as illustrated in Fig. 10c. Contrary to the model in Fig. 10a, this model includes the higher order sources obtained by accounting for the NQS contributions when integrating the intrinsic small-signal equivalent circuit elements with respect to the intrinsic gate and drain voltages.

Alam et al. adopted an ANN based technique to extract a non-linear equivalent circuit for FinFET (see Fig. 10d) [69], which is based on the small-signal equivalent circuit topology proposed by Kang et al. (see Fig. 2e). In particular, a two-layered neural network has been used to model the intrinsic circuit elements and the drain current at different bias conditions by using 3D ATLAS simulations to generate the data for ANN training.

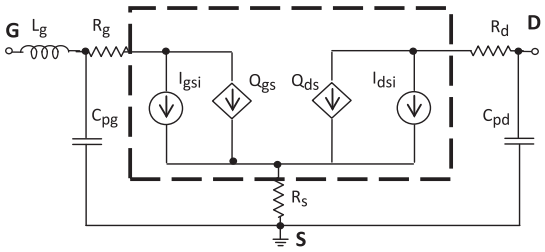
8. Impact of technological FinFET peculiarities on microwave performance

Traditionally, the workhorse technologies for transistors aimed at high-frequency applications are based on III–V semiconductors, such as GaAs and InP. Compared to the conventional Si technology, these materials offer the benefits of enabling superior electron transport channels and semi-insulating substrates. Nevertheless, the semiconductor industry is incessantly struggling to overcome the high-frequency performance limitations of the Si technology, which is significantly less expensive. Nowadays, the microwave community is paying a growing attention to the remarkable development of the Si technology, which is witnessed by the reported high cut-off frequency with SOI substrate (i.e., close to 500 GHz for strained SOI n-MOSFETs with a gate length of 30 nm [152]). However, as the gate length is scaled down into the nanometer regime to achieve higher operating frequencies, the short-channel effects turn out to be much more pronounced. Although the FinFET structure allows reducing the short-channel effects, its performance still needs to be improved for microwave applications. In particular, the main limitations affecting the high-frequency FinFET behavior are the lower electron mobility at the side-walls, the higher extrinsic source and drain resistances, and the higher extrinsic fringing capacitances [17,29,33,153–155].

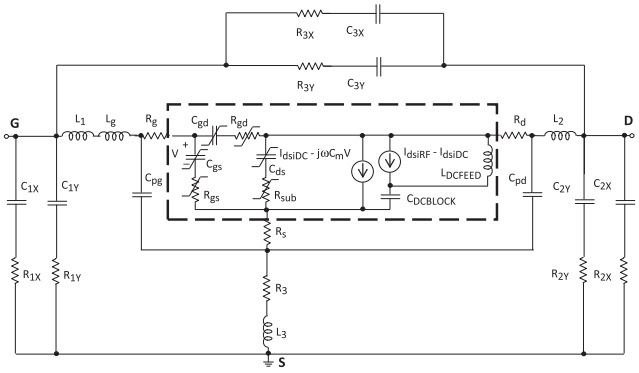
Fig. 12 presents the extracted RF cut-off frequencies of planar and FinFET devices with similar dimensions as a function of channel length. The so-called intrinsic (f_{Ti}) and extrinsic (f_{Te}) cut-off frequencies stand, respectively, for the current gain cut-off frequency related to only the intrinsic lumped parameter elements and the complete small-signal equivalent circuit including the parasitic capacitances as well as the access resistances. It is quite interesting to see that both devices present similar intrinsic cut-off frequencies (around 400 GHz for a channel length of 60 nm) but the extrinsic cut-off frequency, f_{Te}, of FinFET (90 GHz) is nearly twice lower than that of the planar MOSFET (180 GHz).

Based on a wideband analysis, the lumped small-signal equivalent circuit parameters (see Fig. 3c) are extracted from the measured *S*-parameters according to the methods described in [115], [128]. Fig. 13 shows the relative impact of each parasitic parameter on the current gain (f_T, Fig. 13a) and maximum available power gain (f_{max}, Fig. 13b) cut-off frequencies of a 60 nm-long FinFET. As expected the gate resistance has an important impact on f_{max} whereas f_T is unchanged. The sum of fringing capacitances C_{inner} directly linked to the FinFET three-dimensional architecture has a huge impact on both cut-off frequencies. In fact, f_T and f_{max} drop down, respectively, by a factor of 3 and 2. Finally, the source and drain resistances as well as the parasitic capacitances related to the feed connexions outside the active area of the transistor slightly decrease both cut-off frequencies. Based on that analysis, it is quite clear that the fringing capacitances inside the active area of the FinFET are the most important limiting factor for this type of non-planar multiple gate transistors.

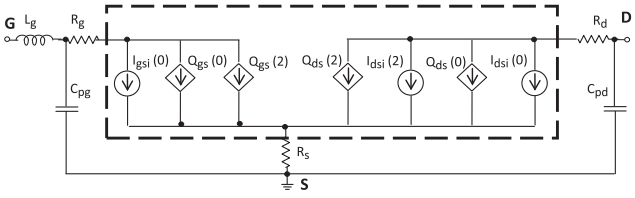
Fig. 14 shows the extracted total input gate capacitance (C_{gg}) in strong inversion ($V_{gs} = 1.7$ V and $V_{ds} = 0$ V) as a function of the active gate width (W_{tot}) for a FinFET and a conventional single gate (SG) MOSFET with 60 nm gate length. Both devices are built simultaneously on the same SOI wafer. A first order extrapolation of the measured data yields C_{gg} values of 1.33 fF/μm for the FinFET devices and only 1.09 fF per μm of active gate width for the SG, indicating a 20% increase of input capacitance in the case of FinFETs.



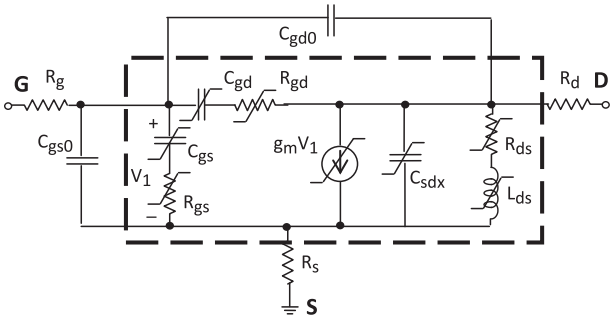
(a) Large-signal equivalent circuit based on quasi-static approximation, where the intrinsic section is composed by two charge sources and two current sources (i.e., Q_{gs}, Q_{ds}, I_{gs}, I_{ds}) representing, respectively, the displacement and the conduction intrinsic current contributions [63]



(b) Large-signal equivalent circuit extended to account for the intrinsic non-quasi-static effects and to include the extrinsic network modeling "open" and "short" test structures [54]



(c) Large-signal equivalent circuit extended with higher order sources (i.e., $Q_{gs}^{(2)}$, $Q_{ds}^{(2)}$, $I_{dsi}^{(2)}$) to account for the intrinsic non-quasi-static effects [67, 68]



(d) Large-signal equivalent circuit based on the small-signal equivalent circuit topology in Fig. 3(e) and extracted by using the ANN approach [69]

Fig. 10. Large-signal circuit topologies proposed in literature for SOI FinFET technology. The intrinsic sections are highlighted within dashed boxes.

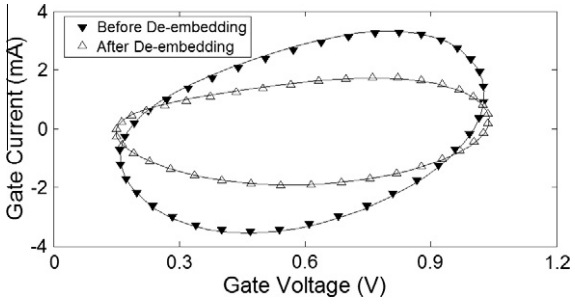


Fig. 11. Measured (symbols) and simulated (lines) input loci before (black down triangles) and after (white up triangles) applying "open/short" de-embedding procedure to the non-linear microwave data of a SOI FinFET with $W = 45.6$ μm and $L_g = 60$ nm at $f_0 = 15$ GHz, $V_{gs} = 0.6$ V, $V_{ds} = 0.6$ V, and $P_{in} = -1.7$ dBm [54].

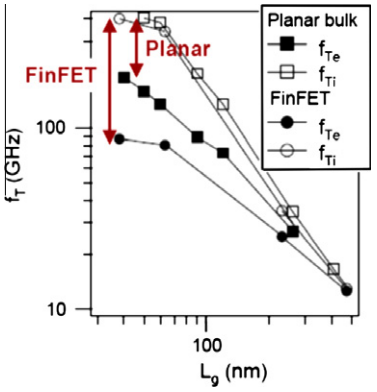


Fig. 12. Extracted intrinsic (f_{Ti}) and extrinsic (f_{Te}) current gain cut-off frequencies for a conventional single gate MOSFET and FinFET as a function of the channel length [29,156].

Assuming that the normalized oxide capacitance is equal in both SG and FinFET devices, this increase is solely due to additional fringing in FinFETs. Using additional capacitance data measured in deep depletion, the extrinsic gate capacitance is actually found to be 40% higher for FinFETs. As explained above, this higher normalized input capacitance for FinFET can be explained by the fact that the gate fingers must run over non active area between each pair of parallel fins, a situation that is not encountered in SG MOSFETs.

A lower electron mobility is achieved at the side-walls with respect to the top-channel surface and the conventional planar MOSFET because the electron mobility is lower in the (1 1 0) crystalline plane with respect to (1 0 0) [31–34,42,157]. Moreover, a reduction of the fin width to improve the gate control implies not only a reduced portion of the channel in the (1 0 0) plane but also an increase in the surface roughness of the side-walls, which leads to a further degradation of the electron mobility [34].

The extrinsic contributions of the source and drain resistances are increased as the fin width is reduced. To minimize the contact resistances, the fin may be enlarged outside of the gate region with the use of selective epitaxial growth (SEG) technology on the source and drain regions [31–34]. Nevertheless, this solution has

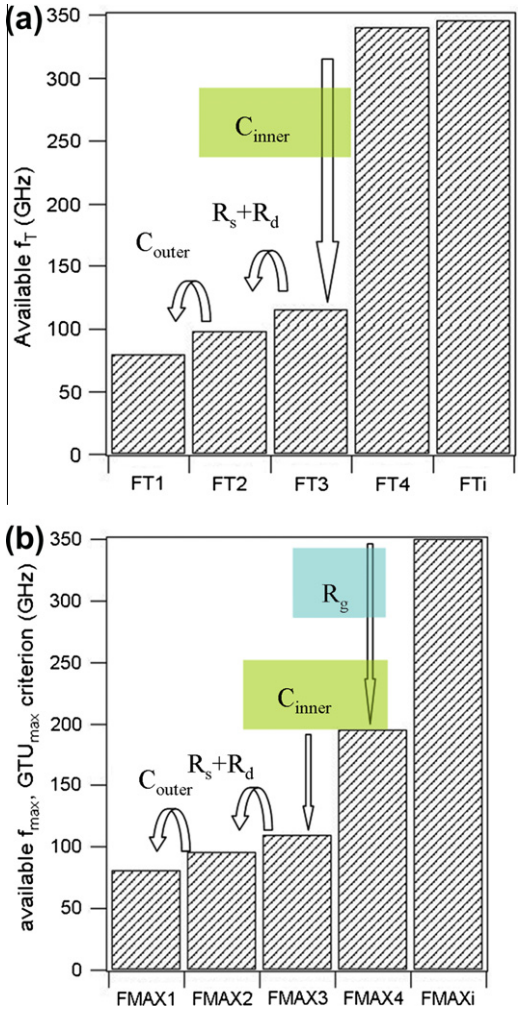


Fig. 13. Relative impact of each lumped extrinsic parameters on (a) the current gain cut-off frequency (f_T) and on (b) the maximum available gain cut-off frequency (f_{max}) for a 60 nm-long FinFET [29,156].

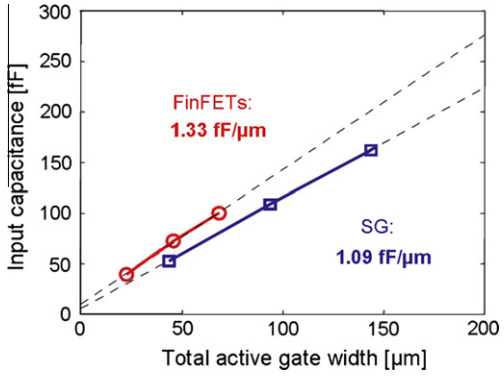


Fig. 14. Extracted input capacitance in strong inversion (V_{gs} = 1.7 V and V_{ds} = 0 V) as a function of W_{tot} for 60-nm SG MOSFET and 60-nm FinFET [43].

the drawback of leading to an increased processing complexity and higher extrinsic fringing capacitances arising from the coupling between gate and source/drain regions via the spacer [32,34].

The higher values of the extrinsic fringing capacitances should be ascribed to the complex 3D nature of the FinFET structure and, in particular, the presence of the gate electrode between each pair of neighboring fins can be considered to be the main cause [17,29–33,153–155]. Hence, the contributions of the extrinsic capacitances can be reduced by minimizing the fin spacing [17,29–32,153–155], which allows also increasing the integration density by consuming less chip area. Nevertheless, an aggressive reduction of the fin spacing is quite limited by technological concerns and a potential increase of the gate resistance [32,37].

The modeling results have been used to analyze the microwave performance of the FinFET technology by quantifying the negative impact of the extrinsic circuit elements [29,31]. The cut-off frequency obtained after applying "open/short" de-embedding to the data of both FinFET (i.e., 90 GHz) and planar MOSFET (i.e., 180 GHz) with a channel length of 60 nm has been analyzed [29,31]. The FinFET has a cut-off frequency around twice lower than that of the corresponding MOSFET, due to the performance limitations associated to the extrinsic contributions, mostly arising from extrinsic fringing capacitances. It should be pointed out that, similarly, the fringing capacitive contributions lead to a significant reduction also of the figure of merit f_{max} [29]. Nevertheless, by removing all extrinsic contributions from the data, both transistors exhibit similar values of the intrinsic cut-off frequency (i.e., around 400 GHz). This result demonstrates that the FinFET technology has attractive high-frequency potential to be further progressed by minimizing the extrinsic contributions of its 3D architecture. A critical role is played by the fin width that should be determined to achieve a trade-off between reduced short-channel effects and improved microwave performance.

In [153–155], based on measurements and 3D numerical simulations the impact of the extrinsic gate capacitances on the RF behavior of FinFETs has been analyzed. It has been shown that the reduction of the fin spacing, the modification of the fin geometrical aspect ratio (H_{fin}/W_{fin}) as well as the optimization of the fin spacing (S_{fin}) – fin source/drain extension (L_{ext}) ratio can significantly improve the FinFET RF behavior. Based on today technological capabilities, 40 nm-node FinFET can increment its cut-off frequency of at least 40% via an optimization of the fin layout with a fin geometry design corresponding to W_{fin} = 12 nm, H_{fin} = 60 nm, S_{fin} = 30 nm, and L_{ext} = 24 nm.

9. Conclusions

This paper has been devoted to present a comprehensive review of the field of microwave FinFET modeling. The reported investigation has covered all aspects ranging from linear (also noise) to nonlinear high-frequency models. Inspired by the traditional procedures for conventional MOSFETs, several techniques have been developed over the last years for modeling the advanced FinFET architecture. The observed differences in the modeling techniques should be attributed to the specific tested device and the investigated operating conditions. The proposed comparative study has provided a valuable modeling background and an important feedback for fabrication process engineers to support the development of the FinFET technology for microwave applications. It should be highlighted that the main advantage of the FinFET consists of enabling the downscaling of the gate length into the nanometer regime, which in turn allows achieving higher operating frequency and better microwave performance. The short-channel effects are reduced especially when the gate control is improved by decreasing the fin width. On the other hand, the microwave performance of the FinFET is degraded by the extrinsic contributions arising from the 3D nature of its structure that is even more pronounced when the fin is narrowed. However, even if research efforts are still required to improve the high-frequency FinFET performance and hopefully to reach state of art characteristics of microwave transistors, the benefit of shrinking the gate length with reduced short-channel effects and the possibility of integrating both analog and

digital circuits on the same chip make this technology very attractive for future microwave and mixed-mode applications.

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