Intrinsic rectification in common-gated graphene field-effect transistors

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Abstract

Terahertz rectifying antennas (rectennas) couple micron-size antennas and high-speed diodes to convert the incident electro-magnetic radiation to useable DC power. At such frequencies, the device acting as the diode requires both a nonlinear electrical behavior and a very low parasitic capacitance. Due to their low-capacitance planar structure and high carrier mobility values, several graphene devices based on various rectification mechanisms have been previously proposed as the rectifying device in the terahertz range. In this paper, we report an asymmetric behavior in micrometer-scale rectangular CVD-grown graphene field-effect transistors (GFETs), both at 77 K and room temperature (295 K). The asymmetry with a measured I_{ON}/I_{OFF} ratio as high as 1.85 is shown to originate from the slight change in graphene conductivity induced by drain-gate voltage variations. This is confirmed by simulations using a simple drift-diffusion transport model. The conclusions can be directly applied to optimize diode-connected GFETs. This nonlinear effect may also be of interest for graphene interconnect considerations as well as circuit designs using GFETs.

Keywords: AC-DC power converters, Energy harvesting, Rectifier, Rectenna, Diode, Graphene.

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1. Introduction

Terahertz rectifying antennas (rectennas) couple micron-size antennas with high-speed diodes to convert incident terahertz electro-magnetic fields to useable DC power (see Fig. 1(a)). These rectennas are investigated for energy harvesting purposes in the infrared region of the electro-magnetic spectrum [1]. To rectify signals at such high frequencies, a nonlinear electrical behavior and a very low parasitic capacitance are required from the device acting as the diode. Recently, graphene field-effect transistors (GFETs) [2] have shown promising rectification results for zero-bias detection at 0.3 THz [3]. GFETs with a diode-connection scheme implemented by split bowtie antennas have also been reported with responses both at 0.6 THz [4] and 1 THz [5]. A GFET with a modified channel geometry has also been reported at 28 THz [6]. This concept called a *geometric diode* relies on the ballistic transport of charge carriers in a funnel-shaped channel (see Fig. 1(b)) with a neck smaller than the mean free path to favor a current flow in one direction and produce a weak asymmetry in the electrical behavior [7].

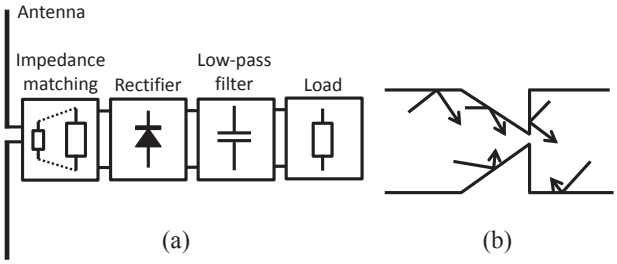

Figure 1: (a) General block-diagram of a rectenna device, consisting of an antenna coupled to a rectifier through a matching circuit. The rectifier output may need to undergo low-pass filtering before connecting to the load. For the terahertz range, the rectifier is usually a single ultra-high-speed diode and no matching circuit is used. (b) Graphene geometric diode concept with its funnel-shaped channel proposed by Moddel et al. [7].

Graphene is a two-dimensional material consisting of a single layer of carbon atoms arranged in a hexagonal lattice [8]. High carrier mobility values in

excess of 200,000 cm^2/Vs have been reported for suspended graphene at low temperatures [9]. On SiO_2 substrates, these values are strongly reduced by impurity and phonon scattering [10]. Mobility values up to 15,000 cm^2/Vs have been demonstrated under ambient conditions [11], however typical values lie in the range between 10^3–10^4 cm^2/Vs [12]. When graphene is encapsulated in hexagonal boron nitride (h-BN), scattering is strongly reduced and mobility values of 130,000 cm^2/Vs have been reported [13]. These high mobility values at room temperature combined with low parasitic capacitances translate to high frequencies of operation for GFETs and mean free paths on the order of a few hundred nanometers (about 500 nm for ref. [13] at 300 K), enabling practical implementations of the geometric diode concept as well as other graphene ballistic rectifiers as demonstrated by Song's group [14, 15, 16].

In this paper, we investigate the rectification capabilities of GFETs with simple rectangular channels by following a characterization methodology in DC biasing conditions similar to ref. [7]. The intrinsic capacitances of the device are another key element to assess its high-frequency rectification capabilities, but these have already been discussed in detail elsewhere [17, 18, 19]. As previously mentioned, terahertz operation of GFETs has already been experimentally demonstrated and we therefore focus our attention on the DC behavior of the GFET. The DC results obtained here are useful to understand and optimize the nonlinear performance of diode-connected GFETs and may also be of interest for graphene interconnect considerations as well as circuit designs using GFETs. After introducing the common figures of merit for rectenna diodes (Sec. 2), we introduce the electronic properties required to understand the results as well as a basic drift-diffusion current transport model used for simulations (Sec. 3). We then present the fabrication and measurement methods (Sec. 4) and examine the obtained characterization results (Sec. 5). The figures of merit associated with rectenna diodes are then applied. We summarize and discuss the results in Sec. 6.

2. Figures of Merit of rectifying devices

As reviewed in ref. [1], three figures of merit (FoMs) have been defined in eqs. (1),(2),(3) and are commonly used to characterize the performance of rectenna diodes. These FoMs can however be applied to any device with a current characteristic $I(V)$ to determine their rectification capabilities. For energy harvesting purposes, their values should be maximized near zero bias ($V \approx 0$).

$$\text{Asymmetry} \qquad \Upsilon(V) = \left| \frac{I(+V)}{I(-V)} \right| \tag{1}$$

$$\text{Nonlinearity} \qquad \mathcal{F}_{NL}(V) = \frac{dI}{dV}(V) \Big/ \frac{I(V)}{V} \tag{2}$$

$$\text{Responsivity} \qquad \mathfrak{R}(V) = \frac{d^2I}{dV^2}(V) \Big/ \frac{dI}{dV}(V) \tag{3}$$

The asymmetry $\Upsilon(V)$ defined in eq. (1) is the absolute ratio of forward to reverse current ($\mathrm{I_{ON}/I_{OFF}}$) at a given bias V. A value of $\Upsilon = 1$ indicates full symmetry and thus no rectification is possible at zero bias. If $\Upsilon > 1$ more current will flow in forward bias than in reverse bias. Conversely, if $\Upsilon < 1$ less current will flow in forward bias than in reverse bias. In both cases, as long as Υ departs from the unit ratio (either towards infinity or towards zero) the device is considered asymmetric. The nonlinearity $\mathcal{F}_{NL}(V)$ defined by eq. (2) is the ratio of the differential conductance to the global conductance. $\mathcal{F}_{NL}$ is therefore a measure of the deviation from a linear resistor, but taken alone it is not sufficient to ensure rectification at zero bias. A device can both be nonlinear and highly symmetric, in this case rectification could still be obtained but at the cost of applying a constant bias to the device to offset its characteristic curves [20]. The responsivity $\mathfrak{R}(V)$ is defined in eq. (3) as the ratio of the second derivative of the current on the differential conductance and is a more accurate predictor of the performance of the rectifying device. The rectified voltage seen at the load is directly proportional to the responsivity and the optical power of the incident wave [20]. Moreover, the rectifying device should not only maximize these FoMs at zero bias to obtain efficient rectification but

for single-diode rectennas it should also match the impedance of the antenna (typical values around a few hundred Ohms).

3. Electronic properties of graphene

This section introduces the electronic properties of graphene required to understand the results in Section 5 as well as a simple drift-diffusion current transport model used to run simulations supporting the results discussion. The electronic transport properties of graphene are based on its cone-shaped $E(K)$ relation around the K-point. It is approximated by a linear relation $E(k) = E(K) - E_D = s\hbar v_F|k|$ illustrated in Fig. 2(a), where $s = -1$ in the valence band and $s = +1$ in the conduction band, k is the wave vector from the K-point, $\hbar$ is the reduced Planck constant and v_F is the Fermi velocity. The energy E_D around which the relation is linearly approximated corresponds to the Dirac charge neutrality point (DNP). At this point, the bottom energy level E_C of the conduction band coincides with the top energy level E_V of the valence band and we have $E_D = E_C = E_V$. Graphene is therefore called a zero-gap semiconductor material, and the DNP is used as a practical reference for energy levels ($E_D = 0$).

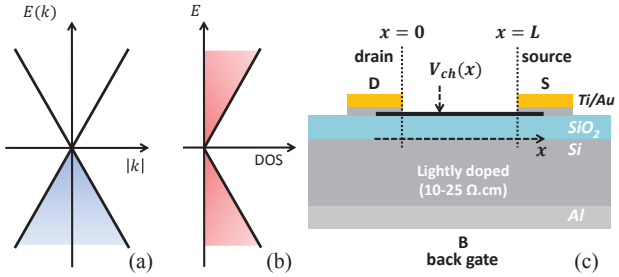

Figure 2: (a) Graphene energy dispersion relation around the K-point, with (b) the corresponding density of states and (c) structure of the GFET under consideration with its source (S), drain (D) and back gate (B) contacts.

3.1. Graphene quantum capacitance

The density of states (DOS) function of graphene vanishes at the DNP and increases linearly from there as illustrated in Fig. 2(b). It plays a key role in the electrostatics of the GFET structure shown in Fig. 2(c) as it affects the Graphene/Oxide/Semiconductor capacitor behavior. This capacitor structure exists between any point in the channel $V_{ch}(x)$ and the back gate contact (B), where V_{ch} is located between the source contact (S) and the drain contact (D). Highly-doped semiconductors and metals have a high DOS around their Fermi level, hence when charges are accumulated on the capacitor their Fermi level moves therefore very little. However, for graphene (or other lightly-doped semiconductors) when the Fermi level is near the DNP (or inside the bandgap) the DOS is vanishingly low (or cancels altogether). Therefore, the Fermi level in the graphene is highly sensitive to the accumulation of charges on the capacitor and moves easily around the DNP. As charges continue to accumulate, the Fermi level is driven further away from the DNP. As the DOS increases, the displacement of the Fermi level is gradually reduced and therefore graphene behaves more and more like a metal.

In an electrostatically biased GFET structure, the displacement of the Fermi level occurs locally everywhere in the graphene channel, and in particular also at the drain and source contacts. When electrical potentials are applied between the back gate and the drain (V_{BD}) and between the back gate and the source (V_{BS}), part of the electric potential energy is not capacitively stored as an electric field E_{ox} in the oxide region, but is instead used to displace the Fermi energy level in the graphene. Therefore, the concept of a quantum capacitance C_q in series with the oxide capacitance C_i is used to described this voltage drop in the graphene channel [21] (see Fig. 3).

To obtain this quantum capacitance, we first provide the free carrier densities of electrons n and holes p as derived by Champlain [22] in Eq. (4), where $\mathcal{F}_j(u)$ is the j^{th}-order Fermi-Dirac integral. The thermal voltage $\phi_T = \frac{k_B T}{q}$ and the effective graphene density of states $N_G = \frac{2(k_B T)^2}{\pi(\hbar v_F)^2}$ are used where q is the elementary charge, k_B the Boltzmann constant and T the absolute temperature.

The graphene channel potential ϕ_c is defined as $-q\phi_c = (E_{F,g} - E_D)$ as shown in Fig. 3, with $E_{F,g}$ the Fermi energy level in graphene.

$$n = N_G \mathcal{F}_1 \left(-\frac{\phi_c}{\phi_T} \right) \qquad p = N_G \mathcal{F}_1 \left(\frac{\phi_c}{\phi_T} \right) \tag{4}$$

The quantum capacitance defined as $C_q \triangleq \frac{dQ_{net}}{d\phi_c}$ [23] is then derived from the net mobile positive charge density in the graphene sheet $Q_{net} = q(p - n)$. Eq. (5) is then obtained by Champlain [22] from this definition and the derivative properties of Fermi-Dirac Integrals. The quantity C_q determines how much additional charge is accumulated in the graphene sheet for a variation of the channel potential (or Fermi level $E_{F,g}$). Since $Q_{net}(\phi_c)$ is an anti-symmetric function $[Q_{net}(\phi_c) = -Q_{net}(-\phi_c)]$, its derivative $C_q(\phi_c)$ is a symmetric function around the DNP ($\phi_c = 0$).

$$C_q = \frac{qN_G}{\phi_T} \ln \left[2 \left(1 + \cosh \left(\frac{\phi_c}{\phi_T} \right) \right) \right] \tag{5}$$

3.2. GFET electrostatics

The charge-voltage (QV) relationship of the GFET is given in Eq. (6) as derived by Champlain [22] assuming a highly-doped semiconductor back gate approximated as a metal. However, the GFET structure used in this work and shown in Fig. 2(c) has a lightly-doped back gate. This introduces additional substrate effects [24], but for simplicity we ignore these effects in this section and consider the back gate to behave as a metal.

$$[V_B - V_{ch}] + \left[\frac{Q_{net}(\phi_c)}{C_i} + \phi_c \right] = \phi_m - \phi_g - \frac{Q_f}{C_i} \tag{6}$$

Eq. (6) solves the electrostatics of the structure for an applied channel voltage $V_{ch}(x)$ and back-gate voltage V_B using both the conditions for energy conservation and charge neutrality. The equation is based on the energy band diagram shown in Fig. 3, where ϕ_m is the equivalent metal work function of the back gate, ϕ_g is the graphene work function, E_{ox} is the electric field in the oxide and t_{ox} is the oxide thickness. The oxide capacitance per unit area is $C_i = \frac{\varepsilon_{ox}}{t_{ox}}$, where ε_{ox} is the oxide permittivity. Due to charge neutrality, the oxide electric

field $E_{ox} = \frac{Q_{net}(\phi_c)+Q_f}{\varepsilon_{ox}}$ is entirely determined by the channel potential ϕ_c, where the charge density Q_f represents any fixed charges within the graphene sheet or the oxide layer [22]. To obtain the electrostatic equilibrium conditions at source and drain, the channel voltage is substituted for $V_{ch}(x = 0) = V_D$ and $V_{ch}(x = L) = V_S$.

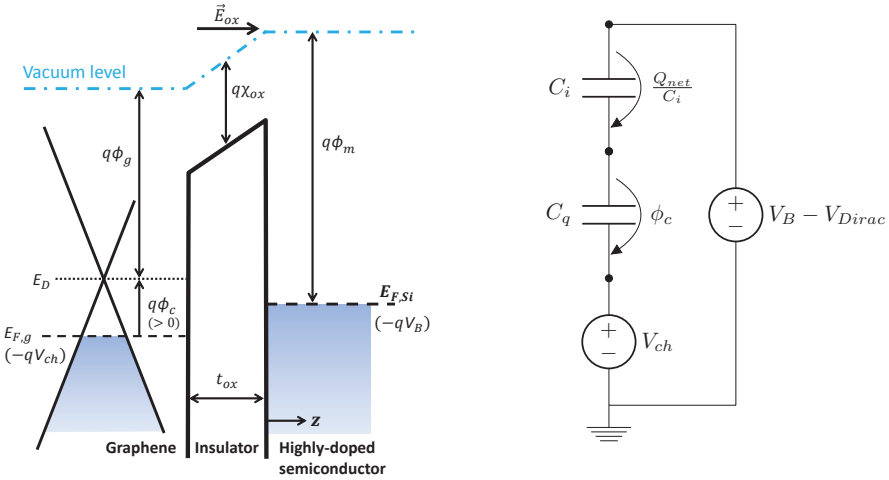

Figure 3: Band diagram of a GFET graphene/SiO_2/silicon structure (left) where the semiconductor back gate is approximated by a perfect metal conductor, and its equivalent circuit representation corresponding to eq. (6) (right).

3.3. Graphene carrier transport model

A simple expression of the graphene drain-source current is given in Eq. (7) based on drift-diffusion theory, it is thus only valid for transistors exhibiting diffusive transport (channel length L longer than the mean free path) [18]. Typical values of the mean free path at room temperature are on the order of a few hundred nanometers for graphene on SiO_2 [10]. Some transport models suggest that the branch separation between electron and hole contributions are due to a voltage-dependent effect of contact resistances [25, 26]. However, since all the measurements in Section 5.1 are made with four contacts we neglect contact resistances. Therefore, different mobility values for holes (μ_p) and electrons (μ_n)

are used to take the branch separation into account as has been proposed in the literature [22, 26, 17, 27, 28].

$$I_{DS} = \frac{W}{L}\int_{V_S}^{V_D}\left(q\mu_p p + q\mu_n n + q\frac{\mu_p+\mu_n}{2}n_{pud}\right)dV_{ch} \tag{7}$$

The conductivity $\sigma = q\mu_p p + q\mu_n n$ in Eq. (7) involves the sum of the electron and hole contributions. Therefore, if $\mu_n = \mu_p$, due to the definitions of p and n in eq. (4) the conductivity is a symmetric function ($\sigma(\phi_c) = \sigma(-\phi_c)$) with the minimum of conductivity occuring at the DNP ($\phi_c = 0$). There, although the DOS vanishes, a residual thermal charge density is taken into account by the fact that $\mathcal{F}_1(\phi_c = 0) \neq 0$ in eq. (4). Another residual charge due to spatial inhomogeneity forming electron-hole puddles is taken into account by adding the term $q\frac{\mu_p+\mu_n}{2}n_{pud}$ [29]. This carrier density is computed as $n_{pud} = \frac{\Delta^2}{\pi(\hbar v_F)^2}$, with Δ the inhomogeneity of the electrostatic potential [10].

The integral of σ over V_{ch} in Eq. (7) is computed by substituting the variable from V_{ch} to ϕ_c. The derivative of Eq. (6) $\frac{dV_{ch}}{d\phi_c} = 1 + \frac{C_q}{C_i}$ is used to obtain Eq. (8).

$$\int_{\phi_{c,S}}^{\phi_{c,D}} \sigma\frac{dV_{ch}}{d\phi_c}\,d\phi_c = \int_{\phi_{c,S}}^{\phi_{c,D}} \sigma(\phi_c)\left(1 + \frac{C_q(\phi_c)}{C_i}\right)d\phi_c \tag{8}$$

When different drain and source biasing conditions are applied to the GFET ($V_D \neq V_S$), the electrostatic equilibrium conditions at source (V_{BS}) and drain (V_{BD}) change. The Fermi level at each terminal becomes different ($\phi_{c,S} \neq \phi_{c,D}$) and a current will flow as illustrated in Fig. 4. Sweeping the substrate voltage V_B then provides the gate transfer characteristics of the GFET for the given drain-source voltages V_{DS}.

Even without solving Eq. (8), it is interesting to notice that both $\sigma(\phi_c)$ (if $\mu_n = \mu_p$) and $C_q(\phi_c)$ are symmetric functions. And due to graphene's DOS, both $\sigma(\phi_c)$ and $C_q(\phi_c)$ have a minimum value at the DNP ($\phi_c = 0$). For graphene at flatband conditions where $V_B = V_{Dirac} = \phi_m - \phi_g - \frac{Q_f}{C_i}$, we see from eq. (6) that for low biasing conditions ($V_{ch} \approx 0$) with $V_D \approx V_S$ we will

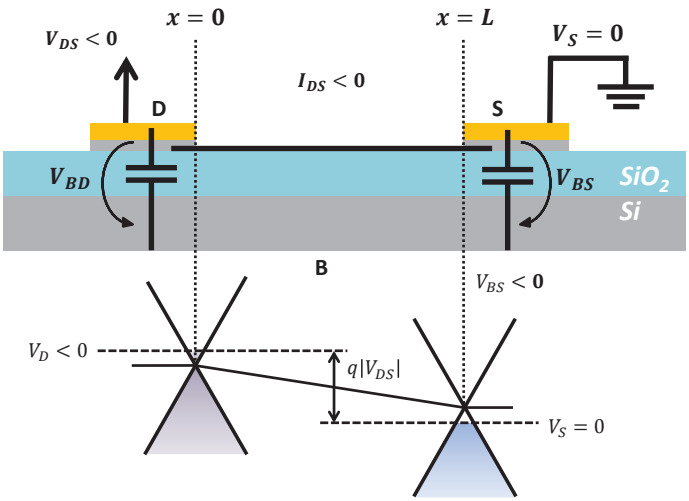

Figure 4: Illustration of the shift in Fermi level at the drain and source contacts resulting from applying a negative V_{DS} bias with a negative V_{BS} bias.

have $\phi_{c,s} \approx \phi_{c,d} \approx 0$ because $Q_{net}(\phi_c)$ and ϕ_c both cancel out in eq. (6) at $\phi_c = 0$. Therefore, the minimum of conductivity or equivalently the maximum of resistance occurs at $V_B - V_{Dirac} = 0$ and V_{Dirac} thus corresponds to the DNP. The gate transfer characteristics of graphene are typically obtained under small drain-source bias $V_{DS} \approx 0$ because this gives a higher precision in probing the number of states available for conduction through the integral from $\phi_{c,s}$ to $\phi_{c,d}$.

4. Methods and materials

4.1. Device fabrication

The graphene devices were fabricated as illustrated in Fig. 2(c) by transferring commercial CVD-grown graphene [30] onto a standard silicon substrate, with a light p-type (Boron) doping concentration $N_A \approx 10^{15}\text{cm}^{-3}$. Before the transfer, the silicon wafer was first thermally oxidized over a thickness $t_{ox} = 20$ nm and the backside was etched with buffered hydrofluoric acid (BHF) to remove the oxide. After the etching, a 200 nm-thick backside aluminium contact was deposited by electron beam evaporation. Because graphene is not

easily visible, optical alignment marks were etched into the oxide to align subsequent processing masks. After graphene transfer, the graphene channels were patterned using optical lithography, protecting the remaining graphene with photoresist AZ5214E and etching the exposed excess graphene using a 30 W RF and 75 W inductively coupled plasma (ICP) for 20 minutes at 20 mTorr with a 50 sccm O_2 flow. Four Ti/Au contacts (5/95 nm) were deposited by evaporation and lift-off. Before measurement, the wafers were diced (protected by AZ6612 resist) and the devices under test were annealed in a rapid thermal annealing furnace at 300 ˚C for 30 minutes under Ar/H_2 forming gas. The resulting four-contact structure is shown in Fig. 5. The presence of monolayer graphene has been confirmed by Raman spectroscopy measurements (see Supplementary Material Fig. S1). The presence of graphene is confirmed by its characteristic G and 2D peaks. The intensity ratio between the 2D and the G peaks is higher than unity indicating predominantly monolayer graphene. The D peak associated with defects is present but its intensity is still quite low compared with the intensity of the G peak. Furthermore, the integrity and uniformity of the graphene has been confirmed for one of the GFET devices presented in Section 4.2 by performing a Raman spectroscopy mapping of the channel (see Supplementary Material Figs. S3 and S4).

4.2. Measurement conditions and reproducibility

The electrical DC measurements were performed in a Lake Shore CPX cryogenic micro-manipulated probe station under vacuum conditions to reduce environmental effects. A pressure below 10^{-5} mbar was obtained using an Agilent TPS-compact turbomolecular pump. Several GFET devices with channel width $W = 30$ µm have been measured and contacted with DC nickel-plated tungsten probe needles. Several devices have been measured, but in Sec. 5 we present the results for two devices at different temperatures: device 1 has length $L = 3$ µm and was measured at 77 K, while device 2 has length $L = 8$ µm and was measured at 295 K. For all measurements, the source contact was kept at ground $V_S = 0$ V and only the back gate V_B and drain V_D voltages were varied.

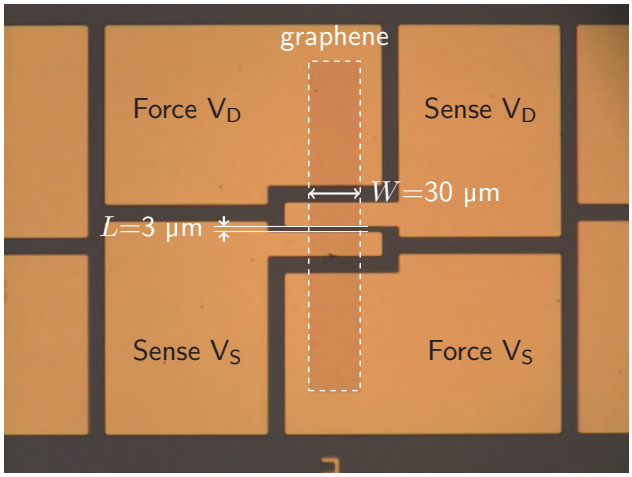

Figure 5: Microphotograph of a typical four-contact GFET device.

To assess reproducibility of the results, baseline gate transfer characteristics at low bias (V_{DS} = 15 mV) were performed regularly between the measurements presented in Sec. 5. Hysteresis effects were observed for these baseline measurements (see Supplementary Material Fig. S5). Although these effects are relatively weak in device 2, they are further reduced for device 1 and motivate the measurements at 77 K in addition to the room-temperature measurements.

The reproducibility of the results was further assessed by observing the current ratio between the successive (bi-directional) baseline gate transfer characteristic curves (see Supplementary Material Fig. S6). Perfect reproducibility of the measurements would result in a unit ratio for all back-gate voltages, but due to noise and other fluctuations this will never be exactly the case. However, at lower temperature these variations are reduced as device 1 shows ±0.5% variation compared with device 2 with ±5% variation at room temperature. These variations provide a lower limit to which the results obtained for the asymmetry Υ in Sec. 5.3 can be directly compared.

5. Results and discussion

5.1. Measurement results

Two sets of measurements of the drain-source current I_{DS} were made for each device: the first is a set of $I_{DS} - V_{BS}$ curves obtained at different V_{DS} drain-source voltage values and the second is a set of $I_{DS} - V_{DS}$ curves obtained at different V_{BS} back-gate voltage values. Due to the limited hysteresis effects, without loss of generality we here present the measurement results of the first set obtained in the direction of increasing V_{BS}. Similarly, we present measurements of the second set obtained in the direction of increasing V_{DS}.

In Fig. 6, the first set of measurements is shown as the resistance $R = V_{DS}/I_{DS}$ as a function of the back-gate voltage V_{BS}. A feature observed due to the use of a lightly-doped silicon substrate is the kink/plateau around $V_{BS} = 0$ V, corresponding to the region where the surface charge density in the silicon substrate changes from accumulation to inversion by forming the depletion layer [24]. For device 1 at 77 K, the 5 seconds hold time used during the measurements was insufficient to thermally generate the inversion layer required for proper gating, pinning the resistance value for $V_{BS} < 0$ only.

To assess if these GFETs exhibit a rectification behavior, we look for signs of asymmetry from the gate transfer characteristics. In Fig. 6, we observe that at any given value of V_{BS} – with the source fixed at $V_S = 0$ – changing the value of the drain voltage V_D shifts the curves and the minimum conduction point associated to the DNP ($V_{Dirac} \approx 4.8$ V for both devices). The corresponding maximum resistance point (MRP) shifts to higher V_{BS} voltages when a positive drain voltage V_D is applied ($V_{MRP} > V_{Dirac}$), and to lower V_{BS} voltages when a negative drain voltage V_D is applied ($V_{MRP} < V_{Dirac}$). The peak resistance value is also reduced with increasing drain-source biasing conditions $|V_{DS}|$.

Due to these shifts, the effect on the resistance of a change in drain voltage is different, roughly depending on whether V_{BS} is lower or higher than the DNP voltage V_{Dirac}: for $V_{BS} < V_{Dirac}$ increasing V_{DS} reduces the resistance, while for $V_{BS} > V_{Dirac}$ this has the opposite effect and increases the resistance. This

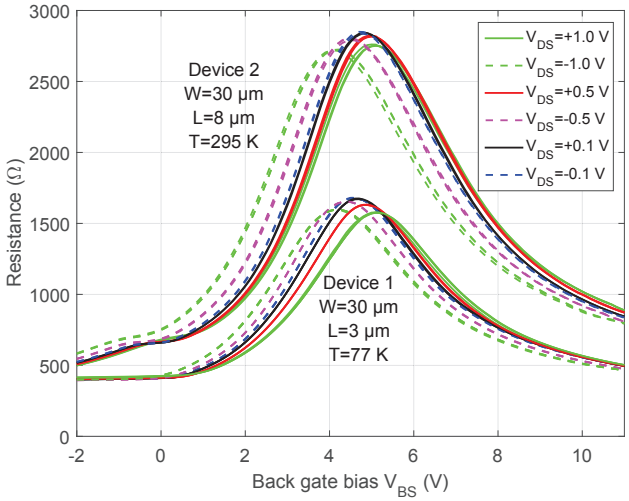

Figure 6: Measured $R - V_{BS}$ curves for the two presented devices at different V_{DS} bias conditions with $V_S = 0$.

can be seen more clearly through the $I_{DS} - V_{DS}$ measurements performed for both devices. In Fig. 7, the resistance has been plotted for increasing V_{BS} values and the results have been separated in two graphs when crossing $V_{BS} \approx V_{Dirac}$. From these figures, we can directly see that the GFETs do not behave symetrically with respect to the applied V_{DS} voltage. The only two notable exceptions to this asymmetry are seen: (i) at the DNP when $V_{BS} = V_{Dirac}$, where the resistance slopes change symmetrically from decreasing to increasing and (ii) very far from the DNP when the channel is highly populated and the GFETs behave essentially like a resistor (almost constant resistance across all V_{DS}).

To be more accurate however, as seen in Fig. 7 the change in resistance slope with V_{DS} (switching between monotonous increasing and monotonous decreasing dependence) does not happen *only* at the DNP. Instead, due to the MRP shifting away from the DNP with increasing $|V_{DS}|$ as shown in Fig. 6, for a given V_{BS} value there will always be a corresponding $V_{DS,MRP}$ value such that the MRP will be located at V_{BS} (i.e. $V_{MRP} = V_{BS}$ for this $V_{DS,MRP}$).

Consequently, this means that the MRP is also visible in the $R - V_{DS}$ curves in Fig. 7. Within the measured V_{DS} range, the resistance peak is indeed observed in curves obtained for V_{BS} values close enough to V_{Dirac}.

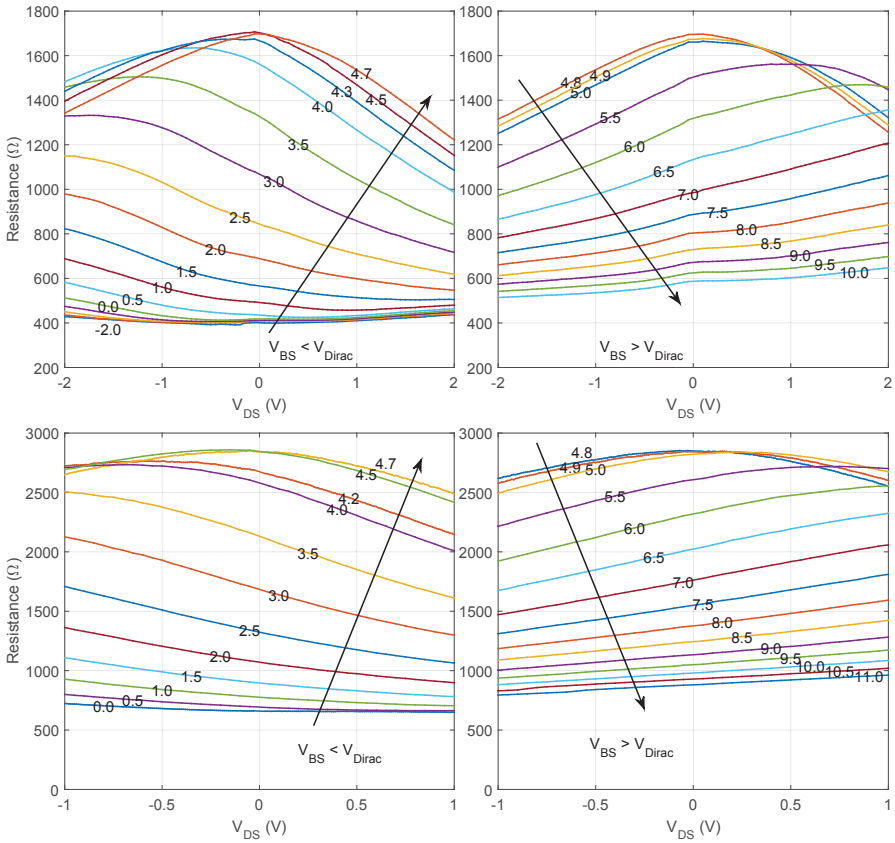

Figure 7: Measured $R - V_{DS}$ curves for device 1 (top) and device 2 (bottom) at different V_{BS} bias conditions (annotated on the curves) with $V_S = 0$.

5.2. Discussion

All these results can be understood based on the DOS of graphene and the fact that changing the V_{BS} and V_{BD} voltages shifts the equilibrium Fermi energy level in the material, as explained in Section 3. When drain-source voltages $V_{DS} \neq 0$ are applied, the Fermi level is electrostatically moved away

from the DNP, as enforced by eq. (6), and additional states are available for conduction as dictated by eq. (8) and illustrated in Fig. 4. The MRP will then shift to another V_B voltage ($V_{BS} = V_{MRP}$) depending on the applied drain and source voltages to reach a configuration that lowers the overall number of states available for conduction. This configuration is shown in Fig. 8 since for $V_S = 0$, when V_D is put at a negative (positive) value the MRP shifts to a lower (higher) V_B value. Since at the MRP more states are used for conduction, this results in a lowering of the peak resistance value compared with the peak resistance achieved when the MRP coincides with the DNP ($V_{MRP} = V_{Dirac}$). If $\mu_n = \mu_p$ as assumed in Fig. 8, the MRP occurs at $V_{MRP} - V_{Dirac} = \pm V_D/2$ if a drain voltage of $\pm V_D$ is applied. If $\mu_n \neq \mu_p$, the symmetry of σ is broken (as discussed in Sec. 5.4) and the position of the MRP has to be determined numerically. However, the difference in V_B voltages between the resistance peak for $+V_D$ and for $-V_D$ will remain equal to $\Delta V_B = V_{MRP,+V_D} - V_{MRP,-V_D} = V_D$.

All these effects have been confirmed by simulations using the simple model presented in Sec. 3.3. A device with realistic parameters has been simulated in Fig. 9(a) and its resistance shows the expected symmetric shift in MRP and lowering of the peak resistance value. The Fermi levels at the drain (d) and source (s) contacts are shown in Fig. 9(b). As discussed above and illustrated in Fig. 8, the MRP is shown in Fig. 9 to occur for $\phi_{c,d} = -\phi_{c,s}$ when both levels are closest in energy to the DNP. The difference of Fermi levels in Fig. 9(c) shows that the difference between the two Fermi levels are maximized (in absolute value) at the MRP. This should however not be surprising as this is where the total number of states between those two levels are minimized.

5.3. Rectification Figures of Merit

Since an asymmetry is observed, we can use the figures of merit reported in [1] and listed in Sec. 2 to qualify the rectification properties of the GFETs. The same figures of merit were reported for the graphene geometric diodes as well except the nonlinearity [7].

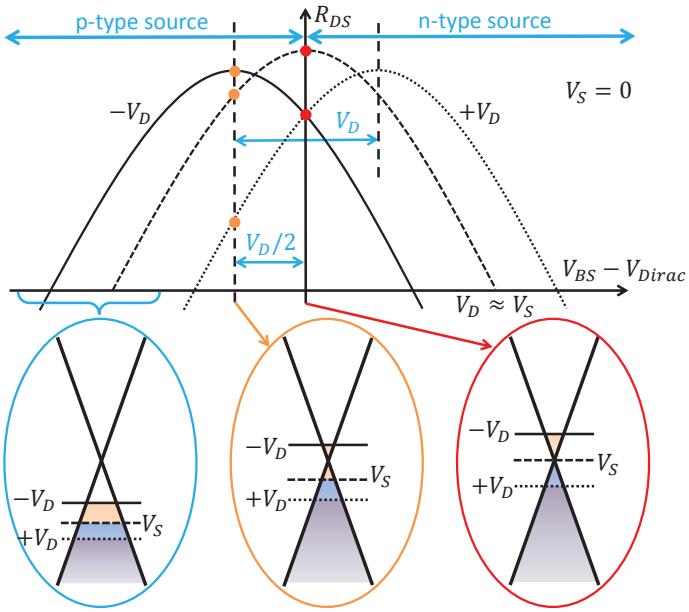

Figure 8: Illustration of the MRP shift due to non-zero V_{DS}, assuming $V_S = 0$ and $\mu_n = \mu_p$. The shift is attributed to the larger number of states available for conduction. If $\mu_n = \mu_p$, the MRP associated with a drain voltage $\pm V_D$ is located at $V_{BS} - V_{Dirac} = \pm V_D/2$.

Asymmetry. The asymmetry FoM defined in eq. (1) corresponds to the absolute ratio of forward to reverse current at a given $|V_{DS}|$ bias. In Fig. 10, the definition of Υ (equivalent to $\frac{R(-V_{DS})}{R(+V_{DS})}$ regarding Figs. 6 and 7) was applied to the two devices on the basis of the $I_{DS} - V_{BS}$ set of measurements from Fig. 6. The asymmetry curves obtained from the $I_{DS} - V_{DS}$ measurements are shown in Supplementary Material Figs. S7 and S8, there the highest value measured is $\Upsilon = 1.85$ for $|V_{DS}| = 2$ V.

The behavior observed in Fig. 10 corresponds to what was expected from the trends in Figs. 6 and 7. Indeed, $\Upsilon = 1$ when crossing the neutrality point ($V_{BS} = V_{Dirac}$) and tends slowly to unity at V_{BS} values far away from the neutrality point, where the channel is highly populated. The kink and clamping for negative V_{BS} values are due to the substrate effects previously mentionned [24]. The observation of $\Upsilon > 1$ for $V_{BS} < V_{Dirac}$ is also consistent with the reduction

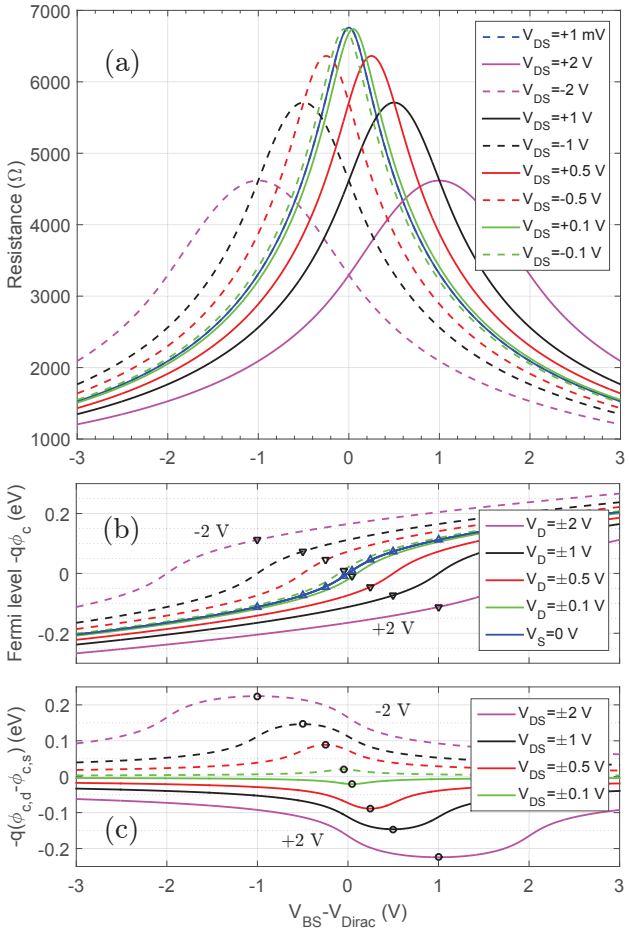

Figure 9: Simulation of a device with μ_n=μ_p=1000 cm^2/Vs, Δ=0.1 eV, v_F=10^6 m/s, W=L=10 µm, t_{ox}=20 nm at T=295 K. The figures show (a) the drain-source resistance, (b) the Fermi level $-q\phi_c$ at the drain (d) and source (s) contacts, and (c) the difference between those two Fermi levels. The triangles and dots indicate the position of the MRP, and since μ_n=μ_p these correspond to locations where $\phi_{c,d} = -\phi_{c,s}$ in (b) and where the largest absolute difference in Fermi levels is observed in (c).

of resistance with increasing V_{DS}, since more current will flow in forward bias than in reverse bias. The GFET then behaves as a forward-connected diode. Conversely, for $V_{BS} > V_{Dirac}$ we have $\Upsilon < 1$ which is also consistent with the increase in resistance for increasing V_{DS}, since less current will flow in forward

bias than in reverse bias. The GFET behaves then as a reverse-connected diode. This reversible polarity feature of the GFET depending on the type of majority carrier in the channel was also reported for the graphene geometric diodes and several other devices [7].

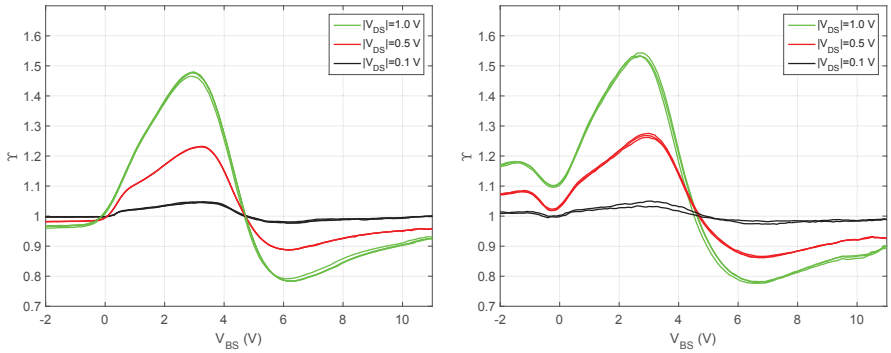

Figure 10: Asymmetry curves obtained for device 1 (left) and device 2 (right) from the $I_{DS} - V_{BS}$ measurements (see Fig. 6). The dip/clamping of the values towards unity around $V_{BS} = 0$ is due to the effect of the depletion layer in the lightly-doped substrate.

In Fig. 11 a I_{DS}-V_{BS} measurement of device 2 at $V_{DS} = \pm 0.5$ V is fitted both using the model without substrate effects presented in Sec. 3.3 and using the model with substrate effects presented in ref. [24]. A Fermi velocity of $v_F = 10^6$ m/s was used for all simulations. The CVD-grown graphene is p-doped as V_{Dirac} is located at a positive V_{BS} value, this was fitted by $Q_f = C_i \cdot (-4.25\,\mathrm{V})$ and $\Delta = 111.5$ meV. The quantitative fitting of the MRP peak was not good for our devices and this translates to an inaccurate fitting of Υ around the DNP as seen in the bottom graph of Fig. 11. The observed peak broadening could be due to simplifications in the model such as the mobility dependence on carrier concentration [10, 31] but is more likely due to the dense presence of µm^2 bilayer flakes on the commercial graphene [30] (see Supplementary Material Fig. S2).

Nonlinearity. The nonlinearity defined as $\mathcal{F}_{NL}$ has been computed for the two devices from the set of $I_{DS} - V_{DS}$ measurements (see Fig. 7). The resulting mapping of $\mathcal{F}_{NL}$ as a function of V_{DS} and V_{BS} is shown in Supplementary Material Fig. S9 for device 1 at 77 K and in Supplementary Material Fig. S10

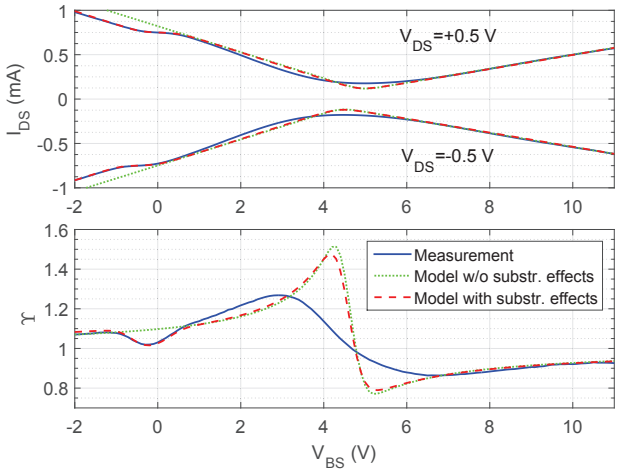

Figure 11: (top) Four-contact I_{DS} measurement of device 2 at 295 K for V_{DS}=±0.5 V, fitted by the model without substrate effects (dotted) by the set of parameters {Δ=111.5 meV, μ_p=445 cm^2/Vs, μ_n=240 cm^2/Vs, Q_f=C_i·(-4.25 V)} and with substrate effects (dashed) by the set {Δ=109.5 meV, μ_p=500 cm^2/Vs, μ_n=255 cm^2/Vs, Q_f=C_i·(-3.95 V)}. (bottom) Resulting asymmetry ϒ for the measurements and the fitting models.

for device 2 at 295 K. The values obtained are in the range from 0.5 to 1.5 for device 1 and 0.8 to 1.25 for device 2. The $\mathcal{F}_{NL}$ values are close to unity near zero bias, but also on a line corresponding to the position of the MRP (comparable with Fig. 7). Hence, the GFET shows little deviation compared with a linear resistor according to this criterion. The measurements of device 1 have been fitted by the model presented in Sec. 3.3 and the resulting $\mathcal{F}_{NL}$ mapping is shown in Supplementary Material Fig. S11. The simulations predict sharper features due to the unbroadened Dirac peak, and higher $\mathcal{F}_{NL}$ values are observed near zero bias around the DNP, however the values remain overall in the 0.8-1.8 range. The small remaining differences observed with the $\mathcal{F}_{NL}$ computed from measurements are due to the substrate effects.

Responsivity. The highest value of the responsivity $\mathfrak{R}$ at zero bias ($V_{DS} = 0$) is $\mathfrak{R} = 0.419\,A/W$ for device 1 and $\mathfrak{R} = 0.558\,A/W$ for device 2, both obtained at $V_{BS} = 3\,V$. Incidentally this V_{BS} value also corresponds to the point of

highest asymmetry Υ, as seen in Fig. 10. The full mappings of the responsivity are shown in Supplementary Material Figs. S12 and S13 for devices 1 and 2, respectively. The measurements of device 1 have been fitted by the model (Sec. 3.3) and the resulting $\mathfrak{R}$ is shown in Supplementary Material Fig. S14. As previously for the nonlinearity, the simulations predict sharper features due to the unbroadened Dirac peak, and higher $\mathfrak{R}$ values are observed at zero bias. The differences observed with the $\mathfrak{R}$ computed from measurements are again due to the substrate effects. The simulated highest value at zero bias is $\mathfrak{R} = 0.575\,A/W$ for $V_{BS} = 3.7\,V$.

5.4. Impact of different mobility values

For simplicity, the discussion in Sec. 5.2 has highlighted the behavior of graphene with a symmetric behavior for holes and electrons ($\mu_n = \mu_p$). If the graphene channel exhibits asymmetric properties for holes and electrons ($\mu_n \neq \mu_p$), this affects the slope of the I_{DS} current in the transfer characteristics on both sides of the MRP (e.g. see Supplementary Material Fig. S15 for $\mu_p/\mu_n = 4$) and the MRP will shift differently on each side of the DNP. This is barely noticeable in our measurements as seen for device 1 in Fig. 6 where $\mu_p \approx 1.9\mu_n$ (when including substrate effects for mobility extraction). However, the ΔV_B between the MRP for $+V_D$ and $-V_D$ remains $\Delta V_B = V_D$.

Due to the presence of bilayer graphene flakes and overall low quality of the graphene material (see Supplementary Material Section S1), the mobility values reported for our GFET devices are far from state of the art devices [2, 32, 33]. Device 1 is fitted without substrate effects at T=77 K with the set of parameters {Δ=139 meV, μ_p=255 cm^2/Vs, μ_n=141 cm^2/Vs, Q_f=C_i(-3.8 V)} and with substrate effects by the set {Δ=139 meV, μ_p=290 cm^2/Vs, μ_n=150 cm^2/Vs, Q_f=C_i(-3.8 V)}. As presented in Fig. 11, device 2 is fitted at 295 K without substrate effects by the set of parameters {Δ=111.5 meV, μ_p=445 cm^2/Vs, μ_n=240 cm^2/Vs, Q_f=C_i·(-4.25 V)} and with substrate effects by the set {Δ=109.5 meV, μ_p=500 cm^2/Vs, μ_n=255 cm^2/Vs, Q_f=C_i·(-3.95 V)}. However, within the limits of our simple model we can show that the

absolute value of the mobility does not affect the asymmetry behavior reported in this work. Assuming $\mu_p = \mu_n$ (i.e. $\mu_p/\mu_n = 1$), the mobility can indeed be brought out of the integral in Eq. (7). Hence, this factor will cancel out when computing the asymmetry using Eq. (1).

For $\mu_p/\mu_n \neq 1$, the absolute value of μ_n can be brought out of the integral and it is the ratio μ_p/μ_n that will act as a weighing factor on the hole concentration and the residual spatial inhomogeneity concentration inside the integral. As for the width W and the length L, the mobility μ_n in front of the integral will cancel out when computing the asymmetry with Eq. (1). However, the mobility ratio μ_p/μ_n remaining in the integral can have a significant impact on the asymmetry. To investigate this impact of the branch separation on the asymmetry, in Fig. 12 we simulated the maximum and minimum asymmetry values for different $|V_{DS}|$ values as a function of the ratio μ_p/μ_n with μ_n=1000 cm^2/Vs. For $\mu_p/\mu_n > 1$ the maximum asymmetry Υ_{max} increases while for $\mu_p/\mu_n < 1$ it decreases and the impact is shown to be significant even for small variations of this ratio.

As established previously, GFETs have a diode-like electrical behavior with reversible polarity (either $\Upsilon > 1$ for $V_{BS} < V_{Dirac}$ or $\Upsilon < 1$ for $V_{BS} > V_{Dirac}$) where each polarity is associated with one type of charge carrier. Therefore, we define Γ in eq. (9) to assess the maximum asymmetry observed in Υ due to the change of carrier mobility ratio.

$$\Gamma = \frac{\Upsilon_{max,\text{forward}}}{\Upsilon_{max,\text{reverse}}} = \Upsilon_{max} \cdot \Upsilon_{min} \tag{9}$$

The parameter Γ compares the maximum asymmetry of the forward diode $\Upsilon_{max,\text{forward}}$ ($V_{BS} < V_{Dirac}$) with the maximum asymmetry of the reverse diode $\Upsilon_{max,\text{reverse}} = 1/\Upsilon_{min}$ ($V_{BS} > V_{Dirac}$). As seen in Fig. 12, if $\mu_n = \mu_p$ then $\Gamma = 1$ for any $|V_{DS}|$ and both the forward and reverse diodes have equal maximum asymmetry. However, when $\mu_n \neq \mu_p$ one of the two diodes exhibits stronger asymmetry. It can also be noted that both mobility values have an equivalent impact on Γ, as we have $\Gamma(\mu_n/\mu_p) = 1/\Gamma(\mu_p/\mu_n)$ for all ratios. More results

are provided in Supplementary Material Section S6.

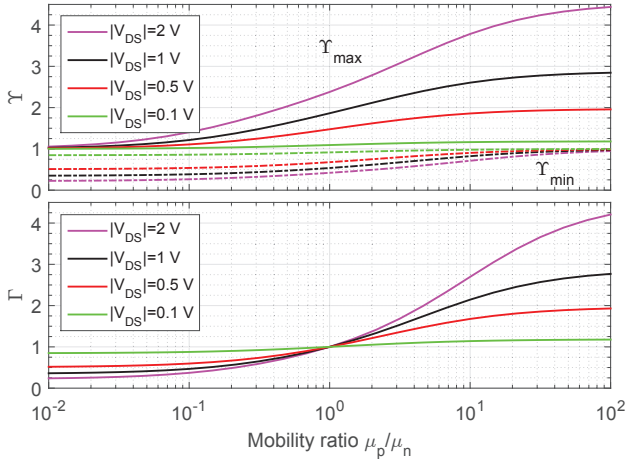

Figure 12: Simulation of the maximum and minimum asymmetry of a device as a function of μ_p/μ_n (top) with μ_n=1000 cm^2/Vs, Δ=0.1 eV, v_F=10^6 m/s, W=L=10 µm, t_{ox}=20 nm at T=295 K. The corresponding Γ (bottom) compares the asymmetry of the forward diode Υ_{max} with the asymmetry of the reverse diode $1/\Upsilon_{min}$.

5.5. Impact of the oxide thickness

The effect reported in this work relies essentially on the distribution of the electrostatic potential applied at each contact between the quantum capacitance (energy stored as Fermi level displacement) and the oxide capacitance (energy stored as electric field). As the oxide capacitance is inversely proportional to the value of the oxide thickness t_{ox}, changing this value should therefore affect the observed asymmetry Υ.

For thin oxide thicknesses, smaller V_{BS} (and V_{BD}) values are required to induce the same change in channel resistance (see Supplementary Material Fig. S19 for t_{ox}=20 nm, 90 nm and 300 nm). Therefore, a higher variation in channel conductivity will be observed with decreasing oxide thickness for a fixed $|V_{DS}|$ value. Consequently, the asymmetry is expected to increase as has been confirmed by the simulations shown in Fig. 13.

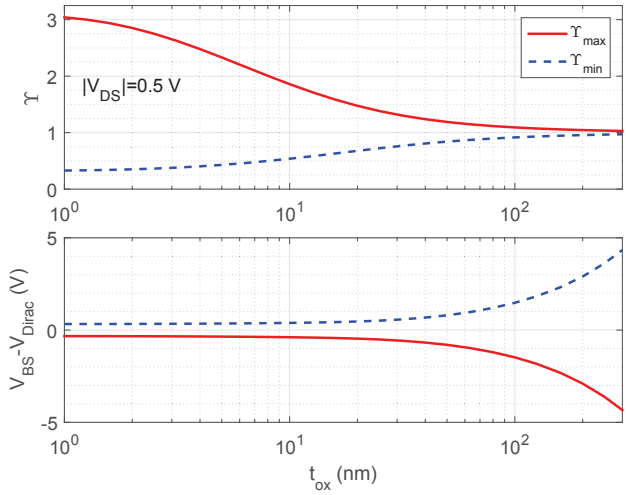

Figure 13: Simulated maximum and minimum values of Υ (top) and the corresponding V_{BS} (bottom) as a function of oxide thickness t_{ox} for $|V_{DS}| = 0.5\,V$ in devices with μ_n=μ_p=1000 cm^2/Vs, Δ=0.1 eV, v_F=10^6 m/s and W=L=10 µm at T=295 K.

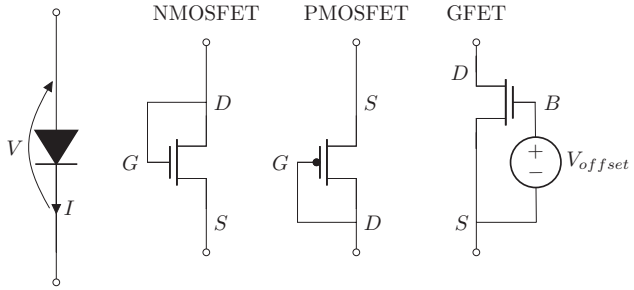

Figure 14: From left to right: diode symbol with its dipole conventions, conventional n-type and p-type diode-connected MOSFETs (with top gate G, source S and drain D contacts) and diode-connected GFET with a V_{BS} source to electrostatically dope the channel.

5.6. Diode-connected GFETs

445 In standard CMOS technologies, a diode can be obtained by connecting the drain and gate contacts ($V_{GD} = 0$) of either the NMOSFET or the PMOSFET transistor as shown in Fig. 14. Due to the symmetric ambipolar transport properties of pristine graphene, a diode-connected GFET could be obtained by indifferently connecting either the drain or the source contact directly to

the gate ($V_{BD} = 0$ or $V_{BS} = 0$, respectively). However, if the graphene is perfectly undoped ($Q_f = 0$) and at flatband conditions ($\phi_m - \phi_g = 0$) then $V_{Dirac} = \phi_m - \phi_g - \frac{Q_f}{C_i} = 0$ and the diode-connected GFET should have no asymmetric behavior ($\Upsilon = 1$) and thus no rectification capabilities. This follows from our previous results and discussion, since the diode-connected GFET simply corresponds to the case where $V_{BS} = 0$ (connecting the gate to the source) and no asymmetry is reported at the DNP ($V_{BS} - V_{Dirac} = 0$).

To enable a diode-connected GFET ($V_{BS} = 0$) to exhibit rectification capabilities using the quantum-capacitance diode effect reported here, the channel should not be at the DNP when the diode is unbiased ($V = 0$). If the graphene channel is doped ($V_{Dirac} \neq 0$) due to the fabrication process or ambient conditions, as is the case for our devices, then for $V_{BS} = 0$ we automatically have $V_{BS} - V_{Dirac} \neq 0$, and thus $\Upsilon \neq 1$ as seen in Fig. 11. In this case, our measurement and simulation results indicate that if V_{Dirac} could be controlled, for rectification purposes it should not be too large since Υ is maximized (or minimized) close to the DNP. Another solution is to electrostatically dope the channel, by applying a fixed $V_{BS} = V_{offset}$ bias as in Fig. 14. Due the reversible polarity effect, this will also allow to choose and change the polarity of the diode-connected GFET independently on the chosen connection scheme (gate connected through the voltage source V_{offset} to drain or to source). This offset voltage could be used to compensate any undesired value of V_{Dirac} and adjust the properties of the diode.

6. Conclusion

In summary, we have demonstrated with a methodology similar to ref. [7] that a weak diode behavior exists in rectangular common-gated graphene FETs. This asymmetric nonlinear effect was observed both at 77 K and 295 K and is accurately modeled and simulated using a simple drift-diffusion model for carrier transport in graphene. We have shown that this effect originates from the asymmetric change in graphene conductivity induced by symmetric variations

of the drain-gate voltage. This effect is highly dependent on the oxide thickness separating the graphene from the gate terminal. Indeed, the oxide capacitance should be maximized compared with the quantum capacitance to enhance the observed transport asymmetry. We have also shown that this transport asymmetry can be affected and enhanced by a difference in mobility values for electrons and holes. The symmetry in the reversible polarity feature of the GFET was indeed shown to be broken ($\Gamma \neq 1$) when $\mu_n \neq \mu_p$. The conventional figures of merit of rectenna diodes have been evaluated and we report asymmetries Υ up to 1.85 (for $|V_{DS}| = 2$ V) and maximum responsivities at zero bias of $\Re = 0.419\,A/W$ at 77 K and $\Re = 0.558\,A/W$ at 295 K. Nonlinearity values $\mathcal{F}_{NL}$ near zero bias are very close to unity and vary between 0.5 and 1.5 in the measured range.

The figures of merit reported in this work for the quantum-capacitance diode effect in GFETs are comparable with those reported for GFETs with a modified channel geometry and ballistic rectification (i.e. geometric diodes). The asymmetry values Υ obtained are overall in the same range of values or even equal: at room temperature and for $|V_{DS}| = 0.5$ V in Fig. 10 we report higher asymmetry values of $\Upsilon_{max} = 1.28$ compared with $\Upsilon_{max} = 1.15$ in ref. [7]. However, the geometric diode results were obtained on a 90-nm oxide instead of the 20-nm oxide used here. Hence, for the realistic parameters chosen in the simulations of Fig. 13 and assuming $\mu_p = \mu_n$, we obtain the same maximum value $\Upsilon_{max} \approx 1.15$ at $t_{ox} = 90$ nm for $|V_{DS}| = 0.5$ V. The responsivity values reported in the present work are also comparable with the adjusted $\Re = 0.22 - 0.24\,A/W$ values reported for the geometric diode in refs. [7, 6] (the figure of merit definition is adjusted for a $\frac{1}{2}$ pre-factor). Hence, all figures of merit reported in this work for the quantum-capacitance diode effect are comparable with those reported in current literature for the geometric diode ballistic effect. However, for similar figures of merit the GFET with a simple rectangular channel compares very favorably with the graphene geometric diode as the fabrication does not require nano-scale patterning of a high-quality graphene channel with ballistic transport properties to enable rectification.

The quantum-capacitance diode effect reported in this work could also play a role in other proposed rectifying graphene devices such as the graphene self-switching diodes [34, 35]. It has also a direct impact on the performance of diode-connected GFETs, as we have shown that these devices rely on this effect to exhibit asymmetric transport properties. Assuming no effect due to the contacts, the rectification capabilities of diode-connected GFETs have been shown to depend solely on the doping level of the channel and work function difference with the back gate. Hence, their rectification properties could be adjusted by either controlling this doping or applying an offset voltage between the diode-connected contacts of the GFET.

Further research is needed to assess the impact of contact resistances and contact doping, and to assess whether for example using metals with different work functions might result in a higher asymmetry. Although the asymmetry reported here is rather weak, the quantum-capacitance diode effect should however still be taken into account in graphene interconnect considerations as well as circuit designs using graphene FETs.

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