Contribution of Substrate Harmonic Distortion to GaN-on-Si RF Switches Linearity

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***Abstract*— We demonstrate high linearity of fully processed GaN on 2 mm HR Si wafers with high effective resistivity (ρ_{eff} > 2 kΩ.cm). Using two common-gate (MOS-)HEMT devices presenting different levels of distortion as demonstrators, we discuss the impact of substrate-induced harmonic distortion on RF switches. By comparing switch and CPW line measurements, it is possible to estimate the substrate contribution to HD. For the relatively non-linear device, the intrinsic device non-linearities dominate by a 16-20 dB margin over the substrate contribution. For a more linear device (-110 dBc of 2nd harmonic power at 900 MHz and P_{in} = 15 dBm), the substrate distortion contributes equally to channel non-linearity, highlighting the necessity of engineering the substrate's RF performance together with the transistor. We provide guidelines for substrate ρ_{eff} to achieve good switch linearity for given device harmonic levels.**

***Index Terms*— GaN-on-Si HEMTs, RF switches, substrate effective resistivity, RF losses, harmonic distortion.**

I. Introduction

GaN-on-Si promises to combine the high power handling capabilities of GaN HEMTs with mature CMOS process technology to enable RF front-end-modules (FEM) with high performance and complexity compared with GaN on small area substrates such as SiC [1], [2]. However, the lossy Si substrate can degrade performance of the devices and the passive components' quality factor [3], [4], and cause increased harmonic distortion (HD). In addition to passive structures, a particularly substrate-sensitive component of the FEM is the RF switch, where high linearity and low insertion loss are key [5]. RF losses are a problem for GaN-on-high resistivity (HR) Si technology, where the RF losses and non-linearities originate from a parasitic surface conduction (PSC) layer, located at nitride-Si interface [6]–[8]. This PSC layer leads to a significant decrease of the substrate effective resistivity, ρ_{eff} compared with the starting Si substrate resistivity ρ_{Si}. While the impact of GaN-on-Si stack on transmission line RF loss and non-linearity has been investigated [6]–[11], studies on active devices and circuits are lacking.

The work of Pieter Cardinael was supported by the Fonds pour la Formation à la Recherche dans l'Industrie et dans l'Agriculture (FRIA), FNRS, Belgium *(Corresponding author: Pieter Cardinael)*.

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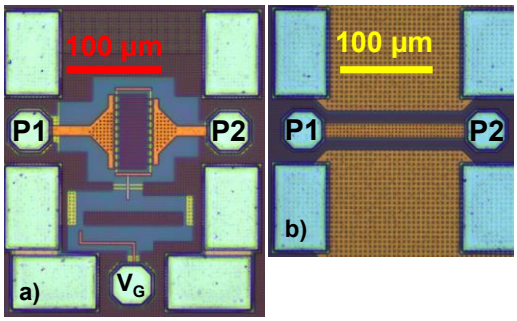

Fig. 1. (a) Optical micrograph of the SPST RF switch reported here, with L_g = 150 nm and W_{tot} = 0.5 mm. (b) A 150-µm-long CPW line of similar dimensions to the switch access lines (Thru line) is used to analyze the relative contribution of the substrate to non-linearities. Port 1 (P1), Port 2 (P2) and DC gate bias pad (V_G) are indicated where applicable.

In this letter, we present small- and large-signal performance of GaN HEMT switches integrated on 200 mm HR Si substrates. Our main objective is to quantify the contribution of the non-linear Si substrate to RF switch non-linearity. We do this by comparing the large-signal measurements of switches with CPW lines of similar dimensions. Two different devices are tested on state-of-the-art low-loss GaN-on-Si substrates. Finally, we translate the experimental data into a substrate engineering specification, in terms of the more commonly used ρ_{eff}.

II. Devices under Test

A. Material Stack and RF Switches

The HEMT stacks considered here were grown using metal organic chemical vapor deposition (MOCVD) on 200 mm, HR-Si wafers (3-6 kΩ.cm). They consist of an AlN nucleation layer, a strain relief III-N superlattice buffer, a C-doped GaN buffer layer, and finally a 50 nm-thick GaN channel. Two wafers with different device architectures are chosen because of their different intrinsic linearity (see Section IV).

Device A. HEMTs comprising 1 nm AlN spacer and 5 nm AlGaN barrier. Equivalent oxide thickness (EOT) is 4.0 nm.

Device B. MOS-HEMTs with 1 nm AlN spacer and 2 nm AlGaN barrier. A 2.5 nm high-K dielectric layer is used as gate oxide. EOT is 2.4 nm

A 3-layer Cu BEOL is used in both wafers. The devices under test have a gate length L_g = 150 nm. An SPST switch with a ~113 kΩ bias resistor at the gate terminal is shown in Fig. 1a. Switches were embedded in GSG pads using a ~10 µm-wide access line, with a total pad-to-pad distance of ~145 µm.

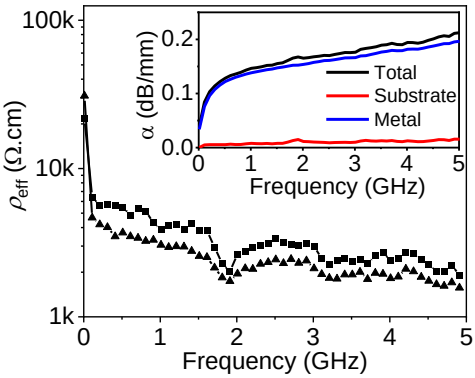

Fig. 2. Effective resistivity [12] higher than 2 kΩ.cm until 5 GHz extracted for a typical die on wafers A (squares) and B (triangles). Inset: series metallic losses are dominating over substrate losses. CPW line cross-section: central conductor width W = 15 µm, pitch S = 12 µm.

B. Substrate HD Evaluation From CPW Lines

The HD measured at the output of the switch is contributed by (i) the intrinsic device and (ii) the substrate-induced non-linearities. It is assumed these contributions add up, as the effect of interference is at most 3 dB. Substrate HD is measured using CPW lines [6], [10], [13]. A fundamental tone is injected at the CPW line input, and the 2nd (H2) and 3rd (H3) harmonic power are measured at the output. Two different CPW lines were fabricated on both wafers:

1. A 2 mm-long CPW line, with pitch S ≅ 12 µm and central conductor width W ≅ 15 µm. Dimensions were chosen to fairly compare it with other RF substrate technologies in terms of HD and ρ_{eff} [14], [15].
2. A 150 µm-long Thru line (Fig. 1b), with same S and W as the 2 mm-long CPW line.

The layout of the Thru line is similar to the switch access line (Fig. 1). It is then possible to use it to isolate the substrate contribution to switch HD from intrinsic device non-linearities, assuming substrate HD is captured by the Thru line measurement.

To evaluate substrate losses, the substrate ρ_{eff}, extracted for the 2 mm-long CPW line, is shown in Fig. 2 for a representative die. Wafer-wide median ρ_{eff} averaged over the frequency range 0.9 GHz - 5 GHz are reported in Table I. These high ρ_{eff} (> 2 kΩ.cm) mean that total RF losses are dominated by series metallic losses over shunt substrate losses [16], as shown in the inset of Fig. 2. This is the case for both wafers.

III. DC and Small-Signal Performance of RF Switches

Fig. 3a shows typical DC characteristics for devices A and B. The high-K dielectric introduced as gate oxide in Device B enables a substantial reduction of gate current (I_g) for these scaled barried devices. The R_{ON}, extracted from RF small-signal measurements is shown as a function of DC gate bias, V_G in Fig. 3b. Device B shows a ~38 % lower R_{ON} compared to the device A, owing to its smaller EOT. For both device architectures R_{ON} is relatively independent of V_G in high gate-overdrive regime (V_G > 1 V), which could be linked to high I_g (see also Section IV).

The insertion loss and isolation were extracted from small-signal RF measurements (Fig. 4). Insertion loss is ~-0.2 dB at 5 GHz and remains below 0.6 dB for both switches until 30

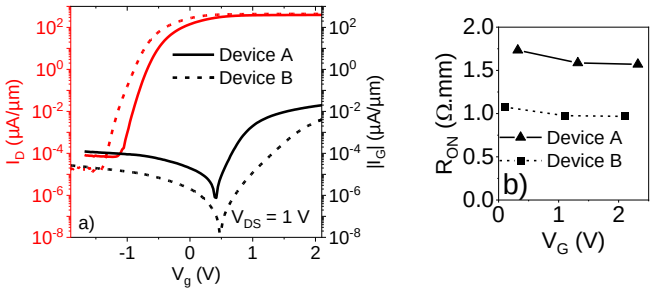

Fig. 3. (a) Addition of a gate oxide in Device B leads to one order of magnitude lower gate leakage. (b) R_{ON} as function of gate bias with a lower value for the Device B due to smaller EOT as compared to Device A. L_g~150 nm

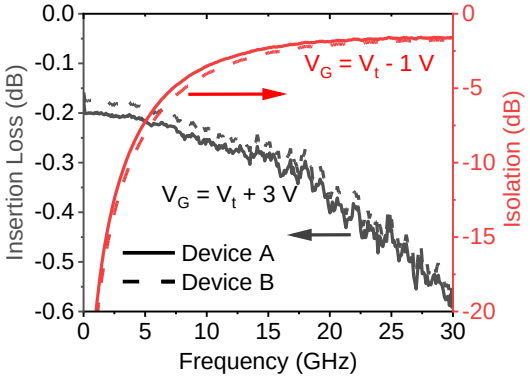

Fig. 4. Insertion loss (at V_G = V_t + 3 V) and isolation (at V_G = V_t – 1 V) for the two device architectures with L_g = 150 nm.

GHz. This is in line with the state-of-the-art in GaN switches [17]–[19]. Both device architectures show similar insertion losses although a slight improvement is achieved for device B thanks to its lower R_{ON}.

The off-state capacitances and corresponding R_{ON}×C_{OFF} figures-of-merit are reported in Table I. While device architecture and switch layout need to be optimized to further reduce R_{ON}×C_{OFF}, these switches provide a relevant framework to study the impact of substrate non-linearity on overall HD.

IV. Large-Signal Performance at 0.9 GHz

In this section, single tone HD data are reported at fundamental frequency of 0.9 GHz, which is a widely used frequency to quantify and benchmark substrate non-linearity [6], [14]. The dc gate bias was set to V_t + 3 V. A description of the experimental setup can be found in [6].

H2 and H3 are measured at the DUT output and plotted in Fig. 5 against the fundamental (H1) to remove the impact of insertion losses. H2 is discussed in more details since it usually dominates total harmonic distortion (THD) for CPW lines and thus represents most of the substrate contribution for switch non-linearity.

For the 2-mm-long CPW line, an H2 level of -84 dBm and -87 dBm at 15dBm of H1 is measured for wafers A and B, respectively (not shown, see Table I), which is on par with commercially available trap- rich (TR) SOI substrates [20] and further proves the potential of an optimized GaN-on-Si stack for RF switches (see also Fig. 6). Next, a Thru line and switch in on-state are compared (Fig. 5a). It is important to compare

TABLE I. MAIN ELECTRICAL RESULTS OF THE TWO WAFERS CONSIDERED HERE. H2 VALUES ARE GIVEN AT 0.9 GHZ FOR H1 = 15 DBM

Device label	Median ρ_{eff} (kΩ.cm)	R_{ON} (Ω.mm)	C_{OFF} (fF/mm)	$R_{ON} \times C_{OFF}$ (fs)	IL (dB)	H2 – Switch (dBm)	H2 – Thru (dBm)	H2 – 2 mm CPW (dBm)
A	2.7	1.47	286	420	0.22	-75	-91	-84
B	2.3	0.97	320	310	0.19	-95	-94	-87

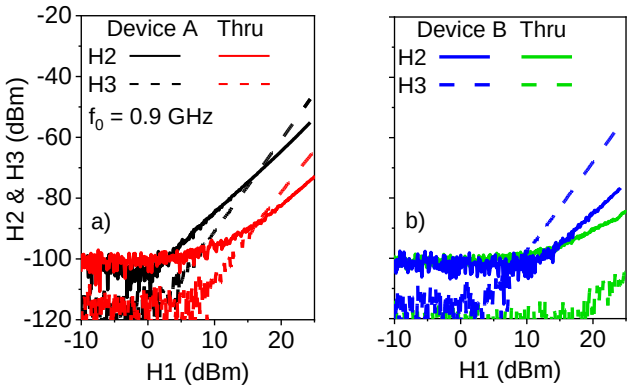

Fig. 5. Large-signal performance of the switch with Device A (a) and Device B (b) in on-state ($V_G = V_t + 3$ V) with L_g = 150 nm, compared with the Thru line on each wafer. 2-mm-long CPW data is reported in Table 1 for both wafers.

the switch with a CPW line of similar dimensions, as substrate-induced HD is strongly dependent on line length (~7 dB difference between 2 mm-long CPW and Thru line, see Table I).

For Device A, H2 ~ -90 dBc, which lies above the Thru line H2 by 16-20 dB at H1 levels of 15-20 dBm. This implies that for such a highly linear III-N/Si stack, switch non-linearities are dominated by the channel by a 16-20 dB margin. The same analysis can be made for H3.

Device B is significantly more linear than Device A (Fig. 5b): H2 is ~ -110 dBc, a ~19 dB reduction compared with Device A. We speculate that this is mostly due to the larger I_g (and thus lower intrinsic V_G) in Device A, although gate dielectric is known to also affect linearity [21]. As V_G is increased, a significant voltage drop can occur on the gate series resistor for the relatively leaky device A (Fig. 3a). This limits the on-state to $V_{G,max}$ = ~ V_t + 1.7 V, which increases intrinsic device distortion compared with higher intrinsic V_G allowed by lower I_g in Device B. For Device B, H2 levels for the Thru line and the switch are very similar (Fig. 5b), implying that for a more linear device, substrate contribution to distortion can be high.

V. EFFECTIVE RESISTIVITY SPECIFICATION FOR GAN-ON-SI RF SWITCHES

A. *Correlation of CPW ρ_{eff} with HD at 0 V DC bias*

Advanced GaN-on-Si substrates are reaching performance comparable to trap-rich SOI substrates (Fig. 6). In addition, H2 power (measured on a 2-mm-long CPW line at f_0 = 0.9 GHz) and ρ_{eff} are strongly correlated. Indeed, by increasing ρ_{eff} the conductivity of the PSC layer (G_{PSC}) is reduced. Furthermore, the relaxation time of free carriers constituting the PSC layer is increased, which increases linearity due to reduced modulation of G_{PSC} [22]. For a variety of fully processed (i.e., device processing and BEOL) GaN-on-Si stacks, an increase of ρ_{eff} by 10× leads to a reduction of H2 levels by ~36dB.

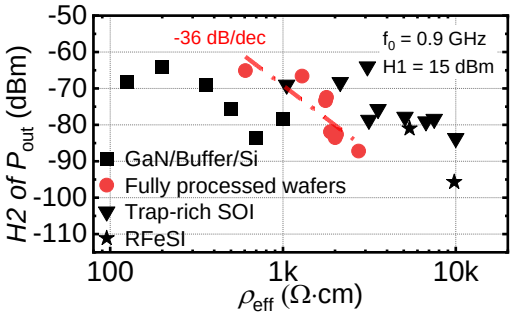

Fig. 6. Correlation between GaN-on-Si effective resistivity and H2 levels measured on 2 mm-long CPW lines at a fundamental tone of 0.9 GHz.

B. *Limiting Substrate Contribution to Switch Distortion*

The switch non-linearity is dominated by device non-linearity if the following is true:

$$H2_{Thru\ Line} \leq H2_{RF\ Switch}. \quad (1)$$

This condition holds for Wafer A, where we have (at H1 = 15 dBm):

$$H2_{Thru\ Line\ A,dBm} = H2_{RF\ Switch\ A,dBm} - 16\ \text{dB} \quad (2)$$

Equation 3 implies that the substrate for Wafer A would need to generate ~16 dB more distortion until it would contribute significantly to the switch distortion.

To obtain an estimate of the corresponding ρ_{eff} decrease, consider the 2-mm-long CPW line on Wafer A. This line showed H2 = -84 dBm (see Table I). From Fig. 6 and small-signal data in Fig. 2, the corresponding ρ_{eff} is ~2 kΩ.cm. Following the ~36 dB/dec trend line, a 16 dB increased H2 would represent a ρ_{eff} of ~700 Ω.cm. For device A , this corresponds to the lowest possible ρ_{eff} for which Eq. 1 is still respected.

It is noted that this lower bound is specific to a particular device performance, requiring a co-optimization of substrate and device linearity. Indeed, for the significantly more linear switch with Device B, this ρ_{eff} requirement is higher: at 0.9 GHz we have $H2_{Thru\ line\ B} \approx H2_{RF\ Switch\ B}$, making the above exercise impractical. However, it is likely less relevant provided that $H2_{RF\ Switch\ B}$ is as low as -110 dB, a level comparable with state-of-the-art commercially available products [23].

VI. CONCLUSION

In this letter, we have demonstrated the high linearity of GaN switches integrated on high resistivity Si wafers. The low distortion of those GaN-on-Si stacks (~-100 dBc at 0.9 GHz and P_{in} = 15 dBm, comparable to state-of-the-art SOI wafers) was shown to be necessary to enable low H2 levels (-110 dBc) for Device B switches. By comparing measurements of a CPW line of similar layout with RF switch data, we proposed guidelines for substrate ρ_{eff} requirements. For a HEMT switch, that requirement was shown to be equivalent to a minimum substrate effective resistivity of ~700 Ω.cm.

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