Substrate effects in GaN-on-Si HEMT technology for RF FEM applications

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Abstract: GaN-on-Si HEMTs are emerging as a viable candidate for front-end-of-module (FEM) implementation in 5G and beyond user equipment and small-cell applications [1][2]. This is because GaN HEMTs based power amplifiers and switches have high power handling capability as well as excellent switch figure-of-merit ($R_{on} \times C_{off}$). The integration of GaN HEMTs on silicon substrates not only can benefit from standard CMOS back-end-of-the-line processing but also wafer-level integration with Si-CMOS [1][3]. Such co-integration can enable hybrid circuitry with complex functionality and better performance than the standalone counterparts. An example can be a hybrid beamformer where GaN HEMTs can enable much smaller antenna array. For 5G wireless applications, this implies an energy efficient and compact system as compared to standalone Si-CMOS technologies. However, for both amplifiers and switches, GaN-on-Si HEMTs present thermal management and substrate loss related issues. In this work, we study and model the impact of GaN HEMT integration on Si substrate on RF substrate losses and non-linearities. The growth of III-N buffer is the most significant factor in determining RF losses and harmonic distortion contribution from the substrate. High temperature annealing and ion implantation steps encountered during HEMT processing can also degrade the substrate performance. In addition, we demonstrate a direct co-relation between substrate losses and harmonic distortion analogous to silicon-on-insulator technologies (Figure 1). However, the bias dependence of RF losses and harmonics show a strong time dependence (memory effects) and is more complex to model [11].

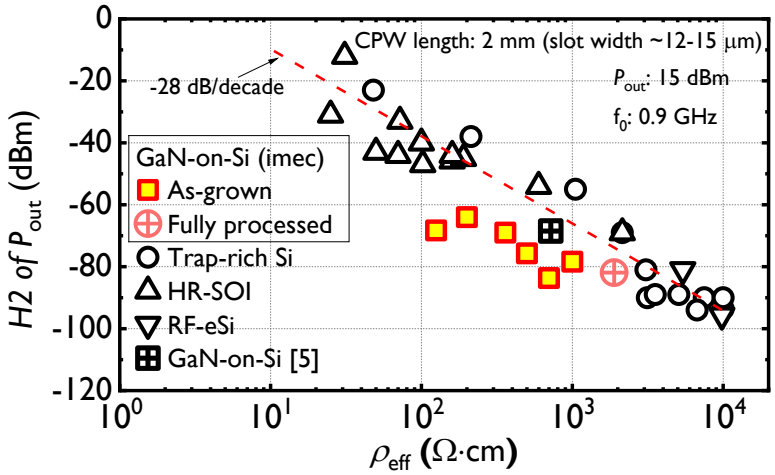

Figure 1. H2 vs ρ_{eff} for advanced HR-SOI technologies and GaN-on-Si technology at fundamental frequency of 0.9 GHz [6-10]. High resistivity SOI substrates follow a ~28 dB/decade change with ρ_{eff} [6]. For various GaN-on-Si substrates, distortion (at 0V DC bias) is co-related to the ρ_{eff}, but overall levers are lower than SOI samples probably due to a thicker buffer in GaN-on-Si samples. For comparison, distortion for a fully processed GaN-on-Si HEMT wafer is also shown.

References:

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