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Ultra-thin body and thin-BOX SOI CMOS technology analog figures of merit

V. Kilchytska [a,*], M.K. Md Arshad [a,b], S. Makovejev [c], S. Olsen [c], F. Andrieu [d], T. Poiroux [d], O. Faynot [d], J.-P. Raskin [a], D. Flandre [a]

[a] ICTEAM Institute, Université Catholique de Louvain, Louvain-la-Neuve, Belgium
[b] School of Microelectronic Engineering, University Malaysia Perlis, Kangar, Malaysia
[c] School of Electrical, Electronic and Computer Engineering, Newcastle University, Newcastle upon Tyne, UK
[d] CEA-Leti, MINATEC Campus, 17 rue des Martyrs, 38054 Grenoble Cedex 9, France

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ABSTRACT

In this paper, we analyze, for the first time to our best knowledge, the perspectives of ultra-thin body and ultra-thin BOX (UTBB) SOI CMOS technology for analog applications. We show that UTBB is a promising contender for analog applications, exhibiting high maximum transconductance, drive current, intrinsic gain and achievable cut-off frequencies in the range of 150–220 GHz. Effect of operation regime, substrate bias, channel width and high temperature (up to 250 °C) on analog figures-of-merit (FoM) are analyzed. Benchmarking of UTBB with other technologies (as planar FD SOI, different FinFETs, UTB with thick BOX) is presented.

1. Introduction

Ultra-thin body (UTB) fully-depleted (FD) Silicon-on-Insulator (SOI) MOSFETs are widely considered as one of the most promising candidates for ultimate device scaling requested by ITRS [1] thanks to their immunity to short channel effects (SCE) [2–11]. Furthermore, employment of ultra thin buried oxide (BOX) allows suppression of fringing electric fields through the BOX thus further improving SCE control, reducing drain induced barrier lowering (DIBL) and subthreshold slope [8–10,12]. Moreover, simulations predict a reduction of self-heating effects (SHE) in MOSFETs with thin BOX [13–15]. Additionally, ultra-thin BOX enables the use of back-gate control schemes [4,6]. Different back (or ground) planes (BP/GP) and substrate biasing were shown to provide a possibility of multi-threshold voltage (V_T) and dynamic-V_T option within the same process [4].

However, the drawback of ultra-thin BOX is enhanced coupling through the substrate. Such coupling may degrade both static behavior [8–10] and frequency response of these devices [15,16], which moreover depends on the substrate–BOX interface space charge conditions [8–10,15,16]. This gives additional motivation to the use of ground plane, which helps to suppress fringing fields through the substrate [12,15,18].

Electrostatics, scalability and variability issues in ultra-thin body and ultra-thin BOX (so called UTBB, or in some other references UTBOX, UT2B and UTB^2) MOSFETs as well as their perspectives for low power digital applications are widely discussed and shown to be excellent [2–10]. However, till now no attention has been paid to their analog figures of merit (FoM). To our best knowledge, there is only one study in this direction [11,19], which is, however, dedicated to UTB MOSFETs with thick BOX and focused mostly on RF figures, without deep analysis over the whole frequency range (starting from DC).

In this work we make a first assessment of UTBB technology for analog applications, paying particular attention to drive current, maximum transconductance, early voltage and intrinsic gain as well as their variations with substrate bias, channel width and in a temperature range up to 250 °C. We then benchmark UTBB with other devices and technologies such as FD SOI, UTB, and different FinFETs.

2. Experimental details

The devices are processed at CEA-Leti on UNIBOND (100) SOI wafers with 10-nm-thick BOX [6]. In the channel region, the Si body is thinned down to about 7 nm. Elevated source-drain structures are employed to reduce parasitic resistance. No channel doping and no ground plane underneath the BOX are used. The gate stack consists of HfSiON with EOT of 1.3 nm and TiN gate electrode. More process details can be found in [6]. The measured devices are n-channel MOSFETs with the gate length L from 30 nm to 10 μm and the channel width W from 80 nm to 10 μm.

Drain current vs. gate voltage I_d–V_g curves are recorded at different drain voltages, V_d, from linear to saturation regimes; I_d–V_d curves are measured at different gate voltages, V_g, in order to cover all possible future regimes of operation, i.e. weak, moderate and

* Corresponding author. Tel.: +32 (0) 10 472564; fax: +32 (0) 10 472598.
E-mail address: valeriya.kilchytska@uclouvain.be (V. Kilchytska).

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strong inversion. I_d–V_g and I_d–V_d curves of certain devices are measured at different substrate biases, V_{sub}, targeting assessment of analog FoM in the case of back-gate control schemes implications. Furthermore, certain devices are studied in a temperature range from room-temperature up to 250 °C. Assessment of device performance at high temperatures is important not only from the view point of their possible future application in high-temperature electronics, but is of great importance also due to SHE, which leads to the increase of the device temperature (especially strong in short-channel and SOI devices) under standard temperature operation conditions. Analog FoM are then extracted from I_d–V_g and I_d–V_d curves at different bias conditions and temperatures.

Multi-fingers devices are used and embedded in coplanar waveguide access pads for performing RF characterization. S-parameters are extracted using vector network analyzers (VNA) in the frequency range from 40 kHz to 110 GHz.

3. Electrostatic behavior

First, to give a brief insight on the electrostatic behavior of the studied devices, Fig. 1 presents I_d–V_g curves of a 30 nm-long n-channel UTBB MOSFET measured at different V_d. The inset to Fig. 1 gives the threshold voltage (V_T) variation (extracted in linear regime using G_m/I_d derivative method [20]) vs. L. It can be seen that difference of V_T between 10 μm- and 30 nm-long devices is 50 mV only; while DIBL, subthreshold slope S, off current, I_{off} and on-to-off current ratio, I_{on}/I_{off} for 30 nm-long device taken at $V_d = 1$ V are ~70 mV/V, ~75 mV/dec, ~180 pA/μm and $\sim 5 \times 10^6$, respectively. Thus, studied devices exhibit excellent SCE control and digital FoM. More detailed investigation of these features is, however, out of scope of this paper and can be found elsewhere [2,4,6].

4. Analog figures of merit

4.1. Methodology

Analog performance is assessed through analysis of device parameters such as: the gate transconductance, G_m, transconductance-over-drain current ratio, G_m/I_d, normalized drain current, $I_d/(W/L)$ taken at constant G_m/I_d of 10 and 5 V^{-1}, early voltage, $V_{EA} = I_d/G_d$ (where G_d is the output conductance), which clearly appear as FoM indicating the device efficiency to convert DC power into AC frequency and gain performance [21,22]. Intrinsic gain, A_v, is then calculated as $A_v = G_m/G_d = G_m/I_d \cdot V_{EA}$.

The use of V_{EA} helps removing the G_d dependence on the drain current which impedes fair comparison between different devices and bias points. Similarly, the G_m/I_d vs. normalized drain current $I_{d\ norm} = (I_d/(W/L))$ plot is a very convenient representation for comparing different devices thanks to its independence on V_T, as well as, to the 1st order, on L [21,22]. Moreover, being independent on V_T this approach allows a fair comparison at different V_{sub} and temperatures. As example, Fig. 2 shows G_m/I_d vs. $I_{d\ norm}$ curves of 30 nm-long device measured at different V_{sub}. It can be seen that G_m/I_d vs. $I_{d\ norm}$ curves, indeed, do not exhibit parallel shift vs. V_{sub}, i.e. do not reflect V_T vs. V_{sub} dependence (which is rather strong in UTBB devices, e.g. [8]), thus mostly highlighting modifications caused by variation of mobility, μ, and body factor, n with V_{sub} (Fig. 2). We then widely use $I_{d\ norm}$ taken at a fixed G_m/I_d to not only fairly assess performance of devices with different geometries and at different V_{sub} and temperatures, but as well as to benchmark devices originating from different processes or technologies.

It is worth to mention that neither "traditional" kink effect in I_d–V_d characteristics at high V_d nor gate-induced floating-body effect in G_m–V_g curves appear in studied devices even at a negative V_{sub} of −2 V.

4.2. $G_{m\ max}$, $I_{d\ norm}$, V_{EA}, A_v

Fig. 3 shows variation of maximum transconductance normalized to W/L, $G_{m\ max\ norm} = G_{m\ max}/(W/L)$, for devices with different lengths and widths. Typical degradation of $G_{m\ max\ norm}$ is observed for very short gate lengths (Fig. 3a), as a result of short channel effects and enhanced impact of series resistance with device shortening. It would be interesting to note an improvement in device performance with channel width narrowing (Fig. 3b): 80 nm-wide channels exhibit almost twice higher values of $G_{m\ max\ norm}$. To explain such improvement several hypotheses can be drawn. One of the main reasons is suggested to be trapezoidal- or even Ω-like channel shape of the devices reported in [5]. This results, firstly, in effective channel width, W_{eff}, higher than nominal channel width W, by twice Si film thickness, $2 \cdot T_{Si}$, or even more, i.e. $W_{eff} \geqslant W + 2 \cdot T_{Si}$ thus increasing performance per device (or per channel). Fig. 3b demonstrates how normalization to W_{eff} (instead of W) affects W-dependence of $G_{m\ max\ norm}$ allowing for better alignment of the values obtained in wide- and narrow-channel devices. Secondly, using an approach similar to that previously proposed for FinFETs [23], one can show that tri- or Ω-gate shape for our geometries provides 2–5% improved and width-dependent

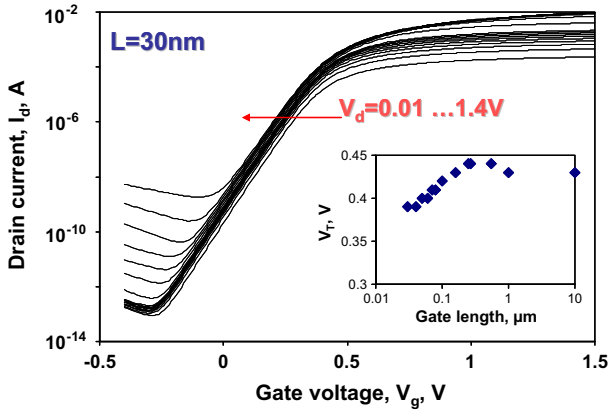

Fig. 1. I_d–V_g curves of 30 nm-long UTBB MOSFET measured at different V_d from 0.01 to 1.4 V. Inset gives linear V_T vs. L variation. W = 10 μm.

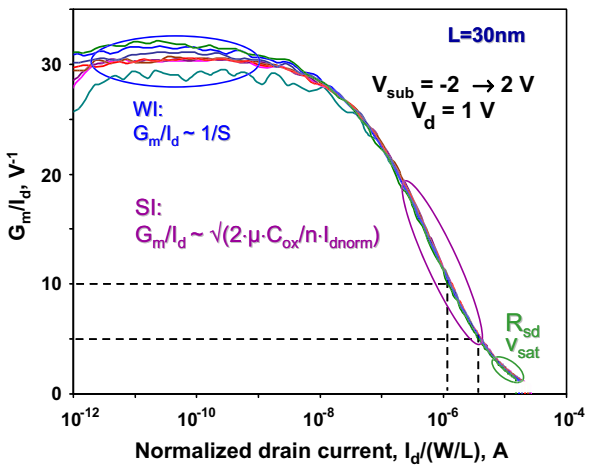

Fig. 2. G_m/I_d vs. $I_{d\ norm}$ curves for 30 nm-long UTBB device measured at different V_{sub} from −2 to 2 V (with 0.5 V step). $V_d = 1$ V. Dashed lines are drawn to schematically demonstrate $I_{d\ norm}$ taken at fixed $G_m/I_d = 10$ or 5 V^{-1} approach used in this paper. Equations yield first-order dependence on device parameters in different operation regimes (WI: weak inversion, SI: strong inversion) [21,22].

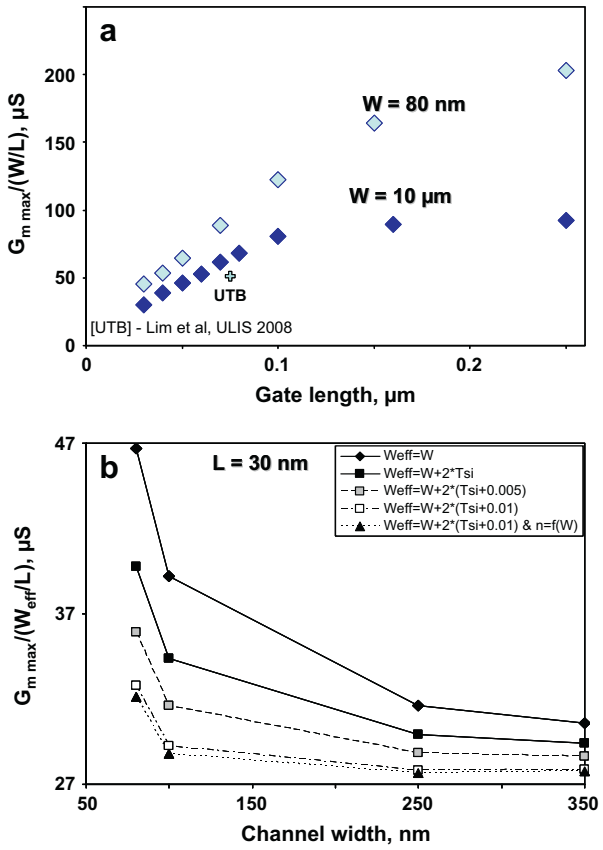

Fig. 3. $G_{m\ max\ norm}$ as a function of (a) L for UTBB devices with W of 80 nm and 10 µm (the cross indicates the value for UTB device [11,19]) and (b) W for 30 nm-long UTBB device, showing effect of normalization to different W_{eff} and $n(W)$ contribution. V_{sub} = 0 V.

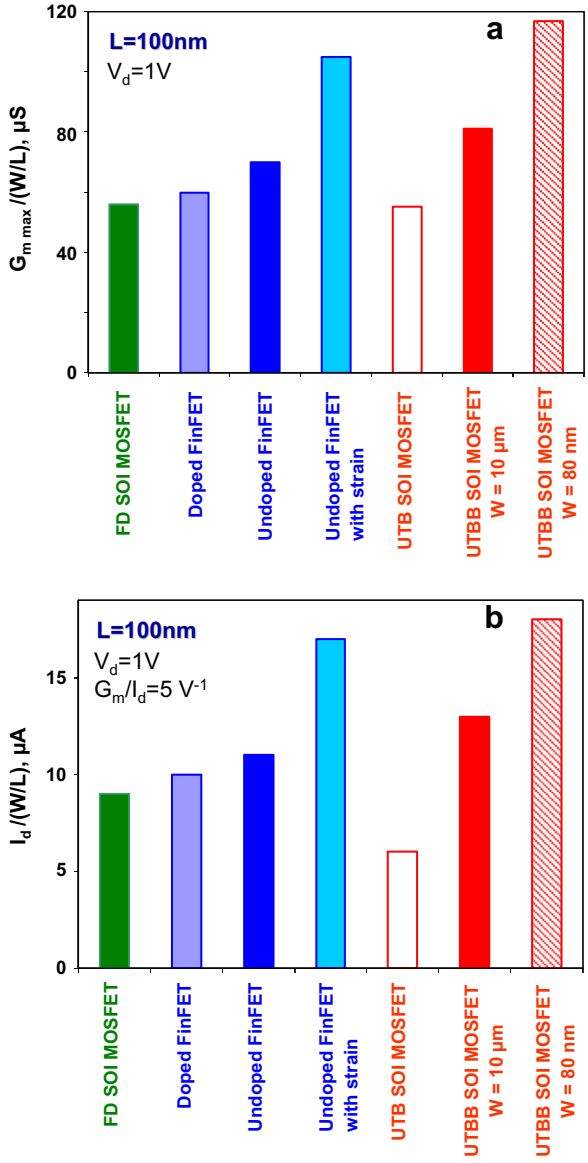

Fig. 4. (a) $G_{m\ max\ norm}$ and (b) $I_{d\ norm}$ taken at G_m/I_d = 5 V^{-1} for different devices and technologies. L = 100 nm (except L = 120 nm for FD SOI MOSFET and L = 70 nm for UTB MOSFET). V_d = 1 V. V_{sub} = 0 V.

body factor. Theoretical prediction is also confirmed experimentally by slightly (few %) lower S and DIBL in narrow-channel devices. Such body factor behavior can provide few additional percents of $G_{m\ max}$ improvement in narrowest channels (Fig. 3b). In addition, experimentally observed 10–20 mV lower V_T of 80 nm-wide devices and variation of series resistance with channel width can contribute to increased $G_{m\ max\ norm}$ in narrower devices. However, in-depth point-by-point analysis of above-mentioned reasons and their competitive effect is out of scope of this paper and will be discussed elsewhere.

Fig. 4 benchmarks $G_{m\ max\ norm}$ and $I_{d\ norm}$ taken at a G_m/I_d = 5 V^{-1} using the approach described above for different devices and technology generations. We consider:

- 0.12 µm-node planar FD SOI MOSFET with doped channel and HALOs [22,24,25].
- FinFETs with doped channel [26–29].
- Undoped FinFETs with and without "global biaxial" strain [30–32].
- UTB MOSFETs [11,19].
- UTBB MOSFETs described above with channel widths of 10 µm and 80 nm.

Table 1 summarizes major process details and V_T for the benchmarked processes.

All devices compared in Fig. 4 feature gate length of 100 nm, except UTB, for which literature gives results for L = 70 nm only [11,19] and doped FD SOI MOSFETs, for which the minimum/nominal gate length is 0.12 µm. Table 2, additionally, provides analog FoM for 30 nm-long channels for the deeply scaled down technologies.

- Firstly, one can see that UTBB MOSFETs exhibit higher values than planar doped FD SOI devices from 0.12 µm process. This is related to: (i) undoped channel in UTBB devices and hence higher expected mobility values; (ii) electrically thinner gate oxide and hence higher gate oxide capacitance, C_{gox}; (iii) thinner gate oxide combined with thinner Si film and thin BOX allowing for improved SCE and DIBL control [2,3]. Similarly, UTBB FoMs are higher than for doped FinFETs (featuring relatively "thick fin" and gate oxide) for the same reasons.
- Secondly, UTBB devices feature about the same performance in terms of $G_{m\ max\ norm}$ and $I_{d\ norm}$ as advanced undoped FinFETs and can in certain regimes even outperform them for both 100 nm and 30 nm-long devices. It can be seen that introduction of strain allows a strong improvement of FinFETs performance resulting in 15–25% higher values in strained FinFETs comparing to UTBB counterpart.

Table 1
Key parameters of compared MOSFETs.

Process/devices	Gate stack		Channel			BOX thickness (nm)	$V_{T\ \mathrm{lin}}$ (V)
	Material	EOT (nm)	T_{Si}, W_{fin} (nm)	Doping, N_A (cm^{-3})	Strain		
FD SOI MOSFET	Poly-Si/SiO_2	2.5	30	$\sim 7 \times 10^{17}$ + HALOs	No	200	~0.09
Doped FinFETs	Poly-Si/SiO_2	2	35	$(1–6) \times 10^{18}$	No	145	~0.12
Undoped FinFETs	Metal/HfSiON	1.5	25	Undoped	No	145	0.53
Strained FinFETs	Metal/HfSiON	1.5	25	Undoped	Global tensile	145	0.47
UTB MOSFETs	Metal/HfO_2	1.7	8	Undoped	No	145	~0.58
UTBB MOSFETs	Metal/HfSiON	1.3	7	Undoped	No	10	~0.4

Table 2
Analog FoM for different devices. V_d = 1 V. V_{sub} = 0 V.

	FinFET	Strained FinFET	UTBB W = 10 μm	UTBB W = 80 nm
L = 30 nm				
$G_{m\ \max\ norm}$, μS	31.5	42.3	30.4	45.5
$I_{d\ norm}$ at G_m/I_d = 10 V^{-1}, μA	1.2	1.3	1.74	2.3
$I_{d\ norm}$ at G_m/I_d = 5 V^{-1}, μA	5.1	6.4	5.4	7.2
V_{EA}, at ~V_T, V	1.2	1.5	3.4	5.5
V_{EA} at ~1 V, V	5.1	6	11	10
A_v (max), dB	33.5	34	36	38
L = 100 nm				
$G_{m\ \max\ norm}$, μS	70	105	81	122
$I_{d\ norm}$ at G_m/I_d = 10 V^{-1}, μA	3.1	4.7	4	6
$I_{d\ norm}$ at G_m/I_d = 5 V^{-1}, μA	10.8	16.6	13	20
V_{EA}, at ~V_T, V	4	5	8	15
V_{EA} at ~1 V, V	12	18	20	20
A_v (max), dB	40	43	46	51

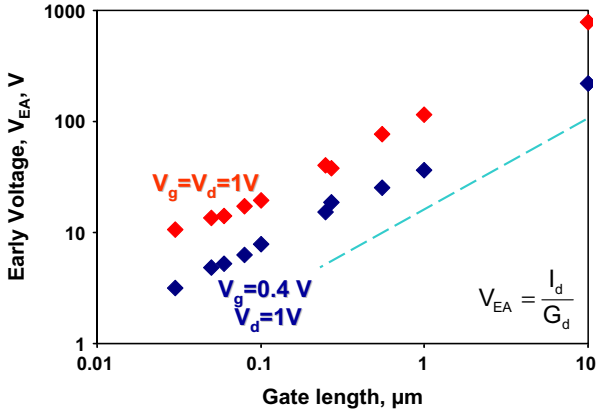

Fig. 5. V_{EA} as a function of L for UTBB MOSFETs taken at different bias conditions. W = 10 μm. Dashed line indicates typical values for FD SOI MOSFETs. V_{sub} = 0 V.

- Thirdly, UTBB figures are a bit higher than previously reported for UTB devices [11,19] (see also Fig. 3 for similar L) thanks to thinner gate oxide EOT, which provides higher C_{gox} and which, combined with thinner Si film and thin BOX, yields improved SCE and DIBL [2,3] control in UTBB devices.
- Fourthly, we can clearly see 25–35% performance improvement in UTBB with 80 nm-narrow channels comparing to 10 μm-wide counterpart. One of the most probable reasons, as discussed above, is related to trapezoidal- or Ω-like shape in narrow UTBB channels, providing effectively wider device and better body factor. Such enhancement allows narrow-channel UTBB devices to outperform all counterparts referred here in terms of $G_{m\ \max\ norm}$ and $I_{d\ norm}$.

Fig. 5 reports early voltages extracted for UTBB devices with different gate lengths and at different operation regimes. V_{EA} as high as ~800 V is achievable in long-channel UTBB devices. This is an extremely high value for planar FD SOI MOSFETs which typically exhibited V_{EA} of about 10 V per μm length only (shown by dashed line in Fig. 5). The UTBB values are close to those observed in long-channel FinFETs, for which $V_{EA} \geqslant 10^3$ V was recorded previously [27,29,33] thanks to the volume inversion regime of operation and improved control of channel from the gate. Indeed, UTBB MOSFETs (featuring 7 nm Si film thickness and undoped channel) also operates in volume inversion-like regime and exhibits good electrostatic control (proven by low S and DIBL values, see Fig. 1). Moreover, short UTBB devices can even provide higher V_{EA} than FinFETs with similar gate lengths (Table 1 and [27–29,33–35]) thanks to excellent SCE and DIBL control.

As a result, extremely high values of intrinsic gain, never reported previously for planar FD SOI MOSFETs, are recorded in UTBB devices. A_v of about 80 dB was achieved for 10 μm-long device, thus approaching the values previously demonstrated for long-channel FinFETs [27,29]. Fig. 6 benchmarks maximum achievable A_v for different processes and devices with about the same L of 100 nm. Table 2 completes with the numbers for 30 nm-long devices. We can see that short-channel UTBBs clearly outperform doped 0.12 μm FD SOI MOSFETs and doped FinFETs. Moreover, A_v in UTBBs can reach even a bit higher values than in short-channel undoped advanced FinFETs. A_v as high as 45–50 dB and 36–38 dB are achievable in 100 nm- and 30 nm-long UTBB devices, respectively. Furthermore, UTBB devices exhibit higher A_v than UTB ones, partially due to improved electrostatic control and reduced SCE in UTBB, and partially because the reported UTB values were extracted in GHz frequency range [11,19], where device performance is expected to degrade, as will be discussed hereafter.

Then, the A_v behavior as a function of applied V_g and V_d is analyzed (Fig. 7). There exists a trade-off between G_m/I_d decrease with V_g increase (Fig. 2), and V_{EA} increase with V_g increase due to improved gate control (Fig. 5). As a result, A_v maximizes in moderate inversion regime, when V_g = 0.4 V, i.e. at about V_T (Fig. 1), exhibiting a wide plateau vs. V_d in saturation, which is profitable for low voltage/low power applications.

Finally, Fig. 8 plots G_m/W as a function of A_v in different devices under the same bias conditions (V_d in saturation and $V_g = V_T + 0.6$ V). It would be worth to point out that this regime is not the most advantageous for UTBB devices, as is described above. Planar MOSFETs, FinFETs and optimized FinFETs data are taken from Ref. [36,37]. More details about "optimized FinFETs" process can be found in [38]. It is seen that UTBB devices provide both higher G_m/W and A_v than "planar" and non-optimized FinFETs. Comparing to the "optimized FinFETs", one can see that 10 μm-wide UTBB MOSFETs outperform them in terms of gain while they exhibit a bit lower G_m/W for the medium-length devices, keeping higher G_m/W for long and deeply scaled channels. Furthermore, in this graph one can see again that channel narrowing allows

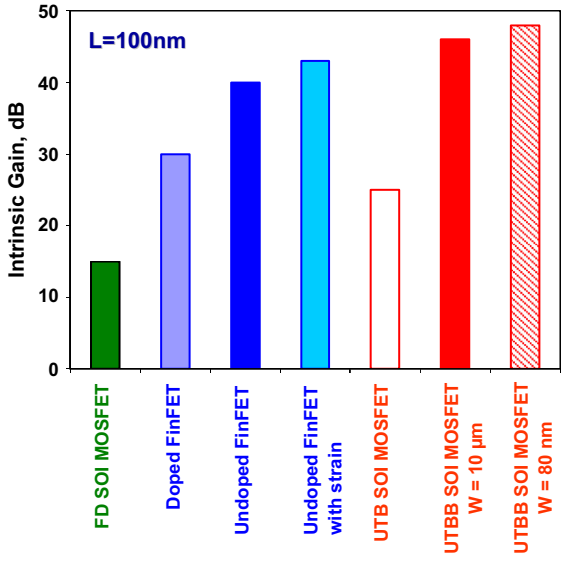

Fig. 6. Intrinsic gain achievable in different devices and technologies. L = 100 nm (except L = 120 nm for FD SOI MOSFET and = 70 nm for UTB MOSFET). V_{sub} = 0 V.

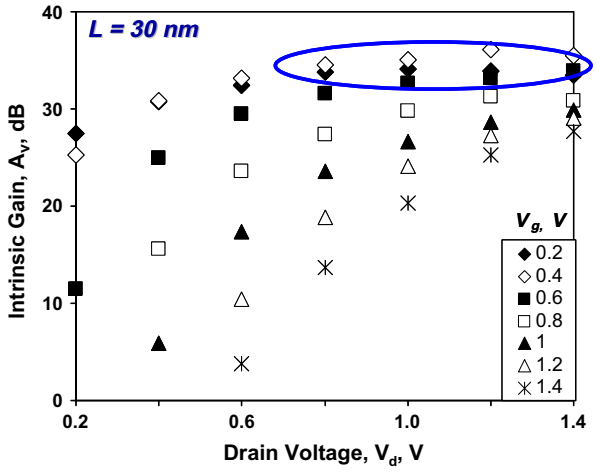

Fig. 7. A_v as a function of V_d with V_g as a parameter for UTBB MOSFET. L = 30 nm. W = 10 μm. V_{sub} = 0 V.

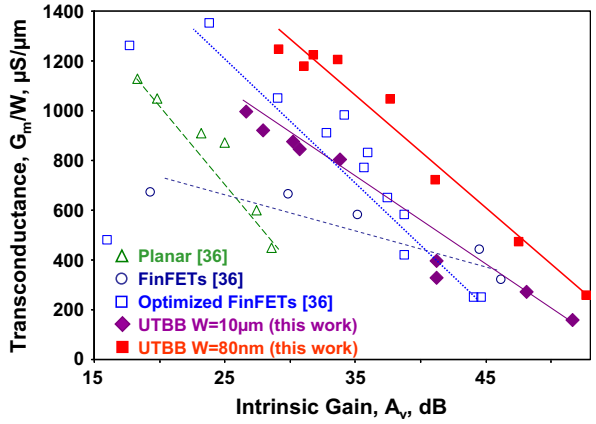

Fig. 8. G_m/W as a function of A_v for different devices and processes. V_d is in saturation (1 V in this work and 1.1 V in [36]). $V_g = V_T + 0.6$ V, V_{sub} = 0 V. L = 30–1 μm for UTBB. L = 45–1 μm for FinFETs. Lines indicate general trends.

further improvement of UTBB device performance. 80 nm-wide channel UTBB devices may offer at the same time higher A_v and higher G_m comparing to other referred devices, thus making UTBB a good contender for high-precision analog circuits.

4.3. Effect of substrate bias

Considering back-gate control schemes, we then analyze the effect of substrate bias on UTBB analog FoM. Effect of V_{sub} is twofold: on one hand, application of negative V_{sub} was demonstrated to result in improvement of both S and DIBL [8–10], especially for short channels; on another hand, application of positive V_{sub} decreases V_T and moves channel position to the bottom film interface featuring higher μ [39], both resulting in higher I_{on}. Therefore, we analyze below which effect dominates analog FoM. G_m/I_d vs. $I_d/(W/L)$ curve is a powerful tool for such analysis since being V_T independent, it allows for discarding effect of strong V_T vs. V_{sub} shift (as is discussed above, Fig. 2). $I_{d\ norm}$ taken at fixed G_m/I_d slightly increases (5–10%) when V_{sub} moves from negative to positive values (not shown here), which is most probably a sign of μ increase demonstrated in [39]. Contrarily, negative V_{sub} seems to be preferable for V_{EA} and G_m/I_d taken at fixed $V_g = V_d$. Indeed, one can see (Fig. 9a) that V_{EA} tends to slightly increase when V_{sub} is shifted to negative values in the low $V_g = V_d$ range, probably as a result of DIBL improvement when the channel moves towards the front gate oxide [9]. Furthermore, G_m/I_d increases strongly when V_{sub} moves to negative values (Fig. 9b) (stronger in the low $V_g = V_d$ range) due to V_g–V_T reduction. As a result, some ~5–10 dB improvement in the intrinsic gain can be expected for the device with negatively biased substrate (Fig. 9c).

4.4. Self-heating and substrate-related device performance degradation

When investigating analog FoM, one should care about SHE [40,41] and substrate-related effect [42–44], which may cause G_d and hence V_{EA} and A_v degradations with frequency. Thermal properties of the UTB devices were predicted to be degraded [14,45] due to interfaces proximity and hence stronger phonon boundary scattering [46]. However, BOX thinning is expected to facilitate heat dissipation [13–15], thus reducing SHE in UTBB devices (comparing to the devices with thick BOX). From another side, BOX thinning and L shortening was predicted [16,17,44] to result in strongly enhanced substrate-related G_d degradation, which appears due to substrate capacitance variation with frequency, when first minority (in a 1–100 Hz range) and then majority (in GHz range) carriers stop to follow AC signal, thus modifying the potential at substrate–BOX interface [42,43].

Fig. 10 presents G_d vs. frequency curves experimentally obtained with 100 nm-long UTBB MOSFET under different bias conditions. G_d is extracted from the measured S-parameters after S-to-Y parameters conversion, taking the real part of the Y_{dd} parameter. G_d vs. frequency curves clearly exhibit transitions due to both SHE (in MHz range) and substrate-related effect (in Hz-range, which can be assumed from the difference between G_d values at 40 kHz and at DC and in GHz-range). As a result, one can observe that G_d values taken at 4 GHz is much higher (3–8 times) than values extracted from DC measurements (indicated by triangles in Fig. 10). It is worth to point out that substrate-related G_d degradation can become as strong as (and even stronger than) SHE-related one (especially at lower V_g) in UTBB devices without ground plane, as was previously predicted in [16,17]. GP implementation is, however, expected to strongly reduce or even suppress the substrate-related degradation. More details about self-heating and substrate-related effects in UTBB SOI MOSFETs can be found in [47].

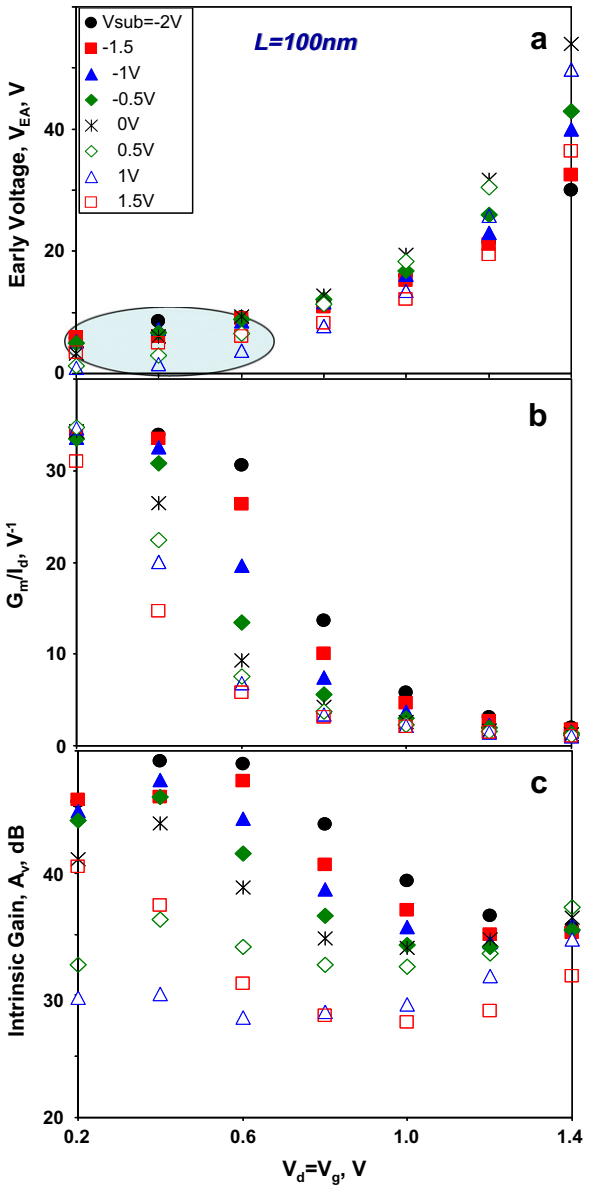

Fig. 9. (a) V_{EA}, (b) G_m/I_d and (c) A_v as a function of applied $V_g = V_d$ at different V_{sub} from −2 V to +2 V (with 0.5 V step) for UTBB MOSFET. L = 100 nm and W = 10 μm.

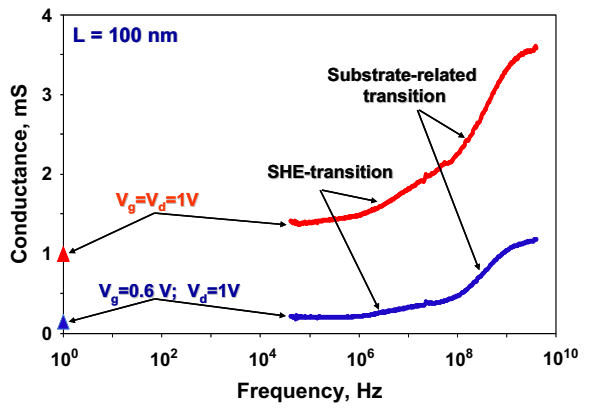

Fig. 10. Output conductance vs. frequency curves measured under different bias conditions in 100 nm-long UTBB MOSFETs. W = 1 μm, N_f = 30, V_{sub} = 0 V.

4.5. Cut-off frequency

Fig. 11 presents cut-off frequencies, f_T, for UTBB MOSFETs with different L and W. It is worth to point out that this process was not specially optimized for RF applications. Nevertheless, one can see that f_T as high as ~170 GHz and ~220 GHz are achievable in 50 nm- and 30 nm-long UTBB devices, respectively. These numbers are well higher than previously reported $f_T \sim 120$ GHz in 70 nm-long UTB MOSFET [11,19], but are in line with them, taking into account shorter L in UTBB devices studied here. Moreover, f_T of UTBB devices are a bit higher than those previously reported in FinFETs with similar L [28,36]. Nevertheless, these values are lower than (while close to) ITRS requirements and surely lower than the best reported f_T (>450 GHz for 30 nm-long PD SOI [48]). However, one should take into account that highest reported f_T numbers were obtained with the high-performance (HP) targeted process/designs. Contrarily, UTBB devices presented here are able to provide not only relatively high f_T but in the same time low V_T, excellent DIBL, I_{off} and I_{on}/I_{off} values, thus being very promising for the applications requesting low operation voltage (LOP) and/or low standby power (LSTP).

One can note that W dependence is opposite to that obtained from DC measurements (Fig. 3). This is related to the increased effect of parasitics (especially fringing capacitances) which appear with channel narrowing in multi-channels, multi-fingers devices (as requested for RF) [49]. Complete equivalent circuit extractions confirm this hypothesis, which is, however, out of scope of this paper.

4.6. Effect of temperature

Fig. 12 shows experimental I_d–V_g curves of 100 nm-long UTBB MOSFETs in the temperature range up to 250 °C. It is worth to point out that even though this process was not optimized for high-temperature applications, excellent high-temperature behavior is observed thanks to ultra-thin undoped body and well-controlled threshold voltage. I_{off} (250 °C) as low as 28 nA/μm and I_{on}/I_{off} (250 °C) higher than 2×10^4 at V_d = 1 V are observed. Moreover, minimum leakage current, observed at slightly negative V_g is a couple orders of magnitude lower than I_{off} at V_g = 0 V, thus keeping space for further improvement.

Extremely low V_T shift with temperature, $\Delta V_T/\Delta T$ = 0.6 mV/°C (similar to that previously reported for undoped FinFETs [50–52]) was observed. This is almost twice lower than the value which

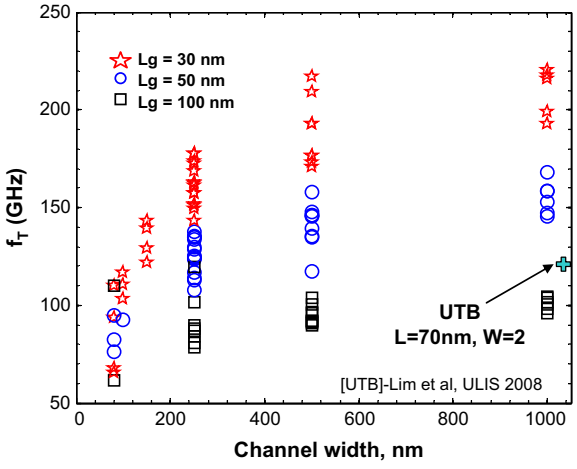

Fig. 11. f_T for UTBB devices with different widths and lengths. The cross shows the value previously reported [11] for UTB MOSFET with L = 70 nm, W = 2 μm, V_{sub} = 0 V.

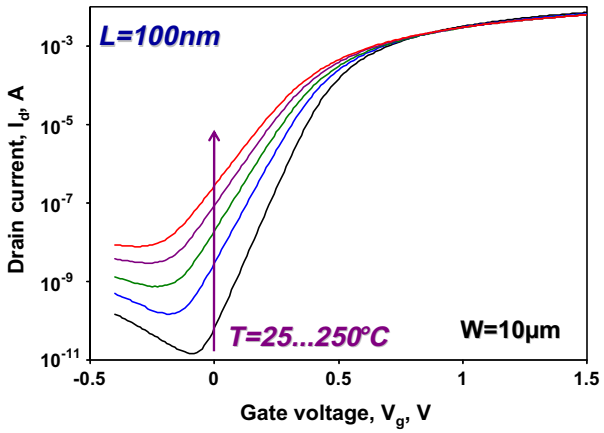

Fig. 12. Experimental I_d–V_g curves of 100 nm-long UTBB SOI MOSFETs at different temperatures. V_d = 20 mV, W = 10 μm, V_{sub} = 0 V.

would be obtained using classically considered V_T shift with temperature in FD SOI MOSFET [53] defined by variation of Fermi potential ($\Delta V_T/\Delta T = \Delta\phi_F/\Delta T$ = 1.2–1 mV/°C for $N_A = 10^{15}$–10^{16} cm^{-3}). Unrealistically high N_A of about 10^{18} cm^{-3} should be assumed to get so small V_T temperature shift using classical modeling approach [50]. The reason is that in ultra-thin undoped devices (as well as in FinFETs), which operate in quasi-volume inversion regime, surface potential at V_T differs significantly from $2\phi_F$ [54], and hence the above approach is no longer valid.

Furthermore, it is worth to point out excellent subthreshold slope behavior which keeps linear $S = n \cdot kT/q \cdot \ln(10)$ variation with temperature up to ~250 °C, which is a transition temperature higher than previously reported values (150–200 °C) for "thick film" FD SOI MOSFETs [55]. The main reasons are smaller degradation of gate-to-channel coupling and smaller deviation from exponential dependence of the inversion charge density on the surface potential with temperature increase in the case of Si film thinning. More details about UTB V_T and S temperature behavior can be found in [56].

Then, the analog FoM variation with temperature is analyzed. Fig. 13 shows $G_{m\ max\ norm}$ (a) and $I_{d\ norm}$ (b) as a function of temperature for UTBB devices with different L and operating under different bias conditions. As described above, $I_{d\ norm}$ values extracted at fixed G_m/I_d are free from the effect of V_T shift with temperature and represent effect of mobility, series resistance and body factor only. It can be seen that degradation of both $I_{d\ norm}$ and $G_{m\ max\ norm}$ over the 200 °C range is limited to 15–30%, which is smaller than could be expected from the phonon mobility degradation (i.e. $\mu \sim T^{-\alpha}$ with α = 1.5–1.8 [57]) previously widely considered as the main factor of G_m and I_d decrease with temperature. Moreover, it is revealed that both $G_{m\ max\ norm}$ and $I_{d\ norm}$ degradations are reduced in the case of higher V_d, shorter L and higher gate voltage overdrive

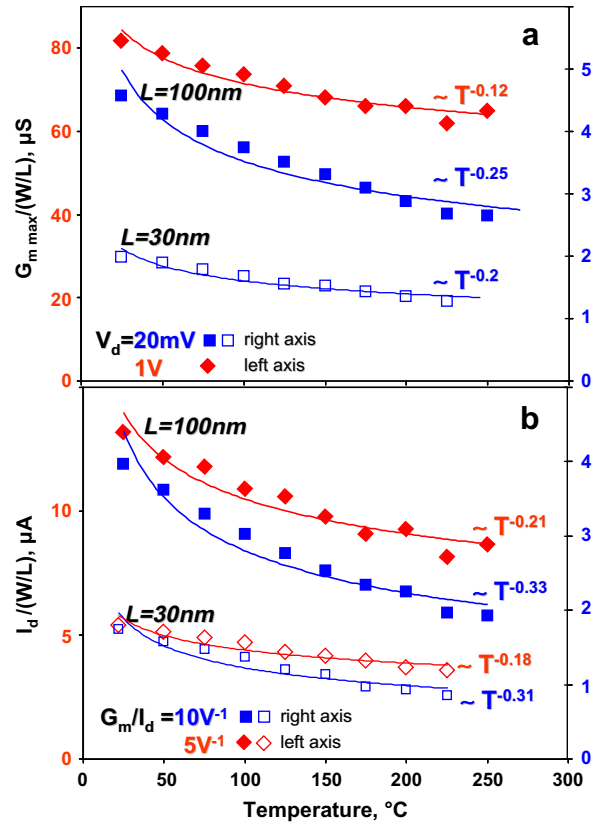

Fig. 13. (a) $G_{m\ max\ norm}$ and (b) $I_{d\ norm}$ as a function of temperature (symbols) for UTBB devices with different L and under different bias conditions. Lines give trends expected from power laws. V_{sub} = 0 V.

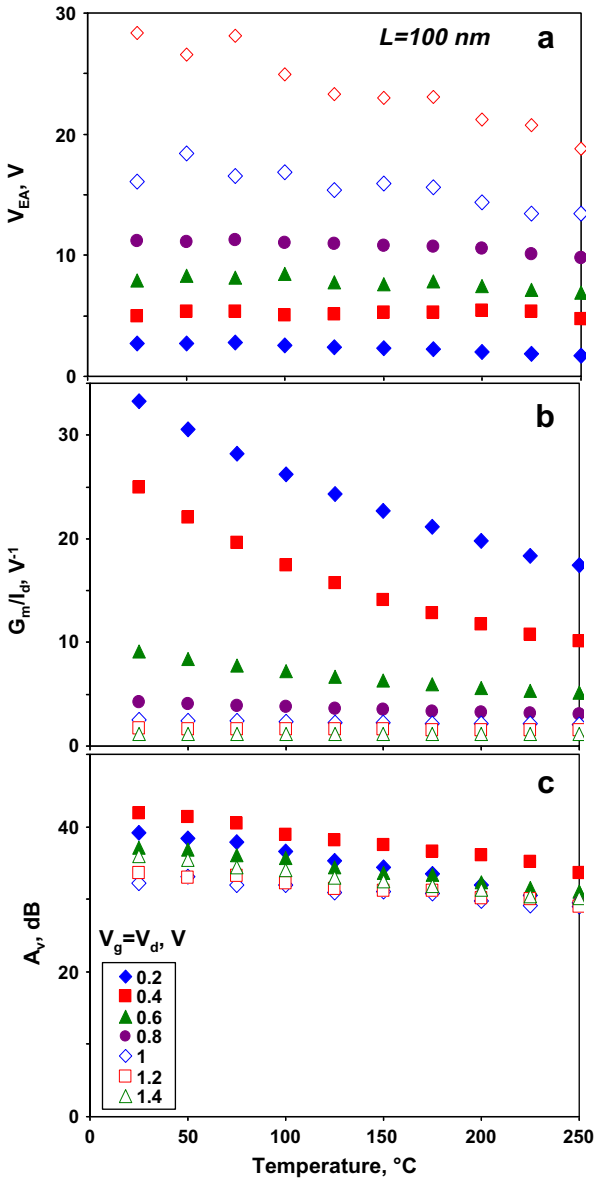

Fig. 14. (a) V_{EA}, (b) G_m/I_d and (c) A_v as a function of temperature at different applied biases for UTBB MOSFET with L = 100 nm and W = 10 μm, V_{sub} = 0 V.

(or lower G_m/I_d), i.e. regimes at which influence of series resistance is stronger. Series resistance normally slightly increases with temperature, which in turn, similarly to mobility decrease, results in G_m and I_d degradation, but its temperature dependence is weaker than that of mobility. This suggests impact of series resistance as one of the possible reasons which could explain attenuated degradation of I_d and $G_{m\ \max}$ with temperature.

Finally, Fig. 14 shows temperature variation of G_m/I_d, V_{EA} and A_v, taken at different $V_g = V_d$, in 100 nm-long UTBB device. One can see that V_{EA} stays quasi-constant in the temperature range up to 250 °C. However, G_m/I_d strongly degrades with temperature increase, due to S increase (in below V_T region) and due to mobility decrease (in strong inversion region). As a result, A_v decreases with temperature increase, but its degradation is limited to 5–8 dB (notwithstanding that G_m/I_d degrades almost twice at $T = 250$ °C under certain bias conditions). It could be interesting to note that higher $V_g = V_d$, while providing lower room temperature A_v, is preferable from the constant A_v vs. temperature point of view.

5. Conclusions

Perspectives of UTBB SOI technology for analog applications were extensively studied. Influence of operation regime, substrate bias and temperature on analog FoM was assessed. It was demonstrated that UTBB has a great potential for analog applications featuring high drive current, maximum transconductance and intrinsic gain. From the applied biases viewpoint, intrinsic gain appears to be maximized in moderate inversion regime (at about V_T), which is good for low-power applications. Negative substrate biasing was shown to allow a further 5–10 dB intrinsic gain increase.

Comparison with other technologies including both FD SOI and different FinFETs revealed that UTBB devices approach to (and can even outperform, in the case of narrow UTBB channels) "optimized FinFETs" in terms of both maximum transconductance and intrinsic gain thus making them particularly attractive for high-precision analog applications.

We demonstrated that, while the process was not specially optimized for RF applications, cut-off frequencies as high as 170 GHz and 220 GHz are achievable for 50 nm and 30 nm-long UTBB MOSFETs, respectively, thus suggesting them as a good contender for mobile/wireless applications with LOP/LSTP options.

It was experimentally shown that both self-heating- and substrate-related degradations appear in G_d evolution with frequency (and the latter can be even larger than the former). Thus, considering wide-frequency range applications, one should particularly care that performance prediction based exclusively on DC data may result in inaccurate evaluation.

Finally, very limited degradation of both digital and analog FoM in temperature range up to 250 °C was observed.

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