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Single- versus Double-layer Spiral Inductor on High-Resistivity Trap-Rich Silicon Substrate

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***Abstract*—On-chip spiral inductors are indispensable components in modern integrated circuits (ICs), enabling critical functions across wireless communication, power management, and emerging technologies. This paper presents a comparative analysis of single- and double-layer square spiral inductors in terms of self-inductance, quality factor and resonant frequency, both fabricated on a high-resistivity trap-rich silicon substrate to minimize substrate losses and improve electrical performance. Electromagnetic simulations using ADS software, together with experimental measurements, show that the double-layer inductor achieves a 34.6% increase in self-inductance compared to its single-layer counterpart. However, the single-layer design outperforms the other in terms of quality factor (29.43% decrease) and resonant frequency (62.9% decrease) due to lower resistance and parasitic capacitance in its structure. By balancing the performance trade-offs for specific applications, using calibrated ADS simulations, these results help in selecting the optimal inductor design.**

***Keywords—double-layer inductor, self-inductance, high-resistivity substrate, trap-rich, quality factor, spiral inductor*.**

I. Introduction

The integration of high-performance passive components, such as resistors, capacitors, and inductors, into modern electronic circuits and systems, including sensors, radio frequency (RF) circuits, and digital isolators, is of paramount importance for reducing the size and assembly cost of electronic circuits and systems [1, 2]. Among these components, planar inductors play a pivotal role. Over the years, significant research has been devoted to improving the performance of spiral inductors, focusing on key parameters such as self-inductance (L_s), quality factor (Q), and self-resonant frequency (f_{res}). Various approaches have been explored, such as optimizing the dimensions and topology of inductors [3], and using advanced substrates to reduce losses and improve performance, such as glass substrates [4], high-resistivity silicon (HR-Si) substrates [5, 6], and HR-Si substrates with a trap-rich layer (HR-Si+TR) [7, 8]. Additionally, techniques such as substrate etching and inductor suspension have been investigated to mitigate the adverse effects of low-resistivity silicon substrates [9, 10], particularly the parasitic surface conduction (PSC) effect. HR-Si+TR substrates have emerged as a quasi-insulating solution that effectively addresses PSC by integrating a trap-rich (TR) polysilicon layer between the high-resistivity substrate and the buried oxide (BOX) layer [7, 8]. Previous studies have compared various inductor topologies, including spiral, tapered, meander, non-spiral, and fractal structures, designed on FR4 composite material [11]. These investigations revealed significant differences in electrical parameters. Among the topologies examined, both spiral and non-spiral inductors exhibit superior quality factors compared to the other structures. Notably, the non-spiral inductor achieved the highest Q and f_{res} values, while the spiral inductor exhibited the highest self-inductance. Optimizing L_s, Q, and f_{res} values remains a primary goal for designers. Although increasing the number of turns (N) in spiral inductors may boost L_s values, it also enlarges the inductor area, parasitic resistance, and capacitance, thereby reducing f_{res} and Q values. On the other hand, increasing metal thickness slightly reduces L_s but lowers the series resistance (R_s), thereby improving Q, although this effect saturates beyond 10 µm [3]. Furthermore, some studies have explored the use of high-permeability magnetic cores in silicon-based inductors to increase L_s without expanding N [12, 13]. However, this approach faces limitations, including the complexity of magnetic film fabrication, increased eddy current losses, and parasitic capacitance at high frequencies. Consequently, double-layer inductors have gained attention for their potential to significantly improve L_s while maintaining adequate Q and f_{res}. Indeed, the double-layer topology, widely used in on-chip RF circuits and high-frequency applications, enhances self-inductance by improving magnetic coupling and interlayer mutual inductance.

Xiao *et al.* [14] compared the performance of single- and double-layer differential symmetric circular spiral inductors on silicon substrates. These inductors featured the following parameters: 3 turns, 8 µm trace width, 2 µm trace thickness, 7 µm inter-trace spacing, and 121.66 µm inner diameter. This study found that double-layer structures increased the L_s value threefold, attributed to enhanced mutual and self-inductance and longer microstrip lines. However, this design also resulted in increased series resistance, resulting in a lower Q. Efforts to mitigate these drawbacks include the use

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of equivalent circuits to improve current-carrying capacity [15]. Chen *et al.* [15] proposed a double-layer square spiral inductor with parallel connection on a silicon substrate and compared it with a single-layer inductor. The study found that the latter has a higher self-inductance (16.19% increase due to the higher magnetic flux density), while the former had a larger quality factor (8.03%). The proposed inductors featured a number of turns of 5, trace width $w = 50\mu m$, thickness $t = 50\mu m$, thickness of the connection columns between the 2 layers $t_x = 50\mu m$, a spacing between traces $s = 50\mu m$, and an outer diameter $D = 1000\mu m$. This paper also analyzed the effect of t, $(w+s)$, and t_x on the quality factor and self-inductance value of the double-layer inductor. The study also demonstrated the advantages of current-carrying capacity and thermal performance of the inductor in high-frequency ranges. Finally, the proposed topology was found to outperform suspended single-layer inductors and those on GaAs substrates in terms of Q, L_s, and f_{res}. In a double-layer squared spiral inductor, increasing the interlayer distance improves Q and f_{res} but reduces L_s, with a significant shift in behavior observed at the 4 µm threshold [16]. Given the proven performance of HR substrates in single-layer spiral inductors [5, 17], they have also been adopted for double-layer designs. A study on double-layer squared spiral inductors using HR-Si substrates reported a 250% increase in L_s compared to single-layer structures while mitigating eddy current effects on R_s (due to the HR-Si substrate) and maintaining Q within the desired frequency range [6]. However, achieving optimal performance for all parameters simultaneously remains challenging, as improvements in L_s, Q, and f_{res} depend heavily on inductor topology, geometric dimensions, substrate properties, and application requirements.

This study investigates the performance of double-layer spiral squared inductors on HR-Si+TR substrates, leveraging the combined advantages of the double-layer structure and low-loss characteristics of the substrate. A single-layer spiral square inductor was also fabricated on the same substrate and simulated for comparison. The HR-Si+TR substrate reduces substrate losses, eddy currents, and parasitic capacitance, thereby improving Q and f_{res}. This work aims to provide insights into improving inductor performance in high-frequency applications. Section II of this paper describes the microfabrication and measurement processes. Section III focuses on the results and discussion. Finally, Section IV concludes the paper.

II. Design, Fabrication and Measurement

Two square on-chip inductors of size 820 µm × 820 µm were fabricated on a 500 µm-thick HR-Si substrate with a resistivity of 5 kΩ·cm. Above, there is an additional 500 nm-thick trap-rich polysilicon top layer with a resistivity of approximately 10 kΩ·cm, as well as a 500 nm-thick PECVD SiO_2 layer. The single-layer structure ('Ind-1' in Fig. 1a) consists of a 10-turn square spiral connected to a lower underpass through two vias. The double-layer inductor ('Ind-2' in Fig. 1b) consists of a 5-turn top layer superimposed on a 5-turn bottom layer. The two square spiral inductors under test have the following geometric properties: number of turns N, track width w, turn spacing s, inner diameter d, outer diameter D, thickness of lower metal track

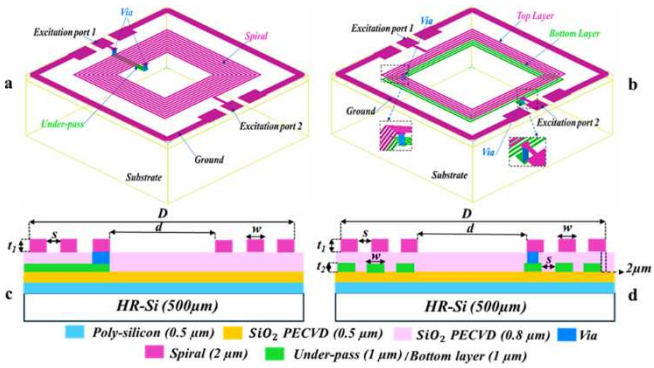


Fig. 1. Inductor layout: simulated structure in ADS: (a) single-layer inductor 'Ind-1', (b) double-layer inductor 'Ind-2', and the cross-section views atop the HR-Si+TR substrates of (c) Ind-1, and (d) Ind-2.

Table I: Geometrical dimensions of the square spiral inductors.

	N	w (µm)	s (µm)	d (µm)	D (µm)	t_1 (µm)	t_2 (µm)
Ind-1	10	10	10	400	820	2	1
Ind-2	5/5			620			

t_2, and thickness of upper metal track t_1, the values of which are given in Table I.

Atop the HR-Si+TR substrate, the microfabrication process comprises four photolithographic steps. A 1 µm-thick aluminum (Al) layer is first deposited by e-beam sputtering and then patterned as an underpass for Ind-1 (measured conductivity: $\sigma = 1.81\ 10^7$ S/m) or as the spiral shape of the lower layer of Ind-2 (measured conductivity: $\sigma = 2.1\ 10^7$ S/m). Next, a 0.8 µm-thick PECVD SiO_2 insulating layer (measured dielectric relative permittivity $\varepsilon_r = 6.3$) is deposited in an Oxford Plasmalab System 100 at 300°C, 1 Torr, 30 W RF power at 13.56 MHz, and a N_2O/SiH_4 gas ratio of 7. This layer is photolithographically patterned and etched with buffered hydrofluoric acid (BHF) to create vias connecting the spiral of Ind-1 to the underpass and the bottom layer of Ind-2 to its top layer. Third, a second 2 µm-thick Al layer is deposited by e-beam and patterned to form the spiral top shape of 'Ind-1' and 'Ind-2', the RF ground-signal-ground (GSG) access pads, and the surrounding ground planes. Both aluminum layers are precisely etched in a Corial system using a mixture of BCl_3 (boron trichloride) and Cl_2 (chlorine) gases.

It should be noted that during microfabrication, a mask alignment error occurred. As a result, the bottom layer was displaced by 2 µm from its normal position below the top layer. Experimental measurements then describe this scenario. The two-port S-parameters of the two inductors, Ind-1 and Ind-2, were measured using a Keysight N5242B PNA-X 26.5 GHz vector network analyzer with on-wafer RF probes in ground-signal-ground (GSG) configuration. SOLT (short-open-load-thru) calibration was used beforehand to calibrate the test setup over a frequency range of 50 MHz to 10 GHz. The characteristic impedance of the test system is 50 Ω. The measured S-parameters of the two DUTs (Devices Under Test) are first validated using ADS software (Fig. 2) and then converted to Y-parameters. Parasitic parameters of the pads were removed using an open/short de-embedding method according to [18]:

$$Y_{ind} = ((Y_{dut} - Y_{open})^{-1} - (Y_{short} - Y_{open})^{-1})^{-1} \quad (1)$$

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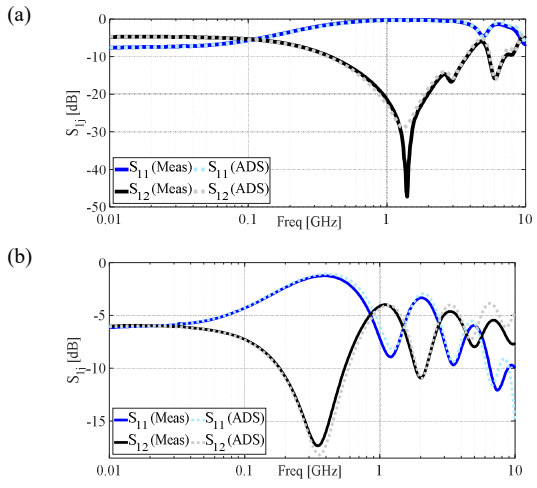


Fig. 2: Measured (plain lines) and simulated (dotted lines) S_{1j}-parameters (j={1, 2}) of the spiral inductors: (a) Ind-1, and (b) Ind-2.

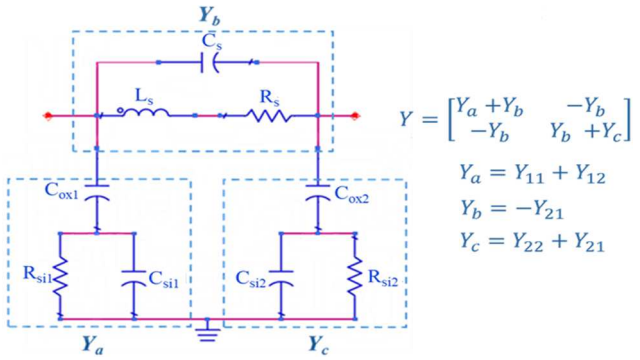


Fig. 3: π-equivalent electrical model of a spiral inductor on silicon and admittance equations [7].

III. Results and Discussion

To represent the electrical behavior of an integrated spiral inductor, a lumped-element model is commonly used, which simplifies the inductor's presentation by using ideal electrical components. This model includes a series resistance R_s, which represents ohmic losses in the traces; a series inductance L_s, which represents magnetic energy storage; and a parallel capacitance C_s, which simulates the overall capacitive coupling between the inductor turns. To account for the substrate effect evident at high frequencies, an equivalent π electrical model, consisting of three complex admittances, Y_a, Y_b, and Y_c, as shown in Fig. 3, provides a more accurate representation by incorporating the oxide capacitance between the spiral and the silicon substrate, modeled by C_{ox1} and C_{ox2}, as well as the capacitance and resistance of the silicon substrate, C_{Si1}, C_{Si2}, R_{Si1}, and R_{Si2}, denoted by subscripts 1 and 2 for each input port. The relationships between the admittances and the measured Y-parameters of the π-network are shown in Fig. 3.

A. Ind-1 versus Ind-2 comparison

To compare the two inductors, the self-inductance is a critical parameter, defined as the ratio of the magnetic flux generated by the inductor to the current flowing through it, which can be extracted from the π-model as:

$$L_s = -\frac{1}{2\pi f}\Im\left(\frac{1}{Y_{21}}\right)|_{f\to low\text{-}band} \quad (2)$$

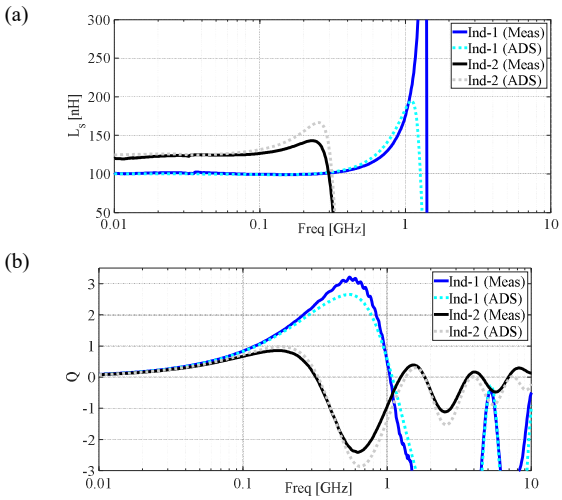


Fig. 4: Measured (solid lines) and simulated (dotted lines) results of spiral inductors versus frequency: (a) self-inductance for Ind-1 and Ind-2, and (b) quality factor for Ind-1 and Ind-2.

Fig. 4a shows the simulated and measured L_s as a function of frequency for both inductors. Good agreement is observed between the ADS simulations and experimental measurements, indicating the accuracy of the ADS simulations. For comparison, at 10 MHz, the measured Ind-1 value is 101 nH and the ADS value is 100 nH, while the measured Ind-2 value is 120 nH and the ADS value is 124.8 nH. The higher L_s value of Ind-2 is related to its topology, where the upper and lower windings interact, resulting in an increase in L_s. We also extract the other inductor figures of merit, R_s, Q, and f_{res}, as follows:

$$R_s = -\Re\left(\frac{1}{Y_{21}}\right)|_{f\to low\text{-}band} \quad (3)$$

$$Q = \frac{\Im\left(\frac{1}{Y_{11}}\right)}{\Re\left(\frac{1}{Y_{11}}\right)} \quad (4)$$

$$f_{res} = \frac{1}{2\pi\sqrt{L_s C_s}} \quad (5)$$

The Q-factor, defined as the ratio of energy lost to energy stored, is a function of L_s and the series resistance R_s. Ind-1 has a lower resistance value (71.74 Ω measured and 71.76 Ω by ADS) because it does not have a spiral in the first metal layer. This lower R_s value positively affects its quality factor, which is 3.2 at 547 MHz (2.65 at 540 MHz in simulation). Ind-2, on the other hand, uses the first metal layer, resulting in a higher resistance (97.65 Ω measured and 97.78 Ω simulated). As a result, it has a much lower quality factor, 0.85 at 179 MHz (0.98 at 186 MHz in simulation). The resonant frequency of Ind-1 and Ind-2 can be determined by analyzing the quality factor curves. The latter is defined as the frequency at which the quality factor curve intersects the x-axis ($Q = 0$). As illustrated in Fig. 4b, Ind-1 reaches its f_{res} at approximately 1.04 GHz (1.08 GHz in simulation). The measured resonance frequency of Ind-2 is approximately 0.32 GHz (and 0.33 GHz in simulation). According to Eq. 5, C_s for Ind-1 can be calculated to be 0.23 pF (0.21 pF measured), while that for Ind-2 was 2.06 pF (1.86 pF measured). The higher overlap capacitance formed between the upper and lower layers of Ind-2 results in a higher C_s. The observed decrease in f_{res} of Ind-2 is attributed to the increased

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C_s. Table II summarizes all measurements and ADS simulation results.

The results showed that the square spiral inductors, with identical geometric dimensions, exhibit distinct characteristics in terms of Q-factor, f_{res}, and L_s. More specifically, Ind-1 exhibits superior performance in Q and f_{res} compared to Ind-2. The latter has a higher self-inductance value than the former (an increase of 18.8%). The self-inductance of Ind-2 is affected by the mutual inductance of its spirals. The total self-inductance and the mutual inductance of each layer are taken into account when calculating the total inductance. The increase in this parameter is due to the increased magnetic coupling between the two layers and the increased number of effective turns resulting from the series connection of turns between the two layers via metal vias. Therefore, the double-layer design is quite promising for certain applications requiring a high degree of self-inductance. In contrast, Ind-1 is particularly advantageous in systems requiring higher Q and f_{res}.

B. *Misalignment effect on Ind-2*

This section presents ADS simulation results for the double-layer inductor with and without the 2 µm offset on an HR-Si+TR substrate. More specifically, the measured Ind-2 will be compared to the original, defect-free structure (Ind-2-I), where the top and bottom spiral layers are perfectly aligned, exhibiting overlapping spirals. Two ADS simulations are performed for both Ind-2 and Ind-2-I.

As illustrated in Fig.5, the L_s and Q-factor curves are displayed. At 10 MHz, Ind-2-I exhibits a self-inductance value of 128.7 nH, compared to 124.8 nH for Ind-2. The higher L_s value for Ind-2-I can be attributed to the optimal alignment of the top and bottom spiral layers, which results in maximum magnetic coupling between them (versus partial coupling in the shifted structure), enhancing the mutual inductance and thus the total inductance value. The Q-factor of Ind-2-I is about 1.26 at 225 MHz, compared to 0.98 at 184 MHz. This increase can be attributed to the slight decrease in R_s (96.16 Ω for Ind-2-I and 97.78 Ω for Ind-2) and the concomitant increase in L_s, since the Q-factor is proportional to their values. The resonant frequency of Ind-2-I is about 400 MHz, compared to 330 MHz for Ind-2. This difference in resonant frequency is attributable to the alteration in series capacitance (C_s), which was about 1.23 pF for Ind-2-I, compared to 1.86 pF for Ind-2. The slight increase in capacitance is attributed to the displacement of the bottom layer. Figures of merit values of the two inductors are summarized in Table III.

A slight misalignment of the bottom layer relative to the top layer still maintains a partial overlap, meaning that some capacitive and inductive coupling remains. In our example, this has a major influence on the performance, as evidenced by the quality factors Q, L_s, and f_{res}, which have undergone an increase of 28.57%, 3.125%, and 21.21%, respectively, compared to the fabricated structure (Ind-2).

C. *Bottom layer thickness effect on Ind-2*

This section investigates how aluminum (Al) layer thickness affects Ind-2's performance using ADS simulations. Initially, the top layer thickness (t_1) was 2 µm and the bottom

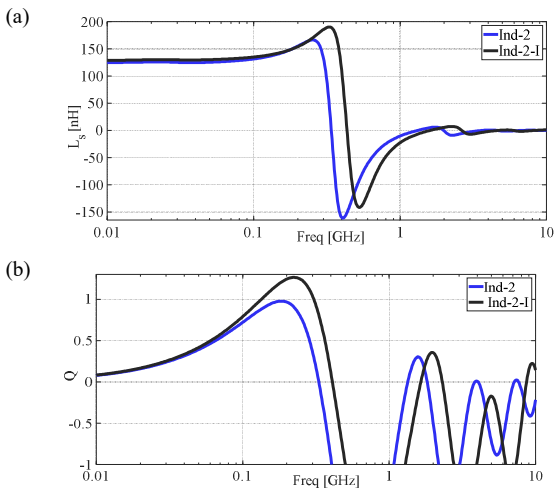


Fig. 5: Simulation results of double spiral inductor versus frequency for Ind-2 and Ind-2-I: (a) self-inductance, and (b) quality factor.

TABLE II. MEASURED AND SIMULATED CHARACTERISTICS AND PERFORMANCES OF IND-1 AND IND-2.

	Ind-1		Ind-2	
	Meas	**ADS**	**Meas**	**ADS**
L_s **(nH)**	101	100	120	124.8
R_s **(Ω)**	71.74	71.76	97.65	97.78
C_s **(pF)**	0.23	0.21	2.06	1.86
Q_{Max}	3.2	2.65	0.85	0.98
f_{res} **(GHz)**	1.04	1.08	0.32	0.33

layer (t_2) 1 µm. We then modified both layers to $t_1 = t_2 = 2$ µm (denoted Ind-2-T), effectively increasing t_2. Both Ind-2 and Ind-2-T maintained a 2 µm horizontal offset between layers. Table III summarizes simulation results, while Fig. 6 compares L_s and Q-factor versus frequency for both structures. As shown, Ind-2-T exhibits a self-inductance of 133 nH and a significantly lower series resistance of 65.9 Ω. Consequently, a slight increase in self-inductance is observed (compared to Ind-2), as it is predominantly influenced by the inductor geometry, particularly mutual coupling. On the other hand, the uniform thickness of the metal layers improves uniform current distribution across both layers. This increases the effective conductive cross-section, reduces the series resistance (R_s) and conduction losses, thereby elevating the quality factor (Q) and inductor efficiency. This results in a high Q-factor of 1.55 at 184 MHz compared to Ind-2. However, the thicker bottom layers intensify parasitic capacitance (C_s) through the inter-conductor fringing fields, which can reduce the self-resonance frequency (f_{res}) and limit high-frequency operation. Consequently, the f_{res} of Ind-2-T is about 335 MHz, which is very close to that of Ind-2.

IV. BRIEF SUMMARY AND COMPARISON

The results of the proposed single- and double-layer squared spiral inductors in this work are compared with those of previous research. Here, we studied the correct structure of the double-layer inductor as it should be manufactured (without offset) and simulated by equalizing the metal thickness of the two layers at $t_1 = t_2 = 2$ µm (denoted Ind-2-IT). Table IV compares the single-layer (SL): (Ind-1) and the double-layer (DL) inductance with the same thickness (Ind-2-IT) with different shape (circular, squared) from

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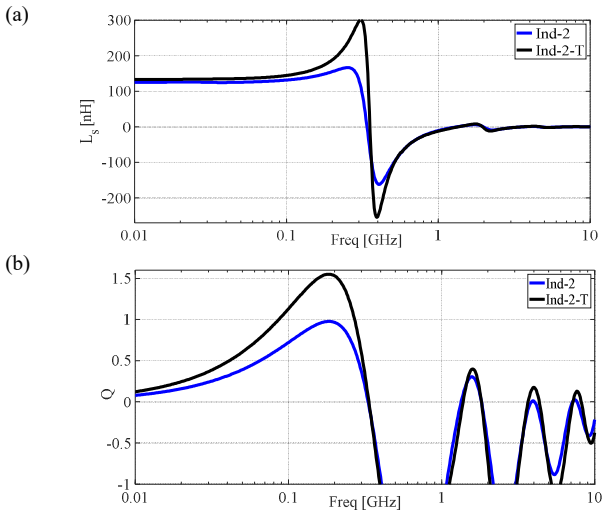


Fig. 6. Measured and simulated results of double-layer spiral inductor versus frequency: (a) self-inductance for Ind-2 and Ind-2-T, and (b) quality factor for Ind-2 and Ind-2-T.

TABLE III. SIMULATED CHARACTERISTICS AND PERFORMANCES OF DOUBLE-LAYER INDUCTORS.

	L_s (nH)	R_s (Ω)	C_s (pF)	Q_{max}	f_{res} (GHz)
Ind-2	124.8	97.78	1.86	0.98	0.33
Ind-2-I	128.75	96.16	1.23	1.26	0.4
Ind-2-T	133	65.9	1.7	1.55	0.335
Ind-2-IT	134.6	64.9	1.17	1.87	0.4

TABLE IV. COMPARISON OF CHARACTERISTICS AND PERFORMANCES WITH PREVIOUSLY REPORTED DOUBLE-LAYER SPIRAL INDUCTORS.

Ref.	Structure	N	D (µm)	w (µm)	L_s (nH)	Q_{max}	f_{res} (GHz)
[6]	SL (HR-Si)	4.5	486	48	2.7	22.1	9.7
	DL (HR-Si)				8.9	11.8	2.3
[14]	SL (Si)	3	-	8	2.23	25.92	16.4
	DL (Si)				7.18	17.22	6.2
[15]	DL (Si)	5	1000	50	12.53	21.91	4.32
[16]	DL (Si)	4	340	20	9	7.25	2.2
This work	SL (HR-Si + TR)	10	820	10	100	2.65	1.08
	DL (HR-Si + TR)				134.6	1.87	0.4

previous work using Si and HR-Si substrates. The table indicates a clear increase in the self- inductance values (34.6%) of the double-layer structures compared to the single-layer structures, while the latter exhibit the highest values of quality factor (29.43% decrease) and resonance frequency (62.9% decrease). The structures proposed in this work exhibit interestingly high self-inductance values due to the high number of turns that can only be achieved on a HR-Si+TR substrate. However, increased parallel turns induce substantial parasitic capacitance that sharply reduces the resonant frequency (f_{res}), despite the significant increase in the self-inductance.

V. CONCLUSIONS

In this work, single- and double-layer squared spiral inductors were designed, fabricated, simulated, and measured. The HR-Si+TR substrate was utilized to minimize substrate losses and enhance electrical performance, especially at high turns. A comparison was conducted in order to assess the performance of two distinct inductor structures. It was found that the single-layer structure has superior performance in terms of quality factor Q and resonant frequency f_{res}. On the other hand, the double-layer structure 'Ind-2' allows for a higher inductance value. The study showed that shifting the bottom Ind-2 layer below the top layer resulted in a decrease in Q, f_{res} and L_s. The findings of the study demonstrated that these values could be increased by increasing the thickness of the bottom layer, thus ensuring equal thickness for both layers. The results, both measured and simulated, demonstrate that for systems requiring a higher Q and f_{res}, the single-layer inductor is the optimal choice. For applications requiring a large self-inductance value, the double-layer inductor is the ideal option.

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