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Impact of thermal coupling effects on the digital and analog figures of merit of UTBB SOI MOSFET pairs

Martin Vanbrabant *, Jean-Pierre Raskin, Denis Flandre, Valeriya Kilchytska

Institute of Information and Communication Technologies, Electronics and Applied Mathematics (ICTEAM), UCLouvain, Louvain-la-Neuve, Belgium

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ABSTRACT

This work studies the thermal cross-coupling between two side-by-side UTBB (ultra-thin body and ultra-thin BOX) fully-depleted Silicon-on-Insulator (FD-SOI) MOSFETs. Due to the operation (i.e. heating) of the neighbor (actuator) device, the temperature of the measured device increases, which deteriorates its electrical parameters. This degradation is studied as a function of the bias applied to (i.e. power dissipated by) the neighbor device on main digital (SS, V_{Th} and I_{on}/I_{off}) and analog (g_m, g_m/I_d and A_v) Figures of Merit as well as the 2nd and 3rd order harmonic distortions (HD_2 and HD_3).

1. Introduction

Enormous progress in the semiconductor industry has been made during the two last decades to enable the continuous technology downscaling to 20 nm and beyond. From the device architecture point of view, UTBB (ultra-thin body and ultra-thin BOX) fully-depleted (FD) Silicon-on-Insulator (SOI) technology is widely considered as one of the main contenders for device downscaling [1]. Indeed, in addition to its outstanding electrostatic control, very low mismatch, high performance in terms of low-power, high-speed, it also features attractive analog and RF figures of merit (FoMs) [2]. However, in spite of its numerous advantages, comparative studies [3,4] of self-heating (SH) reported that the lower thermal conductivity of the buried oxide w.r.t silicon makes it more subject to self-heating than their bulk counterparts, which can affect both device performance and RF figures of merit. Studying device self-heating and thermal cross-coupling between neighbor devices [5,6] is therefore crucial, especially for applications such as current mirrors [7] which strongly rely on matching, quantum computing [8] or 3D resistive random access memory (RRAM) [9], whose proper functioning can be greatly impacted by these unwanted heating sources.

In our previous work [10], the degradation of the characteristics of a UTTB FD-SOI MOSFET caused by the heat originating from a neighbor device operation was shown. Temperature rise up to 14 K was found due a neighbor device biased in strong inversion and saturation. This work extends the previous analysis by studying the impact of thermal cross-coupling on the digital and analog figures of merit (FoM) through DC measurements.

The paper is structured as follows: Section 2 describes the geometry and particularities of the devices under test. In Section 3, the impact of the thermal cross-coupling effect is studied on (i) I_d-V_{GS} characteristics, (ii) digital and (iii) analog figures of merit. 2nd and 3rd order harmonic distortions (HD_2 and HD_3) are extracted as well based on DC measurements.

2. Experimental details

The devices used in this study are fabricated by an industrial FD-SOI CMOS process. They consist of nMOSFETs featuring a gate length below 30 nm and a single finger of 10 μm width. The final buried oxide (BOX) and the SOI film thicknesses are in the order of 20–25 nm and 6–7 nm, respectively. In order to better demonstrate the thermal cross-coupling effect between neighbor devices representative of analog/RF circuits, very wide single finger transistors were designed, and then placed as close as possible according to the design rules of the process fabrication.

Fig. 1 shows a schematic cross-section of two transistors placed side-by-side, parallel to each other, and spaced by distances $L_{G\text{-}G}$ from gate-to-gate and $L_{D\text{-}S}$ from drain-to-source, where $L_{G\text{-}G}$ = 312 nm and $L_{D\text{-}S}$ = 164 nm.

In order to bring these devices as close as possible together while still meeting the design rule checks (DRCs) of the Process Design Kit (PDK),

* Corresponding author.
E-mail address: martin.vanbrabant@uclouvain.be (M. Vanbrabant).

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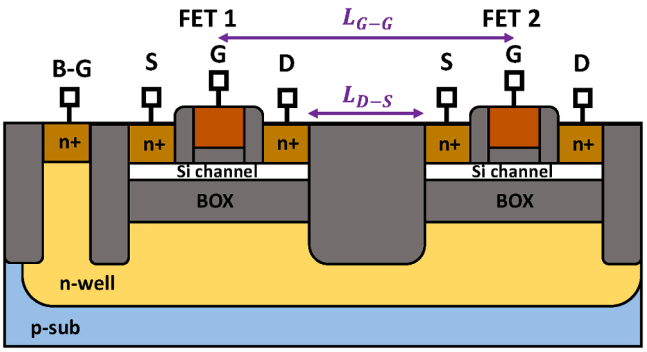

Fig. 1. Schematic cross-section of two side-by-side FD-SOI nMOSFETs spaced by distances $L_{G\text{-}G}$ from gate-to-gate and $L_{D\text{-}S}$ from drain-to-source (not to scale).

both devices have to share the same back-gate connection. Their back-gate (B-G) accesses are thus electrically connected together through the n-well region below the BOX. In this paper, a back-gate bias of V_{BG} = 0 V was applied during all measurements.

One should note that RF devices tend to have very wide geometries with multiple fingers of several μm width in parallel above a common back-gate like the structure shown in Fig. 1.

3. Results and discussion

In this section, the degradation of the key electrical parameters of device 1 caused by the operation of device 2 is studied as a function of the different operation conditions of device 2. First, the impact of the thermal cross-coupling effect is evidenced on I_d-V_{GS} characteristics. Digital figures of merit (FoMs) are then computed and analyzed as a function of the bias applied (i.e. power dissipated by) the neighbor device. Finally, the same study is conducted for analog FoMs.

Measurements presented in this section were done on three dies (not shown) to confirm the observed trends. Another important note is that the observed variations of the output characteristics due to thermal coupling are comparable to process variations but: (i) they will add upon the process variations leading to even more transistor mismatch in the technology; (ii) their physical origin is different meaning that distinct physical-based models are required; (iii) at cryogenic temperature, the impact of thermal coupling effects could be larger than at room temperature.

3.1. I_d-V_{GS} characteristics

Fig. 2 shows I_d-V_{GS} characteristic of device 1 biased in a linear regime at V_{DS} = 50 mV when device 2 is biased in cold FET mode ($V_2 = V_{GS2} = V_{DS2} = 0$ V) and in different operation conditions in saturation and strong inversion regimes (V_2 = 0.6, 0.8 and 0.9 V). In subthreshold regime, one notes that the off-state current defined at V_{GS} = 0 V increases with V_2 whereas in inversion regime, the on-state current defined at V_{GS} = 0.8 V decreases with V_2. The key bias point in between these two opposite behaviors with respect to temperature (V_2 variations translate into temperature variations of device 1) is the zero-temperature coefficient (ZTC) point. This bias point corresponds to the gate voltage V_{GS} at which the drain current remains constant with respect to temperature. This phenomenon is due to the fact that the mobility degradation and threshold voltage shift with temperature effects compensate each other at that particular bias point. From Fig. 2, the ZTC point is $V_{GS,ZTC}$ = 0.5 V in linear regime. For V_{GS} lower than $V_{GS,ZTC}$ the threshold voltage shift predominates and therefore, I_d increases with temperature, while at V_{GS} higher than $V_{GS,ZTC}$, mobility degradation is dominant and I_d decreases with temperature rise.

In order to check the repeatability of the measurements, the electrical parameters of device 1 were measured again with device 2 in a cold FET mode (V_2 = 0 V (rep.)) after the measurements at V_2 = 0.9 V. One can observe in Fig. 3 that the drain current does go back to its initial value by overlapping the curve at V_2 = 0 V when the stressing conditions (power dissipated by device 2) are removed. For the purpose of clarity, all plots in the next subsections do not include V_2 = 0 V (rep.) because no noticeable degradation of the device occurred during the measurement procedure.

As shown in Fig. 4, I_d-V_{GS} characteristic of device 1 biased at V_{DS} = 800 mV displays the same trend with respect to the bias applied to device 2 (V_2). In strong inversion and saturation regimes of device 1, the current variations of device 1 with temperature are however lesser because the relative temperature increase is lower due to the own self-heating of device 1.

From our preliminary findings [10] shown in Fig. 5, a temperature rise up to ~14 K was observed when a neighbor device was biased in strong inversion and saturation regime at V_2 = 1 V (corresponding to a dissipated power of 9 mW). The detailed procedure to estimate the temperature increase based on hot chuck measurements is described in [10].

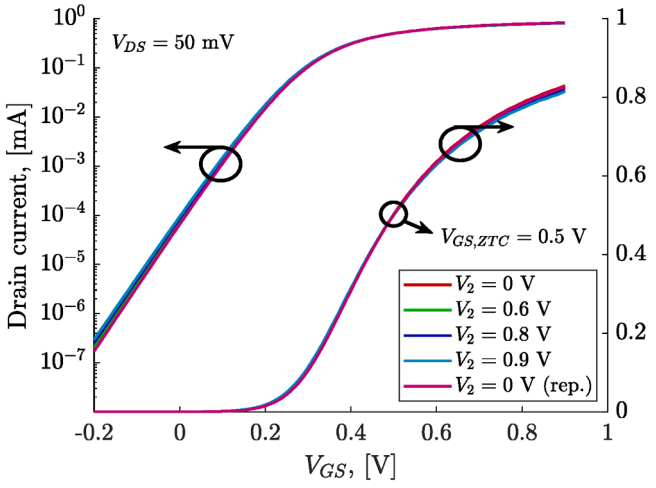

Fig. 2. Drain current I_d of FET 1 vs gate voltage V_{GS} in linear regime at V_{DS} = 50 mV when FET 2 is under different bias conditions.

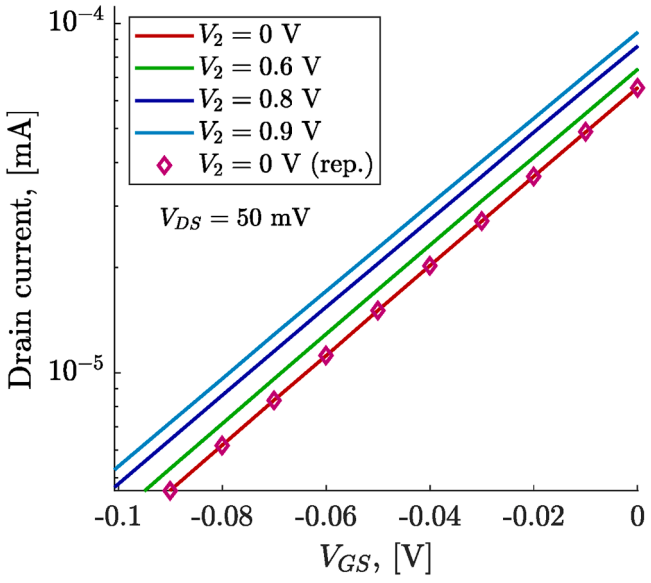

Fig. 3. Drain current I_d of FET 1 vs gate voltage V_{GS} at V_{DS} = 50 mV when FET 2 is under different bias conditions (zoom in the subthreshold region).

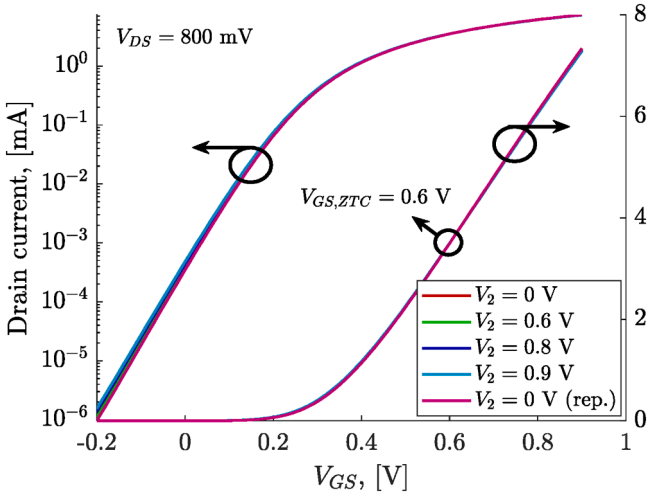

Fig. 4. Drain current I_d of FET 1 vs gate voltage V_{GS} in saturation regime at V_{DS} = 800 mV when FET 2 is under different bias conditions.

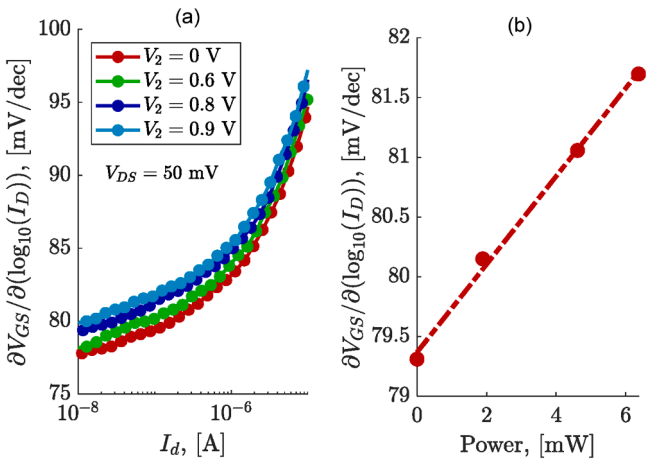

Fig. 6. (a) $\partial V_{GS}/\partial(\log(I_d))$ vs I_d at V_{DS} = 50 mV when FET 2 is under different bias conditions, and (b) $\partial V_{GS}/\partial(\log(I_d))$ at $I_d = 10^{-7}$ A vs dissipated power of FET 2, when FET 1 is biased at V_{DS} = 50 mV.

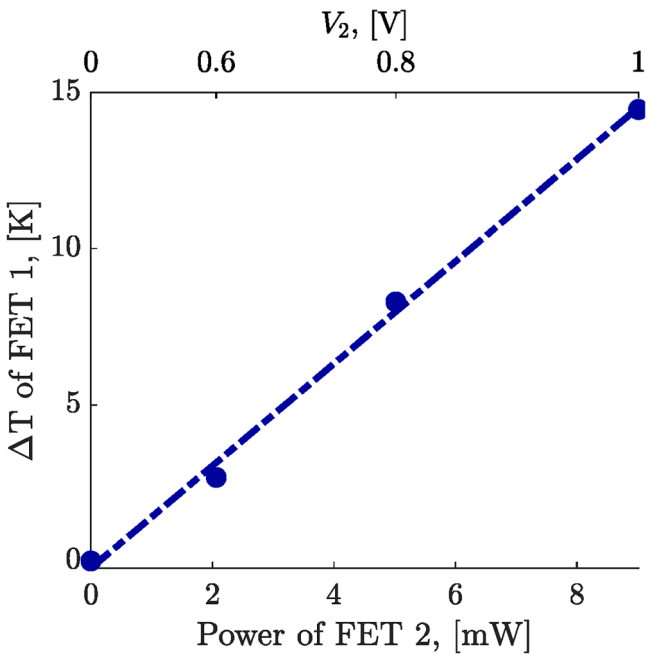

Fig. 5. Relative temperature increase ΔT of FET 1 (extracted at $I_d = 10^{-7}$ A and V_{DS1} = 50 mV) vs dissipated power of FET 2 [10].

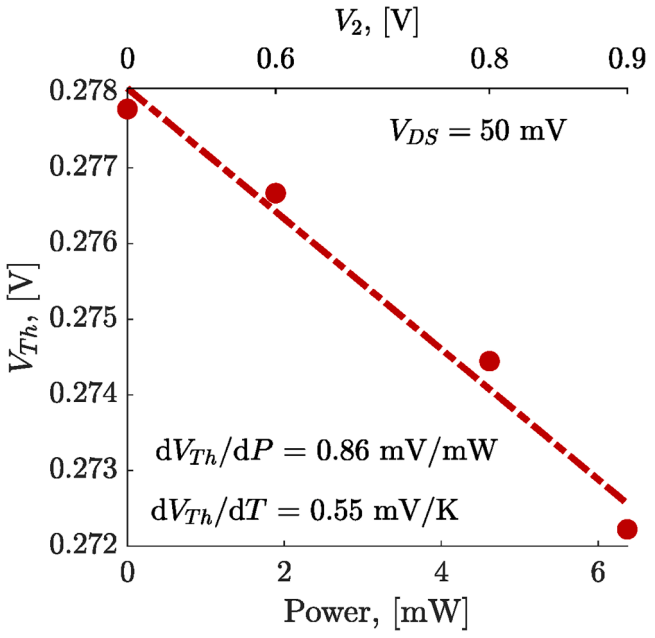

Fig. 7. Threshold voltage V_{Th} of FET 1 vs dissipated power of FET 2, when FET 1 is biased at V_{DS} = 50 mV.

In this study, the maximum dissipated power of the neighbor device is 6.37 mW (at V_2 = 0.9 V), which corresponds to an estimated temperature increase of ΔT = ~10 K.

3.2. Digital FoMs

Fig. 6a shows the subthreshold swing (SS) characteristic of device 1 at V_{DS} = 50 mV for different V_2. The subthreshold swing is computed from I_d-V_{GS} characteristic (Fig. 2) as follows: $SS = \partial V_{GS}/\partial(\log(I_d))$. The different bias conditions of device 2, namely V_2 = 0, 0.6, 0.8 and 0.9 V, correspond to dissipated powers of 0, 1.89, 4.42, 6.37 mW, respectively. A linear increase of SS from 79.31 to 81.71 mV/dec vs the power of device 2 is observed in Fig. 6b, demonstrating the sensibility to thermal coupling effects.

The second derivative method is used to extract the threshold voltage V_{Th} [11]. As shown in Fig. 7, the threshold voltage reduction with the power of device 2 is 0.86 mV/mW. This value can be referred to the typical 0.6 mV/K slope observed in advanced technologies with ultra-thin bodies like FD-SOI and FinFETs [12]. Indeed, based on the results of Fig. 5 (from [10]), the temperature of the measured device is estimated to increase by ΔT = ~10 K when the neighbor device dissipates 6.37 mW (at V_2 = 0.9 V), giving a ratio $\Delta T/\Delta P \approx 1.57$ K/mW. The threshold voltage reduction with respect to temperature can then be computed as $dV_{Th}/dT = dV_{Th}/dP \times \Delta P/\Delta T = 0.55$ mV/K, which is in agreement with the typical 0.6 mV/K slope.

It is worth pointing out that the relationship between temperature and power is only valid if the temperature is linearly dependent on the dissipated power, $\Delta T = R_{th}P$.

Based on the results in [13], R_{th} can be considered constant to the first order in the temperature range of interest. However, this approximation cannot be made at low temperature such as in cryogenic environment.

Another important digital figure of merit is the I_{on}/I_{off} ratio where I_{on}

is here defined as the on-state current measured at $V_{GS} = 800$ mV, $V_{DS} = 800$ mV and I_{off} is defined as the off-state current measured at $V_{GS} = 0$ mV, $V_{DS} = 800$ mV. As shown in Fig. 8, a ~30% reduction of I_{on}/I_{off} ratio is observed when device 2 dissipates 6.37 mW (at $V_2 = 0.9$ V).

This reduction of the I_{on}/I_{off} ratio is strongly related to the increase of I_{off}, changing from 0.35 μA at $V_2 = 0$ V to 0.48 μA at $V_2 = 0.9$ V as observed in Fig. 9a. Therefore, the power consumption of FET 1 in off-state ($I_{off} \times V_{DS}$) increases by a significant ~30% when device 2 operates at $V_2 = 0.9$ V, as presented in Fig. 9b.

3.3. Analog FoMs

g_m-V_{GS} plot is presented in Fig. 10a for different biases applied to device 2 and the corresponding degradation of the g_m peak is 1.4% as observed in Fig. 10b. This small degradation can be explained by the temperature variations of device 1 caused by the operation of device 2 (i.e. 14 K when device 2 dissipates 9 mW [10]) and thus the mobility reduction.

Next to that, g_m/I_d as a function of I_d is a very useful characterization approach for assessing the gain and frequency potential performance in analog applications [13–16]. Fig. 11a shows g_m/I_d vs I_d plot at $V_{DS} = 800$ mV. By taking g_m/I_d at $I_d = 10^{-7}$ A (in weak inversion regime) for different V_2, one can see in Fig. 11b that g_m/I_d decreases linearly with the dissipated power of device 2 from 39.6 to 38.2 V^{-1} (3.5%). This trend is inversely proportional to the subthreshold swing. It is worth mentioning that baseband applications, requiring high gain and precision, therefore favor device operation in weak inversion regime whereas high-frequency applications, requiring high drive current, favor device operation in strong inversion regime [14].

In addition to provide a fair comparison between devices, g_m/I_d can also be fixed at a certain value and the corresponding I_d variations can be extracted. Typical g_m/I_d values are 5 V^{-1} and 10 V^{-1} because they correspond to mid- and strong inversion, respectively. Fig. 12a and 12b show I_d vs dissipated power in FET 2 at $g_m/I_d = 5$ V^{-1} and 10 V^{-1}, respectively. One notices that I_d at both g_m/I_d values follows a decreasing trend, similarly to g_m (Fig. 10b), which is mainly related to the mobility degradation.

From I_d-V_{DS} characteristics (not shown), the output conductance g_d is calculated as dI_d/dV_{DS}. g_d vs V_{DS} plot at $V_{GS} = 0.8$ V is shown in Fig. 13 for different bias conditions of device 2 (V_2). At $V_{DS} = V_{GS} = 0.8$ V, one

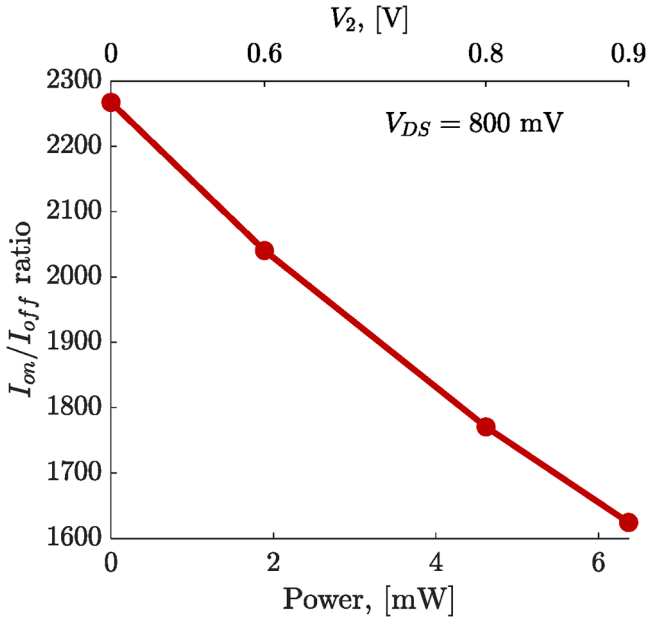

Fig. 8. I_{on}/I_{off} ratio of FET 1 vs dissipated power of FET 2, when FET 1 is biased at $V_{DS} = 800$ mV.

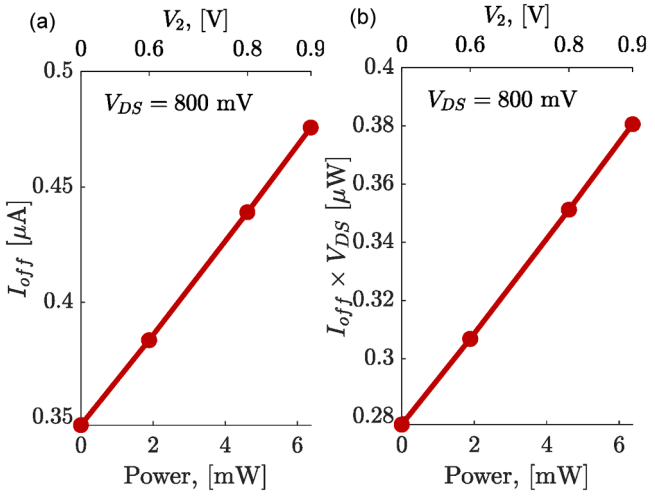

Fig. 9. (a) I_{off} and (b) $I_{off} \times V_{DS}$ of FET 1 vs dissipated power of FET 2, when FET 1 is biased at $V_{DS} = 800$ mV.

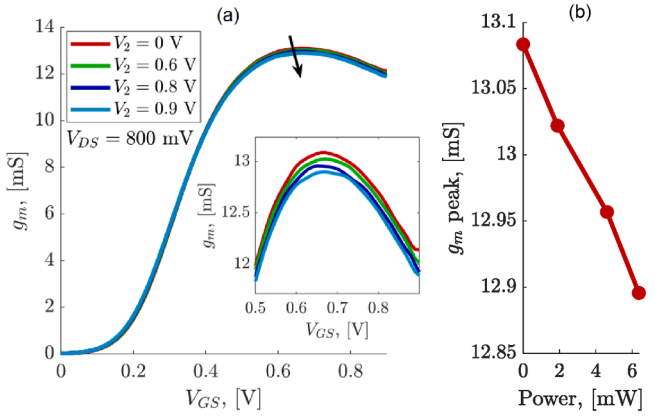

Fig. 10. (a) g_m of FET 1 vs gate voltage V_{GS} at $V_{DS} = 800$ mV when FET 2 is under different bias conditions, and (b) its corresponding variation of g_m peak of FET 1 vs dissipated power of FET 2.

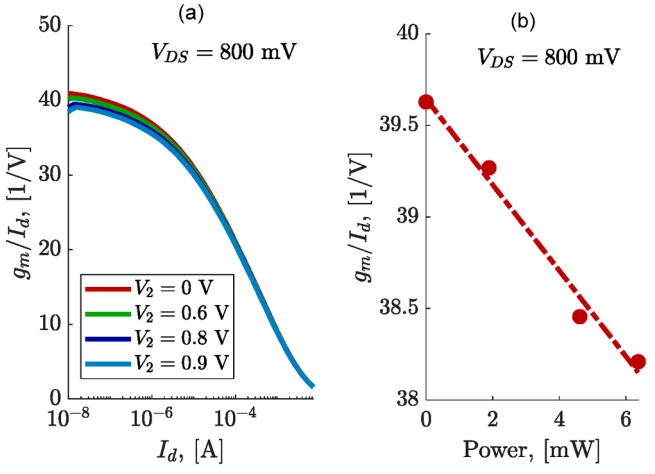

Fig. 11. (a) g_m/I_d of FET 1 vs I_d plot at $V_{DS} = 800$ mV when FET 2 is under different bias conditions, and (b) g_m/I_d of FET 1 at $I_d = 10^{-7}$ A vs dissipated power of FET 2, when FET 1 is biased at $V_{DS} = 800$ mV.

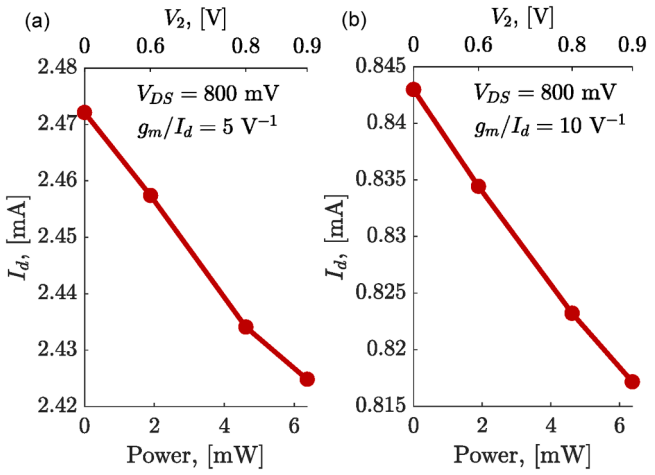

Fig. 12. I_d of FET 1 extracted at (a) $g_m/I_d = 5$ V^{-1} and (b) $g_m/I_d = 10$ V^{-1} vs dissipated power of FET 2, when FET 1 is biased at $V_{DS} = 800$ mV.20.

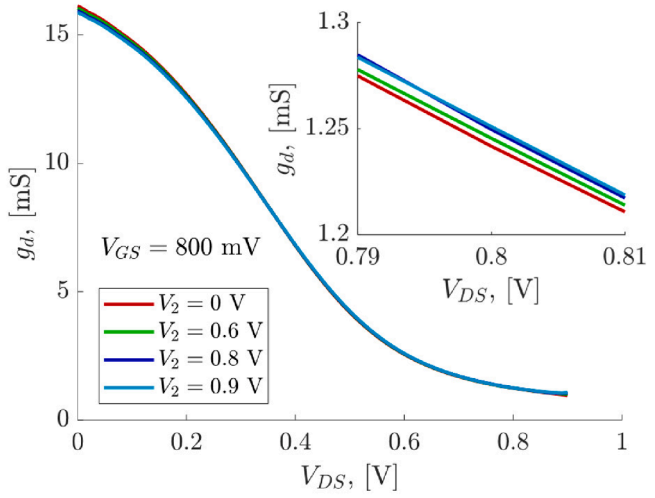

Fig. 13. G_d of FET 1 vs drain voltage V_{DS} at $V_{GS} = 0.8$ V when FET 2 is under different bias conditions.

observes that the g_d variations with V_2 remain rather limited, with a maximum increase of 0.8% from $V_2 = 0$ V to $V_2 = 0.9$ V (inset of Fig. 13).

Another key analog FoM of any MOSFET is its intrinsic voltage gain A_v computed as $A_v = g_m/g_d$, where g_m is the transconductance and g_d is the output conductance. By plotting g_m vs A_v, one can quickly assess device performance and compare different biases or temperature conditions [12]. Both g_m and A_v are desired to be as high as possible (i.e. upper right corner of the plot). Fig. 14 shows $g_m - A_v$ metric of FET 1 at two different biases, $V_{GS1} = V_{DS1} = 0.6$ V and $V_{GS1} = V_{DS1} = 0.8$ V when V_2 is varied from 0 to 0.9 V. One first notices that the voltage gain at $V_{GS} = V_{DS} = 0.6$ V is higher than at $V_{GS} = V_{DS} = 0.8$ V but the transconductance is lower. This is because the output conductance g_d at $V_{GS} = V_{DS} = 0.6$ V is lower than at $V_{GS} = V_{DS} = 0.8$ V (not shown). When device 2 (i.e. heating device) is powered on, the voltage gain A_v at both $V_{GS} = V_{DS} = 0.6$ and 0.8 V degrade by shifting toward the bottom left of the plot. The decrease in g_m (and A_v) can be correlated with Fig. 10a.

In order to assess non-linearities, the first, second and third derivatives of I_d-V_{GS} characteristics of device 1 were computed as follows: $g_m = dI_d/dV_{GS}$; $g_{m2} = d^2I_d/dV_{GS}^2$; $g_{m3} = d^3I_d/dV_{GS}^3$. One then defines the $K_n = 1/n!d^nI_d/V_{GS}^n$ factors. The second and third order harmonic distortions of a memoryless circuit can be calculated using a Taylor expansion [17] as $HD_2 = A/2|K_2/K_1|$ and $HD_3 = A^2/4|K_3/K_1|$, where A would be the AC amplitude of the input sinusoidal signal. A low signal

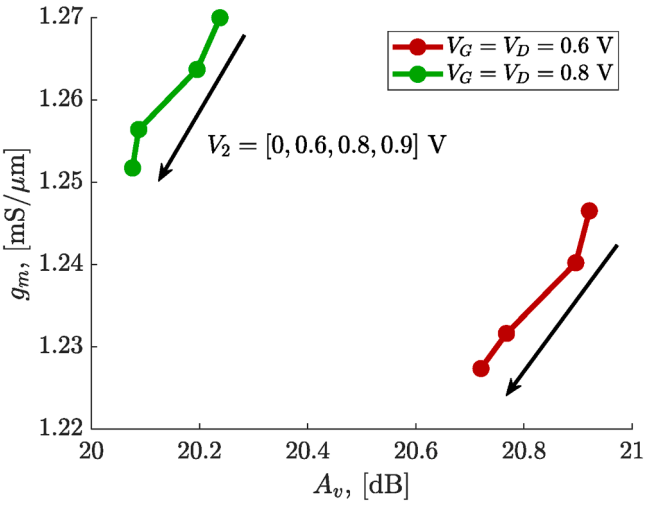

Fig. 14. $G_m - A_v$ metric of FET 1 biased at $V_{GS} = V_{DS} = 0.6$ V and $V_{GS} = V_{DS} = 0.8$ V when FET 2 is under different bias conditions (V_2).

amplitude A of 0.05 V [18] is chosen such that the Taylor expansion remains valid.

Fig. 15 shows g_m vs I_d curves for different bias conditions of device 2 (V_2). One notes that the g_m peak reduces with increasing V_2 (as in Fig. 10b) but more importantly, that g_m at V_2 greater than 0 V is lower than g_m at $V_2 = 0$ V over the whole drain current I_d range, due to mobility reduction with temperature.

Fig. 16 shows g_{m2} vs I_d curves for different bias conditions of device 2 (V_2), where the critical region is around $I_d = 0.5$ mA. Indeed, at this current, g_{m2} displays the strongest dependency on V_2 with g_{m2} peaking above 40 mS/V because this region lies in the vicinity of V_{Th}.

In practice, the 2nd and 3rd order harmonic distortions are more important than the derivatives g_{m2} and g_{m3} by themselves. Figs. 17 and 18 show respectively HD_2 and HD_3 vs I_d for various V_2. One can see in Fig. 17 that although HD_2 is minimized between $I_d = 4$ mA and 5 mA, it is also the most sensitive part of HD_2 with respect to V_2 (equivalent to temperature). Above $I_d = 1$ mA, HD_3 is however relatively independent of V_2 and with values under −55 dB as shown in Fig. 18.

If circuit designers want to avoid HD_2 degradation caused by the operation of a neighbor FET, then they need to avoid a bias point around 4.4 mA, where HD_2 can be degraded by ~10 dB when FET 2 is at $V_2 =$

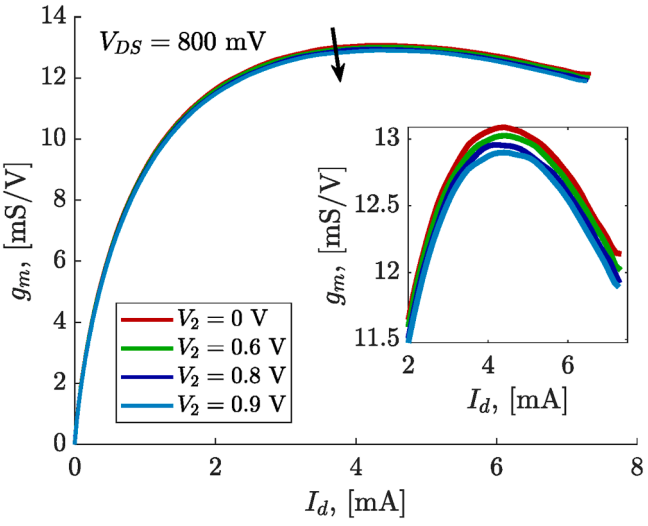

Fig. 15. G_m of FET 1 vs I_d at $V_{DS} = 800$ mV when FET 2 is under different bias conditions.

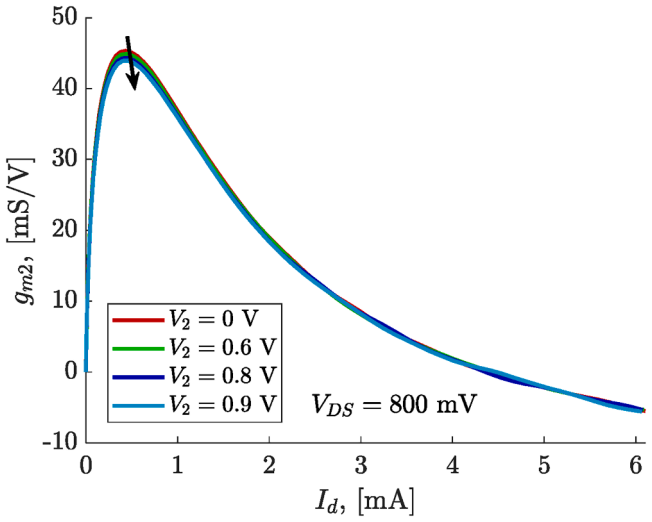

Fig. 16. G_{m2} of FET 1 vs I_d at V_{DS} = 800 mV when FET 2 is under different bias conditions.

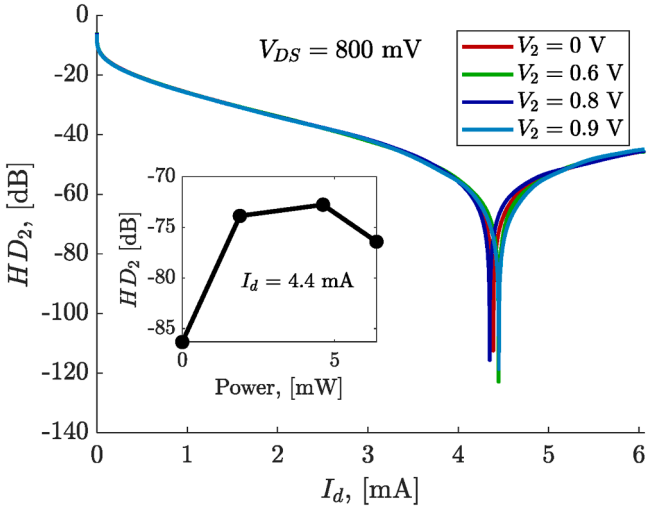

Fig. 17. HD_2 of FET 1 as a function of I_d at V_{DS} = 800 mV when FET 2 is under different bias conditions. A = 0.05 V.

0.9 V (inset of Fig. 17).

4. Conclusion

In this work, the degradation of the device characteristics caused by the heat originated from a neighbor device operation was studied. The impact of the thermal coupling was demonstrated on digital (SS, V_{Th} and I_{on}/I_{off}) and analog (g_m, g_m/I_d and A_v) parameters as well as the 2nd and 3rd order harmonic distortions (HD_2 and HD_3). The degradation due to the bias applied to (i.e. power dissipated by) the neighbor device was evidenced on all the parameters. However, overall variations remain limited with a maximum of 30% increase in I_{off} when the neighbor device is operated at the maximum bias of 0.9 V, hence dissipating 6.37 mW of power, leading to an estimated increase of temperature in device 1 of ~10 K.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

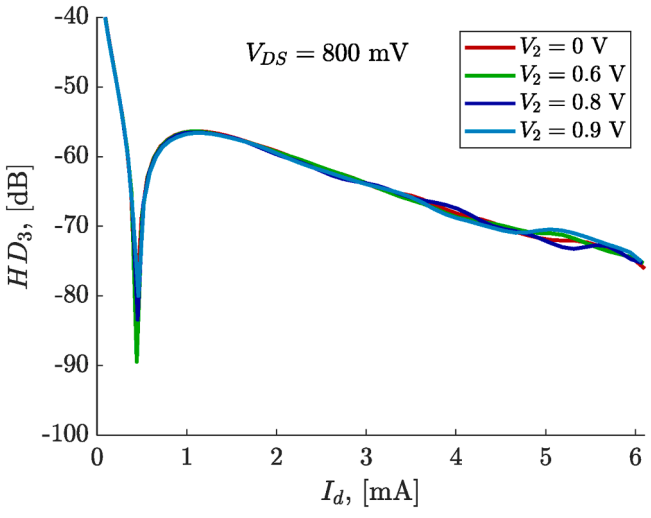

Fig. 18. HD_3 of FET 1 as a function of I_d at V_{DS} = 800 mV when FET 2 is under different bias conditions. A = 0.05 V.

Data availability

The authors do not have permission to share data.

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