Self-Heating in 28 FDSOI UTBB MOSFETs at Cryogenic Temperatures

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***Abstract*—This work studies, for the first time to the authors' best knowledge, the self-heating (SH) effect in ultra-thin body ultra-thin BOX (UTBB) FDSOI MOSFETs at cryogenic temperatures down to 77 K. S-parameter measurements in a wide frequency range, with the so-called RF technique, is employed to assess SH parameters and related degradation of analog figures of merit (FoMs) at different temperatures. Contrary to the expectations, the effect of self-heating on analog FoMs is slightly weaker at cryogenic temperatures with respect to room-temperature case. The extracted thermal resistance and channel temperature rise at 300 K and 77 K are of the same order of magnitude. The observed increase in SH characteristic frequency with temperature reduction emphasizes the advantage of the RF technique for the fair analysis of SH-related features in advanced technologies at cryogenic temperatures.**

Keywords—UTBB, FDSOI, MOSFET, Self-heating, S-parameters, Analog figures of merit

I. Introduction

Ultra-thin body ultra-thin buried oxide (UTBB) fully depleted (FD) silicon on insulator (SOI) technology is widely considered as one of the main contenders for the technology downscaling to 20 nm and beyond [1-4]. Outstanding electrostatic and variability control, high performance in terms of low-power, high-speed, as well as attractive analog and RF figures of merit (FoMs) offered by this technology were demonstrated in numerous publications [1-8]. This technology was also largely investigated at cryogenic temperatures showing promising improvement of device performance [9-12]. Apart from space applications, cryogenic studies are nowadays strongly motivated by a breakthrough in silicon-based quantum bit (qubit) which requires co-integration with the control blocks and read-out electronics for the realization of quantum computers [13-16]. Device self-heating (SH) and related power dissipation is crucial for such applications. Self-heating effect in SOI-based technologies at cryogenic temperatures was previously studied in "older technology generations" [17,18] showing SH intensification both in terms of channel temperature rise, thermal resistance and related parameters degradation at cryogenic temperatures. Our group has studied SH effect in FDSOI technology and its impact on analog FoMs at room temperature and shown that in spite of strong SH with the channel temperature rise reaching ~85 °C, its effect on parameters degradation is limited allowing FDSOI devices to outperform bulk counterparts [5, 19]. However, to the authors' best knowledge, there is no study of SH effect in advanced technologies at cryogenic temperatures.

This work aims to fill this gap by a detailed study of SH effect in 28 FDSOI UTBB technology at cryogenic temperatures down to 77 K. Firstly, the impact of SH on analog FoMs such as transconductance (gm), output conductance (gd) and intrinsic voltage gain (Av) is assessed using S-parameter measurements in a wide frequency range. Secondly, the change of gd with frequency (f) complemented by the drain current (Id) versus temperature (T) variation (also called RF technique [5, 20]) is used to monitor device self-heating. SH parameters, such as thermal resistance (Rth), channel temperature rise (ΔT) and characteristic frequency (fc), are then extracted in a temperature range from 300 to 77 K.

II. Experimental Details

The devices studied in this work originate from ST-Microelectronics 28 FDSOI process [1]. The Si film, BOX and the equivalent gate oxide thicknesses are 7, 25 and 1.3 nm, respectively. The ground plane (GP) doping is of the same type as the channel. More process details can be found in [1]. The n-channel MOSFETs under study feature 60 fingers of 2 µm width, embedded in CPW pads for RF characterization. The gate lengths (L) of the studied devices are from 25 to 90 nm. The back gate and source terminals are grounded. Lake Shore cryogenic probe station is used to extend DC I-V and RF S-parameter measurements temperature range from 300 K down to liquid nitrogen temperature of 77 K. The devices are measured from 50 kHz to 3 GHz with an ENA and a pair of ground-signal-ground Picoprobes. At each temperature, an SOLT calibration is performed on an ISS calkit.

III. Impact of Self-Heating on Analog Figures of Merit

The output conductance, transconductance and intrinsic voltage gain are extracted as the real part of Ydd, the real part of Ydg and gm/gd, respectively. Y-parameters are extracted from measured S-parameters followed by a dedicated open de-embedding for each device. An example of gd and gm versus frequency curves at different temperatures is given in Fig. 1 for the 30 nm-long device. With temperature reduction from 300 K to 77 K, the gm improvement of 30 % is larger than gd degradation of only 12 %, resulting in an overall improvement of Av by about 15% at a fixed bias condition of Vg=Vd=1 V.

It is commonly accepted [21, 22] that the frequency response of gd and gm features a transition related to SH. As the frequency increases, the lattice temperature ceases to follow the ac electrical excitation, such that the values of gd and gm at low frequency are affected by the dynamic and static SH, while their values at high frequency are "dynamic-SH free". Indeed, the analog FoMs are flat below 100 kHz and then tend to a plateau above 1 GHz. It is worth noting that substrate-related transition in gd frequency response is efficiently suppressed in our devices by the ground plane as discussed previously in [5]. Figs. 2-4 show normalized values

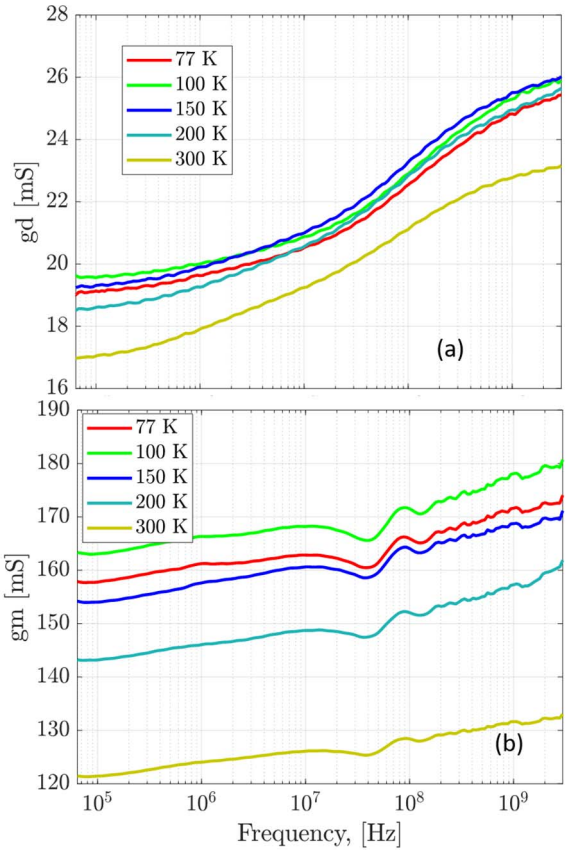

Fig. 1. gd (a) and gm (b) versus frequency of the 30 nm-long FET for different temperatures, at Vd=Vg=1 V.

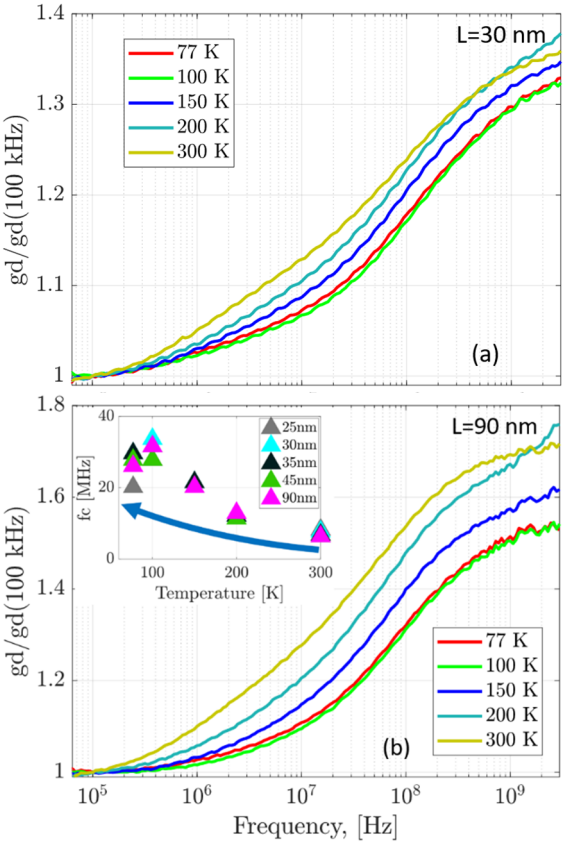

Fig. 2. Normalized gd with frequency for different temperatures of the 30 (a) and 90 (b) nm-long FETs, at Vd=Vg=1 V. The Inset in (b) shows the characteristic frequency of SH effect versus temperature for different device lengths.

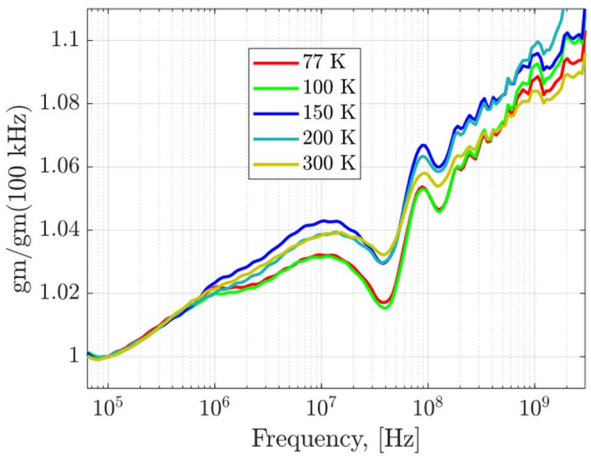

Fig. 3. Normalized gm with frequency for different temperatures of the 30 nm-long FET, at Vd=Vg=1 V.

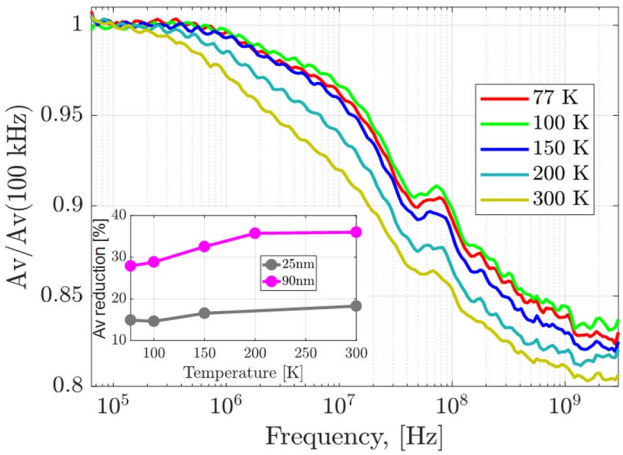

Fig. 4. Normalized Av with frequency for different temperatures of the 30 nm-long FET, at Vd=Vg=1 V. Inset: SH-related Av degradation as a function of temperature for 2 devices.

of analog FoMs with respect to the low frequency ones at several temperatures. One can note in Fig. 2 that gd increases with frequency and tends to a plateau at 1-3 GHz, where the dynamic self-heating effect is removed. SH is seen to result in a very strong reduction of gd at low frequency (~35 % of gd degradation is observed at the "dynamic-SH-free" point for the room temperature case, cfr Fig. 2). At the same time, the gm improvement observed at "dynamic-SH-free" point is relatively smaller (~10 % for the room temperature case, cfr Fig. 3). Because of a stronger variation of gd compared to gm (Figs. 2-3), a degradation of the intrinsic voltage gain at "dynamic-SH-free" frequencies is observed (Fig. 4). Av features a degradation of ~15 % (for the room temperature case) following the gm and gd trends.

The relative effect of self-heating on the output conductance is attenuated at lower temperatures for all the devices (only the 30 nm- and 90 nm-long FETs are shown here, cfr Fig. 2). The effect of self-heating on the transconductance does not vary much (less than 2 %) at different temperatures (Fig. 3). SH-related Av variation is attenuated at lower temperatures (Fig. 4), following gd trends. The inset in Fig. 4 shows the intrinsic voltage gain reduction for the shortest (grey) and longest (pink) devices as a function of temperature. Reduction of SH-related Av degradation at low temperature is more pronounced for the longest device, but still present for all measured devices.

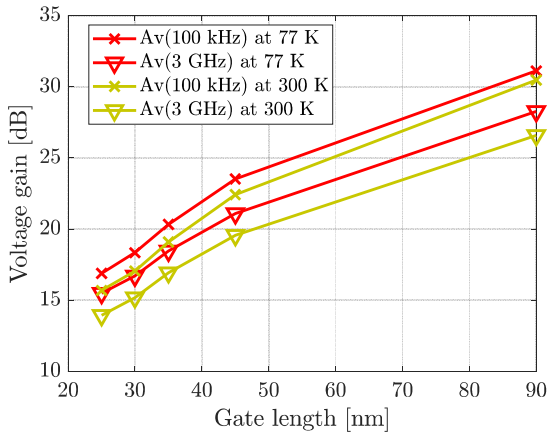

Fig. 5. Voltage gain in dB at 100 kHz and 3 GHz at 77 and 300 K for different device lengths, at Vd=Vg=1 V.

This trend is further detailed in Fig. 5, which shows Av at low and high frequencies (with SH, and dynamic-SH free, respectively) at 77 K and 300 K for devices with different gate lengths. The voltage gain decreases in short devices due to an increased gd that overcompensates the larger gm. The increase in gm with temperature reduction is more important than gd increase, implying a larger gain at low temperature. The effect of self-heating is seen in the difference between the low- and high-frequency curves. One can see that SH-related Av degradation is slightly (~1 dB) smaller at 77 K w.r.t room temperature.

Fig. 6 shows the transconductance as a function of the intrinsic voltage gain taken at 100 kHz and 3 GHz (i.e. affected by SH and "dynamic-SH free", respectively) for 77 K and 300 K. gm versus Av plot is a well-known metric allowing to benchmark devices originating from different processes or operating at different temperatures and bias conditions in terms of their potential for further analog applications [5]. gm as well as its increase due to dynamic SH removal is larger at cryogenic temperatures. The same observation is valid for Av.

IV. Thermal Parameters Extraction

The thermal resistance and channel temperature rise are extracted with the RF technique in a similar way to [21] initially developed for AC gd technique:

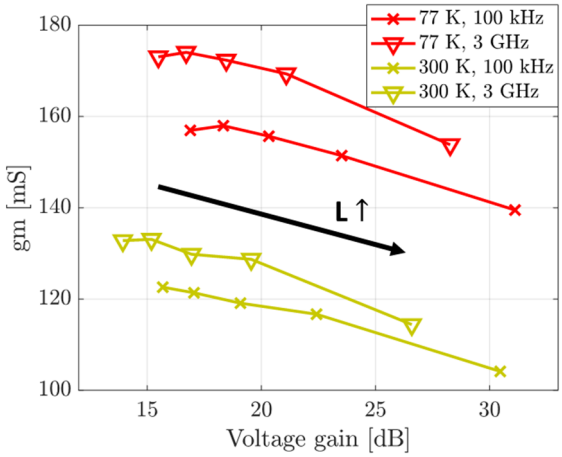

Fig. 6. gm versus Av at 100 kHz ('x') and 3 GHz ('v') at 77 K (red) and 300 K (yellow), at Vd=Vg=1 V.

$$R_{th} = \frac{\Delta g_d}{(I_d + V_d g_{d,LF})\partial I_d/\partial T}, \Delta T = R_{th} I_d V_d \quad (1)$$

where Δg_d is the difference between $g_{d,LF}$, the output conductance at 100 kHz where dynamic SH is present and gd at 3 GHz after the transition, where dynamic SH is removed. Id is the DC drain current and $\partial I_d/\partial T$ its derivative with temperature computed from the Id(T) curve shown at Fig. 7. The extracted values of Rth and the associated channel thermal rise are presented in Table 1.

There is no consensus in the literature about the point at which the $\partial I_d/\partial T$ term is evaluated, i.e. either at the channel temperature or at the chuck (ambient) temperature. The AC conductance in [22] and RF techniques in [20] explicitely specify that it should be evaluated at the channel temperature. Nevertheless, this detail is usually omitted in room temperature measurements, since the Id dependency with temperature is linear from 300 K to ~>500 K. The difference in these approaches becomes crucial at cryogenic temperatures, since Id tends to saturate as temperature goes down (77-100 K), which either (i) leads to unphysically large values of Rth and ΔT if $\partial I_d/\partial T$ is evaluated at ambient/chuck temperature or (ii) means that (Eq. 1) requires an iteration method to be solved and does not necessarily imply a unique solution, since $\partial I_d/\partial T$ is not constant and must be evaluated at the unknown channel temperature. $\partial I_d/\partial T$ in this work is computed in the temperature range of 130-250 K, which corresponds to the expected channel temperature range (according to the extracted Rth at room temperature).

At 300 K, Rth and ΔT increase with the gate length reduction is observed in accordance with [19]. The extracted Rth values are slightly higher at cryogenic temperatures than at room temperature (Table 1). A similar behaviour is observed for the channel temperature rise. Nevertheless, observed increases in Rth and ΔT in our devices are smaller than those reported in previous studies of SH effect in "older generation" SOI MOSFETs at cryogenic temperatures. Indeed, they demonstrated an Rth increase of more than 2 times and ΔT increase of more than 3 times at cryogenic temperatures [17], [18]. The possible reasons are (i) a different dependance of the mobility with temperature and (ii) a different dominant heat evacuation path due to a different geometry (L, Si film and BOX thicknesses), bias condition and doping level in our study w.r.t. previous work.

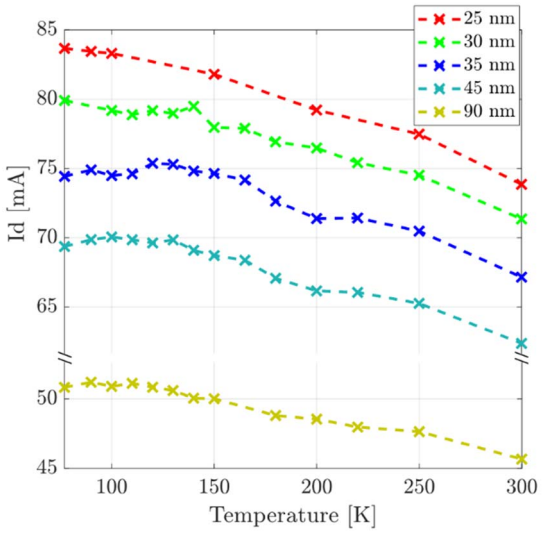

Fig. 7. DC Id with temperature for different devices, at Vd=Vg=1 V.

Table 1, Normalized Rth and thermal rise for different gate lengths and ambient temperatures. Room temperature extractions used additional DC Id measurements up to 400 K.

Gate length	Normalized Rth [Kμm/mW]		Channel temperature rise [K]	
	77 K	***300 K***	***77 K***	***300 K***
25 nm	187	173	130	106
30 nm	201	167	134	99
35 nm	181	128	112	71
45 nm	195	135	113	70
90 nm	154	94	65	36

Another important parameter that characterizes device thermal properties is the characteristic frequency of SH effect, fc. Inset in Fig. 2b shows the characteristic frequency of the SH effect, determined to first order as in [21], i.e. gd(fc) = gd(100 kHz) + Δgd. One can see that fc moves toward higher frequencies as temperature decreases for all devices. An increase of approximately 4 times is observed for each device from 300 K to 77 K. fc is known to be inversely proportional to the thermal resistance and thermal capacitance. As we do not observe an important reduction of Rth down to 77 K, the fc shift to higher frequencies suggests a reduction of the thermal capacitance with temperature reduction. Indeed, this is agreement with other works that report a thermal capacitance reduction with temperature lowering [23, 24]. Furthermore, this fc shift toward higher frequencies as temperature decreases justifies the need of RF method for self-heating features extraction compared with pulsed I-V method that requires a pulse too short for commercially available instruments for on-wafer measurement.

V. Conclusion

A detailed analysis of the impact of self-heating effect on the output conductance, transconductance and intrinsic voltage gain was carried out at cryogenic temperatures. It appears that the performances of these analog FoMs are less degraded by self-heating at 77 K compared to 300 K. The voltage gain reduction due to SH is attenuated by 2 to 8%, depending on the gate length, when the ambient temperature goes to 77 K. Moreover, the dynamic-SH-free voltage gain is increased by 1-2 dB from 300 to 77 K, thanks to mobility enhancement and gate voltage overdrive decrease.

With temperature reduction down to 77 K, the SH characteristic frequency increases about four-fold, motivating the use at cryogenic temperatures of RF extraction method for SH effect over other conventional methods.

Finally, the thermal resistance and channel temperature rise are extracted with the RF method at different ambient temperatures and gate lengths. It is shown that, differently from the "older technology generations", neither Rth nor the temperature rise vary much at cryogenic temperatures, demonstrating the ability of UTBB FDSOI MOSFETs of being used at cryogenic temperatures for space applications or quantum computing. This work is to be further extended to a temperature range down to 4 K.

Acknowledgements

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