

Analysis of Back-Gate Bias Control on EVM Measurements of a Dual-Band Power Amplifier in 22 nm FD-SOI for 5G 28 and 39 GHz Applications

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Abstract—This paper presents a dual-band power amplifier (PA) covering the 5G n257 to n260 frequency 2 bands (24.25 to 29.5 GHz and 37 to 43.5 GHz), fabricated in the 22 nm fully-depleted silicon-on-insulator (FD-SOI) CMOS technology. Its design is based on a distributed balun at the output that efficiently performs a wideband load impedance transformation. The back-gate terminal of each transistor is connected to different pads for detailed back-gate bias variation analysis. Under 5G new radio (NR) modulated signal measurements, we show how the average output power and efficiency can be optimized by varying the back-gate bias, which optimal value depends on (i) the signal bandwidth, (ii) the carrier frequency and (iii) the target error-vector-magnitude (EVM) value. To the best of the authors' knowledge, the impact of back-gate bias control on the system-level EVM figure of merit is shown for the first time in this work. Overall, with 7.5 dBm and 7.3% mean output power and efficiency, respectively, at 27 GHz, 6 dBm and 5% at 40 GHz, for a 800 MHz bandwidth 5G NR signal, the presented PA shows outstanding performance among wideband/multiband FD-SOI-based PAs covering the 28 and 39 GHz bands, featuring comparable performance to best-in-class narrowband PA designs in FD-SOI technology.

Index Terms—Power amplifier, millimeter-wave, FD-SOI, UTBB, dual-band, wideband, 5G, back-gate bias control, EVM measurement.

I. INTRODUCTION

TARGETING ever-increasing data rates, the 3GPP 5G new radio (NR) standard specifies several bands at millimeter-wave (mm-wave) frequencies: n257 (26.5-29.5 GHz), n258 (24.25-27.5 GHz), n259 (39.5-43.5 GHz) and n260 bands (37-40 GHz) for Frequency Range 2 (FR2) [1]. Different FR2 bands or their subsets are adopted by various regions worldwide, which necessitates wideband/multiband mm-wave 5G systems to support international, cross-network roaming,

particularly for user equipment devices. High-order modulations for increased data rate have large peak-to-average power ratio (PAPR) and require highly linear power amplifiers (PAs) working in large back-off power regime, thus with lower efficiency. Despite the lower output power offered by CMOS technology compared to III-V technologies due to inherent device limitations (breakdown voltage and aging constraints, also related to the deeply scaled CMOS technology), beamforming antenna arrays alleviate the power requirement on single PA cells, thus enabling potential deployment of CMOS-based PAs in 5G systems. Its high integration and low manufacturing cost make CMOS a serious contender for 5G applications as complex digital functions can be implemented together with RF functions for increased configurability or additional functions.

This paper presents the design and characterization results of a dual-band PA covering the n257 to n260 5G bands. The PA is designed in the 22 nm ultra-thin body and buried oxide (UTBB) fully-depleted silicon-on-insulator (FD-SOI) technology. In addition to the excellent RF figures of merit (FoMs) [2], [3], the transistors in this technology feature the back-gate terminal that can be used as a tuning knob of the FETs' electrical behavior, hence also to tune the circuits performance. Its effect on the transistor behavior has already been studied to some extent [4], [5], [6], [7], [8], [9]. Its primary effect can be summarized as the modulation of the FET's threshold voltage by the back-gate-to-source voltage with a high sensitivity (70 to 80 mV/V) [6].

Static and, in particular, dynamic modulation of the back-gate bias (also called adaptive body bias, ABB) has already been applied to digital and analog circuits and demonstrated to bring significant improvements in terms of robustness to aging and process-voltage-temperature (PVT) corners, relaxing design constraints, as well as improving the trade-off between performance and power consumption or opening the way to new design techniques [10], [11], [12], [13].

Analysis on how RF circuits respond to back-gate bias modulation (either static or dynamic) is more recent and remains seldom [14], [15], [16], in particular to the case of PAs [17], [18], [19], [20], [21]. Most papers have focused on continuous-wave (CW) performance (gain, output power magnitude and phase distortions - AM-AM and AM-PM, saturated power and

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1 dB compression point - P_{sat} and P1dB, and power added efficiency - PAE FoMs, respectively) [18], [19], [20], and an innovative paper [21] has applied the ABB technique to a highly linear PA to further improve linearity and decrease the amount of back-off power for high-order modulations. Nevertheless, there exists no study of the PA response to back-gate variation on the error-vector-magnitude (EVM) FoM - an important system-level FoM - under modulated signal conditions, to the best of the authors' knowledge.

The paper is organized as follows. Section II presents the whole PA design, including the active core and passive matching network elements. Section III shows the small-signal and CW large-signal measurements, including how the PA responds to back-gate bias variation on CW FoMs. Section IV presents 5G modulated signal measurement results, and how the PA's performance can be optimized by tuning the back-gate bias taking into account its effect on the system-level EVM FoM. Finally, the PA's overall performances are benchmarked to published state-of-the-art SOI-based PAs.

II. PA DESIGN

The PA is based on a pseudo-differential two-stage configuration, with the schematic shown in Fig. 1(a). The power (second) stage uses a 3-stacked FET differential architecture [22], while the driver (first) stage features no FET stacking. Their circuit schematics are shown in Fig. 1(b) and (c). Both stages use cross-coupled neutralization capacitors to stabilize the amplifier in differential operation. The single-ended to differential (and inversely) transformation is operated by the input and output baluns that also perform the required impedance matchings. An inter-stage transformer converts the input impedance of the power stage into the required impedance of the driver stage for optimum large-signal performance. The gate and drain biases are fed to the transistors through the ac-common ground of the transformers' center-taps as shown in Fig. 1. Large bias resistors are added in the gate bias lines to stabilize the PA in common-mode operation. The back-gate terminals of all FETs are connected to dc pads via large bias resistors, to decouple RF and dc operations (not shown in Fig. 1).

A. Power Stage Design

The output stage uses super-low threshold voltage nMOSFETs with a gate length of 20 nm and a total FET width of 160 μm for all FETs. The 20 nm gate length is a good trade-off between high RF performance (cutoff, f_t , and maximum oscillation frequency, f_{max}) and reliability, for which the breakdown voltage is not significantly lower than other sub-30-nm gate lengths [23].

The total transistors width is designed as a trade-off between high output power and wideband frequency operation. By increasing the transistors width and adapting the output load impedance, one can increase the output power. However, such increase in FET width leads to a decrease of the real part of the input impedance and to further parasitics, which, respectively, reduces the bandwidth of the interstage matching network (or input matching when considering the driver stage

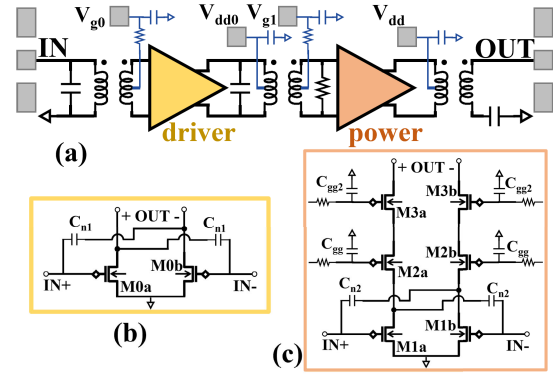


Fig. 1. (a) Schematic of the PA with the (b) driver and (c) power stage, respectively.

FETs width design) and reduces the efficiency of the FET stacking strategy due to phase misalignment [22].

Indeed, a transformer can transform real impedance ratios over a large bandwidth depending on the ratio of turns and the magnetic coupling coefficient ($R_{in}/R_{out} = (n/k_m)^2$): the larger the turns ratio (n), the larger the impedance transformation ratio, and the lower the magnetic coupling coefficient (k_m), the larger the bandwidth but the higher the transmission losses [24]. Therefore, the magnetic coupling efficiency is primarily selected for a desired operating bandwidth with reasonable transmission losses rather than to achieve a target impedance ratio transformation. Whereas the turns ratio is selected to achieve a desired impedance ratio transformation. Furthermore, increasing the number of turns of an inductor decreases the operating frequency of the inductor due to additional parasitic capacitances (the effect is further pronounced in a transformer due to interwinding capacitive coupling). So, the maximum turns ratio (linked to the maximum broadband impedance ratio) that is achievable in practice up to 43 GHz is around 1:2. Larger complex impedance ratios are also achievable but at the cost of a reduced bandwidth by tuning the reactive components.

So, in practice a total FET width of 160 μm yields a good compromise between output power and a reasonable real part of input impedance (4.5 Ω in differential mode). 4.5 Ω is a rather small value to be transformed over a large bandwidth to 50 Ω at 43 GHz due to the above reasons. Nevertheless, by using a driver stage one can relax the trade-off between total PA output power (dominated by the output stage) and the ability to match the input impedance to 50 Ω over a large bandwidth.

The M1a to M3b FETs have all the same geometry (dimensions) and interconnects up to metal 4 (M4). Each FET width is designed with a multiplicity of 4 instances of a unit transistor cell featuring a finger width of 1 μm , 2 vertical fingers (see Fig. 2) and 20 fingers. A relaxed poly-pitch is used (2xCPP), which increases f_t and f_{max} , reduces the drain and source extrinsic resistances, and relaxes the electromigration constraints. The source and drain terminals are contacted via a M1-M4 staggered metal stacking, thus significantly lowering the drain-source capacitance, for a negligible increase in drain-source resistance: reduced reactive elements for phase

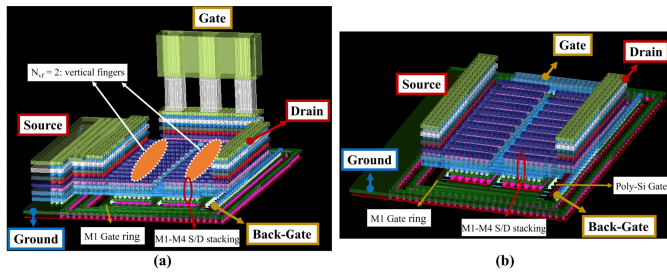


Fig. 2. 3D view of bottom layers (M1-M8) FET interconnects for the CS FETs (a) and stacked FETs (b). The stacked FETs gate terminal does not go beyond M2 at the FETs' vicinity for reduced drain-source capacitance parasitics.

mismatch, and ease of output impedance matching. This optimum design choice yields peak f_t and f_{max} of 320 and 280 GHz, respectively. Fig. 2 shows the interconnects from M1 to M8 for the common-source (CS) FETs and the stacked FETs.

The V_{dd} bias voltage is set to 2.4 V to present a dc drain-to-source voltage (V_{ds}) of 0.8 V (the nominal voltage in this technology) to each FET. A gate-to-source voltage (V_{gs}) of 0.3 V is selected as a trade-off between significant reduction in third harmonic level at medium-to-high power operation (a sweet spot in linearity exists in CMOS-based PAs biased close to class-B operation [25]) and gain that is fundamental at mm-wave frequencies. The back-gate voltage (V_{bg}) changes the threshold voltage (V_{th}), thus drain current and class of operation. $V_{bg} = 0$ V is fixed in this design (with $V_{gs} = 0.3$ V), but access to the back-gate terminal of each FET enables to (i) compensate for V_{th} -process variations (-240 to $+40$ mV for $V_{bg} = -0.5$ to 3 V, respectively) and (ii) change the PA class of operation, at a small penalty of non-optimal load impedance. Indeed, load-pull simulations (Fig. 3) shows that the centers of power and efficiency circles remain roughly constant and close to the selected optimal impedance (Z_{opt}) point with increasing V_{bg} .

Even though the differential topology can remove even harmonics from the output, even harmonics are still present in internal nodes of each branch and generate side-band asymmetries and other effects reducing the PA efficiency [25]. Furthermore, parasitic capacitances in intermediate nodes contribute to phase misalignment, which degrades P_{out} and efficiency [22]. Some methods exist to compensate for these effects, but they are narrowband, hence not suited to a wideband PA design.

The driver stage has a similar design to the power stage but features common-source-only FETs with a width of $80\mu\text{m}$ (half the power stage) and biased in the same way. In this case, the driver FETs width design constraints are (i) to be able to deliver sufficient linear power to the output stage (including the interstage matching network losses, see next section), (ii) and to present an input impedance that can be transformed to 50Ω over a large bandwidth (target from 24 to 43 GHz). As mentioned above, the operating frequency of a transformer converting high impedance ratios over a large bandwidth is limited. We have thus to limit the impedance ratio to be transformed and thereby limit the real part of the input impedance of the driver stage.

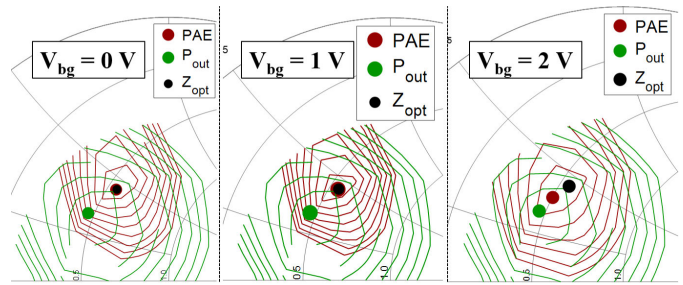


Fig. 3. Power (green) and efficiency (red) contours (load-pull) simulations at 39 GHz of the power stage for different V_{bg} biases, moving from a deep-class AB operation to class A. The Smith charts are normalized to a 100Ω reference impedance.

Therefore, we have selected a FET width for the driver stage that delivers sufficient linear power to the output stage with limited margin, such that the real part of the input impedance is not too low. A FET width of $80\mu\text{m}$ is found as a good trade-off between linear power and input impedance, as well as enabling a swift driver stage design and layout, since the same optimized FET unit cell from the output stage (see Fig. 2(a)) could be used.

B. Passives Design

Load-pull simulations of the output stage show that presenting the complex conjugate of an equivalent impedance made of a 45.5Ω resistance and 74fF capacitance in parallel for each branch (thus a differential impedance of 91Ω in parallel with 37fF , which corresponds to Z_{opt} in Fig. 3) to the output of the power stage, maximizes the output power stage large-signal performance over a large bandwidth and for a wide range of V_{bg} values (see above), such that it is selected as target optimal load impedance.

The output balun is designed accordingly to provide such load impedance across a large frequency range. Its design is based on coupled transmission line elements for an accurate wideband behavior description in a similar way as [26]. The resulting distributed balun is integrated as a standalone structure for thorough characterization (see chip microphotography in Fig. 4(a)). An input pad (port 1) is added at one of the differential inputs and is de-embedded with Open and Short structures. A parallel 45.5Ω resistor and 74fF capacitor are added on-chip at the second differential port. The single-ended output is connected to an output pad (port 2) as in the PA's output matching. Fig. 4(b) shows measurements along with initial (made at PA design time) and post-layout simulations of the standalone distributed balun. Post-layout simulations are found by adjusting the simulation settings (using a corner electromagnetic - EM - stack instead of the nominal one and refining the mesh to improve the simulation accuracy) to fit the standalone balun measurements. Then, the same settings are used for other passives simulations and, subsequently, the PA.

Fig. 4(c) shows the simulated performance of the output matching network as integrated in the actual PA (including the output pad). An ultra-wideband impedance transformation is achieved with 1-1.5 dB insertion loss in the whole 24-45 GHz range. Although it seems a rather large amount of losses for

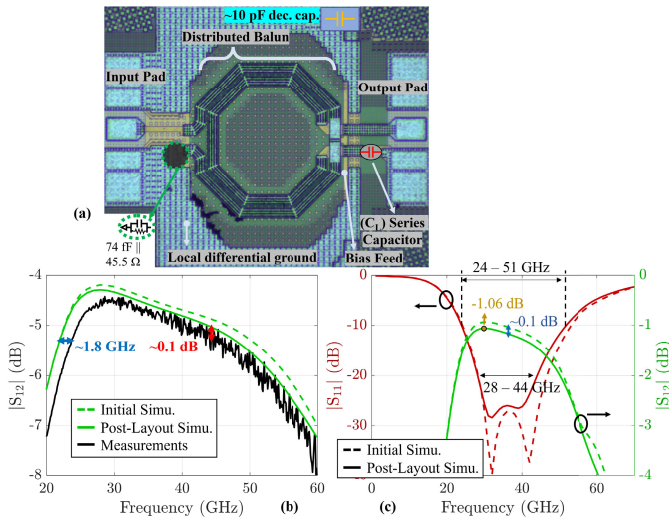


Fig. 4. (a) Microphotography of fabricated standalone output matching network. (b) Simulations (green) and measurements (black) of the standalone output balun. (c) Simulations of the output matching network in the PA.

operation in the 28 or 39 GHz bands, it is worth reminding that it includes losses from the output FETs' drain terminal all the way up to the probe tip on the output pad. Furthermore, it is in line with reported wideband matching networks designed in standard-resistivity Si substrates (such as bulk CMOS [27] and advanced FD-SOI nodes [28]) that are known to entail significant substrate losses [29] compared to high-resistivity substrates (such as in PD-SOI technology, i.e. [26]).

The inter-stage and input matching networks are designed with more compact transformers, based on classic lumped element model. The inter-stage matching includes a 365Ω shunt resistor to achieve a wideband high resistance-ratio impedance transformation. This shunt resistor is designed to withstand medium power level at the power stage input, necessary for high-power PA operation. Fig. 5 shows post-layout simulations of the inter-stage and input matching networks. They feature insertion losses of 7-8 dB and 5.5-6.5 dB, respectively, which does not deteriorate the overall PA performance thanks to sufficient gain at the output power stage (above 15 dB). However, they exhibit a dual-band behavior contrarily to the output balun, which is wideband. Therefore, the PA works as a dual-band amplifier as shown in the next sections. A 3D layout view of the PA with its main passive elements can be visualized in Fig. 6(a). Further design details can be found in [30] in particular concerning the passives design.

III. SMALL-SIGNAL AND CONTINUOUS-WAVE RESULTS

A microphotography of the fabricated PA is shown in Fig. 6(b). Small- and large-signal continuous-wave measurements are performed with the reference plane at the probe tips. A peak 27.7 dB gain is achieved at 28 GHz and a smaller local peak of 18.8 dB at 44 GHz (Fig. 6(c)). The 3 dB-bandwidths associated to the low-and high-frequency peaks span from 24.7 to 30.5 GHz and from 32.8 to 47.3 GHz, respectively. Post-layout simulations agree well with measurements, save for a small shift to higher frequencies in the measured data, similarly to what is observed for the output balun as shown in Fig. 4(b).

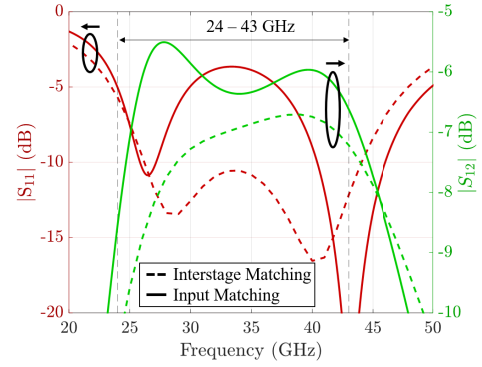


Fig. 5. Post-layout simulations of the input (solid lines) and inter-stage (dashed lines) matching network.

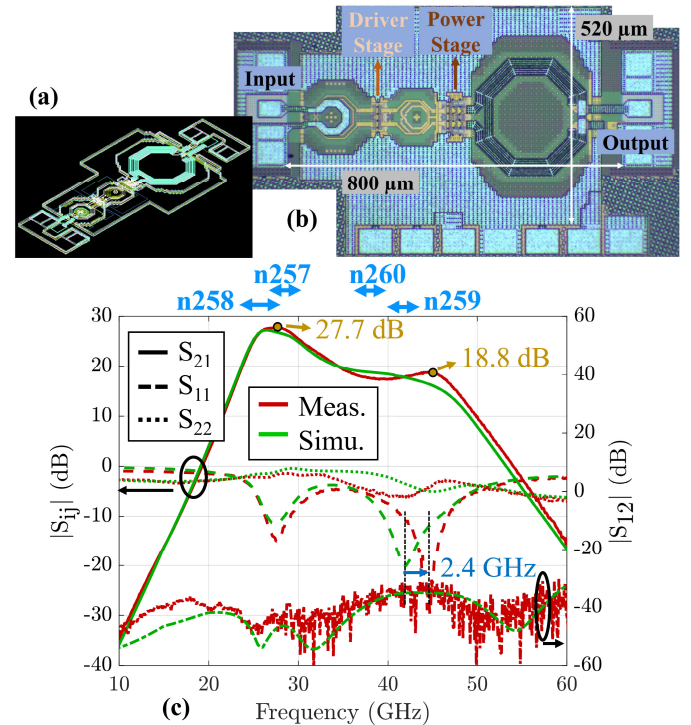


Fig. 6. (a) 3D layout view of the PA. (b) Chip microphotography. (c) Measured and simulated S-parameters of the PA.

Small-signal simulations and measurements in Fig. 7 show that the PA is not unconditionally stable around 23 and 29 GHz. Nevertheless, measurements under 50Ω conditions have shown to be stable across all shown power, frequency and back-gate bias ranges in this paper. Although it is not sufficient for a product that is expected to be able to withstand at least 1:2 voltage standing wave ratio (VSWR) variations for 5G applications [31], [32], the experimentally demonstrated stability under 50Ω conditions is sufficient for the purpose of this paper that is to evaluate the EVM performance of 5G signals with back-gate bias variation.

Fig. 8 shows P_{out} and PAE at 1 dB compression level (P1dB) and at peak PAE. The measured peak PAE goes as high as 36.4 % at 30 GHz, for a corresponding 18.3 dBm P_{out} , P_{sat} is maximum (18.6 dBm) at 31 GHz with an associated peak PAE of 35.7 %. Because of the deep-class AB operation, the P1dB is close to the peak PAE, such that the output-referred P1dB ($P_{out,1dB}$) varies from 16.2 to 18.1 dBm across the 24 to

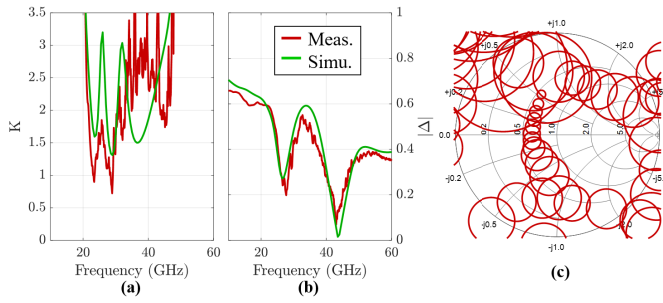


Fig. 7. Rollett's stability factor (a) and the determinant (Δ , b) from measurements (red) and simulations (green). Measured load stability circles (c) from 17 to 50 GHz with frequency steps of 0.5 GHz.

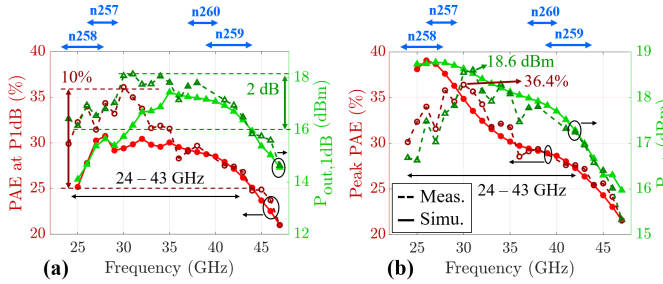


Fig. 8. PAE (left axis) and (right axis) of the PA, at 1 dB compression point (a) and at peak PAE (b). Measurements in dark, dashed lines and simulations in light, solid lines. Nominal bias.

43 GHz bandwidth. The corresponding PAE at P1dB varies from 26.8 % (at 43 GHz) to 36.1 % (at 30 GHz).

From Fig. 8, an excellent agreement is obtained between simulations and measurements above ~ 32 GHz. Below 30 GHz, the peak PAE and P_{sat} are much lower than expected. Additional measurements performed at higher V_{dd} for the power stage (not shown here) seem to indicate that the driver is compressing earlier than expected below 30 GHz. The reason is likely due to a frequency shift in the inter-stage matching that exhibits a sharp transition below 30 GHz, such that a non-optimal impedance is presented at the driver stage output below 30 GHz, thereby making the driver stage compression earlier.

The deep class AB operation features large P_{out} and PAE at P1dB, close to the peak PAE, however, it comes with significant AM-PM distortion at medium power levels, which degrades EVM. As mentioned above, by increasing V_{bg} of all transistors in the 3-stack power stage, the PA operation class shifts to class A, with improved AM-PM distortion. However, AM-AM distortion deteriorates and $P_{out,1dB}$ and associated PAE decrease significantly too. This trade-off is shown via measurements and confirmed through simulations in Fig. 9 at a measured frequency of 35 GHz.

This interesting trade-off is further explored in the next section for modulated signals in which the PA is working in high linearity regime at back-off power.

IV. EVM MEASUREMENTS

5G new radio (NR) modulation signals are applied to the designed PA both via measurements to verify its suitability for 5G applications and to experimentally understand how the back-gate bias influences its operation.

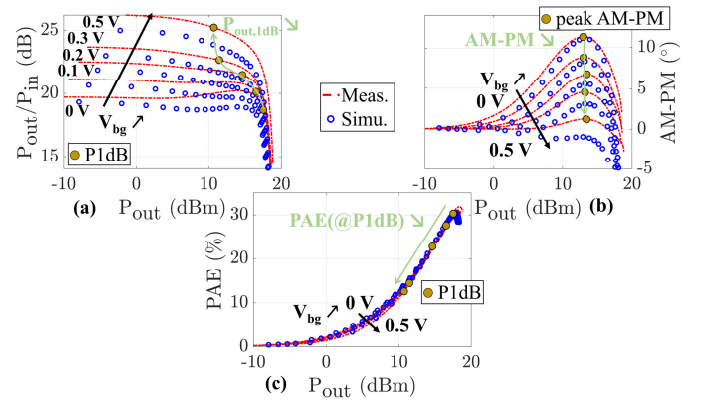


Fig. 9. Measured (red lines) and simulated (blue circles) (a) gain, (b) AM-PM distortion, and (c) PAE versus P_{out} for different V_{bg} biases, at 35 GHz. 1 dB compression point and peak AM-PM distortion shown in yellow dots.

On-wafer measurements are performed with a Vector Signal Generator (VSG, SMW200A) and a Spectrum Analyzer (SA, FSW 50 GHz), both from Rohde & Schwarz. The cables and RF probes at input and output are calibrated from the measurements with built-in tools in both the VSG and SA based on their measured S-parameters.

The EVM and adjacent channel leakage ratio (ACLR) are measured and power levels are recorded for 5G NR modulated signals of different bandwidths (100, 200 to 800 MHz) and at different carrier frequencies (from 25 to 43 GHz). In all measurements a time division duplex (TDD) uplink signal with 64-QAM orthogonal frequency division multiplexing (OFDM) digital modulation was used. The back-gate bias is modified around $V_{bg,0}$, and its effect is analyzed on the EVM performance of the different signals.

The nominal bias $V_{bg,0}$ is the back-gate bias necessary to yield the same designed bias current values of 6.8 mA and 13.5 mA for the driver and output stage, respectively. In simulations it corresponds to $V_{bg,0} = 0$ V. During measurements $V_{bg,0}$ is different from die to die due to process variability. A maximum deviation of 0.6 V was observed in $V_{bg,0}$, which corresponds to an associated threshold voltage shift lower than 50 mV.

As the back-gate bias has a strong impact on the PA's overall behavior (as explained in the previous section), we expect it to also strongly affect the EVM performance. To that end, we record the EVM measurements versus power for different V_{bg} .

Fig. 10(a) shows such curves for two different V_{bg} biases. By increasing V_{bg} , the gain increases and the EVM curves are shifted to higher power values (identical input power points for both V_{bg} biases are shown in Fig. 10(a)). While a larger gain induces a negligible or small increase in EVM at low power (linear regime), it is not the case at higher power. Indeed, the larger $V_{bg} = V_{bg,0} + 0.3$ V bias (dashed lines) compresses earlier (worse AM-AM distortion), which explains the steeper curve at higher power. Overall, the increase in EVM with larger power is due to both AM-AM and AM-PM distortions [33]. As we have seen in the previous section, by varying V_{bg} , one can trade-off one type of distortion for the other and thus maximize the power and efficiency performance for a target EVM.

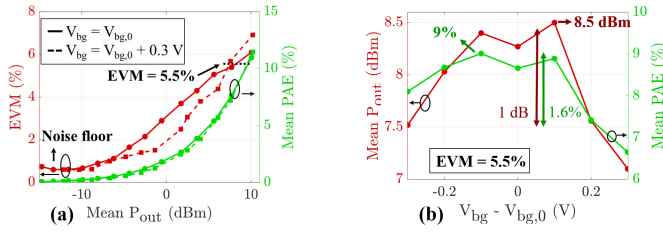


Fig. 10. 5G NR modulated signal measurements, with a 100 MHz bandwidth signal and a carrier of 40 GHz. (a): measured rms EVM, average PAE and P_{out} for $V_{bg} = V_{bg,0}$ (solid lines), $V_{bg} = V_{bg,0} + 0.3$ V (dashed lines), for different input power levels. (b): measured average PAE and P_{out} versus V_{bg} for a target $EVM_{rms} = 5.5\%$.

For a fixed target of 5.5% ($= -25.2$ dB) rms EVM, the corresponding mean output power and PAE for different back-gate biases are shown in Fig. 10(b). An EVM of 5.5% is a usual EVM requirement for low bit error rate in 5G 64-QAM OFDM signals for a standalone amplifier [31]. Note that the 3GPP specification for the complete communication channel is an EVM of 8% for a 64-QAM OFDM 5G signal, whereas it decreases for higher order modulations (3.5% for a 256-QAM OFDM 5G signal [34]).

A peak in overall PA performance -with mean P_{out} and PAE as high as ~ 8.5 dBm and 9%, respectively, for a target EVM of 5.5%- can be achieved by fine tuning the back-gate bias (optimal for $V_{bg} \approx V_{bg,0}$). The double peak in Fig. 10(b) is not physical and is related to measurement uncertainty and an approximated 5.5% EVM target value during measurements. This double peak is indeed not observed on simulation results using slightly different waveforms (data not shown).

The ACLR is also measured in peak conditions (for $V_{bg} = V_{bg,0}$ and an EVM of 5.5%) and is shown in Fig. 11. A worst-case value of -24.9 dBc is measured, which fulfills the 5G requirements (of roughly -30 dB to -25 dB [31]).

The back-gate biases of all PA's transistors are changed together in this paper. Separate back-gate biasing of individual transistors has been tested experimentally, but it has not resulted in improved performance. It is therefore not shown here.

Note that the optimal bias condition of $V_{bg} = V_{bg,0}$ is found above (Fig. 10(b)) by optimizing the PA's performance for a given signal bandwidth (100 MHz), at a given carrier frequency (40 GHz) and for an arbitrary limit of 5.5% EVM. However, it might not be the optimal bias for a different modulated signal (or for different target value of EVM as it can be seen in Fig. 10(a)). To test how the optimal bias depends on the modulated signal, the optimal bias is searched again by varying the back-gate biases for two other modulated signals, in which we change either the signal bandwidth (800 MHz at 40 GHz) or the carrier frequency (100 MHz at 32 GHz). Fig. 12 shows the mean P_{out} and PAE for different back-gate biases for these two new cases.

As shown in Fig. 12, the optimal back-gate bias leading to the best mean output power and PAE results is different from the optimum found for a signal bandwidth of 100 MHz at a carrier frequency of 40 GHz (optimum of $V_{bg,0} + 0.2$ V in Fig. 12(a) and $V_{bg,0} + 0.5$ V in Fig. 12(b)). It therefore

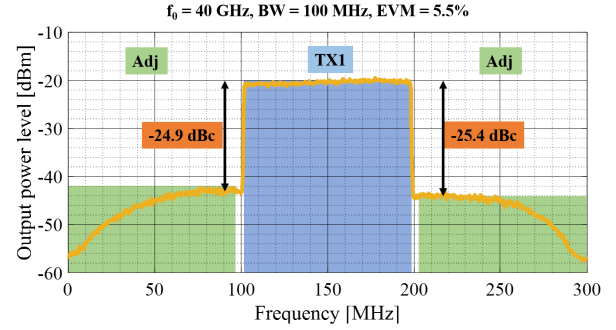


Fig. 11. Output spectrum and ACLR measurements with a 100 MHz bandwidth signal, a carrier of 40 GHz, at the nominal bias of $V_{bg} = V_{bg,0}$ and for an EVM of 5.5%. The corresponding mean output power and PAE are 8.3 dBm and 9%, respectively.

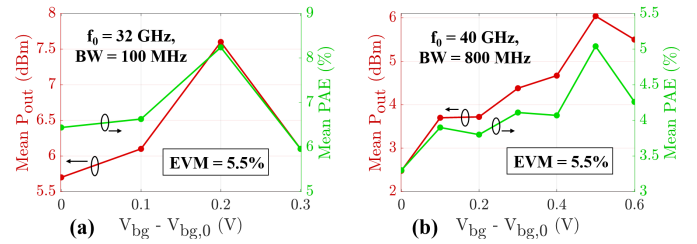


Fig. 12. 5G NR modulated signal measurements, average PAE and P_{out} at a target $EVM_{rms} = 5.5\%$, for different V_{bg} . (a): 100 MHz bandwidth at a carrier of 32 GHz. (b): 800 MHz bandwidth at a carrier of 40 GHz.

shows that the signal bandwidth and carrier frequency can greatly influence the PA biasing point that exhibits the best performance.

Furthermore, the peak is rather well pronounced, meaning that applying a non-optimal bias can lead to substantially reduced performance, i.e. a 0.2 V variation around the optimal V_{bg} in Fig. 10(b) leads to a 1 dB decrease in mean P_{out} and 1.6% in PAE. The value of using the back-gate terminal to reach such an optimum should be emphasized here. A similar result could likely be obtained by varying the gate terminal bias (thus overdrive voltage), but the sensitivity required is much larger and complex to achieve with high accuracy. Indeed, a variation of 0.2 V in V_{bg} is equivalent to a variation of ~ 15 mV in overdrive voltage. FD-SOI technology therefore offers unique high-sensitivity configurability capabilities for PAs thanks to the back-gate terminal.

Measurements of PA performance (mean P_{out} and PAE) for a target EVM of 5.5% at different carrier frequencies are shown in Fig. 13 for two biases: $V_{bg} = V_{bg,0}$ and $V_{bg} = V_{bg,0} + 0.5$ V. Here again we show the benefits of re-optimizing the back-gate bias for different modulated signals. Indeed, the improvement with the new bias (optimal for an 800 MHz signal bandwidth at a 40 GHz carrier) of $V_{bg} = V_{bg,0} + 0.5$ V is great in both output power (3 dB) and efficiency (1.8%) for a carrier frequency around 39 – 40 GHz. At the other carrier frequencies, the output power is increased but at the cost of a reduced efficiency.

Fig. 14 shows similar results for the nominal V_{bg} ($= V_{bg,0}$) and $V_{bg,0} + 0.2$ V with a modulation bandwidth of 100 MHz at a carrier frequency of 32 and 40 GHz.

TABLE I
SUMMARY OF STATE-OF-THE-ART CMOS-SOI-BASED PA PERFORMANCE IN CONTINUOUS-WAVE (CW) MODE
AND WITH 64-QAM ON A SINGLE-CARRIER (SC) OR ON OFDM (5G NR)

	This work	ISCAS'22 [35]	ISSCC'20 [26]	JSSC'19 [36]	CICC'20 [37]	TMTT'21 [38]	EuMC'22 [39]	SSCL'21 [21]	EuMIC'23 [40]
Technology	22 nm FD-SOI		45 nm PD-SOI		22 nm FD-SOI			28 nm FD-SOI	
Architecture	Distributed balun	RC feedback 1-stage diff.	Distributed balun	Mixed-signal Doherty	Current combining	Doherty	2-stacked diff.	Adaptive bias control	Broadband balanced
Supply (V)	2.4	1.8	2	2	2.4	2.4	1.6	2	2
Frequency (GHz)	24-43	19.1-46.5	24-42	27	28	28	28	28-34	22-42
Gain (dB)	17.4-27.7	13.4-16.4	17.5-20*	19.1	27	26.1	23.5	13.8	21*-23
P_{sat} (dBm)	16.6-18.6	12.9-14.6	17.9-20.4	23.3	21.7	22.5	21	17.4-17.8	18*-20.7
PAE_{max} (%)	27.2-36.4	15.2-26.1	35-45	40.1	27.1	28.5	31.5	37.8-42.5	20-34.9
$P_{out,1dB}$ (dBm)	16.2-18.1	9.2-11.5	15.7-19.6	22.4	19.1	21.1	19.2*	16.9-17.4	N/A
Modulation	64-QAM 5G NR	256-QAM 5G NR	64-QAM 5G NR	64-QAM SC	64-QAM SC	64-QAM SC	64-QAM OFDM	64-QAM SC	64-QAM 5G NR
Bandwidth	100 MHz 800 MHz	9x100 MHz	800 MHz	N/A	N/A	N/A	100 MHz	400 MHz	200 MHz
PAPR (dB)	12.43	8	9.64	6.5	6.4	N/A	N/A	8.65	N/A
EVM _{rms} (dB)	-25.2	N/A	-25.4	-25.3	-25	-25.1	-28	-25.1	-22.1
Carrier frequency (GHz)	27/40 27/40	28/39	28/39	27	28	28	28	28/31	28
P_{mean} (dBm)	9.2/8.3 7.5/6	6.6/5.6	11.3/10.2	15.9	12.9	10.9	12.5	9.4/9.1	12.2
PAE_{mean} (%)	13/8.7 7.3/5	6.2/5	16.6/13.4	29.1	9	9.2	6.7	12.8/12.7	11.8

*: Estimated from graph.

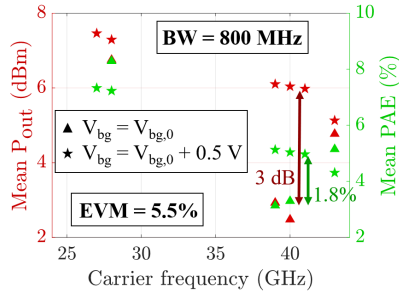


Fig. 13. 5G NR 800MHz-bandwidth modulated signal measurements of different carrier frequencies at the EVM target of 5.5 %, average PAE and P_{out} versus carrier frequency. Measurements for two biases: $V_{bg} = V_{bg,0}$ (triangles) and $V_{bg} = V_{bg,0} + 0.5$ V (stars).

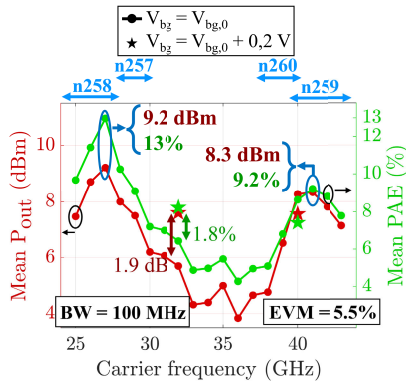


Fig. 14. 5G NR 100MHz bandwidth modulated signal measurements of different carrier frequencies at the EVM target of 5.5 %, average PAE and P_{out} versus carrier frequency, at $V_{bg} = V_{bg,0}$ (dots, solid lines) and $V_{bg} = V_{bg,0} + 0.2$ V (stars).

V. BENCHMARKING

For completeness and benchmarking this PA's performance, measured mean P_{out} and PAE for a target EVM of 5.5 % of the PA fed by a 5G NR 100 MHz bandwidth input signal are shown at different carrier frequencies in Fig. 14 for a

$V_{bg} = V_{bg,0}$ bias, which is the optimal bias at 40 GHz with a 100 MHz bandwidth signal.

Even though it does not provide the best achievable performance, it is enough for proper benchmarking. Indeed, tracking the optimal bias condition for each carrier frequency and signal bandwidth would require extensive characterization and is out of scope of this paper, which demonstrates instead with different 5G signals that the back-gate bias is an interesting and straightforward solution to fine tune the PA behavior and performance.

Table I presents state-of-the-art PAs in SOI CMOS technologies in 24 to 43 GHz bands. The presented PA features 1dB P_{out} and PAE in line with the state of the art of narrow-band PAs over a broad frequency range. It even outperforms other wideband PA in 22 nm FD-SOI technology. The recent wideband PA design in 28 nm FD-SOI [40] features increased output power for a similar efficiency. The reason is partially due to the use of a larger V_{ds} bias of 1 V for each stacked FET (instead of 0.8 V here) that greatly boosts the output power. Using a V_{ds} bias larger than the value recommended by the technology can improve performance, but it increases the voltage stress on transistors, which can speed up the aging process and lead to early circuit failure. Reliability considerations are primordial in PA design, but they are out of scope for this paper.

Paper [21] describes an interesting PA design making use of the back-gate feature in FD-SOI technology. With a special care to linearity in the PA design, they use adaptive back-gate biasing to further improve the PA linearity, hence reducing the amount of back-off power needed to fulfill modulated signal measurements requirements and achieving a boost in mean power and efficiency. The PA in [21] features similar performance to our design, but it is restricted to a lower bandwidth (around 28 to 34 GHz).

Modulated signals measurements indicate that the PA is well suited to 5G modulations and performs well compared to the state of the art, taking into account that the test signal used

in this paper features a larger PAPR of 2 – 3 dB. Techniques to reduce the PAPR of 5G signals exist (such as transform precoding [41]), but they have not been applied to this work. Operating with a larger PAPR implies that the PA needs to work even more in backoff power (with 2-3 dB more) to achieve the same EVM. In other terms, for the same EVM target, this waveform (instead of the ones with lower PAPR used in the literature) will result in lower PA efficiency and output power, thus underestimating its performance under modulated signal measurements when compared with other publications. Even though [40] seems to be performing better than the presented PA under modulated signal measurements, it should be noted that the mean P_{out} and PAE are reported for an EVM of 7.9 % (-22.1 dB) in [40] instead of 5.5 % (-25.2 dB) for the remaining papers. So, the output power and efficiency figures reported in [40] for 5G NR modulated signal do not compare well with this paper (see Fig. 10(a)).

Although the proposed FD-SOI-based PA features close but lower performance than 45 nm PD-SOI PAs, it can benefit from (i) tuning provided by the back-gate access as demonstrated above, and (ii) higher logic density from the advanced 22 nm FD-SOI CMOS node to integrate more functions in a single low-cost chip.

VI. CONCLUSION

The worldwide deployment of the new 5G telecommunication standard necessitates wideband or multiband 5G systems to support international cross-network roaming. In this context of configurability, flexibility and large scale deployment, CMOS technology becomes a serious contender for 5G applications, singularly FD-SOI technology that benefits from the unique tuning capabilities of its back-gate bias.

A dual-band PA covering the n257 to n260 bands in the 22 nm FD-SOI CMOS technology is presented, featuring a wideband distributed balun at the output. It achieves a saturated output power and peak efficiency up to 18.6 dBm and 36.4 %, respectively, which are comparable with narrow-band PAs reported in the literature at similar frequencies and on similar technologies. An experimental analysis on how the PA responds to back-gate bias variation is carried out both in CW and 5G NR modulated signal conditions. CW measurements show that the back-gate bias can be used to fine control the operating class and thereby trade-off AM-AM for AM-PM distortion. Modulated signal measurements show that, thanks to this trade-off, the average output power and efficiency can be optimized by varying the back-gate bias, and the optimal value of V_{bg} depends on (i) the signal bandwidth, (ii) the carrier frequency and (iii) the target EVM value. This study therefore opens a direct path toward configurable PA design with dynamic back-gate configuration, i.e. where the back-gate can be chosen to optimize in real time the FD-SOI-based PA performance with a high sensitivity level as a function of the 5G signal modulation properties.

Finally, the PA exhibits a mean output power and efficiency of 7.5 dBm and 7.3 % at 27 GHz, 6 dBm and 5 % at 40 GHz, for a 800 MHz bandwidth 64-QAM 5G NR signal with a realistic >12 dB PAPR (without precoding). This dual-band PA outperforms other wideband/multiband PAs in FD-SOI

technology and even competes with narrow-band designs in FD-SOI.

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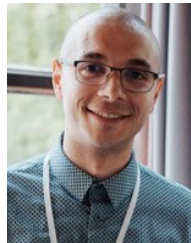
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M. Rack (Member, IEEE) was born in Oxford, England, in 1991. He received the B.S., M.S., and Ph.D. degrees in electrical engineering from Université catholique de Louvain, Louvain-la-Neuve, Belgium, in 2012, 2014, and 2021, respectively. Since then, he has been a Senior Researcher at Université catholique de Louvain, Belgium, whose interests include the integration of RF and mm-wave functionalities in silicon technologies. To that end he is involved in the complete modeling of semiconductor substrates for the evaluation of their impact on RF and mm-wave front-end circuitry, along with the development of novel high-performance RF substrate solutions. In particular, he is working on modelling and understanding substrate effects from fundamental material parameters to the high-level impact on the design and performance of mm-wave circuit modules in advanced SOI nodes.



Y. Bendou (Graduate Student Member, IEEE) was born in Rabat, Morocco, in 1997. Starting 2015, he studied for two years under engineering preparatory classes in CPGE Moulay, his hometown. He joined the Grenoble Institute of Technology, France, in 2017, to continue his engineering curriculum. He then enrolled a M.S. degree in micro and nanotechnology for integrated systems, jointly delivered by l'École Polytechnique Fédérale de Lausanne (EPFL), Switzerland, the Politecnico di Torino (Polito), Italy, and Grenoble INP Phelma, France, in

2020. He is currently pursuing the Ph.D. degree with the Université catholique de Louvain, Belgium, in collaboration with the company STMicroelectronics in France, on the design of RF and mm-wave integrated circuits on the 28nm FDSOI technology benefiting from the advantages of high resistivity substrates.

S. Wane (Member, IEEE), photograph and biography not available at the time of publication.

J. B. Sombrin (Member, IEEE), photograph and biography not available at the time of publication.



J.-P. Raskin (Fellow, IEEE) received the M.S. and Ph.D. degrees in applied sciences from Université catholique de Louvain (UCLouvain), Louvain-la-Neuve, Belgium, in 1994 and 1997, respectively. In 1998, he joined the EECS Department of The University of Michigan, Ann Arbor, USA, for a post-doc of two years. In 2000, he joined the Microwave Laboratory of UCLouvain, Louvain-la-Neuve, Belgium, as an Associate Professor, and he has been a Full Professor since 2007. From September 2009 to September 2010, he was Visiting Professor at Newcastle University, Newcastle Upon Tyne, U.K. He is author or co-author of more than 400 scientific journal articles. His research interests are the modeling, wideband characterization and fabrication of advanced SOI MOSFETs as well as micro and nanofabrication of MEMS / NEMS sensors and actuators, including the extraction of intrinsic material properties at nanometer scale. He is involved in the development of a more sustainable electronics. He has been managing a Chair of Excellence in eco-innovation at CEA-Leti since January 2024. He received the Médaille BLONDEL 2015, the SOI Consortium Award 2016, the European SEMI Award 2017, the Médaille AMPERE 2019, the Georges Vanderlinden Prize 2021 and the IET Achievement Medal in Electronics 2022, in recognition in his vision and pioneering work for RF SOI. He has been elected member of the Royal Academy of Belgium in 2023.



D. Lederer (Member, IEEE) received the Electrical Engineering and Ph.D. degrees in applied sciences degree from the Université catholique de Louvain, Belgium, in 2000 and 2006, respectively. He then pursued post-doctoral studies at the Tyndall National Institute, Cork, Ireland where he worked on the fabrication and characterization of Si nanowires. From 2000 till 2006, he was a Research Assistant on the wideband characterization of advanced SOI material and devices for high frequency applications.

He joined the private sector in 2008 to develop electronics and microwave products for circa 15 years within the Research and Development teams of various small and large companies. From 2016 till 2020, he joined Global Foundries where he worked on the development of SOI-based technologies for microwave and mmWave applications (5G, 6G, IOT, automotive radars). He joined UCLouvain in 2020 as a Professor and conducts research in the field of THz technologies, devices and circuits. He is the owner of six patents and the author and co-author of more than 140 technical papers and conference contributions.