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Area-Efficient nA-to-μA Constant-with-Temperature CMOS Current References for the Internet of Things

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Thesis submitted in partial fulfillment
of the requirements for the degree of
Docteur en sciences de l'ingénieur et technologie

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April 2024

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Abstract

OVER more than a decade, Internet-of-Things (IoT) applications have driven the development of ultra-low-power sensor nodes embedding intelligence at the edge, which must comply with several critical design constraints to operate reliably and efficiently over time. First, they need to meet stringent constraints on their power consumption as they are either supplied by limited-capacity batteries or energy harvesting, thus requiring an average power consumption ranging from 0.1 to 100 μW. Next, the silicon area they occupy must be minimized to limit the footprint and the cost of their production. Finally, they must be robust against process, supply voltage and temperature (PVT) variations, to withstand a wide range of operating conditions. Among such integrated circuits (ICs), reference circuits and more specifically current references are crucial components as their sensitivity to PVT variations undermines the performance of common analog building blocks of IoT nodes, such as real-time clock generators, data converters, temperature sensors, resistive or capacitive sensor interfaces, etc. In addition, the current they generate to bias these analog blocks must usually lie within the nA range to comply with the power constraints of IoT nodes while providing a reasonable performance.

In this thesis, we aim at identifying the main current generation techniques, at understanding their fundamental trade-offs, and at developing novel current reference architectures whose characteristics better concur with the needs of IoT applications. To do so, we first categorize existing current generation mechanisms through a comprehensive review of the literature of constant-with-temperature (CWT) current references. We then establish the requirements of IoT applications and discuss their impact on the references' specifications. This study also highlights that current references that are simultaneously simple, area-efficient, robust to PVT variations, and able to generate a current in the nA range, are scarce in the state of the art or have not been validated by silicon measurements.

Next, we develop current references that are well suited to the needs of IoT applications, with a focus on keeping design complexity to a minimum, minimizing

their impact in terms of power consumption and silicon area without compromising other key figures of merit such as line sensitivity (LS) and temperature coefficient (TC), and maintaining performance across process corners using trimming. These novel architectures rest upon two main elements. On the one hand, a first group of references exploits the threshold voltage difference between two transistors, obtained through forward body/back-gate biasing and applied to a voltage-to-current (V-to-I) converter to generate a nA-range CWT current. On the other hand, a second group makes use of two-transistor subthreshold voltage references buffered by a single transistor on a V-to-I converter, to generate CWT current references in the μA and nA range. Moreover, this work reveals that self-cascode MOSFETs (SCMs) biased by a proportional-to-absolute-temperature (PTAT) voltage with a CWT offset voltage can be used as a nonlinear yet area-efficient V-to-I converter for the generation of a nA-range CWT current, thus further reducing silicon area. In the nA range, these SCM-based references are more area-efficient than their resistor-based counterparts, but typically lead to a slightly larger TC between 100 and 500 ppm/°C, as the nonlinear temperature dependence of the specific sheet current is compensated by that of the transistor's inversion level. On the contrary, resistor-based references rely on matching the TCs of a reference voltage and a resistance, whose temperature dependence is typically quasi-linear. These references are thus able to achieve sub-100-ppm/°C TCs at the cost of increasing the silicon area they occupy. These concepts are demonstrated through post-layout simulations, and measurements of four fabricated chips in bulk, partially-depleted silicon-on-insulator (PD-SOI), and fully-depleted SOI (FD-SOI) technologies, thus validating that the proposed ideas can be readily applied to a wide range of technologies. The improvement of the state of the art in terms of a figure of merit combining TC and silicon area reaches at least 34.6× for the most competitive CWT nA-range references and 8.7× for the CWT μA-range one.

At last, we come back to our review of CWT current references to identify which applications and analog circuits actually require a temperature-independent current. This analysis highlights that biomedical devices either do not require a CWT current as they operate in a temperature-regulated environment, or only mildly benefit from it as they function over a reduced temperature range that a human can withstand. In contrast, IoT sensor nodes are a relevant use case of CWT references. In addition, our study reveals that, among analog circuits, only a limited number of them actually require a CWT current, contrary to what is traditionally claimed in the literature. Amplifiers and comparators indeed require a PTAT current to maintain a constant bandwidth and delay with temperature. Oscillators and temperature sensors can benefit from a CWT current, but effective alternative architectures which can do without it have emerged to cope with the absence of simple CWT nA-range references. Only data converters such as current-steering DACs and current-mode ADCs are in critical need of a CWT current.

Author's publication list

Related journal papers

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DOI: 10.1109/TCSI.2022.3172647

JP2. M. Lefebvre, D. Flandre, and D. Bol, "A 1.1- / 0.9-nA Temperature-Independent 213- / 565-ppm/°C Self-Biased CMOS-Only Current Reference in 65-nm Bulk and 22-nm FDSOI", *IEEE Journal of Solid-State Circuits*, vol. 58, no. 8, pp. 2239–2251, Aug. 2023.
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UJP1. J. Van Verdeghem, M. Lefebvre, V. Kluyskens, and B. Dehez, "Dynamical Modeling of Passively Levitated Electrodynamic Thrust Self-Bearing Machines", *IEEE Transactions on Industry Applications*, vol. 55, no. 2, pp. 1447–1460, Nov. 2018.
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*These authors have contributed equally to this work.
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List of acronyms

ACM	Analog Compact MOSFET
ADC	Analog-to-Digital Converter
AFE	Analog Front-End
BBCO	Back-Bias-Controlled Oscillator
BGR	Bandgap Reference
BJT	Bipolar Junction Transistor
BPSK	Binary Phase-Shift Keying
CAS	Circuits and Systems
CDF	Cumulative Distribution Function
CS	Current-Steering
CSRO	Current-Starved Ring Oscillator
CTAT	Complementary-To-Absolute-Temperature
CV	Coefficient of Variation
CWT	Constant-With-Temperature
DAC	Digital-to-Analog Converter
DIBL	Drain-Induced Barrier Lowering
DTI	Deep Trench Isolation
ECG	Electrocardiogram
EEG	Electroencephalogram
EKV	Enz-Krummenacher-Vittoz
EMG	Electromyogram
FBB	Forward Body Bias
FD-SOI	Fully-Depleted Silicon-on-Insulator
FLL	Frequency-Locked Loop
FF	Fast nMOS-Fast pMOS
FS	Fast nMOS-Slow pMOS
FoM	Figure of Merit
GAA	Gate-All-Around
GBW	Gain-Bandwidth
GF	GlobalFoundries
GhG	Greenhouse Gases
GIDL	Gate-Induced Drain Leakage
HS	High-Speed
HVT	High-V_T
IA	Instrumentation Amplifier
IC	Integrated Circuit

ICT	Information and Communication Technologies
IMD	Implantable Medical Device
IoT	Internet of Things
LDO	Low Dropout
LL	Low-Leakage
LPF	Low-Pass Filter
LS	Line Sensitivity
LVT	Low-V_T
MC	Monte-Carlo
MCU	Micro-Controller Unit
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
OTA	Operational Transconductance Amplifier
PC	Personal Computer
PDK	Process Development Kit
PCR	Peaking Current Reference
PD-SOI	Partially-Depleted Silicon-on-Insulator
PLL	Phase-Locked Loop
PMU	Power Management Unit
PPA	Power Performance Area
PTAT	Proportional-To-Absolute-Temperature
PVT	Process, Voltage and Temperature
RBB	Reverse Body Bias
RF	Radio Frequency
RTC	Real-Time Clock
RVT	Regular-V_T
SAR	Successive Approximation
SCM	Self-Cascode MOSFET
SF	Slow nMOS-Fast pMOS
SLVT	Super-Low-V_T
SMU	Source Measure Unit
SS	Slow nMOS-Slow pMOS
SS	Single-Slope
TC	Temperature Coefficient
TCR	Temperature Coefficient of Resistance
TSMC	Taiwan Semiconductor Manufacturing Company
TT	Typical nMOS-Typical pMOS
ULL	Ultra-Low-Leakage
ULP	Ultra-Low-Power
UMC	United Microelectronics Corporation

Acknowledgments

Before diving into the technical content of this thesis, I would like to address my deepest gratitude to the people who contributed directly or indirectly, largely or more modestly, to my journey as a Ph.D. candidate. To do so, I will switch to my native language, French, except for the acknowledgements addressed to non-French speakers.

Avant tout, je tiens sincèrement à remercier mon promoteur, le Professeur David Bol, qui m'a accompagné durant toutes ces années au sein du groupe de circuits et systèmes électroniques (ECS). David, merci pour ton encadrement, ta franchise, ton regard critique, et ta recherche de l'essentiel, tant dans le développement de circuits électroniques que dans le choix de leurs applications. J'ai apprécié l'ouverture que tu as apportée au groupe de recherche, initialement centré sur les circuits à basse consommation, au travers de questions d'analyse de cycle de vie et de soutenabilité. Cette ouverture a vraiment été enrichissante pour moi, et m'aura clairement permis d'être plus conscient des enjeux environnementaux liés à notre activité professionnelle, ainsi que de pouvoir poser un regard plus critique sur les applications visées. Merci également de m'avoir fait confiance dans le chemin sinueux qu'a été ma thèse, passant par les capteurs d'image convolutifs au début, faisant un détour par les algorithmes bio-inspirés ensuite, et se terminant par beaucoup de circuits de références de courant. Merci également pour ton attention dans les moments difficiles, en particulier lors du décès de mon grand-père maternel. Je te souhaite d'arriver à trouver l'équilibre idéal dans le groupe entre les circuits électroniques d'une part et l'analyse de leurs impacts d'autre part, et de garder la curiosité intellectuelle qui est la tienne.

Je tiens ensuite à adresser mes remerciements au Professeur Denis Flandre, qui a par ailleurs accepté d'occuper le rôle de secrétaire de mon jury de thèse. Denis, merci à toi pour les discussions que nous avons pu avoir autour de mon sujet de thèse, mais également autour du sujet des capteurs d'image convolutifs. J'ai particulièrement apprécié ta rigueur scientifique toujours au rendez-vous et ta capacité incroyable à tout de suite mettre le doigt sur ce qui ne va pas dans un circuit élec-

tronique, couplée à une connaissance encyclopédique de l'état de l'art. Merci également d'avoir pu te rendre disponible malgré ton agenda de ministre pour discuter, entre autres, de la meilleure façon de répondre à certains reviewers récalcitrants, ou de l'une ou l'autre idée farfelue de circuits qui me trottait en tête.

I also want to personally thank all the other members of my Ph.D. thesis jury, namely Prof. Christophe Craeye, Prof. Paolo Crovetti, Prof. Pieter Harpe, and Dr. Julien De Vos, for the interesting discussions that we had during the private defense. People sometimes dislike the private defense as they feel like it is some kind of interrogatory. Yet, in my case, I felt that this was a really positive and constructive discussion, and I would like to thank you for that. Christophe, merci d'avoir accepté de présider mon jury de thèse et d'avoir parsemé le processus de tes traits d'humour habituels. Paolo, I really want to thank you for making the trip from Torino and for giving such an interesting talk to our research group before my private defense. It was a very enriching experience for me, and I hope we will find an opportunity to collaborate in the future. Pieter, I want to thank you for coming from Eindhoven, and for the interesting yet always-too-short discussions that we had before and during the private defense. It was a pleasure for me to have you in the jury and to benefit from your vast expertise in mixed-signal circuits. I am happy that we will see each other again at CICC and ESSERC this year. Julien, merci d'avoir apporté ta vision à mi-chemin entre le monde académique dont tu es issu, et le monde industriel dans lequel tu travailles. J'ai trouvé vraiment intéressant et utile d'avoir un point de vue plus extérieur pour challenger les résultats obtenus dans ma thèse. Merci à toi pour cela. J'espère que nous aurons encore l'occasion d'échanger à l'avenir.

Malgré ce que beaucoup de personnes semblent croire, une thèse est loin d'être une aventure solitaire, bien loin de là ! Et je dois admettre que j'ai été bien entouré par mes collègues, en particulier du groupe ECS, du début à la fin de ma thèse. Je tenais donc à remercier celles et ceux qui ont croisé ma route. D'abord, l'équipe des assistants et chercheurs qui m'ont donné cours et m'ont par la suite accueilli dans le groupe: Pierre-Antoine, Thomas, Ludovic, Charlotte, Cecilia, François. Merci à vous de m'avoir donné envie de découvrir l'électronique et d'en faire mon métier. Merci ensuite à tous les membres du groupe avec qui j'ai partagé de beaux moments, dans la joie comme dans l'effort, en conférence ou pendant de sacrées aventures de tape-out: Maxime, Pengcheng, Rémi, Marco, Mathieu, Roghayeh, Julien, Thibault, Pol, Sylvain, et bien sûr Adrian. On en aura parfois bien bavé, mais quand je vois le chemin parcouru en terme de complexité et de qualité des chips qu'on a réalisés, je pense qu'il y a de quoi être collectivement fiers du travail accompli ces dernières années. Merci enfin aux chercheuses et chercheurs qui se sont courageusement lancé·e·s dans une nouvelle page du groupe, centrée sur l'analyse des impacts des circuits et systèmes électroniques au sens large: Thibault, Louis, Augustin, Robin, et Ludmila. Merci pour l'ouverture apportée au groupe par vos

nouvelles directions de recherche, et merci d'avoir gentiment supporté nos vieilles histoires de tape-out qui ne devaient pas vous parler beaucoup en arrivant. De façon générale, merci à toutes et tous pour les chouettes moments passés ensemble, autour d'un verre, lors des activités de team building du groupe, des mémorables *Questions pour un chercheur* préparées par Adrian, des fameuses chasses des temps de midi, et j'en passe. Si j'arrive au bout de cette thèse avec tant de bons souvenirs, c'est grâce à vous ! Parmi tous les collègues déjà cités plus haut, je me dois quand même de remercier encore plus particulièrement certains d'entre eux. Charlotte, je ne te remercierai probablement jamais assez de m'avoir pris sous ton aile au début de ma thèse. Merci pour ta bienveillance, ton écoute, tes conseils toujours avisés, mais merci aussi de m'avoir transmis, au moins en partie, ta rigueur scientifique, ton éthique professionnelle, ton sens du détail, et ton intérêt pour les circuits neuromorphiques digitaux. Je me réjouis des aventures scientifiques qui nous attendent dans les années à venir, peut-être avec une pointe de circuits mixtes en plus ? Rémi, on aura partagé le même bureau pendant la quasi-totalité de mes années dans le groupe, mais je dois dire que tu as su trouver la porte de sortie de la thèse nettement plus vite que moi. Merci pour les coups de main donnés à des moments critiques, qui m'auront permis de terminer les tape-outs de SleepSpotter et MANTIS dans les temps (ou presque). Merci aussi pour les discussions techniques et moins techniques qu'on a pu avoir autour des nombreux chips réalisés ensemble. Maxime, merci pour ta présence bienveillante dans le groupe tout au long de ma thèse, ton partage d'expérience, et tes commentaires toujours constructifs. Merci aussi pour les courses à pied pendant la période du COVID, qui m'ont permis de prendre un peu l'air et de se connaitre un peu mieux. Thibault, merci pour ta curiosité et ta confiance, d'abord en tant que mémorant, et ensuite en tant que collègue. J'ai beaucoup apprécié les interactions qu'on a pu avoir au travers du pool de review ECS et tes commentaires toujours très pertinents et bienveillants, même dans un domaine qui était éloigné de ton expertise première. Merci aussi pour ton énergie débordante, ta volonté et ta détermination à faire bouger les lignes, et ton enthousiasme communicatif ! Adrian, c'était vraiment un plaisir de partager le bureau, et à l'occasion la scène, avec toi. Merci pour l'émulation positive autour de nos questions de recherche respectives, pour les échanges informels du style *Est-ce que tu penses que ça marcherait si je faisais ça dans mon circuit ?*, pour les animations diverses et variées que tu as mises en place dans le groupe, ainsi que pour les grognements et bruitages dans le bureau. Je me réjouis que nos chemins se recroisent bientôt !

I would also like to more broadly thank colleagues in the Maxwell A.1 corridor, the ELEN departement, and the ICTEAM institute for the nice atmosphere and the discussions at the coffee machine during the last years. Among others, Léopold, Nicolas, Noémie, Grégoire, Margo, Charles, Anne-Sophie, Karim, Eléonore, Tom, Ottilie, Loïc, Clémentine, the COSY group, the RF team, the Crypto team, etc. J'aimerais également remercier les membres de la chorale du personnel pour avoir animé mes temps de midi pendant la dernière année de ma thèse. Un merci partic-

ulier à Laurine pour m'avoir une fois de plus entrainé dans un projet musical, et à notre ancien chef de chœur Stefano Poletto, pour sa rigueur et sa passion communicative de la musique, ainsi que pour l'opportunité de chanter avec un orchestre.

En tant qu'assistant, je tenais également à remercier les enseignants avec qui j'ai pu collaborer au cours des dernières années: Claude, Bruno, Christophe, Denis, Jean-Didier, David, Laurent, Delphine, Benoit, Thomas, et Jean-Charles. J'ai également une pensée pour tous les collègues et tuteurs avec qui j'ai participé à l'encadrement des TPs, mais dont je n'oserais en tout cas pas faire une liste de peur d'oublier quelqu'un. Je tenais également à adresser un merci tout spécial à Delphine Ducarme et Sophie Labrique, que j'ai eu l'occasion de côtoyer pendant presque dix ans maintenant, d'abord comme tuteur puis comme assistant, et qui sont le fer de lance de tant d'initiatives pédagogiques à l'EPL et au-delà. Merci à vous deux pour votre énergie, votre motivation à changer les choses et à faire évoluer les mentalités et les pratiques, votre bienveillance. Merci également aux membres de l'association des assistants de l'EPL, dont je fais partie, pour le travail de représentation que vous réalisez chaque année.

Enfin, je tenais à saluer le travail formidable réalisé par les membres du personnel administratif et technique. Merci à Anne et Viviane pour votre aide toujours efficace et rapide avec les différentes commandes et pour les papotes de temps à autre, à Christel pour ta gestion des comptes, à Isabelle pour tout ce que tu fais pour les commissions de programme et le département, souvent sans que les gens en soient conscients. Merci également à Pascal et Valeriya pour votre temps et votre aide si précieuse en Welcome. Un merci tout particulier à Pierre Gérard pour la réalisation des setups de mesure utilisés dans le cadre de ma thèse. Sans ton travail, il m'aurait tout simplement été impossible d'obtenir les résultats que j'ai obtenus dans cette thèse. Merci également pour ta disponiblité, ta flexibilité, et ta créativité pour répondre à des demandes pas toujours évidentes ni claires. Merci également à Souley et Benoit pour votre gestion du matériel pour les cours, et pour l'aide et les conseils avisés dans la réalisation de circuits imprimés et de soudures diverses et variées. Finalement, merci à Brigitte pour ta gestion de notre infrastructure informatique et de nos serveurs. Merci pour ton énergie et ton dévouement, il est évident que tu joues un rôle clé dans notre capacité à pouvoir mener à bien notre recherche. A titre personnel, j'espère avoir finalement accédé au titre tant convoité de *gypaète barbu* qui me fera certainement autant plaisir que celui de docteur.

Finalement, sur une note plus personnelle, il me reste à remercier mes amis et ma famille, qui m'ont soutenu pendant toute la durée de cette thèse. Mes anciens colocataires Céline, Sébastien, Nicolas, Antoine, Charles, Victoria, pour les discussions cathartiques à propos de nos thèses respectives. Un merci tout particulier à Antoine et Charles pour les repas et boissons de qualité pendant le confinement, et les discussions jusqu'à pas d'heure, qui ont permis de mettre un peu de fun dans cette période pas très drôle. Merci aussi à tout le cercle d'amis du Kotangente et

associés: Philippe, Olivier, François, Vincent, Nicolas, Joachim, Charles, Antoine, Louis, et Florimond. Etant donné la proportion d'entre vous qui a aussi fait une thèse, qui plus est à l'UCLouvain, vous étiez bien placés pour en comprendre les hauts et les bas. Merci pour votre présence bienveillante tout au long de ces années. Merci également aux amis doctorants/docteurs de la team *Mariage en Italie*, à savoir Nicolas, Pauline, Alessandra, Jacopo, Colin, Antoine, Oriane, pour les bons moments passés ensemble dans un passé plus récent.

Toutefois, je n'en serais pas là aujourd'hui sans le soutien de deux personnes très spéciales. D'abord, ma maman, qui m'a transmis son sens du devoir, sa passion du travail bien fait, et sa propension à remplir son agenda à outrance. Merci pour ton soutien indéfectible depuis toujours, et merci d'avoir toujours été une présence discrète mais importante quand j'en avais besoin. La seconde personne que je tiens absolument à remercier, c'est ma compagne Eléonore. Merci pour ta patience et ta compréhension dans les moments difficiles, en particulier les périodes de rush de fin de tape-out où je terminais à pas d'heure de façon récurrente. Merci pour ton soutien inconditionnel dans les hauts comme dans les bas, ainsi que pour les *cookies d'urgence spécial tape-out* et les petits gâteaux dans leur étui à gâteau, qui m'ont permis de traverser ces épreuves avec si pas le sourire, au moins le ventre plein. Merci également pour les *shootings* de tous les chips récents du labo, qui m'auront permis d'avoir de jolies images à mettre dans mes articles.

Finalement, je voudrais conclure ces remerciements en rendant hommage à mon grand-père maternel, qui est décédé pendant la rédaction de cette thèse. Merci à toi pour l'exemple que tu nous as donnés, et pour ta vie passée à te battre pour les plus démunis. Puissent tes actions continuer à nous inspirer pendant de nombreuses années encore.

Introduction

To invent, you need a good imagination and a pile of junk
– Thomas Edison

SINCE the invention of the point-contact transistor by Bardeen, Brattain, and Shockley in 1947, electronic circuits and systems have never ceased to reduce in size following Moore's law [1], leading to a consistent increase in the number of transistors per chip as well as a steady reduction of the cost per transistor. This trend has allowed chips to fulfill tasks of increasing complexity while becoming a commodity affordable to most people. Therefore, electronic circuits have been a crucial enabler of technological innovations that have profoundly changed our societies and our way of living, such as personal computers (PCs) and information and communication technologies (ICT). For more than a decade, the Internet of Things (IoT) has been presented as the latest step in this quest for an evermore comfortable life supported by technological progress. The key idea of the IoT consists in equipping every *thing* with sensing, processing and communication capabilities, all of these *things* being connected together through the Internet or mobile networks. This concept has led to the development of so-called smart objects, i.e., objects embarking some computing power in order to extract meaningful information from the sensed data, before transmitting it to the cloud through a wireless link [Fig. 0.1(a)]. Two striking features of the IoT are (i) the massive number of devices projected to be deployed, estimated between 20 and 50 billions in 2020 [2] and expected to reach a trillion devices by 2035 [3], even though more recent predictions suggest that the annual production of IoT devices would only be of 29 billions in 2030 [4] compared to more than 50 billions in [3], and (ii) the unprecedented level of pervasiveness targeted by this new kind of electronic device. From an applicative standpoint, the IoT is poised to support a broad range of applications among which health monitoring with wearable devices [5], environmental and ecosystem monitoring with edge sensor nodes [6], predictive maintenance of machines for the industry 4.0 [7, 8], smart homes [9], buildings [10], and cities [11], etc. Nonethe-

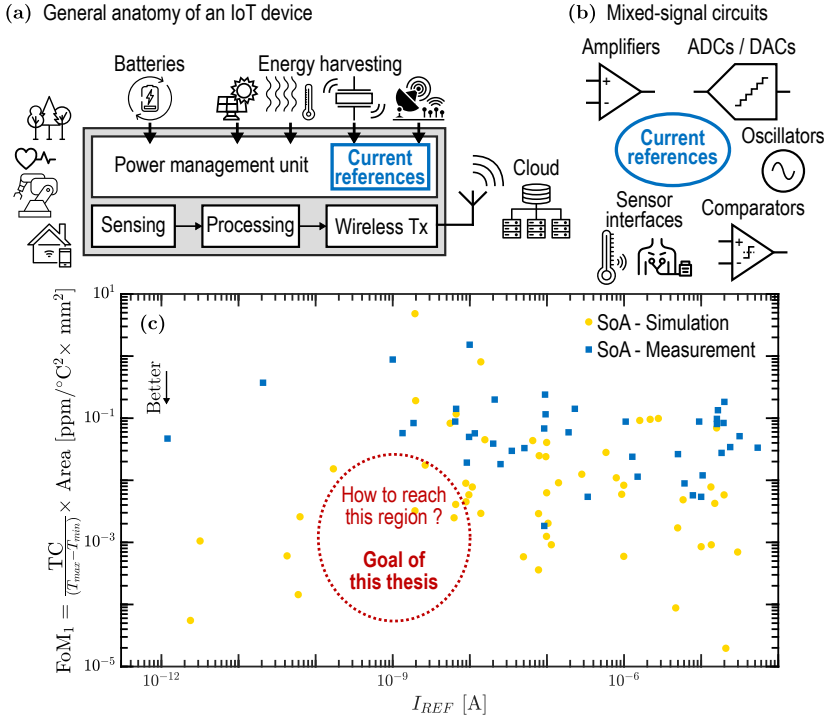

Fig. 0.1 (a) Structure of an IoT device, going from applications on the left to data transmission to the cloud on the right. (b) Examples of mixed-signal circuits relying on current references for their operation. (c) Illustration of the state of the art of CWT current references, with the performance in terms of silicon area and temperature independence on the y-axis, based on a figure of merit (FoM) defined in Chapter 1, and the reference current on the x-axis. The highlighted region corresponds to the region targeted by current references in the context of the IoT, and thus to the goal of this thesis.

less, the advent of the IoT also raises serious concerns regarding the relevance of some of these applications to our societies, especially in the context of the climate crisis that our world is facing, which calls for a necessary transition towards a more sustainable lifestyle so as to remain below planetary boundaries [12]. Besides, the IoT inevitably comes with direct environmental impacts, the most obvious ones being related to the embodied carbon footprint due to the production of the devices. A worst-case deployment scenario predicts that the IoT footprint could reach as much as 1 $GtCO_2$-eq/year by 2027 [13], emphasizing the need for environmental constraints and political action to keep the IoT development in check. From a technical standpoint, the development of IoT devices and sensor nodes comes with significant challenges. First, these devices are usually supplied by limited-capacity batteries [14, 15] or by harvesting energy from the environment [16, 17], e.g., solar power, vibrations, heat, radio-frequency (RF) signals, etc [Fig. 0.1(a)]. This imposes

stringent constraints on their average power consumption and requires to develop circuits operating at an ultra-low power in the sub-mW range or below. Furthermore, IoT devices are deployed in a broad diversity of applicative contexts, and must therefore be able to cope with variations of their supply voltage and temperature of operation. Finally, given the excessively large production volumes projected for IoT nodes, the silicon area of each device must be minimized to limit the economical costs, a first concern that is well understood by circuit designers. Reducing the silicon area for a fixed technology node also allows to decrease direct environmental impacts, a second concern that has emerged in recent years. The order of magnitude of these direct impacts is currently estimated between 1 and 4 $kgCO_2$-eq/cm^2 [18, 19], depending on the technology node and on the scope of assessment, and should therefore be considered in further technological developments.

Research Question

As the vast majority of electronic devices, IoT sensor nodes include analog and mixed-signal circuits such as amplifiers, comparators, data converters, oscillators, sensors and interface circuits, whose operation requires a bias current [Fig. 0.1(b)]. Current references are thus a crucial component of any integrated circuit (IC), whose dependence to process, voltage and temperature (PVT) variations can significantly impact the performance of the circuits they bias. Moreover, this dependence also affects the overall performance of the electronic system in which they are embedded. In the context of IoT devices, references generating a current in the nA range are well suited to the requirement for an ultra-low power consumption, as they allow to support analog functions (i) in sleep mode for devices with a relatively large power budget such a low-power micro-controller units (MCUs) [20, 21], or (ii) in active mode for devices with a highly-constrained power budget such as millimeter-size sensor nodes [14]. However, existing architectures currently fail at simultaneously achieving area efficiency and temperature independence in the nA range, as illustrated in Fig. 0.1(c) using a proposed figure of merit (FoM) combining the temperature coefficient (TC) and silicon area of the reference, and based on the state of the art of constant-with-temperature (CWT) current references over the time period 2000-2023. Furthermore, in the last two decades, research has led to significant progress in voltage references, yielding simple yet power- and area-efficient architectures consisting of only a handful of transistors [22, 23, 24, 25], without degrading other key performance metrics such as the line sensitivity (LS) and temperature coefficient (TC). The improvements of voltage references and the fact that existing current references have not been designed to meet the specific requirements of IoT sensor nodes suggest that further improvements could be obtained by revisiting existing current reference architectures. In this thesis, we conduct an in-depth analysis of existing CWT current references and of their applica-

tions, based on which we develop novel area-efficient and CWT current reference architectures providing answers to the research question

How can current references be improved to better suit the needs of Internet-of-Things (IoT) sensor nodes ?

Thesis Outline

In order to tackle this main research question, this thesis will consecutively address the three following secondary research questions:

1. *What are the specific requirements for current references in the context of the IoT ?*
2. *How can we practically modify existing current references to meet the specific requirements of the IoT ?*
3. *Do these improvements bring meaningful benefits to the applications of current references mentioned in the state of the art ?*

The general structure of this thesis reflects this thought process. Chapter 2 deals with the first research question, and analyzes the needs of IoT sensor nodes to identify the specifications that they must meet, and how these specifications translate into specific requirements for the current references they embed. It concludes by outlining potentially interesting research directions to be pursued in order to improve current references in the context of the IoT. Then, Chapters 3 and 4 investigate these leads to address the second research question, and propose five simple and area-efficient current reference topologies significantly improving the state of the art in terms of silicon area and temperature independence. All of them are demonstrated through post-layout simulations in several technologies, to ensure portability to various nodes, and through silicon measurements in at least one technology, to prove their correct operation in real-life conditions. Chapter 5 ultimately examines the applicative contexts and analog circuits commonly mentioned as requiring a reference current. It then assesses the relevance of CWT current references in these various contexts, to provide answers to the third research question. In this thesis, each chapter will start with a brief introduction indicating its location in the thought process outlined hereabove, and will end with concluding remarks summarizing the take-away messages. Besides, a brief summary of the content of each chapter and, most importantly, of its main contributions is provided herebelow.

Chapter 1 starts by introducing the **basic concepts and background knowledge** related to current references, namely their performance metrics, figures of merit (FoMs), and ways of categorizing them. Then, we conduct a **comprehensive literature review of CWT current references** over the period 2000-2023 and establish a

corpus of papers which will be used throughout this thesis. This second part identifies four main techniques to generate a CWT current: (i) to bias a voltage-to-current (V-to-I) converter with the difference of gate-to-source voltages ΔV_{GS} between two transistors, (ii) to bias a MOSFET close to its zero TC (ZTC) operation point with a temperature-dependent V_{GS}, (iii) to subtract or add currents with different TCs, and (iv) to bias a V-to-I converter with a voltage matching its TC. Finally, this chapter presents **trimming techniques** allowing to tune the reference current and its TC.

Chapter 2 analyzes the requirements of IoT sensor nodes in terms of power consumption, dependence to PVT variations, and silicon area, and translates them into **specifications for the current references in the context of IoT devices**. Next, we use the corpus established in Chapter 1 to **study the trends in existing current references** using four different categorizations, namely the type of work (simulation vs. measurement), the category of CWT current generation technique, the type of V-to-I converter, and the type of transistors used (MOSFET vs. BJT), in order to identify research directions to be explored in the next chapters. This analysis yields three potentially interesting **research directions for the development of area-efficient and CWT current references operating in the nA range**: (i) to use a resistor as V-to-I converter to benefit from its quasi-linear dependence to temperature, but with a lower bias voltage than previous works to reduce the silicon area necessary to implement it for a nA current, (ii) to use a self-cascode MOSFET (SCM) usually employed as V-to-I converter in PTAT references [26, 27, 28] to take advantage of its high area efficiency, but to devise a novel biasing scheme to obtain a CWT reference current, and (iii) to leverage the concept of two-transistor (2T) voltage reference buffered by a single transistor [29, 30] to reduce the area conventionally used by bandgap voltage references and their buffering stage implemented with an operational transconductance amplifier (OTA).

Chapter 3 presents **two CWT nA-range current references based on $\Delta V_{GS}/R$ structures** and on the threshold voltage difference ΔV_T between two weak-inversion transistors, obtained by **forward body biasing (FBB)** one of them to reduce its V_T. The first reference employs an **SCM biased by a β-multiplier which generates a PTAT voltage with a CWT offset voltage obtained by FBB**. This reference, fabricated in 22-nm fully-depleted silicon-on-insulator (FD-SOI), generates a 0.9-nA current with a 565-ppm/°C TC from -40 to 85°C, consumes 5.8 nW at 0.9 V, and occupies a silicon area of 0.0132 mm^2. However, the generated current presents a 9.2-% variability and a TC degraded by 2.7× compared to post-layout simulations, both effects being attributed to a skewed process corner. These shortcomings call for trimming mechanisms of I_{REF} and its TC to be implemented in further works. The second reference **biases a resistor with a ΔV_T generated by a peaking current reference through FBB**, and includes trimming mechanisms for I_{REF} and its TC, as well a leakage suppression circuit to mitigate the impact of parasitic diode leakage

at high temperature. It relies on a 2T voltage reference to generate the FBB of an nMOS, and a replica of the 2T reference to bias the nMOS' deep n-well so as to suppress the diode leakage. This reference, also fabricated in 22-nm FD-SOI, produces a trimmed 1.5-nA current with a 89-ppm/°C TC from -40 to 85°C, a power consumption of 2.87 nW at 0.75 V, and a silicon area of 0.00214 mm^2. The content of this chapter is adapted from our ESSCIRC [CP1] and JSSC papers [JP2] for the first reference, and from our upcoming JSSC paper [JP4] for the second reference.

Chapter 4 proposes **three *V*/*R* current references based on simple 2T/4T structures**, generating a reference voltage buffered on a V-to-I converter by a single transistor. In addition, these references **do not require any startup circuit** as the 2T reference makes the current references unstable at zero I_{REF}. The two first references employ a **2T voltage reference** respectively biasing (i) a **resistor with a voltage matching the temperature coefficient of resistance (TCR)** to generate a CWT μA-range current, and (ii) an **SCM with a PTAT voltage** to generate a PTAT nA-range current. Both references are fabricated in 0.18-μm partially-depleted SOI (PD-SOI). The first reference generates a 1.09-μA current with a 38-ppm/°C TC from -40 to 85°C, while consuming 0.71 μW at 0.65 V and using a silicon area of 0.0043 mm^2. In contrast, the second reference provides a 96-pA PTAT current with a power consumption of 0.28 nW at 0.55 V and a 0.0087-mm^2 area. Then, the third reference builds upon the **SCM-based architecture** presented in Chapter 3, and changes the way the PTAT voltage with a CWT offset voltage is generated from a β-multiplier to a **4T voltage reference**, thereby solving the limitations of the previous design. In addition, it includes a mechanism to trim the TC of I_{REF}. This reference is fabricated in 0.11-μm bulk and 22-nm FD-SOI. The 0.11-μm design delivers a 2.3-nA current with a 176-ppm/°C TC, while the 22-nm achieves a 2.5-nA current with a 82-ppm/°C TC. These designs respectively consume 11.1 and 10.4 nW at 0.8 and 1 V, with silicon areas of 0.0106 and 0.00255 mm^2. The content of this chapter is adapted from our TCAS-I paper [JP1] for the two first references, and from our upcoming JSSC paper [JP3] for the third reference.

Chapter 5 comes back to the corpus of current reference papers formed in Chapter 1, and identifies the **applications and mixed-signal circuits** in which current references are mentioned to be used. We identify that **the contexts in which a CWT reference current is relevant are actually less numerous than claimed in the literature**. In terms of applications, we observe that biomedical devices either do not require a CWT reference current, as implantable medical devices operate at a regulated temperature within the human body, or have a relatively limited need for it, as wearables work over a limited temperature range withstandable by a human. Nonetheless, IoT sensor nodes remain a relevant application of CWT current references. Next, in terms of analog and mixed-signal circuits, amplifiers and comparators often require a constant-g_m current, i.e., a PTAT current, to maintain their

bandwidth and delay constant with temperature, while oscillators and temperature sensors might benefit from a CWT current but also present effective alternatives which have emerged to cope with the absence of simple CWT nA-range current reference architectures. The only applications that clearly require a CWT current are data converters, mostly current-steering DACs which transform the digitally-controlled current into an output voltage, and current-mode ADCs comparing an input current to a CWT reference current.

At last, the conclusion of this thesis discusses the extent to which the proposed current reference topologies have advanced the state of the art, and thereby answered the main research question introduced hereabove. We ultimately discuss the limitations of the proposed architectures, outline research directions to be investigated in further works, and share some perspectives of this thesis.

1

Basics

If you cannot explain it to a six year old,
you do not understand it yourself.
– Albert Einstein

THE goal of this chapter is to present the basic concepts related to current references: (i) their performance metrics and figures of merit, (ii) the different topologies of current references, with a focus on constant-with-temperature (CWT) topologies, and (iii) the calibration techniques employed to trim the reference current and its temperature coefficient (TC).

1.1 What is a Current Reference ?

A current reference is an analog circuit that generates a reference current when it is properly power-supplied. This reference current is required by an overwhelming majority of analog blocks, such as operational amplifiers, data converters, oscillators, voltage regulators, sensor interfaces, temperature sensors, etc, generally to be used as a bias current. As such, its dependence on process, voltage, and temperature (PVT) variations, can significantly impact the performance of these analog blocks, and therefore, the overall performance of the system in which they are used. Practically, a current reference generates a bias voltage for an nMOS and/or a pMOS transistor, which can be used to copy this current in other analog blocks using a simple current mirror structure.

1.2 Performance Metrics and Figures of Merit

As any electronic circuit, current references are characterized by power, performance, and area (PPA) metrics. The power and area metrics are obvious ones and simply correspond to the **quiescent power** it consumes and the **silicon area** it occupies. Hence, we will not discuss those further here. This section therefore focuses on the specific performance metrics commonly employed to characterize current references in Section 1.2.1, and discusses their various definitions as well as good practices. Next, Section 1.2.2 presents various figures of merit (FoMs) proposed in the literature to study trade-offs between PPA metrics, and introduces novel FoMs which we believe to be of interest for the study of current references.

1.2.1 Performance Metrics

1.2.1.1 I_{REF} Line Sensitivity (LS) and Temperature Coefficient (TC)

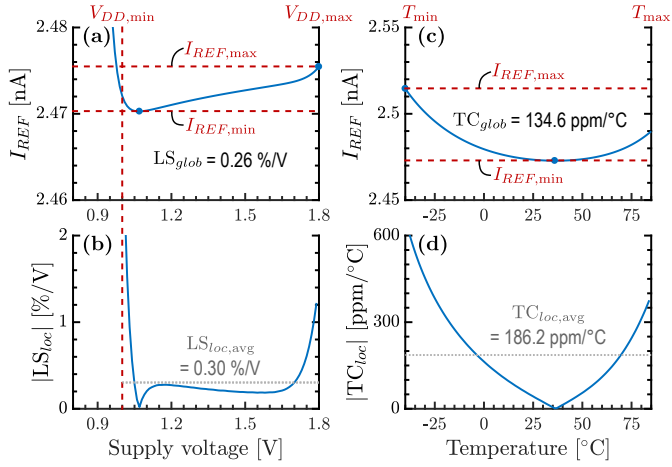

Fig. 1.1 Calculation of the line sensitivity (LS) and temperature coefficient (TC) of I_{REF} using the box method to obtain the *global* definition, or averaging the absolute value of the *local* definition to obtain a fairer estimation. The displayed results are based on a design in GlobalFoundries (GF) 22-nm fully-depleted silicon-on-insulator (FD-SOI) discussed in Section 4.2, just for the sake of providing a concrete example. (a) Supply voltage dependence of I_{REF} at 25°C, and (b) corresponding LS_{loc}, computed using finite differences. (c) Temperature dependence of I_{REF} at 1.8 V, and (d) corresponding TC_{loc}, computed using finite differences.

The most important performance metrics used to characterize current references are the **line sensitivity (LS)**, i.e., the dependence of the reference current I_{REF} to

supply voltage V_{DD}, and the **temperature coefficient (TC)**, i.e., the dependence of I_{REF} to temperature T. These two dependences are depicted in Fig. 1.1 for one of the designs developed in this thesis, as a concrete example on how to measure these performance metrics. Another quantity of interest, even though less frequently reported in the literature, is the **load sensitivity**, i.e., the dependence of the reference current to the voltage applied to the current source, which is simply the drain-to-source voltage of a transistor in a simple current mirror. It should be noted that this quantity can be linked with the output impedance of the current source.

First, the LS can either be expressed around a given operation point Q corresponding to a single V_{DD}, what we refer to as a *local* quantity, or across a range of supply voltages, what we refer to as a *global* quantity. The conventional definition of the *local* LS is

$$\mathrm{LS}_{loc} = \frac{1}{I_{REF}} \frac{\partial I_{REF}}{\partial V_{DD}}\bigg|_{Q} \quad [1/\mathrm{V}], \tag{1.1}$$

while the *global* LS is computed using the box method, and given by

$$\mathrm{LS}_{glob} = \frac{I_{REF,\max} - I_{REF,\min}}{I_{REF,\mathrm{avg}}(V_{DD,\max} - V_{DD,\min})} \times 100 \quad [\%/\mathrm{V}], \tag{1.2}$$

where $I_{REF,\min/\mathrm{avg}/\max}$ respectively stand for the minimum, average, and maximum reference current among the considered range, and $V_{DD,\min/\max}$, to the lower and upper bounds of the supply voltage range.

Next, similarly to the LS, the TC can be defined *locally* and *globally*, with

$$\mathrm{TC}_{loc} = \frac{1}{I_{REF}} \frac{\partial I_{REF}}{\partial T}\bigg|_{Q} \quad [1/^{\circ}\mathrm{C}], \tag{1.3}$$

evaluated around a single temperature T, and

$$\mathrm{TC}_{glob} = \frac{I_{REF,\max} - I_{REF,\min}}{I_{REF,\mathrm{avg}}(T_{\max} - T_{\min})} \times 10^{6} \quad [\mathrm{ppm}/^{\circ}\mathrm{C}], \tag{1.4}$$

computed across a temperature range spanning from $T_{\min}$ to $T_{\max}$.

In a vast majority of literature, the *global* quantity is employed, as it presents the advantage of being simple to compute given that it solely relies on the minimum / maximum values of I_{REF} is the considered range, which can easily be extracted from the I_{REF} vs. V_{DD} and I_{REF} vs. T curves in Figs. 1.1(a) and (c). These curves can either be obtained from simulation results, or from measurements, without impacting the way these metrics are calculated. However, we could argue that this way of measuring the LS and TC is not the fairest one, as it does not account for fine details in the dependence of I_{REF} to supply voltage and temperature. Hence,

we could also rely on the following quantities

$$\mathrm{LS}_{loc,\mathrm{avg}} = \frac{1}{(V_{DD,\max} - V_{DD,\min})} \int_{V_{DD,\min}}^{V_{DD,\max}} |\mathrm{LS}_{loc}(V)|\, dV \quad [1/\mathrm{V}], \tag{1.5}$$

$$\mathrm{TC}_{loc,\mathrm{avg}} = \frac{1}{(T_{\max} - T_{\min})} \int_{T_{\min}}^{T_{\max}} |\mathrm{TC}_{loc}(T)|\, dT \quad [1/^{\circ}\mathrm{C}], \tag{1.6}$$

obtained by averaging the absolute value of the *local* LS and TC over the considered range. Figs. 1.1(b) and (d) present the *local* definitions of the LS and TC, with the definitions (1.5) and (1.6) illustrated in grey dashed lines. We observe that, compared to the *global* definitions computed in Figs. 1.1(a) and (c), the *local* averages yield LS and TC values that are respectively 15 and 38% larger than the *global* ones. Yet, albeit these definitions are in our opinion fairer than the *global* LS and TC computed with the box method, (i) they are more tedious to evaluate, as they require to compute a derivative to estimate LS_{loc} and TC_{loc}, (ii) in the case of measurement results, they are more subject to noise in the curves I_{REF} vs. V_{DD} and I_{REF} vs. T and require more data points because they rely on derivatives, and (iii) they are not commonly used in the literature, making it difficult to compare works using these metrics with the state of the art. In the rest of this thesis, we will therefore rely on the *global* LS and TC given by (1.2) and (1.4), and will no longer explicitly mention that the *global* definitions are employed.

1.2.1.2 Variability of I_{REF} due to Local Mismatch and Global Process Variations

Another important performance metric that needs to be defined is the **variability of I_{REF}** due to local mismatch, global process variations, and their combined effects, which is typically obtained from Monte-Carlo (MC) simulations. Of course, this variability also impacts the LS and TC of I_{REF}. Fig. 1.2 shows an example of such variations for local mismatch, with Fig. 1.2(a) presenting variability results for the temperature dependence of I_{REF}, and featuring variability of I_{REF} and of its TC. Regarding I_{REF}, the quantity of interest is the ratio between the standard deviation σ and the mean μ, i.e., (σ/μ), which is also called the coefficient of variation (CV). It is relevant to report this quantity to characterize the variability of I_{REF} as it usually follows a normal distribution, as shown in Fig. 1.2(b). In contrast, for the TC of I_{REF}, the *global* definition (1.4) used in the literature and in this thesis constrains the TC to be positive, resulting in a distribution which is more accurately described by a log-normal, as depicted in Fig. 1.2(c). For this reason, we believe that reporting the mean and standard deviation, as it is done in many papers in the literature, is not the best practice because it completely disregards the skewness of the TC distribution. Hence, we argue that using the median, in addition to the 1st and 99th percentiles, provides a more complete understanding of the variability [Fig. 1.2(d)]. Moreover, reporting a value for the TC that represents the typical performance of a statistical distribution, such as the median, is a much better practice than only reporting the TC for a typical-typical (TT) simulation, as the former provides a

more comprehensive view of the design's performance, while the latter too often yields overoptimistic results.

Another source of variations of I_{REF} is related to intrinsic noise, but this metric is only rarely reported in the literature of current references and is more frequently encountered in the context of voltage references. Nevertheless, the reason why intrinsic noise is not traditionally considered in the context of current references is not clear to us.

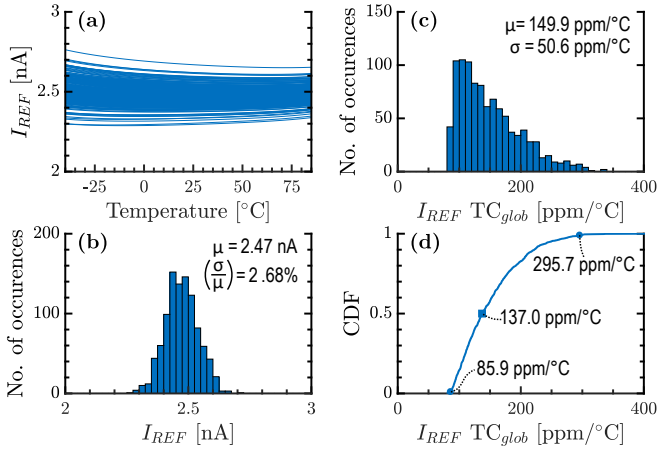

Fig. 1.2 For the same reference current [Section 4.2] as in Fig. 1.1, (a) I_{REF} vs. T curves at 1.8 V for 10^3 Monte-Carlo (MC) simulations due to local mismatch, histograms of (b) I_{REF} at 25°C and (c) I_{REF} TC_{glob} from -40 to 85°C, and (d) cumulative distribution function (CDF) of I_{REF} TC_{glob}, with the 1st, 50th (median), and 99th percentiles highlighted.

1.2.1.3 Startup Time

A last metric of interest is the **startup time** of the reference current, which is the time required by the reference current to reach stability when the power supply is switched on. Formally, we define the x-% startup time as the time at which I_{REF} remains within $\pm(100-x)$% of its steady-state value. For example, the 99-% startup time corresponds to the time at which I_{REF} remains within 1 % of its steady-state value. Mathematically, the x-% startup time can be expressed as

$$t_{start,x\%} = t^* \quad \text{such that} \quad \left|\frac{I_{REF}(t) - I_{REF}(+\infty)}{I_{REF}(+\infty)}\right| < \frac{(100-x)}{100} \quad \forall t > t^*. \tag{1.7}$$

An example is represented in Fig. 1.3, with Fig. 1.3(a) providing a global view of the startup waveform, and Fig. 1.3(b) zooming in on the steady-state value of I_{REF}.

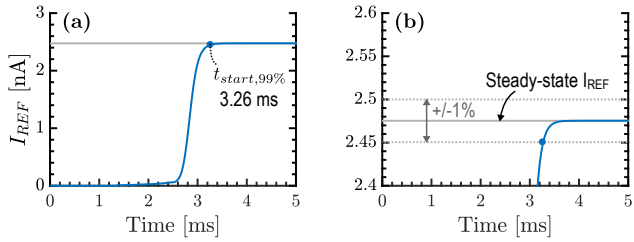

Fig. 1.3 For the same reference current [Section 4.2] as in Fig. 1.1, (a) startup waveform in the TT process corner, and (b) detail of the stabilization of I_{REF}. The marker corresponds to the 99-% startup time.

1.2.2 Figures of Merit

1.2.2.1 Existing Figures of Merit

Various FoMs have been proposed in the literature to capture the trade-offs between the PPA metrics describing current references. We have identified four different FoMs based on our review of the state of the art, but other might exist that are not discussed here. First, [24] proposes an FoM to be maximized, expressed as

$$\text{FoM}_\text{I} = \frac{(T_\text{max} - T_\text{min})^2}{\text{TC}} \times \frac{1}{\text{Power} \times \text{Area}} \times \frac{1}{10^{21}} \quad [^\circ\text{C}^3/(\text{W}\times\text{mm}^2)]. \tag{1.8}$$

It has been proposed in the context of voltage references, but can also be used for current references, as has been done in [31]. The interest of this FoM lies in the fact that it combines power and area with a performance metric, here the temperature dependence, and we believe it to be a suitable level of complexity for an FoM. However, the square on the temperature range puts unnecessary emphasis on this characteristic on the current reference, and the power consumption alone is not a good metric as it does not account for the current level generated by the reference, which conditions the range in which the power consumption will eventually lie. A well-designed FoM should rather rely on the power consumption normalized by the reference current, which we believe to be a fairer metric.

Then, [32, 33] proposes an FoM to be minimized, given by

$$\text{FoM}_\text{II} = \frac{\text{TC}}{(T_\text{max} - T_\text{min})} \times \frac{I_{VDD}}{I_{REF}} \quad [\text{ppm}/^\circ\text{C}^2], \tag{1.9}$$

where I_{VDD} is the quiescent current drawn from the power supply. This FoM relates the temperature dependence to the supply current normalized to the reference current. Nevertheless, we could argue that the second factor should make use of the power consumption rather than I_{VDD} to account for the minimum supply voltage of the reference current.

Next, [34] proposes a rather complex FoM, also to be minimized, calculated as

$$\text{FoM}_{\text{III}} = \frac{\text{TC}}{(T_{\max} - T_{\min})} \times \frac{I_{VDD}}{I_{REF}} \times \text{LS} \times 3 \left(\frac{\sigma}{\mu}\right)_{I_{REF}} \quad [(\text{ppm}\times\%)/(^{\circ}\text{C}^2\times\text{V})]. \tag{1.10}$$

In our opinion, this FoM tries to combine too many performance metrics, as it involves the supply voltage and temperature dependence, in addition to the variability of I_{REF} due to local mismatch. As for most analog circuits, attempting to reduce the complexity of a circuit to a single number is unreasonable, and leads to an FoM which fails to provide intuition regarding the trade-offs it captures.

Finally, [35] adopts a different approach compared to the three other ones, and proposes an FoM to be minimized combining process variations, supply voltage and temperature dependence, expressed as

$$\begin{aligned}\text{FoM}_{\text{IV}} = &|\text{Proc. var. accuracy}| \\ &+ \text{Temp. var. over } 100\ ^{\circ}\text{C span} \\ &+ \text{Supply var. over } 10\ \%\ V_{DD} \text{ change} \quad [\%].\end{aligned} \tag{1.11}$$

While it is an interesting way to combine different performance metrics, it relies on an implicit use case to do so, as a given supply voltage and temperature ranges are required to compute variations of I_{REF}. This FoM should therefore be dedicated to comparisons between current references in a well-defined applicative context, instead of general comparisons between different architectures.

1.2.2.2 *Proposed Figures of Merit*

Based on the FoMs described in the previous section, we establish three main requirements for a well-defined FoM:

1. The FoM combines at most power, area, and a single performance metric;
2. If power consumption is used, it must be normalized to the reference current, and must be evaluated at $V_{DD,\min}$ to account for the minimum supply voltage in the comparison;
3. It can only involve linear terms.

In this thesis, as will be explained later on in Chapter 2, our main focus will be on the reduction of the silicon area and temperature dependence of current references, so the most relevant FoM to capture this objective is

$$\text{FoM}_1 = \frac{\text{TC}}{(T_{\max} - T_{\min})} \times \text{Area} \quad [\text{ppm}/^{\circ}\text{C}^2\times\text{mm}^2], \tag{1.12}$$

which shares similarities with (1.8) and (1.9), and needs to be minimized. It is also possible to include power consumption into this FoM by modifying it to

$$\text{FoM}_2 = \frac{\text{TC}}{(T_{\max} - T_{\min})} \times \text{Area} \times \frac{\text{Power}(V_{DD,\min})}{1\,\text{V} \times I_{REF}} \quad [\text{ppm}/^\circ\text{C}^2 \times \text{mm}^2]. \quad (1.13)$$

If the focus needs to be put on the supply voltage dependence instead of the temperature dependence, these two FoMs can be modified as follows,

$$\text{FoM}_3 = \frac{\text{LS}}{(V_{DD,\max} - V_{DD,\min})} \times \text{Area} \quad [\%/\text{V}^2 \times \text{mm}^2], \quad (1.14)$$

and with the power consumption,

$$\text{FoM}_4 = \frac{\text{LS}}{(V_{DD,\max} - V_{DD,\min})} \times \text{Area} \times \frac{\text{Power}(V_{DD,\min})}{1\,\text{V} \times I_{REF}} \quad [\%/\text{V}^2 \times \text{mm}^2]. \quad (1.15)$$

In the proposed FoMs, we choose not to normalize silicon area to the technology node for several reasons:

1. Analog circuits do not benefit from technology scaling as much as digital ones, as they have to cope with exacerbated analog nonidealities in advanced nodes [36];
2. An alternative scaling, whose idea is to maintain the same variability σ_{V_T} in any technology, could rely on Pelgrom's mismatch parameter A_{V_T}. Using Pelgrom's law with a constant σ_{V_T}, we observe that silicon area is proportional to $A_{V_T}^2$.
$$\sigma_{V_T}^2 = \frac{A_{V_T}^2}{WL} \quad \Leftrightarrow \quad \text{Area} \propto WL \propto A_{V_T}^2. \quad (1.16)$$
As an example, based on values of A_{V_T} of 4.5 mV$\times\mu$m and 3 mV$\times\mu$m in 0.18 and 0.11 μm [36], and 2.4 mV$\times\mu$m in 28 nm [37], the scaling factor with respect to 0.18 μm would be 2.3$\times$ for 0.11 μm and 3.5$\times$ for 28 nm, as opposed to 2.7$\times$ and 41.3$\times$ for a conventional scaling based on the feature size. The latter thus disproportionately penalizes advanced technologies. Although this alternative scaling based on A_{V_T} might seem attractive, it is not conventionally done in the literature and difficult to apply in a fair and rigorous way, as a circuit consists of several transistors of different types and lengths and A_{V_T} is precisely impacted by these two parameters. Moreover, the A_{V_T} of I/O devices exceeds that of core devices due to the increased oxide thickness [38], leading to further uncertainties;
3. The area of some current references such as [39, 40, 41] is dominated by the resistor used as V-to-I converter, for which the scaling factor to be used is not obvious.

Besides, to improve the physical relevance of these FoMs, we could relax the third requirement set for a well-defined FoM and exploit trends capturing how TC and LS can be traded for silicon area or normalized power consumption. Such trends are depicted in Fig. 2.2 based on the literature of current references, but are not sufficiently reliable in our opinion to modify the proposed FoMs. Finally, process variations of the reference are not accounted for in the proposed FoMs. If this characteristic is of interest, we believe that an approach focusing on the absolute accuracy of the reference, similar to the one employed to establish $\mathrm{FoM_{IV}}$, should be considered.

1.3 Current Reference Topologies

1.3.1 Classification of Current Reference Topologies

Because of the wide variety of current reference topologies, it is useful to try to classify them based on different criteria, to build an understanding of the main concepts and operation principles. To do so, we propose three criteria through which we can examine the state of the art of current references;

1. The voltage-to-current (V-to-I) converter used in the reference, among the following list: resistor, diode-connected transistor, transistor in triode, self-cascode MOSFET (SCM), gate-leakage transistor, switched capacitor;
2. The transistor type, i.e., bipolar junction transistor (BJT) of metal-oxide-semiconductor field-effect transistor (MOSFET);
3. The temperature dependence of I_{REF}, which can be PTAT, CTAT, or CWT.

1.3.1.1 Voltage-to-Current Converters

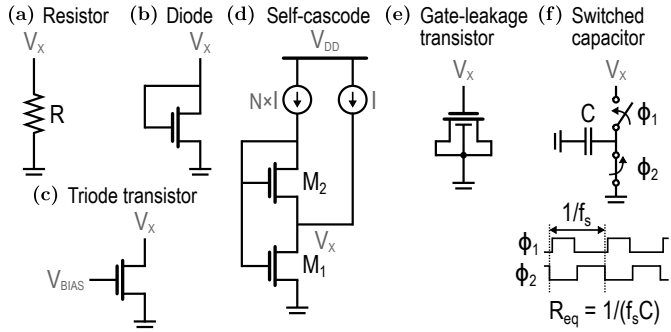

Fig. 1.4 Overview of the V-to-I converters used in current references, biased by a voltage V_X. (a) Resistor, (b) diode-connected transistor, (c) transistor in triode, (d) self-cascode MOSFET, (e) gate-leakage transistor, and (f) switched capacitor.

Current references generally rely on a reference voltage biasing a V-to-I converter to generate a reference current. A first axis along which current references can be organized is thus the V-to-I converter they employ. The most common one is the resistor [Fig. 1.4(a)], which can be implemented using on-chip n-well or polysilicon (poly) resistors, with the n-well resistor presenting a lower resistance density and larger temperature coefficient of resistance (TCR) than poly resistors. The typical values that can be obtained with a resistor occupying a reasonable silicon area are ranging from a few kΩ to MΩ, and stem from a resistance density between 10 and 10000 Ω/□. Resistors are thus well-suited to the generation of currents in the μA

range. Next, several V-to-I converters consists of transistors in different configurations: in diode [Fig. 1.4(b)], in triode, with a gate voltage V_{BIAS} [Fig. 1.4(c)], or in an SCM structure [Fig. 1.4(d)]. Contrary to resistors, transistors are better suited to the generation of currents comprised between nA and μA. More recently, in technology nodes equal to or lower than 0.13 μm, some works [42, 29, 30, 43, 44, 45, 46] have started to exploit the gate leakage of core transistors to implement resistances in the GΩ range within a very dense silicon area [Fig. 1.4(e)], making them ideal for the generation of currents in the pA range. Finally, a limited number of works such as [47] have proposed to replace large resistors by switched capacitors [Fig. 1.4(f)]. However, the attractiveness of this solution remains limited, as a clock signal is required to generate the switch control signals ϕ_1 and ϕ_2 and could potentially lead to an area overhead exceeding that of the resistor. This solution also leads to some ripples on the generated current.

1.3.1.2 Transistor Type: Hybrid vs. MOSFET-Only

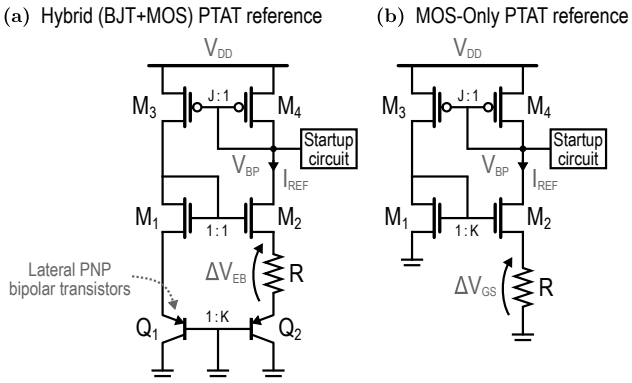

Fig. 1.5 (a) Hybrid implementation of a PTAT current reference, in which I_{REF} is generated by the ΔV_{EB} between lateral PNP transistors Q_1 and Q_2, and (b) MOSFET-only implementation of a PTAT current reference, in which I_{REF} is generated by the ΔV_{GS} between nMOS transistors M_1 and M_2, which can either be operated in weak or in strong inversion.

The second criterion based on which current references can be classified is the type of transistors they are built with. The first transistor to be invented was the PNP BJT in 1947 by J. Bardeen, W. Brattain, and W. Shockley, and the current references developed in the early years of electronics thus solely relied on BJTs. However, the BJT has progressively given way to the MOSFET, invented in the early 1960s by M. Atalla and D. Kahng, given the easier manufacturing of this new transistor type and the absence of base current allowing to reduce power consumption. Modern current references are no longer constituted of only BJTs, but either use a mix of BJTs and MOSFETs, with the BJTs implemented as lateral bipolar transistors, or

employ only MOSFETs. The former is a type of current references that we refer to as *hybrid*, while the latter is called *MOSFET-only*. Fig. 1.5 depicts two versions of a PTAT current reference, corresponding to the *hybrid* version in Fig. 1.5(a), in which the resistor is biased by the difference of emitter-to-body voltages ΔV_{EB} between lateral PNP transistors Q_1 and Q_2, and to the *MOSFET-only* version in Fig. 1.5(b), in which the resistor is biased by the difference of gate-to-source voltages ΔV_{GS} between nMOS transistors M_1 and M_2.

1.3.1.3 Temperature Dependence: PTAT, CTAT, and CWT

A reference current can have three types of first-order temperature dependence:

1. Proportional-to-absolute-temperature (PTAT);
2. Complementary-to-absolute-temperature (CTAT);
3. Temperature-independent or constant-with-temperature (CWT).

In this section, we will focus on PTAT and CTAT current references, as presenting the main categories of CWT current references requires an in-depth discussion, which will be conducted in Section 1.3.2.

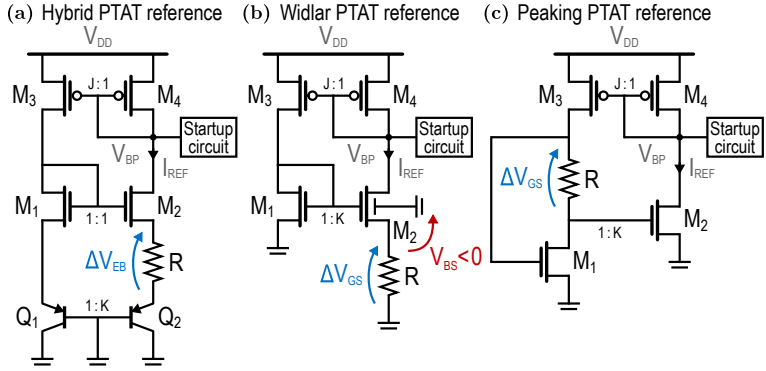

Fig. 1.6 Common topologies of PTAT current references. (a) Hybrid PTAT reference, biasing the resistor with the ΔV_{EB} between two PNP BJTs. (b) Widlar current reference and (c) peaking or Nagata current reference, biasing the resistor with the ΔV_{GS} between two nMOS transistors.

Firstly, conventional PTAT and CTAT current references, respectively illustrated in Figs. 1.6 to 1.8, rely on a β-multiplier structure formed by the nMOS transistors M_{1-2} and the pMOS current mirror M_{3-4}. In the first PTAT topology in Fig. 1.6(a), this β-multiplier leads to a voltage across the resistor equal to the ΔV_{EB} of the two PNP BJTs Q_{1-2}. The collector current I_C in a PNP BJT can be expressed as

$$I_C = I_S \exp\left(\frac{V_{EB}}{U_T}\right), \tag{1.17}$$

where I_S is the specific current of the transistor and $U_T = k_B T/q$ is the thermal voltage. From (1.17), we can isolate the emitter-to-base voltage V_{EB} as

$$V_{BE} = U_T \log\left(\frac{I_C}{I_S}\right). \tag{1.18}$$

Coming back to the topology in Fig. 1.6(a), the reference current it generates is given by

$$I_{REF} = \frac{\Delta V_{EB}}{R} = \frac{U_T \log\left(\frac{I_{S2}}{I_{S1}}\frac{I_{C1}}{I_{C2}}\right)}{R} = \frac{U_T \log(JK)}{R}, \tag{1.19}$$

where J is the pMOS current mirror ratio and K the number of BJTs with the same dimensions as Q_1 put in parallel to implement Q_2. This reference voltage is purely PTAT, to the extent that the TCR is not positive, and equal to or larger than the TC of ΔV_{EB}.

Furthermore, MOSFET-only architectures for PTAT current references are shown in Figs. 1.6(b) and (c), and can operate either in strong or in weak inversion. Their structure shares the pMOS current mirror M_{3-4}, but differs in the type of nMOS current source it employs. The reference in Fig. 1.6(b) indeed makes use a Widlar current source, invented by R. Widlar in 1965 [48], while the reference in Fig. 1.6(c) employs a so-called peaking current source, developed by M. Nagata in 1966. Both of these structures impose a resistor bias voltage equal to the difference of V_{GS} between M_1 and M_2. Using the weak-inversion equations in Appendix A.1, and more specifically (A.3), the reference current is provided by

$$I_{REF} = \frac{\Delta V_{GS}}{R} = \frac{nU_T \log\left(\frac{S_2}{S_1}\frac{I_{DS1}}{I_{DS2}}\right)}{R} = \frac{nU_T \log(JK)}{R}, \tag{1.20}$$

where n is the subthreshold slope factor and $S = W/L$ is the transistor's aspect ratio. We observe that the operation principle is very similar to the hybrid PTAT reference, and that I_{REF} is again purely PTAT when neglecting the TCR. In Fig. 1.6(b), because the body-to-source voltage V_{BS2} is negative as the body of M_2 is grounded, the reverse body bias (RBB) effect increases the threshold voltage V_{T2}, introducing a slight imbalance between M_1 and M_2, and thereby a deviation from the purely PTAT behavior. This issue can either be corrected by implanting M_2 in a triple well, allowing to connect its body to its source, or by using the architecture in Fig. 1.6(c), as the Nagata current source does not suffer from this nonideality.

Another MOSFET-only PTAT architecture of interest is the one proposed in [26, 27], which is obtained by replacing the resistor in Fig. 1.6(b) by a two-transistor (2T) SCM. The equations of the SCM are not detailed here, but are derived in full in Appendix B. The main conclusion to draw from them is that, when the SCM is biased by a PTAT voltage such as the ΔV_{GS} of weak-inversion transistors, it generates a reference current proportional to the specific sheet current $I_{SQ} = \frac{1}{2}\mu C'_{ox} n U_T^2$.

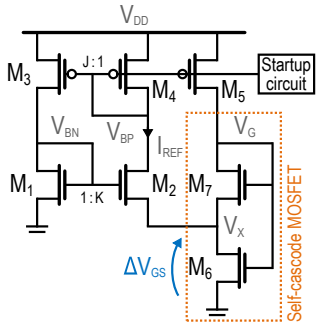

Fig. 1.7 Variant of the Widlar current source in Fig. 1.6(b), in which the resistor has been replaced by an SCM, proposed in [27, 28].

The temperature dependence of I_{SQ} stems from two factors. On the one hand, from the carrier mobility μ, which is usually modeled as $\mu(T) = \mu(T_0)\,(T/T_0)^{-m}$, where m is the temperature exponent of mobility. On the other hand, from the factor U_T^2, which brings a dependence to T^2. Therefore, $I_{SQ}(T) \propto T^{2-m}$ and, as m is comprised between 1.2 and 2 in bulk CMOS [49], I_{SQ} and I_{REF} depend quasi-linearly on temperature. Variants of this topology improve the LS through cascoding [28] or a 1T feedback amplifier [50]. While the PTAT β-multiplier only requires a handful of components, the SCM sizing can be tedious because transistors are operated in moderate inversion. However, an SCM can be implemented with transistors from a single threshold voltage (V_T) type and reaches a low current within a small area.

These PTAT current references can be used in many applications, but let us cite three of them. First, for operational transconductance amplifiers (OTAs), maintaining the transconductance g_m CWT can be useful, as frequency compensation techniques such as the pole-zero compensation in a two-stage Miller OTA requires to size components based on the value of g_m. In weak inversion, the transconductance is given by

$$g_m = \frac{I_{DS}}{nU_T}, \tag{1.21}$$

and feeding the transistors with a PTAT I_{DS} results in a constant g_m, hence the name constant-g_m references also given to PTAT references. Second, voltage comparators biased with a CWT current present an increased delay at high temperature. In contrast, biasing them with a PTAT current stabilizes the delay with respect to temperature variations. Finally, PTAT current references can be used in conjunction with CTAT ones, more specifically, by summing them, to generate a CWT reference current. This concept will be further discussed in Section 1.3.2.

CTAT current references are the counterpart of PTAT ones, with the conventional topologies illustrated in Fig. 1.8. Similarly to the PTAT references, they rely on a β-multiplier to bias the resistor. In the hybrid topology [Fig. 1.8(a)], the resis-

tor is biased by the CTAT V_{EB} of PNP transistor Q_1, whose TC has a typical value of -2 mV/°C, while in the MOSFET-only architectures, the resistor is biased by the CTAT V_{GS} of an nMOS transistor, either M_{DIO} in Fig. 1.8(b) or M_1 in Fig. 1.8(c). This CTAT behavior originates from the CTAT behavior of the threshold voltage, whose temperature dependence is captured by

$$V_T(T) = V_T(T_0) - \alpha_{V_T}(T - T0), \tag{1.22}$$

where T_0 is a reference temperature and α_{V_T} is the first-order temperature coefficient of V_T. These CTAT current references are predominantly used in conjunction with PTAT ones to generate a CWT current, as already mentioned hereabove.

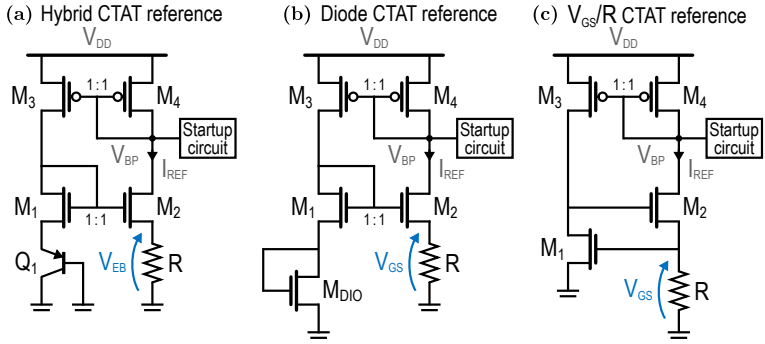

Fig. 1.8 Common topologies of CTAT current references. (a) Hybrid CTAT reference, biasing the resistor with the V_{EB} of a PNP BJT. MOSFET-only CTAT current references, in which the resistor in biased by the V_{GS} of an nMOS transistor, using (b) a modified Widlar current reference with a transistor in diode or (c) a feedback loop formed by M_{1-2}.

1.3.2 Constant-with-Temperature Current References

To provide a comprehensive view of the techniques allowing to generate a CWT current, we conduct a thorough review of the state of the art using the following methodology:

- Step 1) consists of the search for relevant papers over the period 2000-2023. To do so, we use IEEEXplore and Google Scholar with a combination of the three keywords 'current', 'reference', and 'temperature' or 'ppm'. This allows us to collect 91 papers from IEEEXplore, 35 additional papers from Google Scholar, and 28 papers which were already present in our state of the art but did not appear in this search because they either use the terminology 'current source' instead of 'current reference', or because they do not explicitly mention that the current reference is temperature-independent. We thus gather a total of 154 papers at the end of this first step.
- Step 2) aims at selecting the papers that are actually relevant to our study and provide sufficient information to be exploited. We thus set four requirements for a paper to be selected in our review:

  1. The paper belongs to an international journal or conference;
  2. The main focus of the paper is a current reference;
  3. The paper must present a current reference topology using solely on-chip components;
  4. Because we concentrate on the temperature dependence of the reference, the TC of I_{REF} must be provided, in addition to the power consumption and/or the silicon area.

  After this selection steps, 39 papers are discarded for failing to comply with the four criteria, one paper is a review paper [51] which is interesting for our work but is not included in the study per se, and we are thus left with a corpus of 114 papers.
- Step 3) exploits this corpus in three ways. First, to highlight the main CWT current generation techniques in this chapter. Then, to provide an overview of the performance of existing current references in Chapter 2, and compare our work to the state of the art in Chapters 3, 4 and the conclusion of this thesis. At last, to identify the typical applications of current references and discuss the significance of the advances brought forward by this thesis for these applications in Chapter 5.

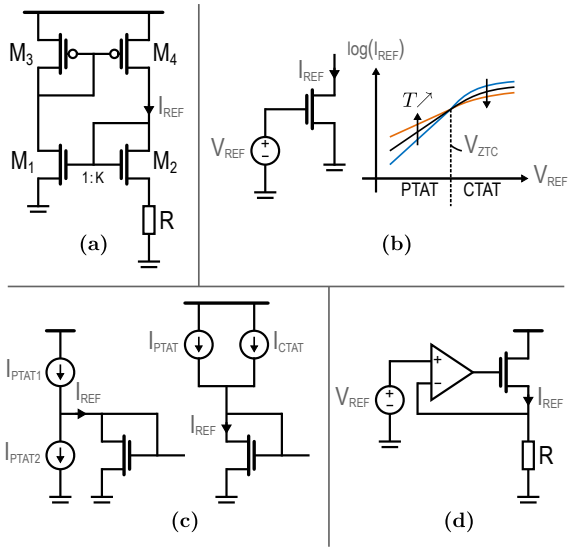

Fig. 1.9 The techniques to generate a CWT current can be divided into four categories. (a) Self-biased β-multiplier, also called $\Delta V_{GS}/R$ references. (b) Temperature-dependent V_{GS} close to the ZTC, removing the temperature dependence of I_{DS}. (c) Subtraction (resp. addition) of two PTAT currents (resp. a PTAT and a CTAT current). (d) Ratio between a reference voltage and a resistance with matched TCs, also called V/R references.

Based on this corpus, we identify four main topologies, depicted in Fig. 1.9, that can be used to generate a CWT reference current.

1. $\Delta V_{GS}/R$ references [Fig. 1.9(a)], such as β-multipliers or peaking current references (PCRs), in which a V-to-I converter is biased by the ΔV_{GS} of MOSFETs or by the ΔV_{BE} of BJTs;
2. A MOSFET biased close to its zero temperature coefficient (ZTC) operation point by a temperature-dependent V_{GS} [Fig. 1.9(b)];
3. The subtraction of two PTAT or two CTAT currents, or the addition of a PTAT and CTAT currents [Fig. 1.9(c)];
4. V/R references [Fig. 1.9(d)], in which a CWT I_{REF} is obtained by dividing a reference voltage by a resistance with a matched TC.

It should be noted that this classification differs from the one proposed in the current reference review of S. Lee *et al.* in [51] for the $\Delta V_{GS}/R$ and subtraction/addition of currents, which Lee rather divides into BJT-based and β-multiplier-based references. However, we believe that $\Delta V_{GS}/R$ architectures such as PCRs, and some topologies based on the subtraction/addition of currents are not properly captured by Lee's classification.

1.3.2.1 $\Delta V_{GS}/R$ References

The first category of CWT current references consists of $\Delta V_{GS}/R$ references, which can be divided into four main sub-categories: (i) hybrid β-multipliers, MOSFET-only β-multipliers in which the transistors generating the ΔV_{GS} are either operated in (ii) strong or (iii) weak inversion, and (iv) peaking current references.

First, hybrid β-multipliers [52, 53, 54, 55, 56] rely on a structure similar to Fig. 1.6(a), in which the PTAT behavior of an n-well resistor matches the TC of the ΔV_{EB} between two PNP BJTs to achieve temperature independence.

Then, MOSFET-only β-multipliers operating in strong inversion employ several approaches which mainly differ by the type of V-to-I converter used to replace the resistor in Fig. 1.9(a):

- Two triode transistors connected in parallel, with different gate voltages leading to PTAT and CTAT behaviors of their equivalent resistance [57, 58] and ultimately, to temperature independence;
- A resistor biased with a reference voltage whose TC matches the TCR, obtained as the sum of a PTAT ΔV_{GS} and a CTAT V_{GS} [59, 60], the CTAT V_{GS} originating from a diode-connected transistor;
- A resistor and a transistor connected in series [61], with the TCR of their equivalent resistance matching the TC of ΔV_{GS};
- A weak-inversion transistor in diode [62], with forward body biasing (FBB) applied to one of the strong-inversion transistors generating the ΔV_{GS};
- A second-order temperature compensation can also be obtained by combining a diode-connected transistor, either with two resistors [63] or with a triode transistor [64].

Next, the sub-category of $\Delta V_{GS}/R$ references regrouping the largest number of works (22 papers) is made up of MOSFET-only β-multipliers operating in weak inversion. Similarly to strong-inversion β-multipliers, they can be classified in terms of the V-to-I converter they use: a PTAT n-well resistor [65, 60, 33] or an SCM [66, 67, 68], in which case the PTAT ΔV_{GS} of weak-inversion transistors is used as is, or a switched capacitor [47] or a gate-leakage transistor [43, 69], for which the ΔV_{GS} is made CWT by employing different V_T types [43] or the same V_T type but different transistor's lengths [47]. Other references rely on a transistor in triode, for which temperature compensation is obtained by tuning the TC of its gate voltage [70, 71, 72, 73, 74, 75, 34, 76], its drain voltage [77, 78, 79] or its body voltage [80].

Finally, CWT PCRs all rely on a resistor as V-to-I converter, and can be made CWT by biasing this resistor with a ΔV_{GS} of weak-inversion transistors of the same V_T type, in which a V_T imbalance is created by forward body biasing of one of the transistors with a CTAT V_{BS} [81], or by making use of different transistor's lengths [82]. Another approach to achieve temperature independence consists in using a carefully-selected source degeneration resistor connected between the source of M_2

and ground in Fig. 1.6(c).

This first CWT current generation technique offers an unparalleled versatility, as the wide variety of V-to-I converters allows for the generation of current in any range, with a relatively limited silicon area if the choice of converter has been properly made. However, transistor-based V-to-I converters typically result in a poorer TC than resistors or gate-leakage transistors, as they present a nonlinear and stronger temperature dependence.

1.3.2.2 MOSFET Biased by a Temperature-Dependent V_{GS}

The second category of CWT current references builds upon the idea that a CWT current can be produced by biasing a transistor close to its ZTC with a slightly temperature-dependent V_{GS} [Fig. 1.9(b)]. On the one hand, the transistor can be biased at its ZTC either by a CWT reference voltage tracking V_T process variations [83, 84], or by an OTA-based feedback loop transforming back the CWT current into the ZTC gate voltage through a resistor [85] or a switched capacitor [86]. On the other hand, Fig. 1.9(b) illustrates that the drain-to-source current of a weak-inversion (resp. strong-inversion) MOSFET presents a PTAT (resp. CTAT) behavior when biased with a CWT gate voltage, and thus requires a CTAT (resp. PTAT) gate voltage to achieve temperature independence. Current references based on weak-inversion transistors can achieve this CTAT V_{GS} by generating a CTAT V_G [87, 88], a PTAT V_S [89], CTAT V_G and V_B [90], or a CTAT V_G and a PTAT V_S [84]. In contrast, current references based on strong-inversion transistors can achieve the required PTAT V_{GS} using a PTAT V_G [91, 92], a dedicated pMOS-only bias circuit [93], or two pMOS in strong inversion producing a V_G tracking V_T, and a source degeneration resistor [94].

Overall, this current generation technique can be made process-independent with relative ease, by letting the gate voltage track process variations of V_T, and has the advantage of a pW-to-nW power consumption. However, a competitive TC can only be achieved close to the ZTC, often resulting in a large value of the generated reference current. Regarding the reference voltage generation, older architectures [83, 84] rely on relatively complex voltage generators tracking V_T variations, often entailing a considerable area overhead, but recent advances have led to the emergence of voltage references consisting of only a handful of transistors, without significantly compromising other performance metrics [22, 23, 24, 25]. Such voltage references are used in [91, 88, 92], and will be one of the central elements leveraged in this thesis.

1.3.2.3 Subtraction or Addition of Currents

The third category of CWT current references is based on the subtraction or addition of currents with different TCs. First, the subtraction of currents is generally performed between two PTAT currents with different TCs [Fig. 1.9(c) left]. The two subtracted currents can be generated by two independent PTAT current refer-

ences with the same topology as Fig. 1.6(b) [95, 96, 97, 98], for which the different TCs stem from different sizings, by zero-V_{GS} transistors biasing a ladder of diode-connected transistors [99], which obtain different TCs based on the sizing and the number of diode transistors in the ladder, or by nMOS and pMOS β-multipliers with a triode transistor as V-to-I converter [100], for which the TCs differ because of the different temperature exponent of the electron and hole mobilities. It is also possible to subtract two PTAT currents produced by a single PTAT reference [101], by removing the purely temperature-dependent component from the PTAT current produced by a MOSFET-only current reference as the one in Fig. 1.6(b). Only [102] subtracts two CTAT currents with different TCs, generated by two β-multiplier variants, one similar to Fig. 1.8(b), and one relying on two different V_T types.

Next, the weighted sum of PTAT and CTAT currents [Fig. 1.9(c) right] is performed with PTAT and CTAT currents respectively generated by hybrid references such as the ones in Figs. 1.6(a) and 1.8(a) [103, 104, 105, 106, 107, 108], by MOSFET-only references such as the ones in Figs. 1.6(b), 1.6(c), 1.8(b), and 1.8(c) [109, 110, 111, 112, 31, 113], by an hybrid and a MOSFET-only references [114, 115, 116, 117], by a conventional structure and an unconventional one [118, 119, 120, 121, 122, 123, 124, 125], or by variants of β-multipliers [32, 126]. A last approch stands out compared to the rest of the state of the art, as it relies on weak-inversion MOSFETs biased with CTAT gate voltages to produce PTAT and CTAT currents [127]. The TC of the current depends on the CTAT TC of the gate voltage generated by self-biased SCM-based CTAT references [128]. This technique to generate a CWT reference current is quite popular, with 27 papers out of 114 opting for it.

This topology is quite simple, but suffers from several limitations: (i) a calibration of the relative weighting of the currents is necessary to achieve a competitive TC, (ii) the generation of PTAT and CTAT currents can require the use of bipolar transistors, and (iii) two current generators are needed instead of one, resulting in significant area usage.

1.3.2.4 V / R References

Finally, the fourth category of CWT current reference is based on the ratio between a voltage and a resistance with matched TCs [Fig. 1.9(d)]. A first sub-category relies on the ratio of a CWT voltage applied to a CWT resistance, either by an OTA [129, 42, 39, 40, 41, 45, 130, 46], a single-transistor (1T) buffer [29, 44, 30, 131], or through the current reference structure itself [132, 133]. The CWT reference voltage can either be generated by a bandgap reference (BGR) [132, 130], by an SCM with different V_T types [40] or different lengths [41], or by a voltage reference constituted of two to four transisors [42, 29, 30, 44, 46, 131]. Furhtermore, the CWT resistance is achieved by the series connection of PTAT n-well resistors and CTAT poly resistors [129, 40, 41, 133] or more recently, by gate-leakage transistors [42, 29, 30, 44].

A second sub-category uses the ratio of a temperature-dependent voltage whose TC matches the TCR. It can be achieved by a PTAT voltage applied to PTAT n-well

or poly resistor [134, 135] or a transistor in triode [136], or by a CTAT voltage applied to a CTAT poly resistor with first- [102, 137] or second-order [35] TCR compensation. Other approaches used matching voltage and resistance TCs, but do not specify the temperature dependence they rely on [138, 139, 140].

This type of current reference can easily be calibrated to reach a competitive TC performance by matching the first-order TCR, but usually relies on an operational amplifier to buffer the reference voltage onto the resistor, and can lead to rather complex voltage generator architectures if second-order TC matching is required. Obviously, the buffer and voltage generator can result in a considerable power and area overhead, but the development of 2T voltage references with a 1T buffer are gradually making this category of CWT current references more attractive.

1.3.2.5 Other Techniques

Only a handful of papers, namely 4 out of 114, do not fit in the four categories detailed hereabove, confirming the relevance of the proposed categorization. For the sake of completeness, we provide some words of explanations regarding these other techniques. First, [141] obtains a CWT reference current by connecting in parallel a Widlar and a Nagata current sources. Second, [142] compensates the PTAT behavior of leakage of a zero-V_{GS} nMOS by the CTAT behavior of pMOS current mirrors with different V_T types. Third, [143] uses a cascade of three Nagata current mirrors to reduce the dependence to temperature. Lastly, [144] periodically calibrates a current digital-to-analog conveter (DAC) based on a high-accuracy current reference employing a topology similar to [134]. While these approaches are original, [141, 142, 143] do not demonstrate outstandingly good results in terms of TC, and [144] requires to periodically recalibrate the DAC, but also occupies a very large silicon area which is not acceptable in most applications.

1.4 Calibration Techniques

Calibration or trimming techniques in the context of current references can be divided into two categories. The trimming of the reference current itself, addressed in Section 1.4.1, and the trimming of its TC in the context of CWT references, covered in Section 1.4.2.

1.4.1 Reference Current Calibration

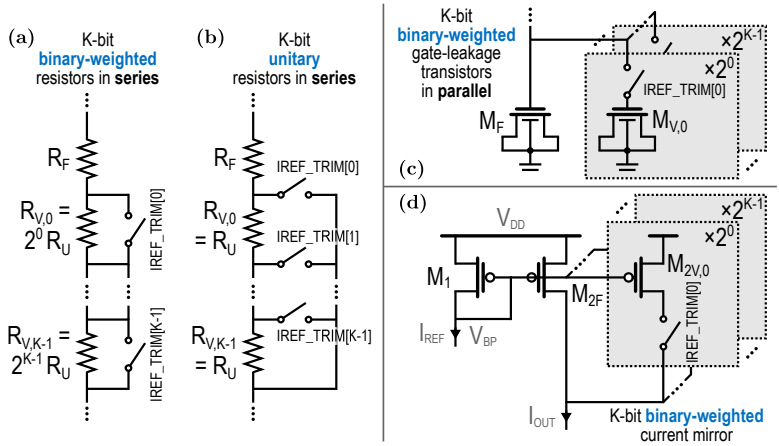

Fig. 1.10 Techniques to calibrate the reference current: Trimming of the resistance using (a) binary-weighted segments in series which can be individually shorted by switches or (b) unitary segments in series which can be bypassed by a single switch, controlled by a one-hot digital code. (c) Trimming of the equivalent resistance of gate-leakage transistors by changing the number of binary-weighted gate-leakage transistors connected in parallel. (d) Trimming of the output current I_{OUT} generated from the reference current I_{REF} using a binary-weighted current mirror.

Based on our corpus of current references, we identify two main techniques to calibrate the reference current. This calibration of I_{REF} can either be performed directly into the current reference, in which case it relies on a trimming of the V-to-I converter [Figs. 1.10(a) to (c)], or in the periphery of the current reference, in which case it relies on a tunable current mirror [Fig. 1.10(d)]. First, a trimming of the V-to-I converter is mostly performed in resistor- or gate-leakage-based topologies. The trimming of the resistor [138, 55, 56, 135, 33, 130, 31, 113] can either be performed by using several binary-weighted resistors in series, with switches allowing to individually short each resistor with a binary control [56, 135, 33, 31, 113], as shown

in Fig. 1.10(a), or unitary resistors connected in series in a thermometer fashion with a one-hot control [138], as illustrated in Fig. 1.10(b). The control signal ranges from 4 to 8 bits. By opposition, the trimming of a gate-leakage transistor consists in switching on or off parallel segments constituted of gate-leakage transistors with binary-weighted dimensions [43, 44, 46, 69], as represented in Fig. 1.10(c), using a 4-to-5-bit control signal.

If the calibration is performed in the periphery of the current reference, it is implemented with a binary-weighted current mirror [109, 105, 57, 108, 144, 111, 45, 75] with a control signal from 2 to 8 bits, allowing to change the ratio between the output current I_{OUT} and the reference current I_{REF} [Fig. 1.10(d)]. This second calibration technique is generally not as power- and area-efficient as a trimming directly integrated in the current reference, because it requires an additional branch to generate a bias voltage allowing to replicate the calibrated current I_{OUT}.

The calibration of the reference current presents the advantage that it can be performed at ambient temperature, and could be automated with a dedicated circuit on-chip.

1.4.2 Temperature Coefficient Calibration

The calibration of the TC of I_{REF} is closely linked with the category of CWT current generation technique. This section hence discusses the calibration techniques for each of the categories outlined in Section 1.3.2, based on the corpus of current references.

- $\Delta V_{GS}/R$ references: Two main techniques are used for this first category of current references. First, weak-inversion β-multipliers using two triode transistors as V-to-I converters, with different TCs stemming from different gate voltages, can change the TC of I_{REF} by modifying the number of triode transistors with a CTAT resistance behavior connected in parallel [57, 75]. Second, in [33, 47], a tunable pMOS current mirror ratio in a weak-inversion β-multiplier allows to trim the TC of I_{REF} by changing the TC of the ΔV_{GS} biasing the V-to-I converter;
- MOSFET biased by a temperature-dependent V_{GS}: In this category of current references, the TC trimming strategy consists in changing the aspect ratio of a transistor in the voltage reference circuit, so as to change the TC of the gate voltage and consequently, the TC of I_{REF} [89, 90];
- Subtraction or addition of currents: Two strategies are employed to trim the TC of I_{REF}. First, it is possible to tune the relative weights of the PTAT and CTAT currents that are summed with a binary-weighted current mirror [105, 100]. Then, the TC can also be trimmed by changing the TC of the PTAT and CTAT currents themselves, either by changing the TC of the gate voltage

applied to nMOS transistors [127], or by changing the value of the resistance in a PTAT $\Delta V_{GS}/R$ reference;

- V/R references: In this last category of CWT current references, the trimming of the TC is quite straightforward as it consists in trimming the TC of V_{REF} to match the TC of the V-to-I converter. Practically, this is achieved by changing the aspect ratio of a transistor in the voltage reference circuit using a binary-weighted structure, in a 2T voltage reference [42, 29, 30], or in an SCM [40, 41]. This can also be achieved by changing the value of a resistance in a BGR [138].

One of the difficulties of trimming the TC of I_{REF} is that it requires at least a two-point calibration, i.e., a calibration based on measurements at two different temperatures, to achieve a decent result. This strategy hence necessitates to control the temperature at which the circuit is operating when trimming the TC, for example using a climatic chamber. An additional level of complexity compared to the trimming of the reference current is thus necessary, making it difficult to implement a trimming of the TC at large scale, as this would require to calibrate each chip individually. To alleviate this problem, current references should therefore have a TC of I_{REF} which is only marginally affected by process variations to avoid TC calibration, or feature a TC which does not significantly suffer from local mismatch and can therefore use the same TC calibration code for an entire batch of chips originating from the same process corner.

2

Current References for the Internet of Things

The Internet of Things is not a concept;
it is a network, the true technology-enabled Network of all networks.
– Edewede Oriwoh

The last decade has seen the deployment of the Internet of Things (IoT), consisting of ultra-low-power (ULP) sensor nodes that embed processing and decision-making capabilities to support intelligence at the edge. Yet, the design of such sensor nodes presents several technical challenges. The objective of this second chapter is thus to understand the unique constraints of IoT sensor nodes and how they subsequently impact the specifications of the current references they embed, to answer the first research question identified in the introduction of this thesis, namely:

What are the specific requirements for current references in the context of the IoT ?

To do so, Section 2.1 first details the power constraints of such sensor nodes, related to the fact that they are supplied by limited-capacity batteries or energy harvesting sources, and makes the case for the generation of a nA-range bias current. Then, their robustness against process, voltage and temperature (PVT) variations is discussed, and the specifications of current references that are well suited to the IoT are inferred from the design challenges of IoT sensor nodes. Section 2.2 then studies the state of the art of existing current references based on the corpus of papers

formed in Chapter 1 to identify potential directions of improvement for the performance of current references, listed in Section 2.3, allowing to better fulfill the requirements identified in Section 2.1.

2.1 Design Challenges of IoT Sensor Nodes

Fig. 2.1(a) illustrates the general structure of an IoT sensor node, which includes three main functionalities. First, it must be able to collect data by sensing physical quantities of the environment in which it is operating. Then, it must be able to perform some processing of this data directly on the sensor node, either to compress the raw data acquired by the sensor or to decide whether this data is relevant or not. Finally, data is transmitted from the sensor node to the cloud through a wireless link, usually with a gateway as an intermediate step between the sensor node and the cloud itself. A power management unit (PMU) supports these three main functionalities by generating adapted supply voltages and bias currents from the power sources implemented as batteries or energy harvesting sources, such as photovoltaic, heat, vibrations, or radio-frequency (RF) signals. As for all circuits, the designer tries to optimize the power, performance and area (PPA) metrics. In this section, we will discuss these three dimensions into details.

2.1.1 Power Consumption

2.1.1.1 What is the Power Budget of IoT Sensor Nodes ?

The power budget of IoT sensor nodes is limited by the fact that they are either supplied by limited-capacity batteries or by energy harvesting sources, and must therefore cope with stringent constraints on their average power consumption. The objective of this section is thus to evaluate the order of magnitude of the power available from these two sources. In this analysis, we do not account for the efficiency of the power conversion in the PMU, as a well-designed PMU should not significantly change the order of magnitude of the power ultimately delivered to the circuits on the sensor node, with respect to the power provided by batteries and energy harvesting. On the one hand, Fig. 2.1(b) presents the average power P_{avg} available from different types of batteries, ranging from a lithium (Li) thin-film battery to a basic Alkaline AA one, based on data from [14, 15] and assuming a lifetime of 10 years for the sensor node. The battery with the most limited capacity is a 1-mm^2 Li thin-film battery, with a 3.3-μAh capacity at 1.5 V, delivering an average power below 0.1 nW. This type of battery is not sufficient to supply the majority of IoT sensor nodes and can only find use in what Blaauw *et al.* referred to as millimiter-size devices in [14], i.e., sensor nodes with extremely limited func-

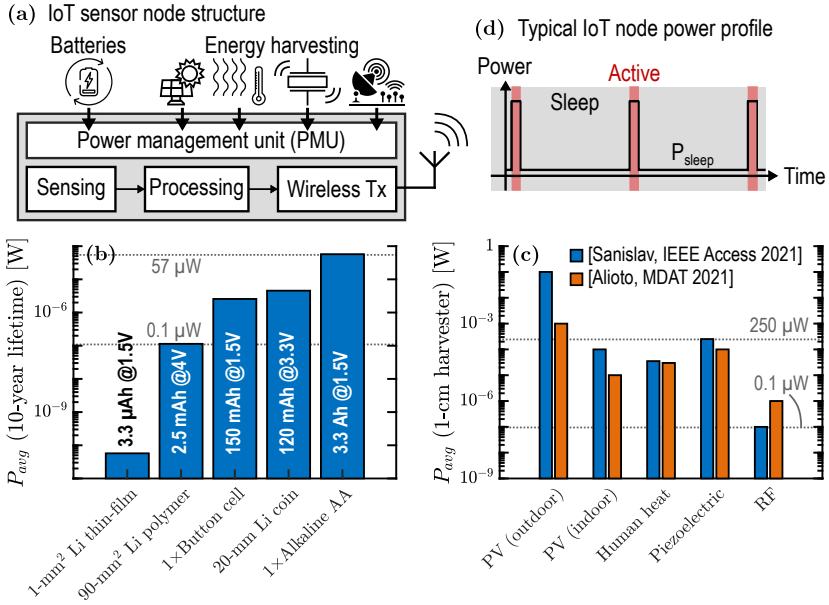

Fig. 2.1 (a) Typical structure of an IoT sensor node, incluuding sensing, processing, and communication functionalities, as well as a power management unit supplied by batteries or energy harvesting. Average power consumption available from (b) different battery types, assuming a 10-year lifetime and no other energy source than the battery, based on [14, 15], and (c) different energy harvesting sources, assuming a harvester with a maximum size of 1 cm, based on [16, 17]. RF power is provided for a relatively short distance between the emitter and the antenna, comprised between 3 and 10 m. (d) Typical power profile of a sensor node, characterized by long periods of sleep and peaks of activity.

tionalities operating at the extreme edge and surviving on a power budget of a few nW. The 90-mm^2 Li polymer (LiPo) battery, providing an average power around 0.1 μW, is a more realistic choice and corresponds to the lower limit of the power budget available from batteries. At the other end of the spectrum, Alkaline AA batteries can deliver an average power of approximately 57 μW, while button and coin cells lie in the middle of the range with 2.6 and 4.6 μW, respectively. On the other hand, Fig. 2.1(c) depicts the average power provided by various energy harvesting sources, based on the data provided in recent studies from Sanislav *et al.* [16] and Alioto *et al.* [17], and assuming that the maximum size of the energy harvester is limited to 1 cm, i.e., 1 cm^2 for a planar harvester and 1 cm^3 for a three-dimensional one. The energy source from which the maximum power can be extracted is photovoltaic, with a power in outdoor conditions ranging from 1 to 100 mW per cm^2, and comprised between 10 to 100 μW per cm^2 in indoor ones. Next, piezoelectric energy harvesters, generating power from vibrations due to walking in the case of wearables, or vibrations of industrial machines in the case of IoT nodes for the industry 4.0, can generate a power between 100 and 250 μW per cm^3. Then, lever-

aging human heat using pyroelectric harvesters allows for a more modest power output around 30-35 μW per cm^2. At last, the power harvested from RF GSM and WiFi signals typically lies between 0.1 and 1 μW per cm^2 for a distance between the emitter and the antenna comprised between 3 and 10 m. Therefore, these analyses of batteries and energy harvesting sources yield an estimated power budget for IoT sensor nodes comprised between 0.1 and 100 μW.

2.1.1.2 The Case for nA-Range Current References

The typical power profile of an IoT sensor node is shown in Fig. 2.1(d), and is often characterized by short activity peaks intertwined with relatively long periods of sleep. Therefore, batteries are frequently used in conjunction with energy harvesting, to store the harvested power in the battery so as to support the higher power consumption in active mode. In such systems, nA-range current references have two interesting use cases. First, for IoT nodes with an average power consumption in the upper end of the power budget, i.e., between 10 and 100 μW, the power in sleep mode P_{sleep} often lies in the 1-to-10-μW range. A good example of such devices are ULP micro-controller units (MCUs) developed in our research group, codenamed SleepRunner [20] and SleepRider [21], whose active power consumptions are respectively 121.2 and 460 μW, and sleep power consumptions 4.4 and 8.4 μW. Commercial ULP MCUs such as Microchip's SAML21 [145] and Ambiq's Apollo3 [146] tell the same story, with a minimum active power of respectively 518 and 864 μW, and a sleep power between 4.9 and 14.2 μW for the SAML21, and between 2.9 and 8.5 μW for the Apollo3. As the fraction of the sleep power allocated to logic and SRAM leakage, as well as unavoidable switching, ranges from 80 to 90 %, this usually leaves a sub-μW power budget for the generation of voltage, current, and frequency references. Due to the absence of switching in voltage and current references, they are typically attributed a small fraction of this remaining budget, so around 100 nW. nA-range current references can thus be leveraged in this use case to support basic analog functions in sleep mode, e.g., a clock generator in the kHz range or a wake-up timer. The second use case in which nA-range current references can be useful is IoT nodes whose power budget is in the lower end of the spectrum defined hereabove, i.e., between 0.1 and 1 μW. In applicative terms, this corresponds to IoT nodes operating at the extreme edge rather than to ULP MCUs. In this case, nA-range current references are employed in active mode and can be useful to bias amplifiers [147, 148] with a constant bandwidth or comparators with a constant delay, if they present a proportional-to-absolute-temperature (PTAT) temperature dependence, or to bias current-mode data converters, oscillators [149, 150], and temperature sensors [151, 152], if they are constant-with-temperature (CWT).

2.1.2 Process, Voltage and Temperature Dependence

An important characteristic of IoT sensor nodes is that they will be deployed in a wide variety of applicative contexts, such as wearables for biomedical applications, fixed nodes used as part of a network for environmental monitoring, smart sensors for the predictive maintenance of machines in industrial plants, etc. Therefore, a desirable feature of the mixed-signal and analog circuits realizing the sensing, processing and communication tasks required by sensor nodes is that they be robust against process, supply voltage and temperature variations. The same requirements extend to current references integrated in sensor nodes. First, three main trends exist to deal with process variations: (i) to rely on hybrid current references using BJTs, as their process variations are less harmful to the reference's performance than process variations of a MOSFET's threshold voltage V_T, (ii) to use a structure which tracks V_T variations to automatically stabilize performance across process corners [153, 131], or (iii) to trim the performance of the reference and store the calibration code using either electrical fuses or a non-volatile memory. Then, the robustness against supply voltage variations required by analog circuits used in sensor nodes is different depending on the fact that the analog circuit is supplied by a regulated voltage generated by the PMU, or by an unregulated voltage. nA-range references employed in sleep mode are typically supplied by an unregulated voltage, to allow powering down parts of the PMU in order to save power consumption. The specification on the dependence to supply voltage or line sensitivity (LS) of the reference current thus really depends on the application, but we observe that a value of 1 %/V is usually acceptable in most cases. Nonetheless, there are various well-known ways to improve the LS of I_{REF}: (i) to employ a technology in which the intrinsic gain (g_m/g_d) of the transistors is inherently large, (ii) to use cascoding where possible, at the cost of an increased minimum supply voltage and thus power consumption, and (iii) to rely on a feedback loop based on an operational transconductance amplifier (OTA) or a single transistor, resulting in power and area overheads. Finally, IoT sensor nodes are usually required to operate over the industrial temperature range, i.e., from -40 to 85°C, or the extended industrial range, i.e., from -40 to 125°C. This is particularly relevant for sensor nodes used for environmental monitoring, but less so for wearables, as they operate in an environment that is withstandable by a human being. Regarding the temperature dependence or temperature coefficient (TC) of the current references, the requirements of IoT sensor nodes are usually relaxed compared to high-precision circuits. An acceptable target for most applications is thus to reach a TC between 100 and 500 ppm/°C, and below 100 ppm/°C for applications requiring a high accuracy of I_{REF}, for example current-mode data converters, and some oscillators and temperature sensor architectures. However, as will be further discussed in Chapter 5, one must keep in mind that a CWT reference current does not necessarily lead to the temperature independence of the performance of interest, and that a non-zero TC

is actually necessary for several analog circuits.

2.1.3 Silicon Area

A last characteristic that still needs to be briefly discussed is silicon area. Historically, minimizing silicon area was sought in order to minimize economical cost. This argument remains valid today at the level of a sensor node, and translates into the minimization of the area occupied the different analog and digital blocks constituting it. In addition, in recent years, discussions around the environmental impacts of electronic circuits and systems have aroused the interest of an increasing number of researchers, and have led to the conclusion that the direct environmental impacts of the production of such systems could be directly related to their silicon area [13]. So minimizing silicon area is also beneficial from an environmental perspective, with two important caveats. First, the reduction of the area of a circuit should not be used to add more functionalities to the system, a trend that has been consistently observed in the past in the context of commercial electronic devices, and which nullifies the area reduction efforts at the level of a single analog block. Next, even though the direct environmental impacts of a single IoT sensor node might benefit from a reduction of its silicon area, the massive production volumes projected for the IoT are likely to lead to a rebound effect, i.e., to an increase of the total impact of all the sensor nodes deployed, despite a potential improvement of the impacts of a single node. Again, this is a well-known pitfall in which the electronics industry has consistently fallen along its history.

2.2 State of the Art of CWT Current References

The outcome of the previous section is that current references used in the context of the IoT should aim at minimizing their silicon area, while providing a nA-range reference current which is as constant as possible with respect to PVT variations. In this thesis, we focus on the minimization of the silicon area and temperature dependence in the nA current range, as current references with such characteristics are of particular interest for IoT sensor nodes, and as techniques to reduce process variations through trimming, or supply voltage dependence through cascoding or OTA-based feedback loops have already been extensively explored in the literature. Firstly, we discuss empirical trends linking the TC and LS with silicon area and normalized power consumption based on the corpus of current reference papers constituted in Chapter 1. These trends are illustrated in Fig. 2.2 and computed using least-square linear regressions of the available data in a log-log scale, for the simulated and measured designs. Figs. 2.2(a) and (b) highlight that

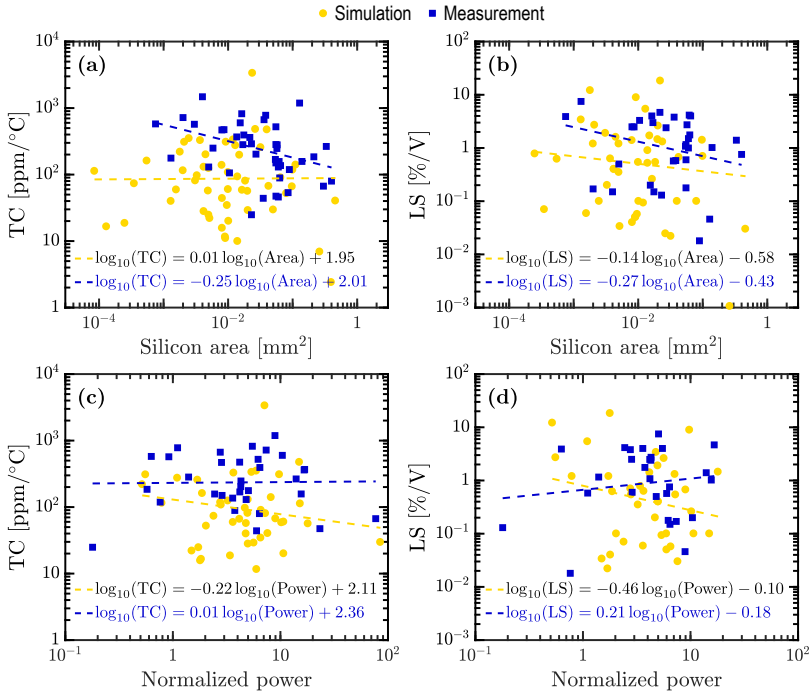

Fig. 2.2 Empirical trends linking the TC and LS with silicon area and normalized power, expressed as Power$(V_{DD,\text{min}})/(1\ \text{V} \times I_{REF})$, extracted from the corpus of current reference papers established in Chapter 1. (a) TC and (b) LS as a function of silicon area, and (c) TC and (d) LS as a function of normalized power. Trends are shown in dashed lines and are computed as least-square linear regressions of the available data in a log-log scale (power law).

reducing the TC and LS requires to increase the silicon area occupied by the reference. Empirical trends based on measured references show that TC $\propto$ Area$^{-0.25}$ and LS $\propto$ Area$^{-0.27}$. Therefore, it could be interesting to modify FoM_1 (1.12) and FoM_3 (1.14) accordingly, to take into account how TC and LS can be traded for area. However, in practice, we believe that the large variability of the available data does not lead to a sufficiently reliable prediction to be able to do so. The variability of the results can likely be explained by the use of different technologies as well as different design specifications regarding for example the variability due to local mismatch, ultimately leading to a different sizing of the reference. Besides, Figs. 2.2(c) and (d) do not establish a clear trend linking the TC and LS with normalized power consumption. Further works could try to refine the observed empirical trends by relying on models combining (i) features enabling TC and LS improvements used in the reference as discrete tuning knobs, and (ii) specifications impacting the sizing of the reference as continuous ones.

Then, to identify the directions in which existing current references could be improved, we also exploit the corpus of papers and plot several metrics as a func-

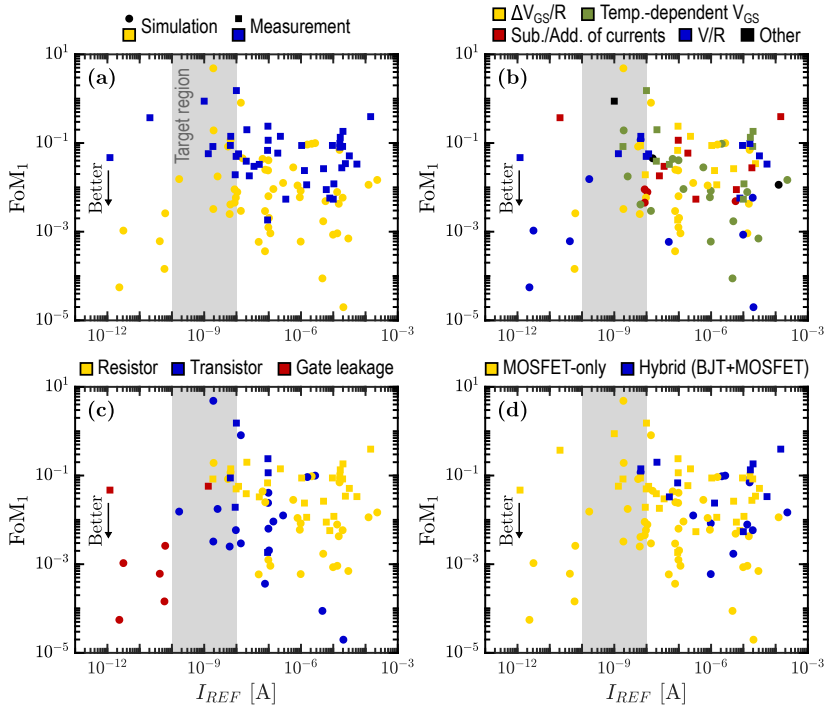

Fig. 2.3 Figure of merit FoM_1 (1.12) combining temperature dependence and silicon area as a function of I_{REF}, providing an overview of existing current references in terms of (a) type of work (simulation vs. measurement), (b) category of CWT current generation technique, (c) V-to-I converter, and (d) transistor type.

tion of the generated reference current [Figs. 2.3 to 2.5], namely the FoM_1 (1.12), the silicon area and the TC of I_{REF}, using four different categorizations:

1. The type of work, i.e., simulation or silicon measurements, as these two types cannot be discussed on equal terms. The TC is indeed often degraded from post-layout simulations to measurements due to inaccuracies in the leakage models of parasitic diodes, or the impact of I/O cells on the measured reference;
2. The four categories of CWT current generation techniques presented in Section 1.3.2, namely $\Delta V_{GS}/R$ references, temperature-dependent V_{GS}, subtraction or addition of currents, or V/R references;
3. The voltage-to-current (V-to-I) converter used in the reference, which is either a resistor, a structure based on transistors, or a gate-leakage transistor;
4. The type of transistors used in the reference, that is only MOSFETs, or a combination of BJTs and MOSFETs that we refer to as hybrid.

In Figs. 2.3 to 2.5, we highlight the region corresponding to a reference cur-

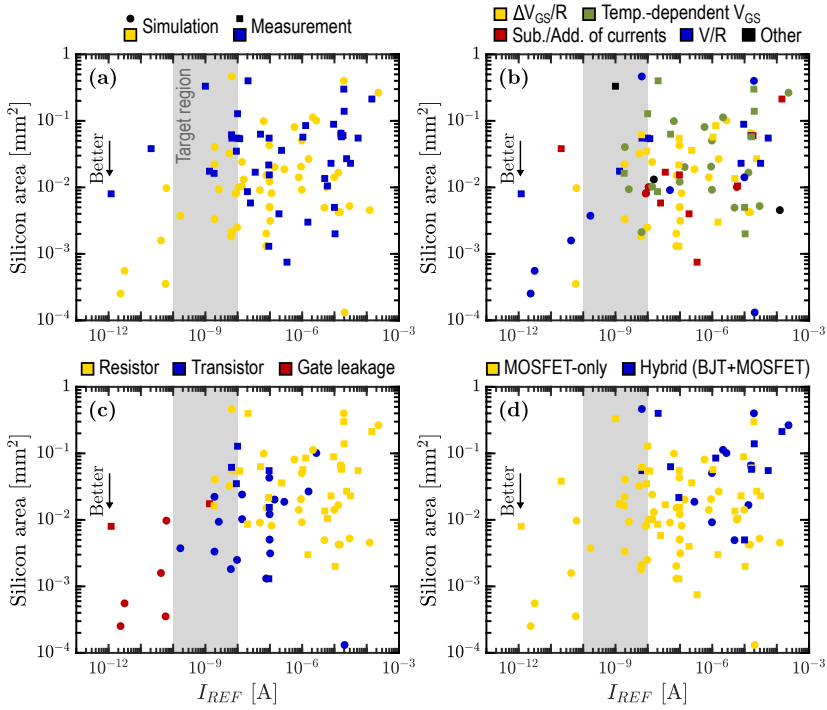

Fig. 2.4 Silicon area as a function of I_{REF}, providing an overview of existing current references in terms of (a) type of work (simulation vs. measurement), (b) category of CWT current generation technique, (c) V-to-I converter, and (d) transistor type.

rent between 0.1 and 10 nA, which corresponds to the design target for IoT current references set in Section 2.1. In contrast, Fig. 2.6 depicts the TC of I_{REF} as a function of silicon area in the target region, to better understand the trade-off between these two characteristics of nA-range current references. An important finding which can immediately be seen from Fig. 2.3 is that, in the target region, there is a lack of current references that are simultaneously area-efficient and temperature-independent, and there is thus room for improvement in this area. To kick off our in-depth discussion of the results, let us focus on the comparison between simulated and measured current references in Fig. 2.3(a). In the case of simulated designs, a difference of at least two orders of magnitude in terms of FoM_1 is observed between current references inside and outside the target region. This difference reduces to one or two orders of magnitude for measured references, but the absolute value of the FoM lags at least one order of magnitude behind that of simulated references. In addition, Fig. 2.3(b) details how the categories of CWT current generation techniques distribute across the current level range. A temperature-dependent V_{GS} has mostly been used to generate currents above 1 nA, which makes sense as the zero TC operation point (ZTC) of a transistor usually corresponds to a current

between 1 and 100 nA. The subtraction or addition of currents is limited to references above 10 nA, with a single exception for the generation of a current around 30 pA. This is likely explained by the fact that two current references with different TCs are required, thereby making this technique less attractive than others in terms of power and area overheads. Finally, $\Delta V_{GS}/R$ and V/R references can be found across the whole current level range, with a center of mass shifted towards lower currents for V/R references. We can explain this trend by the fact that these two categories of CWT current generation techniques can employ different types of V-to-I converters, and that only the converter needs to be replaced to change the generated current level while the rest of the current reference structure remains unchanged. This assumption is confirmed by Fig. 2.3(c), unveiling that gate-leakage transistors are the only type of V-to-I converter used in the region below 0.1 nA, that resistors are predominantly used above 10 nA, and that V-to-I converters based on a transistor-only structure are an interesting solution in the target region between 0.1 and 10 nA. Nonetheless, they coexist with gate-leakage transistors and resistors in this region, stressing the idea that different trade-offs can be achieved based on the choice of V-to-I converter. Lastly, Fig. 2.3(d) shows that hybrid references are only present above 10 nA, and even concentrate in the μA-range region, whereas MOSFET-only references can be found across the whole range of current levels.

Furthermore, we can separately look at the silicon area and TC of I_{REF}, respectively depicted in Figs. 2.4 and 2.5, to better understand the trends underlying Fig. 2.3. First, when comparing the silicon area occupied by simulated and measured references in Fig. 2.4(a), we observe that in the target region and for simulated designs, the smallest area is around 1800 μm^2. This is more than for other current levels, for which some simulated designs manage to reach silicon areas between 100 and 1000 μm^2 in the pA and μA ranges. Then, regarding fabricated references, the smallest design in the target region occupies an area of 16250 μm^2, while designs in the pA and μA range can respectively go as low as 8000 and 750 μm^2. Moreover, Fig. 2.4(c) indicates that resistors are well suited to the generation of currents in the μA range, as a resistance in the order of a few hundreds of kΩ is required and can be realized on chip within a reasonable silicon area. The same can be said for gate-leakage transistors in the pA range, as their equivalent resistance is around a few hundreds of GΩ and is thus adapted to this current level. In the target region, an equivalent resistance of a few hundreds of MΩ is required and is notoriously challenging to implement with either resistors or gate-leakage transistors, as this would require to significantly increase the number of resistors connected in series or the number of gate-leakage transistors connected in parallel to achieve the targeted resistance. This explains why V-to-I converters solely constituted of transistors have emerged as an area-efficient solution to implement current references in the nA range. Besides, Figs. 2.4(b) and (d) do not really offer additional insights and are thus not discussed into details here. Two alternative strategies could however

be followed to achieve a nA-range current based on existing architectures. The first one would be to change the sizes of the resistor or gate-leakage transistor to achieve the required resistance in the order of a few hundreds MΩ. In terms of silicon area, this means that a resistor-based reference operating in the μA range would see its area increased by 100 to 1000$\times$ to reach the nA range, depending on the fraction of the initial area used by the resistor and on the ratio between the initial and target current. The same reasoning holds true for gate-leakage-based references operating in the pA range. In addition, gate leakage cannot be used in technology nodes older than 0.13 μm or 90 nm as it is negligible in such technologies, and can likely not be exploited either in nodes employing high-κ metal gates, as the goal of this techological innovation was precisely to significantly reduce gate leakage. Whether gate leakage could again become more significant and ultimately usable in sub-20-nm technology nodes remains unclear. The second alternative based on existing architectures consists in using a current reference in the μA (resp. pA) range and divide (resp. multiply) the reference current by 100 to 1000$\times$ using several current mirror stages. The requirements in terms of silicon area to implement this solution are mainly related to the mismatch that can be tolerated in the mirroring stages. To provide a quantitative example, let us consider a use case in which a 1-μA current would be decreased down to 1 nA, with the following assumptions:

1. The current division is performed in three stages with a 10:1 ratio;
2. The mismatch in each stage is dominated by the smaller transistor. Using Pelgrom's law, this means that $\sigma^2(\Delta V_T) \approx \sigma^2(V_T)$. In addition, an A_{V_T} of 4.5 mV$\times\mu$m, corresponding to a 0.18-µm bulk technology, is employed [154];
3. Each stage is assumed to operate with a (g_m/I_D) of 25, corresponding to weak/medium inversion, and to predominantly suffer from variations of the threshold voltage V_T, as is usually assumed in the case of weak/medium inversion;
4. The variability of the 1-nA current due to the three mirroring stages should be 1 %. This means that the current variability in each stage must be 1 %/$\sqrt{3}$.

Based on these assumptions and on Pelgrom's law applied to a current mirror [154], we find that

$$\left(\frac{\sigma(\Delta I_{DS})}{I_{DS}}\right)^2 \approx \left(\frac{g_m}{I_D}\right)^2 \sigma^2(\Delta V_T) = \left(\frac{g_m}{I_D}\right)^2 \frac{A_{V_T}^2}{WL}, \tag{2.1}$$

and thus, that the active area required for each mirroring stage is given by

$$(WL)_{\text{stage}} = (10+1)\left[\left(\frac{g_m}{I_D}\right)^2 \frac{A_{V_T}^2}{\left(\frac{\sigma(\Delta I_{DS})}{I_{DS}}\right)^2}\right]. \tag{2.2}$$

With the technological parameters and specifications set hereabove, this leads to

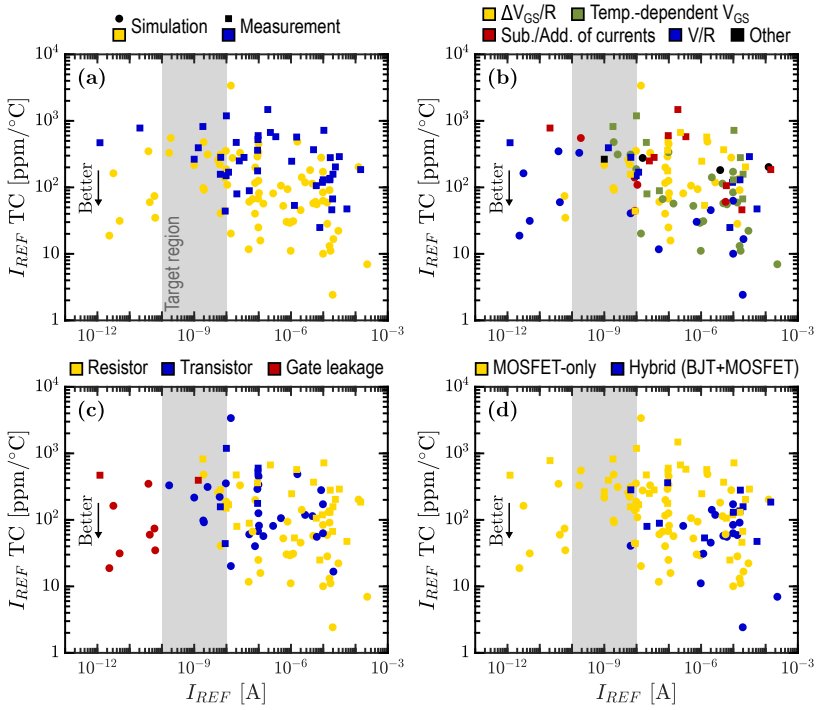

Fig. 2.5 TC of I_{REF} as a function of I_{REF}, providing an overview of existing current references in terms of (a) type of work (simulation vs. measurement), (b) category of CWT current generation technique, (c) V-to-I converter, and (d) transistor type.

an active area of 4176 μm^2 for each stage, and thus, to a total active area around 12500 μm^2 for the current divider. It should be noted that this area needs to be multiplied by a factor 2 or 3$\times$ to obtain the final silicon area, as it does not account for the spacing between devices, source and drain contacts, and the common-centroid layout with dummies necessary to mitigate first-order gradient effects in current mirroring stages. This would ultimately lead to a silicon area between 25000 and 37500 μm^2 which is significant and likely larger than the area occupied by the μA-range reference. However, note that conclusions could be different in a use case in which the required current division factor is not as large as in this example.

Then, we continue with the analysis of the TC of I_{REF} in Fig. 2.5. In Fig. 2.5(a), for simulated references, TCs between 10 and 100 ppm/°C are often attained in the pA and μA ranges, while most of the references in the targeted nA range lie between 100 and 500 ppm/°C and only a handful of references close to 10 nA manage to cross the 100-ppm/°C threshold. Regarding measured references, above 10 nA, the best TC is 25 ppm/°C for a 7.8-μA current and some references are located between 50 and 100 ppm/°C. Nevertheless, when the current level decreases below 10 nA, only one reference reaches a TC below 100 ppm/°C, with a 44-ppm/°C

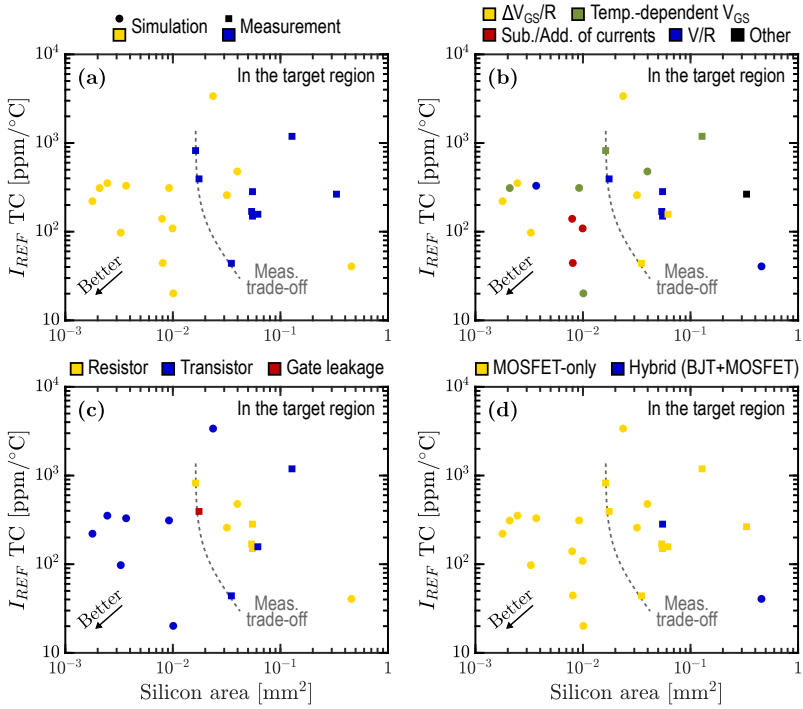

Fig. 2.6 TC of I_{REF} as a function of silicon area in the target region, corresponding to a reference current between 0.1 and 10 nA, providing an overview of existing nA-range current references in terms of (a) type of work (simulation vs. measurement), (b) category of CWT current generation technique, (c) V-to-I converter, and (d) transistor type.

9.1-nA current. All the other fabricated references lie in the 100-to-500-ppm/°C range, with the best TC around 150 ppm/°C attained close to 10 nA. It is also interesting to note that extremely few references based on gate-leakage transistors have been validated with silicon measurements, and that the best TC obtained by such references is only of 470 ppm/°C at 1.2 pA. If we now go through the categories of CWT current generation techniques in Fig. 2.5(b), a striking observation is that V/R references tend to provide the best TC results, closely followed by temperature-dependent V_{GS} and $\Delta V_{GS}/R$ references above 10 nA. Across the whole current level range, the subtraction or addition of currents tends to lag behind, with only a limited number of designs crossing the 100-ppm/°C threshold around 10 μA. Next, the type of V-to-I converter in Fig. 2.5(c) certainly plays a role on the TC that can be reached, with resistors and gate-leakage transistors easily allowing to reduce the TC below 100 ppm/°C, and even below 10 ppm/°C around 10 μA. On the contrary, transistor-based V-to-I converters clearly lag behind resistors above 10 nA, with few designs lying below 100 ppm/°C and a vast majority located above this threshold. This phenomenon originates from the fact

that resistors and gate-leakage transistors present a relatively linear dependence to temperature, while the temperature dependence of the drain-to-source current of transistors stems from the concurrent linear decrease of the threshold voltage V_T and nonlinear increase of the specific current I_{SQ}, proportional to T^{2-m} where T is the absolute temperature and m is the temperature exponent of carrier mobility, usually comprised between 1.2 and 2 in bulk technologies [49]. Finally, Fig. 2.5(d) emphasizes that hybrid references are superior to MOSFET-only ones in terms of TC in the μA range, partly due to the use of curvature or second-order compensation techniques in such references, whereas these techniques are less mature and thus less widely used in MOSFET-only references.

Lastly, we study the trade-off between the TC of I_{REF} and silicon area in the target region, corresponding to a reference current between 0.1 and 10 nA. Fig. 2.6(a) illustrates the measured trade-off between TC and area, with the three points on this trade-off curve corresponding to [31], [45] and [71] from the smallest to the largest silicon area. These works respectively occupy an area of 0.0163, 0.0175 and 0.035 mm^2, and attain TCs of 822, 394 and 44 ppm/°C. Regarding the CWT current generation techniques in Fig. 2.6, we notice that all the techniques coexist in the target region. Using a temperature-dependent V_{GS} does not appear to yield a outstandingly good TC, as all of the works except for one present a TC above 300 ppm/°C. The references based on the subtraction or addition of currents are not particularly area-efficient, with the three simulated references belonging to this category featuring an area around 0.01 mm^2. Besides, $\Delta V_{GS}/R$ and V/R references present a wide diversity of results and it is not really possible to conclude anything regarding their expected level of performance. In Fig. 2.6(c), all the simulated designs on the left of the measured trade-off line make use of a transistor-based V-to-I converter, and are characterized by an improved TC and silicon area compared to existing fabricated references. An improvement of one order of magnitude in terms of both of these characteristics could potentially be obtained, if new references were able to match the simulated performance. Fig. 2.6(d) ultimately tells us that very few hybrid references are used in the target region, as BJTs are not well suited to this level of current.

2.3 Research Directions to Improve Existing References

To conclude this chapter, we outline research directions that could potentially improve the performance of existing current references, to enhance their suitability with respect to the requirements of IoT sensor nodes. As already stated in this chapter, the main focus of this thesis is the improvement of the silicon area and TC of existing current references. Therefore, the research directions that we deem relevant in that regard are:

1. To use a resistor or gate-leakage transistor to reach a low TC by leveraging their quasi-linear dependence to temperature, but to reduce the voltage used to bias them compared to existing designs, in order to reduce the required resistance and the silicon area necessary to their implementation. A way of generating such a small bias voltage is for example to rely on a slight difference of threshold voltage ΔV_T between two transistors in a $\Delta V_{GS}/R$ architecture, obtained by using forward body biasing (FBB) on one of the two transistors so as to reduce its V_T. This first research direction will be explored in Section 3.2 of Chapter 3;
2. To use a transistor-based V-to-I converter to exploit its inherently low area usage, but to devise a new biasing strategy to improve the TC compared to existing architectures. The self-cascode MOSFET (SCM) presented in the context of nA-range PTAT current references [26, 27, 28] appears as an interesting candidate, as little research has been conducted on this structure in the context of CWT current references, likely because of its relatively complex sizing compared to alternative solutions. This second research direction will be pursued in Section 3.1 of Chapter 3 and Section 4.2 of Chapter 4;
3. To rely on V/R references, which appear to provide a low TC within a small silicon area, especially in the pA range, thanks to the replacement of the area-hungry bandgap reference and OTA-based feedback loop, used to implement the voltage reference and buffering stage, by a two-transistor (2T) voltage reference with a single-transistor (1T) buffer [29, 30]. This final research direction will be investigated in Chapter 4, with both resistors and SCMs as V-to-I converters, yielding a complete family of current references.

3

$\Delta V_{GS}/R$ Current References Operating in the nA Range

Analog design is not black or white as in "ones" and "zeros",
analog design is shades of gray.
– Samuel Wilensky

CURRENT references for the Internet of Things (IoT) need to generate a current in the nA range while being area-efficient and robust to process, voltage and temperature (PVT) variations, as established in Chapter 2. Therefore, this chapter explores two research directions in the context of $\Delta V_{GS}/R$ current references generating a nA-range current, each research direction yielding a different trade-off between silicon area and temperature coefficient (TC) of the reference current. These research directions both aim at answering the research question

"How can we practically modify existing current references to meet the specific requirements of the IoT ?",

identified in the introduction of this thesis. The first research direction presented in Section 3.1 consists in using a voltage-to-current (V-to-I) converter well-suited to the generation of a nA-range current, namely a self-cascode MOSFET (SCM), biased by a proportional-to-absolute-temperature (PTAT) voltage with a constant-with-temperature (CWT) offset voltage to make the reference current CWT. This offset voltage is obtained as the threshold voltage difference ΔV_T between two weak-inversion transistors of the same V_T type, one of them being forward body-biased

to reduce its V_T. Then, the second research direction developed in Section 3.2 is to bias a resistor with a lower voltage compared to previous current reference topologies to reduce the required resistance and the silicon area necessary to implement it. The resistor is biased by a peaking current reference (PCR), using the same ΔV_T between two subthreshold MOSFETs of the same V_T type as in the first research direction implemented by the forward body biasing (FBB) of one of the transistors, here implemented by a two-transistor (2T) ultra-low-power (ULP) voltage reference. Finally, Section 3.3 summarizes the key messages of this chapter.

3.1 An SCM-Based β-Multiplier

In this first part of Chapter 3, we propose a nA-range CWT current reference based on an SCM, which differs from [27, 28] by the addition of a CWT offset to the PTAT voltage biasing the SCM. This offset voltage is key in making SCM-based references CWT, and is obtained as the threshold voltage difference ΔV_T between two transistors of the same V_T type, one of them being forward body-biased to reduce its threshold voltage. For the sake of generalization, this section expands on our conference paper [155] by demonstrating the feasibility of the proposed reference in a conventional bulk technology, compared to fully-depleted silicon-on-insulator (FD-SOI) only in [155]. The proposed reference is validated in two CMOS technologies through post-layout simulations in TSMC 65-nm bulk and measurements in GlobalFoundries (GF) 22-nm FD-SOI. In addition, it provides additional insight into the design, architecture and post-layout simulations of the reference in both technologies. This section is structured as follows. Section 3.1.1 explains the operation principle of the proposed reference based on its governing equations. Next, Section 3.1.2 details the methodology used to size the reference. Then, Section 3.1.3 discusses design optimizations, as well as simulation results in 65 and 22 nm, while Section 3.1.4 presents the measurement results in 22 nm. Finally, Section 3.1.5 compares the proposed reference to the state of the art, and Section 3.1.6 offers some concluding remarks.

3.1.1 Governing Equations and Operation Principle

In this section, our first objective is to explain how the addition of a CWT offset to the voltage biasing the SCM leads to a temperature-independent reference current, based on general equations governing the current reference behavior. Then, we highlight the differences with respect to PTAT references [27, 28] and detail how temperature independence is achieved in the proposed reference with generic parameters. Finally, we compare different ways of implementing the offset voltage.

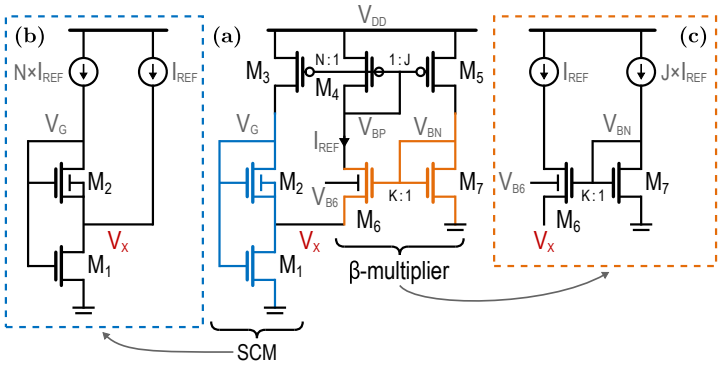

Fig. 3.1 Basic schematic of the proposed current reference, which consists of an SCM formed by M_{1-2} (in blue) and further simplified in (b), and a β-multiplier composed of M_{6-7} (in orange) summarized in (c).

3.1.1.1 *Governing Equations*

To establish the equations governing the reference, we rely on the schematic in Fig. 3.1(a), which consists of two main elements: an SCM and a β-multiplier, both supplied by pMOS current mirrors. First, the SCM relies on long-channel transistors in moderate inversion, for which a simplified model such as the analog compact MOSFET (ACM) model [156] is adequate to describe the transistor current-voltage (I-V) curve. Detailed equations of this model are provided in Appendix A.2.

The ACM equations are applied to the SCM [Fig. 3.1(b)] in Appendix B, but in this work, the connection of the body of M_2 to its source leads to some differences requiring to derive the equations while taking this connection into account. This leads to two distinct equations. The first one is obtained by defining $\alpha \triangleq i_{f1}/i_{f2} > 1$ and expresses voltage V_X as

$$V_X = nU_T \left[\left(\sqrt{1+\alpha i_{f2}} - \sqrt{1+i_{f2}} \right) + \log \left(\frac{\sqrt{1+\alpha i_{f2}} - 1}{\sqrt{1+i_{f2}} - 1} \right) \right], \tag{3.1}$$

while the second one relates $\beta \triangleq i_{r1}/i_{f2} \in [0;1]$ to voltage V_X and amounts to

$$V_X(n-1) = nU_T \left[\left(\sqrt{1+i_{f2}} - \sqrt{1+\beta i_{f2}} \right) + \log \left(\frac{\sqrt{1+i_{f2}} - 1}{\sqrt{1+\beta i_{f2}} - 1} \right) \right]. \tag{3.2}$$

Then, the ratio of the aspect ratios of M_{1-2} must comply with

$$\frac{S_1}{S_2} = \frac{I_{SQ2}}{I_{SQ1}} \frac{1+N}{N} \frac{1}{\alpha - \beta} \tag{3.3}$$

to ensure that Kirchhoff's current law is respected, N being the current ratio between M_3 and M_4. Next, the ACM equations are applied to the weak-inversion transistors M_{6-7} constituting the β-multiplier [Fig. 3.1(c)]. We consider two distinct cases to obtain the expression of voltage V_X. First, the case in which $V_{B6} = V_X$ and M_{6-7} have different threshold voltages. In this case, V_X is given by

$$V_X \simeq n_6 U_T \log(JK) + \left(\frac{n_6}{n_7} V_{T07} - V_{T06}\right), \tag{3.4}$$

$$= n U_T \log(JK) + (V_{T07} - V_{T06}), \tag{3.5}$$

J and K being current mirror ratios, with (3.4) corresponding to transistors with different V_T types and hence entirely distinct characteristics, and (3.5) to transistors of the same V_T type but with different lengths, and thus similar characteristics except for their V_{T0}. Second, we deal with the case in which $V_{B6} > V_X$, M_{6-7} have the same V_T type and length, and forward body / back-gate biasing (FBB) is leveraged to reduce V_{T6}. If the impact of the body effect on threshold voltage is modeled as $V_T = V_{T0} - \gamma_b^* V_{BS}$ for an nMOS, with γ_b^* denoting the linearization of the body factor around $V_{BS} = 0$, voltage V_X is computed as

$$V_X = n U_T \log(JK) + \gamma_b^* (V_{B6} - V_X). \tag{3.6}$$

Ultimately, regardless of the origin of ΔV_T, (3.4) to (3.6) boil down to a single expression

$$V_X = n U_T \log(K_{PTAT}) + \Delta V_T, \tag{3.7}$$

with $K_{PTAT} \triangleq JK$. Connecting the SCM and the β-multiplier as in Fig. 3.1(a) amounts to equating (3.1) and (3.7), and leads to

$$\left[\left(\sqrt{1+\alpha i_{f2}} - \sqrt{1+i_{f2}}\right) + \log\left(\frac{\sqrt{1+\alpha i_{f2}} - 1}{\sqrt{1+i_{f2}} - 1}\right)\right] = \log(K_{PTAT}) + \frac{\Delta V_T}{n U_T}, \tag{3.8}$$

in which only the term highlighted in red is temperature-dependent due to the combined temperature dependence of ΔV_T and U_T. Besides, applying (A.4) to M_2 gives the expression of the reference current

$$I_{REF}(T) = I_{SQ2}(T) i_{f2}(T)(S_2/N), \tag{3.9}$$

where $I_{SQ2}(T) \propto U_T^2 \mu(T) \propto T^{2-m}$, with $\mu(T) = \mu(T_0)\,(T/T_0)^{-m}$, and m is the temperature exponent of the carrier mobility. An important quantity which remains to be defined is the sensitivity of the reference current to V_X,

$$S_{I_{REF}} = \frac{1}{I_{REF}} \frac{dI_{REF}}{dV_X} = \frac{1}{I_{REF}} \frac{dI_{REF}}{di_{f2}} \frac{di_{f2}}{dV_X}, \tag{3.10}$$

with I_{REF} expressed by (3.9) and di_{f2}/dV_X computed from (3.1), consequently yielding

$$S_{I_{REF}} = \frac{2}{i_{f2} n_2 U_T} \left[\frac{\alpha}{\sqrt{1+\alpha i_{f2}}-1} - \frac{1}{\sqrt{1+i_{f2}}-1} \right]^{-1}. \tag{3.11}$$

This quantity is linked to the small-signal resistance of the SCM by (3.16), and is of particular interest as it allows to relate the performance metrics of I_{REF}, such as LS and variability, to those of V_X, which depend entirely on the β-multiplier, through (3.18) and (3.21). In addition, in what follows, the LS and TC are computed using the box method following (1.2) and (1.4), as discussed in Chapter 1.

3.1.1.2 Operation Principle

In prior art [27, 28], a PTAT reference current is obtained with $V_{B6} = V_X$ and M_{6-7} sharing the same V_T type and length, thus yielding $\Delta V_T = 0$ and resulting in a purely PTAT voltage V_X [Fig. 3.2(a)]. Equation (3.8) subsequently becomes temperature-independent as the term in red amounts to zero. It also means that i_{f2} does not change with temperature [Fig. 3.2(b)]. Ultimately, this forces I_{REF} to have the same temperature dependence as I_{SQ}, as stated by (3.9), and to follow a PTAT trend dictated by T^{2-m} [Fig. 3.2(c)].

In the proposed CWT current reference, an offset voltage $\Delta V_T > 0$ which is made CWT by design is added to V_X [Fig. 3.2(a)], augmenting (3.8) with the temperature-dependent term in red. This causes i_{f2} to decrease with temperature [Fig. 3.2(b)] and, with a proper selection of parameters $(K_{PTAT}; \alpha)$, can make the temperature dependence of i_{f2} compensate that of I_{SQ}. This results in a temperature-independent I_{REF} as depicted in Fig. 3.2(c). An obvious question which arises at this stage is how to choose $(K_{PTAT}; \alpha)$ to reach temperature independence. In Figs. 3.3(a) and (b), we study their impact on two figures of merit (FoMs) of the current reference, namely the TC of I_{REF} and $S_{I_{REF}}$, for a fixed CWT ΔV_T = 20 mV, and generic technological parameters n = 1.2 and m = 1.25. Fig. 3.3(a) reveals the existence of an I_{REF} TC valley for a linear relationship between K_{PTAT} and α. Furthermore, this valley corresponds to an iso-sensitivity curve in Fig. 3.3(b). In Fig. 3.3(c), we assess the influence of ΔV_T on the location of the I_{REF} TC valley, and notice that increasing ΔV_T raises both the slope and offset of the linear relation between these two parameters. Technological parameters also have an influence on the valley location, with n and m having respectively an effect opposite and similar to ΔV_T. However, these parameters are fixed by the technology and we do not consider them as potential tuning knobs for design. Lastly, Fig. 3.3(d) depicts the evolution of the FoMs for ΔV_T ranging from 10 to 30 mV, $\alpha = 4$, and K_{PTAT} corresponding to the I_{REF} TC valley. It emphasizes that a constant 80-ppm/°C TC can be achieved with a proper choice of parameters, but that $S_{I_{REF}}$ improves from 7.33 to 2.45 %/mV with a growing ΔV_T. This trend is explained by the fact that an increase in V_X pushes M_{1-2} further into moderate inversion and decreases $S_{I_{REF}}$, at the cost

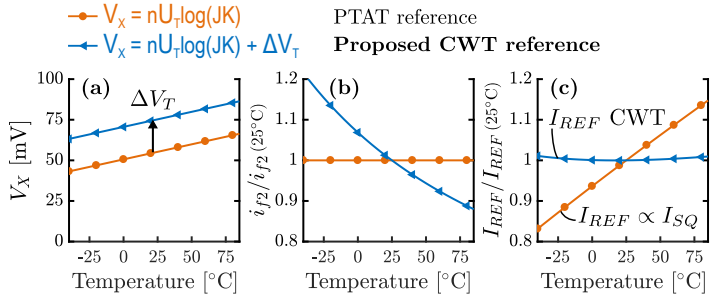

Fig. 3.2 Operation principle of PTAT references proposed in prior art [27, 28] (in orange) and of the proposed CWT reference (in blue). Analytical expression of (a) the voltage V_X applied to the SCM, (b) the inversion level of M_2, denoted as i_{f2}, and (c) the reference current I_{REF}, as a function of temperature and for ΔV_T = 20 mV. Generic technological parameters n = 1.2 and m = 1.25 are selected. (b) and (c) are normalized by their value at 25°C. For the proposed CWT reference, the parameters leading to a minimum I_{REF} TC are K_{PTAT} = 6 and α = 2.9.

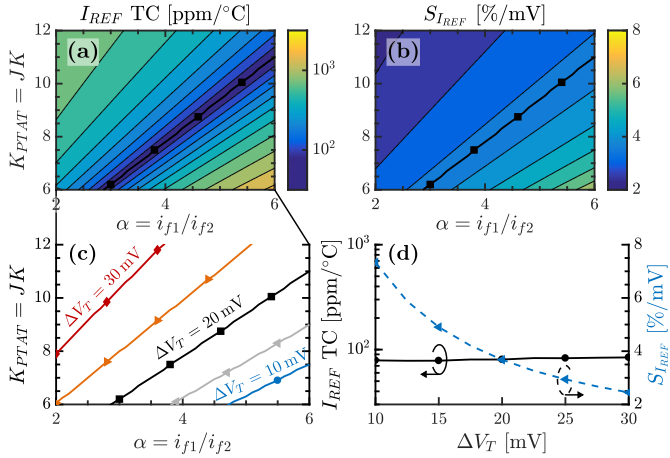

Fig. 3.3 Analytical expression for (a) the TC of I_{REF} and (b) the sensitivity $S_{I_{REF}}$, as a function of K_{PTAT} and α, and for the same technological parameters as Fig. 3.2. (c) Location of the I_{REF} TC valley in the $(K_{PTAT}; \alpha)$ space, for ΔV_T ranging from 10 to 30 mV. (d) I_{REF} TC and $S_{I_{REF}}$ as a function of ΔV_T, for α = 4 and the optimal value of K_{PTAT}.

of an increased area for the SCM and a larger minimum supply voltage. The values taken by parameters $(K_{PTAT}; \alpha)$ are thus practically limited by such considerations during the sizing.

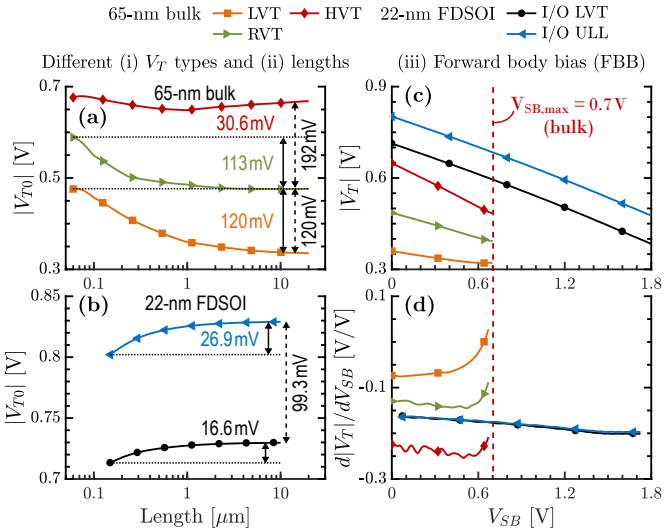

Fig. 3.4 All figures correspond to 1-μm-wide standard-well pMOS devices simulated at 25°C, and the threshold voltage is extracted from g_m/I_D vs. V_{SG} curves as described in [157]. $|V_{T0}|$ variations with the transistor length for (a) LVT, RVT and HVT core pMOS in 65-nm bulk and (b) LVT and ULL I/O pMOS in 22-nm FD-SOI. For 1-μm-long devices, (c) $|V_T|$ and (d) $d|V_T|/dV_{SB}$ with V_{SB} for 65- and 22-nm devices. V_{SB} is limited by 0.7 V in 65 nm, to avoid the forward biasing of the parasitic diode between the transistor's source and body, and by the 1.8-V supply voltage in 22 nm.

3.1.1.3 *Practical Implementation of* ΔV_T

The question that remains to be answered is how the offset voltage ΔV_T is practically achieved in the proposed current reference, knowing that it should ideally be CWT to ease the sizing, and that it does not need to be very large, as $S_{I_{REF}}$ improves less and less for large ΔV_T values [Fig. 3.3(d)]. In addition, a large ΔV_T also increases voltage $V_{GS1} = V_G$ in the SCM, resulting in a larger minimum supply voltage. A good trade-off is thus to have ΔV_T around 20 to 25 mV. Note that in what follows, we opt for an implementation based on a pMOS SCM as it limits the area overhead by using nwells instead of triple wells, and by leveraging the lower specific current of pMOS devices compared to nMOS ones. Three options are available to obtain a threshold voltage difference between two transistors: (i) different V_T types, (ii) the same V_T type but different lengths, and (iii) leveraging FBB to change the V_T of one out of two transistors sharing the same V_T type and length. Figs. 3.4(a) and (b) illustrate the variations of $|V_{T0}|$ for pMOS devices, respectively in TSMC 65-nm bulk [Fig. 3.4(a)] in which low-, regular- and high-V_T (LVT / RVT / HVT) core devices are available, and GF 22-nm FD-SOI [Fig. 3.4(b)], in which low-V_T (LVT) and ultra-low-leakage (ULL) I/O devices are available. Both figures show that the V_T difference resulting from using different transistor types is typically between 0.1 and 0.2 V, and is hence much larger than the ΔV_T we seek to

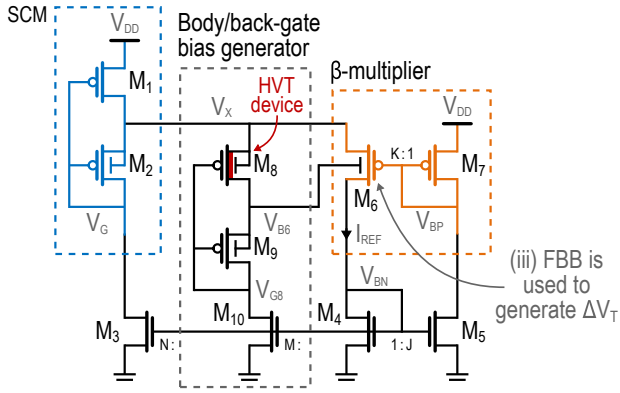

Fig. 3.5 Schematic of the proposed reference with a pMOS-based topology, featuring a low-power voltage reference to generate the body / back-gate voltage V_{B6}. This voltage reference is formed by transistors M_{8-10} and relies on the V_T difference between HVT and LVT pMOS in 65-nm bulk (resp. ULL and LVT pMOS in 22-nm FD-SOI). Note that an nMOS-based topology is also possible, at the cost of a slightly larger silicon area due to the use of triple-well devices.

achieve. Then, the same V_T type but different lengths is a possibility to implement a ΔV_T in the desired range, with a difference from 31 to 120 mV in 65 nm, and from 17 to 27 mV in 22 nm. Nevertheless, this solution requires one of the transistors to be close to minimum length, which degrades other FoMs such as line sensitivity and mismatch, and leads to undesired second order effects due to the use of short-channel devices. Lastly, Figs. 3.4(c) and (d) represent the evolution of V_T and the derivative dV_T/dV_{SB} as a function of V_{SB}. Fig. 3.4(d) shows that in 65 nm, the body factor ranges from 74 to 244 mV/V depending on the V_T type, while in 22 nm, it is around 165 mV/V close to zero V_{SB}, i.e., body / back-gate and source connected to the same voltage. In this work, we choose to exploit FBB as it allows to obtain a positive offset ΔV_T contrary to RBB, provides a sufficient tuning range for a 20-to-25-mV ΔV_T, and offers the advantage of having devices M_{6-7} with the same technological parameters.

A schematic of the proposed current reference including the body / back-gate bias generator (M_{8-10}) is represented in Fig. 3.5. Note that the topology has been inverted compared to Fig. 3.1(a), i.e., nMOS and pMOS devices are swapped, as well as ground and supply voltage connections. The proposed reference is thus built around a pMOS-based SCM. The voltage reference is based on the ΔV_{SG} between an HVT (M_8) and LVT (M_9) devices biased by a current source (M_{10}). It generates a positive reference voltage thanks to the V_T difference between M_{8-9}, which are practically implemented with core HVT and LVT devices in 65 nm (resp. I/O ULL and LVT devices in 22 nm). Assuming a weak-inversion transistor in

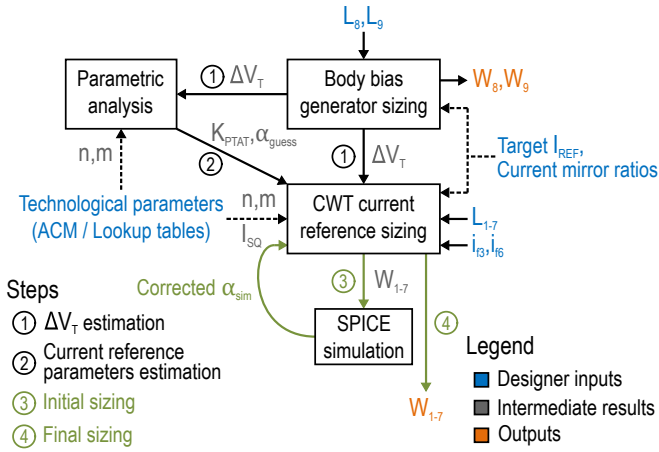

Fig. 3.6 Four-step flowchart of the design and sizing methodology.

saturation, i.e., with $V_{SD} > 4U_T$, V_{SG} is expressed as

$$V_{SG} = |V_{T0}| + nU_T \log\left(\frac{I_{SD}}{I_{SQ}S}\right), \tag{3.12}$$

where $I_{SQ} = \mu C'_{ox}(n-1)U_T^2$ is another definition of the specific sheet current. Using (3.12), V_{SB6} is equal to

$$V_X - V_{B6} = |V_{T08} - V_{T09}| + nU_T \log\left(\frac{I_{SQ9}S_9}{I_{SQ8}S_8}\right), \tag{3.13}$$

in which the first term is either PTAT or complementary-to-absolute-temperature (CTAT) depending on the TC of the threshold voltages, and the second term's TC can be tuned by changing the ratio S_9/S_8. This voltage reference will be sized so that ΔV_T between M_6 and M_7 is temperature-independent, as detailed in Section 3.1.2.2. Finally, the voltage reference changes the ratio (3.3) to

$$\frac{S_1}{S_2} = \frac{I_{SQ2}}{I_{SQ1}} \frac{1 + \mathbf{M} + N}{N} \frac{1}{\alpha - \beta}. \tag{3.14}$$

3.1.2 Design and Sizing Methodology

3.1.2.1 Overview of the Methodology

Fig. 3.6 provides a flowchart of the sizing methodology. It requires inputs from the designer, i.e., a target reference current, current mirror ratios, transistor lengths and inversion levels, as well as technological parameters, and it outputs transistor

widths. The methodology is divided into four steps.

Step 1) consists in sizing the body / back-gate bias generator by selecting W_{8-9} such that ΔV_T's TC is minimized.

Step 2) makes an educated guess of the value of α minimizing the TC of I_{REF} for a fixed K_{PTAT}, which is denoted as α_{guess}. The prediction is based on the linear relationship between K_{PTAT} and α obtained through the parametric analysis developed in Section 3.1.1.1. It requires the ΔV_T computed by step 1), and technological parameters n and m, obtained by fitting the ACM model to g_m/I_D curves extracted from SPICE simulations as lookup tables [157].

Step 3) sizes the current reference for a range of α values and a fixed K_{PTAT}, based on ΔV_T and parameters n, m and I_{SQ}. Several sizings, which differ by the widths of M_{1-2}, are used to perform pre-layout SPICE simulations, from which we extract the value of α leading to a minimum I_{REF} TC. This value is referred to as α_{sim} and should be close to α_{guess}.

Step 4) simply consists in running the sizing algorithm with $\alpha = \alpha_{\text{sim}}$, thereby delivering the final transistor widths.

3.1.2.2 Body / Back-Gate Bias Generator

The setup employed to size the body / back-gate bias generator is illustrated in Fig. 3.7(a). It is composed of a low-power voltage reference formed by M_{8-9}, biased by an ideal current source $M \times I_{REF}$ with $M = 1$ and $I_{REF} = 1.25$ nA, and transistors M_{6-7}, respectively body-biased by a positive and zero V_{SB}. For M_{8-9}, we choose a relatively long length of 5 μm in 65 nm and 8 μm in 22 nm to reduce LS and variability. In Figs. 3.7(b) and (c), the width of M_{8-9} is swept from 0.5 to 5 μm in 0.1-μm steps to select the design point minimizing the TC of ΔV_T in 22 nm. Figs. 3.7(b) and (d) show that it corresponds to a slightly CTAT yet close to CWT $V_X - V_{B6}$, with a 123-ppm/°C TC, and achieves a 31-ppm/°C ΔV_T in Figs. 3.7(c) and (e). This result is consistent with the fact that ΔV_T is obtained through the back-gate effect, as described for an nMOS by $V_T(V_{BS}) = V_{T0} - \gamma_b^* V_{BS}$, where the linearized body factor γ_b^* is temperature-independent at first order in FD-SOI [158]. In 65 nm, a CTAT 1230-ppm/°C $V_X - V_{B6}$ voltage is required to obtain a CWT 46-ppm/°C ΔV_T, as it is obtained through the temperature-dependent body effect

$$V_T(V_{BS}) = V_{T0} + \gamma_b \left(\sqrt{2\phi_{fp} - V_{BS}} - \sqrt{2\phi_{fp}} \right), \tag{3.15}$$

where ϕ_{fp} is Fermi's potential.

3.1.2.3 Temperature-Independent Current Reference

The parametric analysis yields Figs. 3.8(a) and (b), which are akin to Fig. 3.3, but for 22 nm and a ΔV_T of 17.6 mV. As already described in Section 3.1.1.2, the I_{REF} TC valley corresponds to a linear relationship between K_{PTAT} and α, along with an iso-$S_{I_{REF}}$ curve. Next, the current reference sizing per se can be performed in two

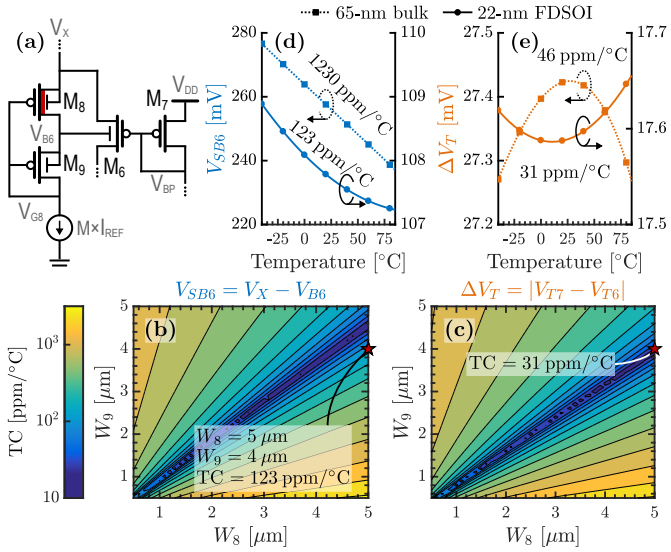

Fig. 3.7 ΔV_T is made CWT by tuning the TC of V_{SB6} by means of the ratio S_9/S_8 (3.13). All figures correspond to the behavior in TT. (a) Schematic and testbench of the low-power voltage reference used to generate V_{B6}. TC of (b) $V_X - V_{B6}$ and (c) ΔV_T, for different widths of M_{8-9} with $L = 8\ \mu$m in 22 nm. (d) Reference voltage $V_X - V_{B6}$ and (e) resulting threshold voltage difference ΔV_T as a function of temperature at the chosen design point.

ways. The first one is similar to the sizing methodology proposed in [27, 28] and is based solely on the ACM model. It consists of five main steps:

1. Compute voltage V_X using (3.7);
2. Solve (3.1) for i_{f2}, then calculate $i_{f1} = \alpha i_{f2}$, $S_{I_{REF}}$ from (3.11), and S_2 from (A.4);
3. Solve (3.2) for β, calculate $i_{r1} = \beta i_{f2}$ and S_1 from (3.14);
4. Compute the aspect ratio of M_{6-7} using (A.4);
5. Compute the aspect ratio of transistors M_{3-5} and M_{10} forming the current mirrors using (A.4).

The second way to perform the sizing replaces steps b) – c) by a direct use of lookup tables. The gate voltage of M_{1-2} is swept while keeping V_X to the value fixed by a), thus providing sizes complying with the SCM structure. This second method is theoretically more accurate, as transistors are better described by lookup tables than by a limited set of parameters.

Let us now take a closer look at the results of the sizing algorithm, with Figs. 3.8(a) to (d) presenting sizing results in 22 nm and Figs. 3.8(e) and (f), results in both 65 and 22 nm. Fig. 3.8(c) is obtained by fixing K_{PTAT} to 6 and extracting a slice of the 3D surface in Fig. 3.8(a). It reveals that the 70-ppm/°C TC found for $\alpha_{\text{guess}} = 4.975$ closely matches the location of the minimum TC obtained from pre-layout simulations for $\alpha_{\text{sim}} = 5$, but differs in terms of value with a slightly larger 119-ppm/°C

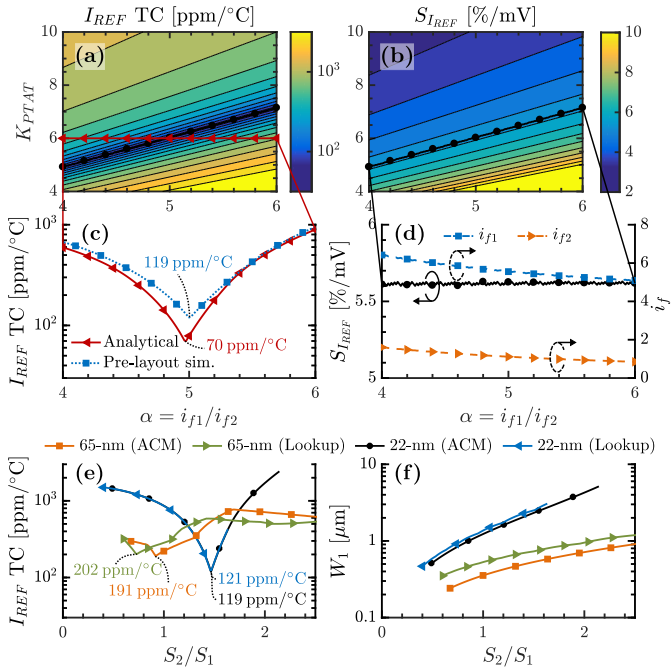

Fig. 3.8 I_{REF} is made CWT by properly selecting K_{PTAT} and α. (a) I_{REF} TC and (b) $S_{I_{REF}}$ for different values of (K_{PTAT}; α) with ΔV_T = 17.6 mV, m = 1, and n = 1.2, obtained from step 1) of the sizing methodology. In 22 nm and for different values of α, (c) I_{REF} TC computed from the analytical model and pre-layout simulation results, with the reference sized using an ACM-based approach, and (d) $S_{I_{REF}}$ and i_{f1}, i_{f2}. In 65 and 22 nm, (e) I_{REF} TC and (f) W_1 as a function of S_2/S_1, for both ACM- and lookup-table-based sizings.

TC. Moreover, Fig. 3.8(d) indicates that, along the I_{REF} TC valley, $S_{I_{REF}}$ remains stable around 5.62 %/mV while i_{f1}, i_{f2} decrease for larger values of α, as M_{1-2} are pushed closer to weak inversion. Then, Fig. 3.8(e) depicts the TC of I_{REF} computed from pre-layout simulations as a function of S_2/S_1, which is a proxy for α (3.14). In 65 nm, pre-layout simulation results faintly diverge, with the ACM-based sizing leading to a 191-ppm/°C TC at S_2/S_1 = 0.92, and the lookup-table-based one to a 202-ppm/°C TC at S_2/S_1 = 0.73. In addition, the ACM-based sizing tends to output a narrower transistor M_1 than its lookup-table-based counterpart [Fig. 3.8(f)]. These discrepancies are presumably related to the approximated transistor behavior resulting from the estimation of ACM model parameters, as well as second order effects such as channel width modulation. In 22 nm, both sizing methods come up with a minimum at S_2/S_1 = 1.47, and Fig. 3.8(f) confirms that the sizes output by both algorithms are in close agreement.

3.1.3 Optimization and Simulation Results

This section comes in two parts. First, Sections 3.1.3.1 and 3.1.3.2 introduce architectural optimizations to the proposed reference, by respectively discussing how to improve LS and how to limit the TC degradation due to parasitic diode leakage at high temperature. Next, Section 3.1.3.3 presents the schematic and post-layout simulation results of the proposed reference implemented in two common scaled technologies, i.e., TSMC 65-nm bulk and GF 22-nm FD-SOI.

3.1.3.1 Line Sensitivity Improvement by Low-Voltage Cascoding

Low-voltage cascoding is often used in scaled technologies to improve LS without compromising the minimum supply voltage. An analytical approach allows to better grasp which transistors induce a dependence to supply voltage in the first place. The SCM in Fig. 3.5 can be simplified by a resistor [Fig. 3.9(a)] with an equivalent behavior around the operation point, denoted as Q. For this pMOS implementation, the resistance is given by

$$r_{SCM} = \left.\frac{\partial\left(V_{DD} - V_X\right)}{\partial I_{REF}}\right|_Q = \frac{1}{I_{REF} S_{I_{REF}}}. \tag{3.16}$$

Relying on the small signal schematic in Fig. 3.9(b) and first considering the case without transistor M_{6C}, i.e., $v_y = v_{bn}$, the absolute LS of V_X and the relative LS of I_{REF} around Q can be expressed as

$$\left.\frac{\partial\left(V_{DD} - V_X\right)}{\partial V_{DD}}\right|_Q = \frac{v_{dd} - v_x}{v_{dd}} = \frac{\frac{g_{d5}}{f} + g_{d6}}{g_{m6}}, \tag{3.17}$$

$$\left.\frac{1}{I_{REF}}\,\frac{\partial I_{REF}}{\partial V_{DD}}\right|_Q = \frac{1}{I_{REF}}\frac{i_{ref}}{v_{dd}} = S_{I_{REF}}\frac{v_{dd} - v_x}{v_{dd}}, \tag{3.18}$$

under the common assumption that $g_m \gg g_d = 1/r_o$. Equation (3.17) indicates that the dependence of $v_{dd} - v_x$ to v_{dd} can be attributed to M_{5-6}'s output conductance. Next, M_{6C} in Fig. 3.9(a) is used to cascode M_6, and is biased by voltage V_{G8} originating from the body / back-gate bias generator [Fig. 3.5]. A complete low-voltage cascode as depicted in Fig. 3.13(b) can also be used, but does not bring any significant LS improvement as M_7 is in diode and already has negligible V_{DS} variations. Based on Fig. 3.9(b) and assuming that $v_{g8} \simeq v_x$, the absolute LS of V_X becomes

$$\frac{v_{dd} - v_x}{v_{dd}} = \frac{\frac{g_{d5}}{f}}{g_{m6} + \left(\frac{g_{d6}}{g_{m6c}}\right) r_{SCM}} \simeq \frac{\frac{g_{d5}}{f}}{g_{m6}}, \tag{3.19}$$

while the relative LS of I_{REF} is still given by (3.18). LS is reduced because g_{d6} no longer appears in (3.19), which is highly beneficial as M_6 is in weak inversion while M_5 is closer to moderate inversion, meaning that M_6 is shorter than M_5 and there-

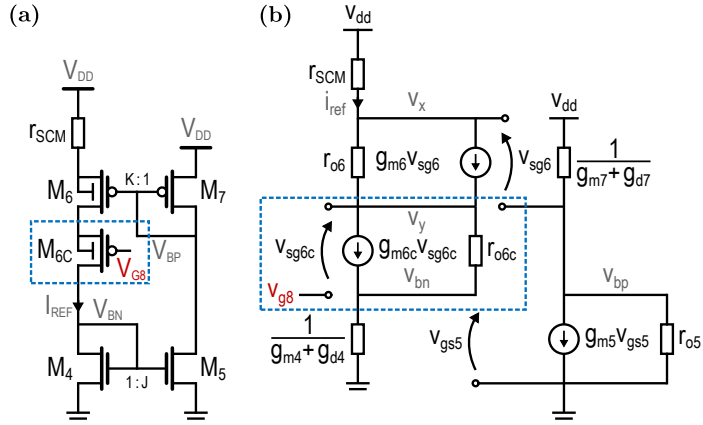

Fig. 3.9 (a) Schematic of the β-multiplier with low-voltage cascoding of M_6 through transistor M_{6C}. (b) Small signal schematic of (a).

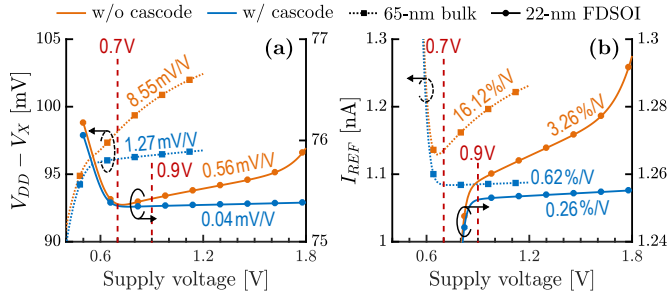

Fig. 3.10 Pre-layout simulations of (a) $V_{DD} - V_X$ and (b) I_{REF} with respect to the supply voltage in the TT 25°C corner, highlighting the improvement of LS achieved by cascoding M_6 in both 65- and 22-nm technologies. The minimum supply voltage is 0.7 V in 65 nm and 0.9 V in 22 nm.

fore has a larger output conductance. In addition, current mirrors are implemented using composite transistors, i.e., the series connection of devices sharing the same V_G and V_B [159], further reducing the output conductance.

In 65 nm, simulations without cascoding exhibit an LS of V_X and I_{REF} [Fig. 3.10] respectively worth 8.55 mV/V and 16.12 %/V, computed from 0.7 to 1.2 V using the **box method**. Based on the small signal parameters extracted at the center of the supply voltage range, i.e., 0.95 V, (3.17) predicts an LS of V_X of 7.81 mV/V which compares fairly well to the 8.25-mV/V simulated value, computed with **first-order finite differences** around Q rather than with the box method. Equation (3.18) links the LS of I_{REF} to $v_{dd} - v_x/v_{dd}$, and yields a 21.33-%/V value diverging from the 15.75-%/V simulation, likely due to an overestimation of $S_{I_{REF}}$. With cascoding, the LS of V_X and I_{REF} improve to 1.27 mV/V and 0.62 %/V. Besides, the 0.90-mV/V LS of V_X prediction agrees with the 1.25-mV/V simulation. Similarly to the non-

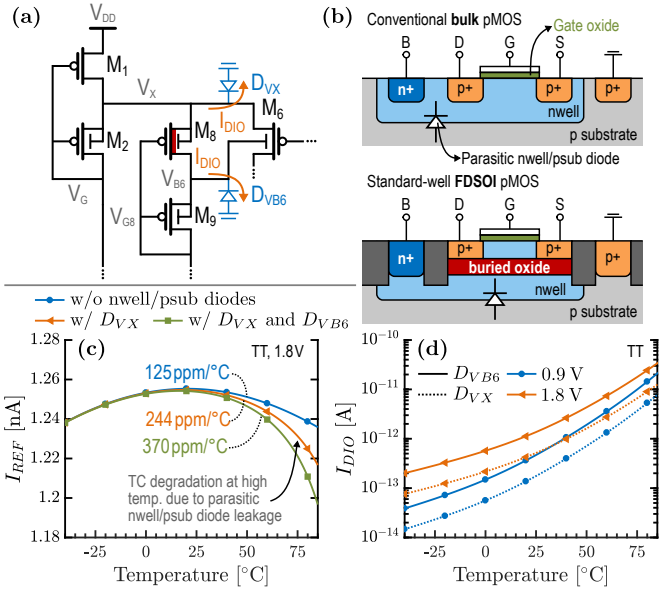

Fig. 3.11 I_{REF} TC is degraded by the leakage of parasitic nwell/psub diodes. (a) Schematic of the SCM and body / back-gate bias generator with parasitic diodes. (b) Cross-section of pMOS devices in conventional bulk and standard-well FD-SOI technologies. (c) Temperature dependence of I_{REF} in TT 1.8 V, based on pre- and post-layout simulations in 22 nm. (d) Diode leakage as a function of temperature in 22 nm, for reverse voltages of 0.9 and 1.8 V.

cascoded case, the 2.46-%/V prediction for the LS of I_{REF} is exaggerated compared to the 0.83-%/V simulation.

Simulations without cascoding in 22 nm yield a 0.56-mV/V LS of V_X and a 3.26-%/V LS of I_{REF} from 0.9 to 1.8 V. The small signal approach estimates an LS of V_X worth 0.35 mV/V around 1.35 V, which compares fairly well to the 0.33-mV/V simulated value. A 1.96-%/V LS of I_{REF} is predicted by (3.18) and closely matches the 1.89-%/V simulation, thus confirming the correct evaluation of $S_{I_{REF}} = 5.85\,\%/\mathrm{mV}$. Cascoding reduces LS to 0.04 mV/V and 0.26 %/V for V_X and I_{REF}. Moreover, predictions give a 0.04-mV/V LS of V_X which agrees with the 0.038-mV/V simulation, while the LS of I_{REF} is accurately predicted to be 0.22 %/V, which is close to the 0.23-%/V simulation as for the case without cascoding.

To conclude, cascoding decisively diminishes I_{REF} LS by a factor 26× in 65 nm (resp. 12.5× in 22 nm) and comes for free in the proposed reference as V_{G8} is readily available from the body / back-gate bias generator.

3.1.3.2 *Parasitic Diode Leakage Mitigation*

In the case of a pMOS-based SCM [Fig. 3.11(a)] and at high temperature, I_{REF} TC is degraded by leakage currents flowing from V_X and V_{B6} to ground through parasitic nwell/psub diodes. The origin of these diodes is illustrated by the cross-

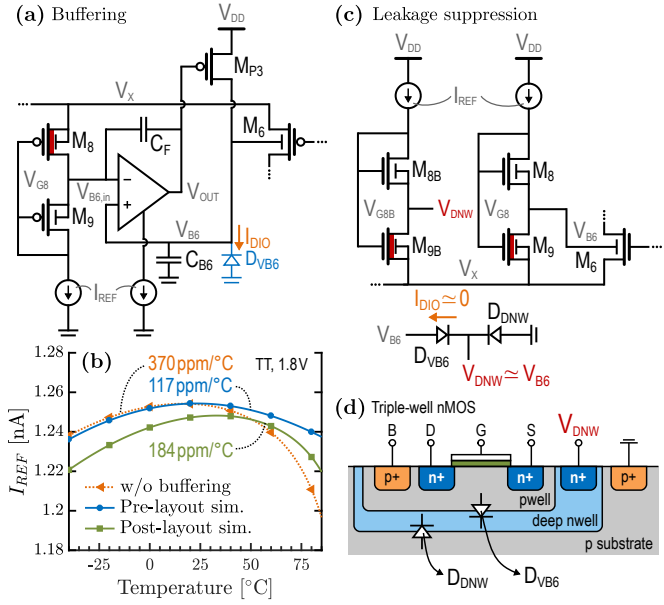

Fig. 3.12 Schematic of the body / back-gate bias generator (a) with a buffering stage implemented as an LDO, or (c) with a leakage suppression mechanism, obtained by implementing M_6 with a triple-well nMOS device whose deep nwell is biased by a body bias generator replica. (b) Temperature dependence of I_{REF} in pre- and post-layout simulations, with a fine-tuning of the SCM sizes in TT 1.8 V. (d) Cross-section of triple-well nMOS devices.

section of pMOS devices in Fig. 3.11(b). This issue does not occur in 65 nm due to the lower reverse voltage applied to the diodes and the limited nwell area required by M_{6-6C-9}, as smaller devices can be used because of the low $S_{I_{REF}}$. Therefore, we only discuss the 22-nm design in what follows. Next, Fig. 3.11(c) shows that in 22 nm, the pre-layout simulation in TT 1.8 V features a 125-ppm/°C TC, while post-layout simulations with either diode D_{VX} or both diodes D_{VX} and D_{VB6} result in a degraded I_{REF} TC of 244 and 370 ppm/°C, respectively. This degradation arises from the exponential increase of diode leakage with temperature [Fig. 3.11(d)], causing a deviation from the pre-layout behavior above 50°C. D_{VB6}'s leakage attains 21 to 33.8 pA at 85°C and mostly has an indirect impact on I_{REF} by inducing a change in V_{B6}, passed on I_{REF} through ΔV_T. Furthermore, D_{VX}'s leakage at 85°C lies between 7.8 and 12.5 pA and has a direct impact on I_{REF} by drawing some current away from the SCM and β-multiplier. However, it should be noted that this impact can be alleviated by connecting the body of M_2 to V_{DD} while accounting for this change in the sizing of the SCM.

In Fig. 3.12, two solutions are proposed to combat the adverse effect of parasitic diode leakage. First, a low-dropout (LDO) regulator copes with D_{VB6}'s leakage by buffering node $V_{B6,\text{in}}$ [Fig. 3.12(a)]. It consists of four main components: (i)

a self-biased 4T operational transconductance amplifier (OTA) with an nMOS differential pair, (ii) a regulation pMOS M_{P3} delivering the leakage current of D_{VB6}, (iii) a capacitor C_{B6} ensuring the stability of the LDO, and (iv) a Miller capacitor C_F ensuring the stability of the whole reference by adding a dominant pole $f_{pd} = (g_{m8} + g_{d8})/(2\pi C_F A_{v,OTA})$ at node $V_{B6,\text{in}}$, with $A_{v,OTA}$ the differential voltage gain of the OTA in DC conditions. Fig. 3.12(b) reveals that a 117-ppm/°C I_{REF} TC is obtained pre-layout with this additional buffering stage. With a fine-tuning of the SCM sizes to alleviate the impact of D_{VX}'s residual leakage, an increase of the TC to 184 ppm/°C is observed post-layout, albeit the degradation is lessened compared to the 370 ppm/°C without buffering. At last, the buffering stage entails power and area overheads corresponding to 14.3 % (0.83 nW) and 14.7 % (1940 μm^2) of the total power and area usage.

Second, in the case of an nMOS-based SCM, leakage suppression could be achieved by biasing the deep nwell with a voltage $V_{DNW} \simeq V_{B6}$. This technique is inspired from ultra-low-power voltage references [25], and forces a voltage drop close to zero across the parasitic pwell/deep-nwell diode D_{VB6} [Fig. 3.12(c)], thus suppressing the leakage from V_{B6}. Voltage V_{DNW} is easily generated by a replica of the low-power voltage reference which provides the leakage of D_{DNW}. The origin of diodes D_{VB6} and D_{DNW} is illustrated by the cross-section of triple-well devices in Fig. 3.12(d).

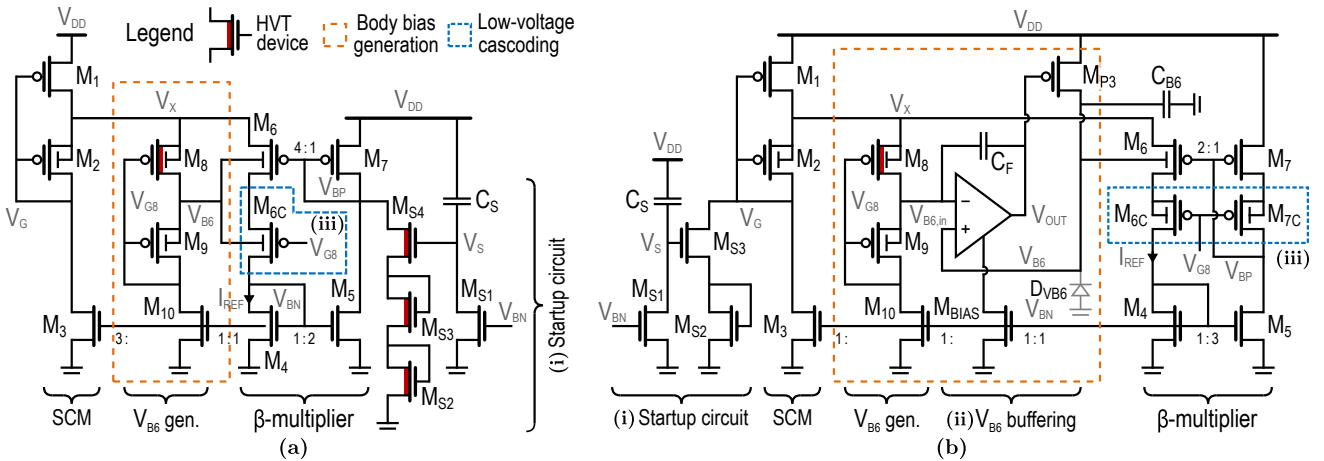

Fig. 3.13 Complete schematic of the proposed nA-range CWT reference in (a) TSMC 65-nm bulk and (b) GF 22-nm FD-SOI. The schematic includes a dynamic startup circuit similar to [28], a buffering stage of the body / back-gate voltage of M_6, and a low-voltage cascode. Note that the startup circuits are slightly different due to the presence of the buffering stage in 22 nm. In the 65-nm design, M_8 and M_{S2-S4} are implemented with core HVT pMOS devices, while in the 22-nm one, M_8 is implemented with an I/O ULL pMOS devices.

3.1.3.3 Final Implementation Performance

The complete schematic of the proposed reference is disclosed in Fig. 3.13 for the 65- and 22-nm designs, and features three additions compared to Fig. 3.5. Firstly, a dynamic startup circuit [27, 28], to make sure the reference is not stuck around its zero-I_{REF} stable operation point. For applications relying on a low-slew-rate supply voltage, a suitable startup circuit can be obtained by replacing C_S by a diode-connected pMOS or by relying on the conventional circuit in [160], at the cost of an increased power consumption. Second, a buffering stage for V_{B6} in 22 nm. Lastly, a low-voltage cascode to improve LS, which is either implemented with a single transistor in 65 nm, or in full in 22 nm. Our analysis in Section 3.1.3.1 nevertheless suggests that the 22-nm cascode could be simplified to a single transistor without loss of performance. Furthermore, a pMOS-based SCM has been selected to avoid the minor area penalty and slightly more complex body / back-gate connections entailed by the use of triple-well devices, albeit a design relying on an nMOS-based SCM is totally feasible. Then, the layout is presented in Fig. 3.14, and transistor sizes are summarized in Table 3.1, with core (resp. I/O) LVT devices used by default in 65 nm (resp. 22 nm). Most transistors present relatively small aspect ratios, as they are biased with a current in the nA range lower than their specific sheet current I_{SQ} and, for some of them, are operated in moderate inversion, thus reducing their aspect ratio even further. This effect is more pronounced in the 65-nm design because the body / back-gate bias generator produces a 28-mV ΔV_T, as opposed to 17 mV in 22 nm, which pushes M_{1-2} closer to strong inversion.

Next, we discuss the performance of the proposed reference. First, Fig. 3.15 illustrates the dependence to supply voltage, with the minimum supply voltage given by

$$\begin{aligned} V_{DD,\text{min}} = V_{DS,\text{sat}} + \max\big(&V_{SG1}, V_{SG8} + V_{SG1} - V_{SG2}, \\ &V_{GS4} + V_{SD6C,\text{sat}} + V_{SG1} - V_{SG2}, V_{SG7}\big), \end{aligned} \tag{3.20}$$

in which each expression inside the max function corresponds to one of the branches of the schematic in Fig. 3.13(a). Second, Fig. 3.16 displays the temperature dependence of V_X and I_{REF}. Third, Fig. 3.17 studies the variability of I_{REF} and its TC for 10^3 Monte-Carlo (MC) simulations. Note that I_{REF} variability can be estimated from σ_{V_X} at first order using

$$(\sigma/\mu)_{I_{REF}} = S_{I_{REF}}\sigma_{V_X}. \tag{3.21}$$

Finally, Fig. 3.18 depicts the startup waveforms in nominal and extreme corners for a 100-μs rise-time voltage source.

In 65 nm, the layout [Fig. 3.14(a)] is dominated by the SCM which occupies 23.8 % of the 0.0021-mm^2 area, followed by the current mirrors with 22.8 %. In TT, the LS of V_X is equal to 1.28 mV/V from 0.7 to 1.2 V [Fig. 3.15(a)] and yields

Table 3.1 Sizing of the proposed nA-range CWT reference.

	TSMC 65-nm bulk			GF 22-nm FD-SOI		
	W [μm]	L [μm]	i_f	W [μm]	L [μm]	i_f
M_1	0.365	20×10	52.46	2.39	20×8	5.17
M_2	0.3	20×10	22.09	2.74	16×8	1.10
M_3	3×0.35	5×10	0.69	1	5×8	0.25
M_4	0.35	5×10	0.69	1	5×8	0.25
M_5	2×0.35	5×10	0.69	3×1	5×8	0.25
M_6	4×1	10	0.03	20×5	2×8	0.003
M_7	1	10	0.03	10×5	2×8	0.003
M_{6C}	0.22	10	-	8×5	4	-
M_{7C}	-	-	-	24×5	4	-
M_8	2×2.34	4×5	-	4×5	8	-
M_9	2×0.22	4×5	-	4×4	8	-
M_{10}	0.35	5×10	0.69	1	5×8	0.25
M_{S1}	0.35	5×10	0.69	0.16	5×8	0.25
M_{S2-S4}	0.2	20	-	4	8	-
C_S	2.5	2	-	12.5	5	-

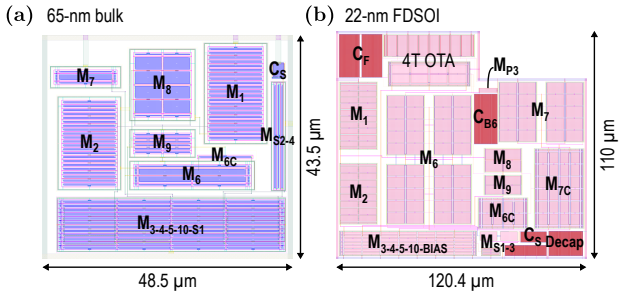

Fig. 3.14 Layout of the reference in (a) 65-nm bulk and (b) 22-nm FD-SOI.

a 0.69-%V LS of I_{REF} [Fig. 3.15(b)]. Process variations have negligible impact on the LS but change I_{REF} by +19.09 % in FF and -7.20 % in SF. Fig. 3.16(a) highlights the slightly different TC of V_X due to process variations of the subthreshold slope factor. These differences result in I_{REF} TC discrepancies, with a typical and worst-case values of 208 and 393 ppm/°C. Regarding variability, only mismatch can be simulated in 65 nm as no statistical models for global process variations are available in the process design kit (PDK) used in this work. Fig. 3.17(a) exhibits a 2.92-% (σ/μ) lower than the 3.74 % inferred from (3.21) and the 1.37-mV σ_{V_X}, concurring with the hypothesis of an $S_{I_{REF}}$ overestimation. Regarding TC, its median and 99th percentile are 213 and 431 ppm/°C [Figs. 3.17(b) and (c)]. Finally, the typical and worst-case startup times t_s are 3.4 and 29.2 ms [Fig. 3.18(a)].

In 22 nm, the layout [Fig. 3.14(b)] is dominated by M_{6-7}, which need to be large to minimize σ_{V_X} and thus account for 28.7 % of the 0.0132-mm^2 area. Then, regarding supply voltage dependence, the slender process variations impacting V_X [Fig. 3.15(c)] stem from V_{B6} through ΔV_T. However, I_{REF} is mainly impacted by I_{SQ} variations [Fig. 3.15(d)], and changes by at most +9.85 % in SF and -9.51 % in FS. From 0.9 to 1.8 V, the LS of V_X is worth 50 μV/V in TT, and translates to a

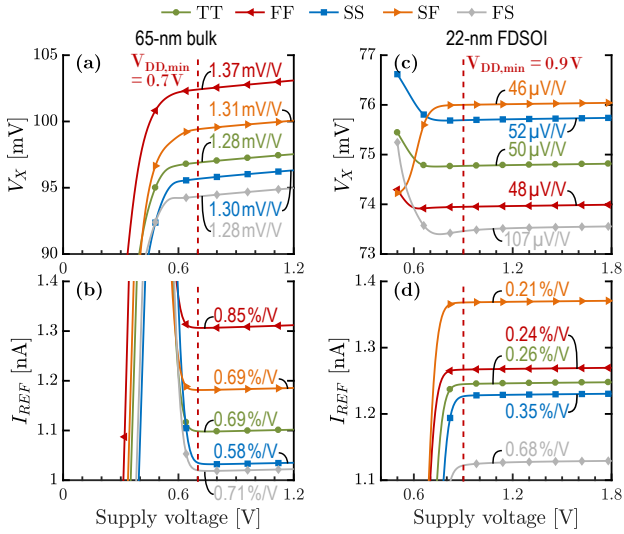

Fig. 3.15 Post-layout simulations of the supply voltage dependence of V_X and I_{REF} in all process corners and at 25°C, in 65-nm bulk [(a) and (b)] and in 22-nm FD-SOI [(c) and (d)].

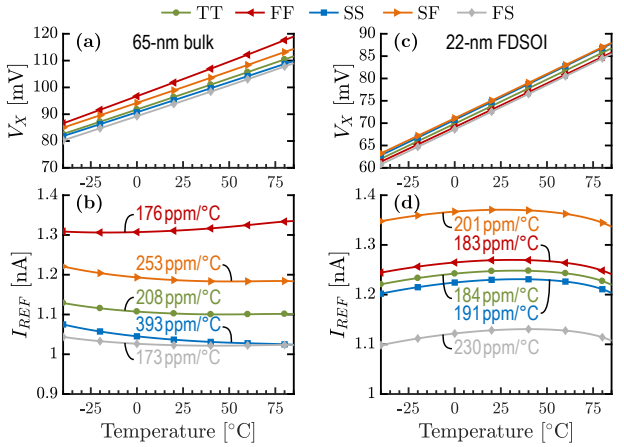

Fig. 3.16 Post-layout simulations of the temperature dependence of V_X and I_{REF} in all process corners, at 1.2 V in 65-nm bulk [(a) and (b)] and at 1.8 V in 22-nm FD-SOI [(c) and (d)].

0.26-%/V LS of I_{REF}. Furthermore, LS is relatively constant across process corners except in FS, for which the 0.68-%/V value can be explained by the distortion close to 0.9 V. It requires a higher V_{DD} to cope with the increased pMOS V_T. Then, V_X has the same TC across process corners [Fig. 3.16(c)], leading to similar I_{REF} TCs in Fig. 3.16(d). The typical and worst-case TCs are 184 and 230 ppm/°C, the latter being partially explained by the lower I_{REF} value in this process corner, as I_{REF} TC is a relative metric. As far as variability is concerned, in 22 nm, we can sim-

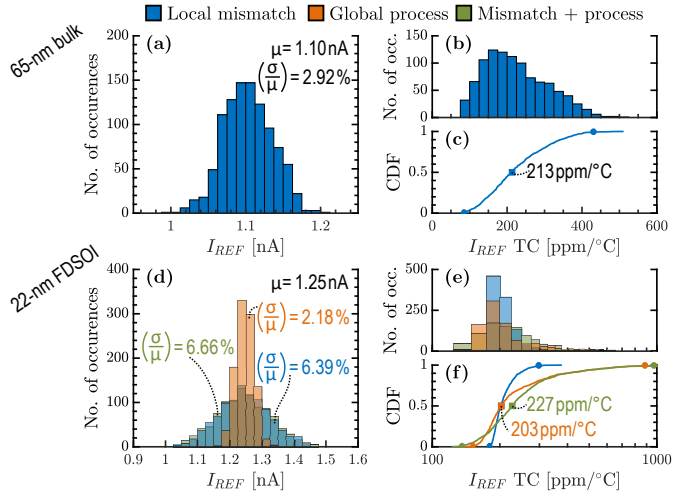

Fig. 3.17 For 10^3 post-layout MC simulations in TT, histograms of I_{REF} at 25°C, and I_{REF} TC from -40 to 85°C, at 1.2 V in 65-nm bulk [(a) to (c)] and 1.8 V in 22-nm FD-SOI [(d) to (f)]. (d) to (f) correspond to simulations of local mismatch, global process variations, and their combined effects.

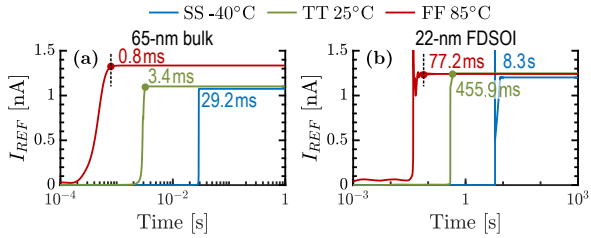

Fig. 3.18 Post-layout startup waveforms in the fastest (FF 85°C), typical (TT 25°C), and slowest (SS -40°C) corners, (a) at 1.2 V in 65-nm bulk and (b) 1.8 V in 22-nm FD-SOI in the three process and temperature corners, using a voltage source with a rise time of 100 μs.

ulate the impact of mismatch, process variations, and their combined effects. On the one hand, mismatch has a strong impact on I_{REF} (σ/μ) due to the large $S_{I_{REF}}$. The simulated 0.87-mV σ_{V_X} leads to a 4.92-% (σ/μ) prediction, which falls short of the 6.39-% simulation [Fig. 3.17(d)] due to additional mismatch in the SCM and the mirrors. Besides, TC variability is relatively limited, with a 203- and 299-ppm/°C median and 99$^{\text{th}}$ percentile [Figs. 3.17(e) and (f)]. On the other hand, process variations have a restricted impact on I_{REF}, with a 2.18-% (σ/μ), but deteriorate I_{REF} TC, with a 99$^{\text{th}}$ percentile shifted to 887 ppm/°C due to a malfunction of the buffer for extreme process realizations causing I_{REF} to drop at high temperature. Unsurprisingly, the combined effects yield a 6.66-% (σ/μ) for I_{REF}, together with a 227- and 972-ppm/°C median and 99$^{\text{th}}$ percentile for I_{REF} TC. Lastly, the typical and worst-case t_s are 456 ms and 8.3 s [Fig. 3.18(b)], because of the parasitic caps of

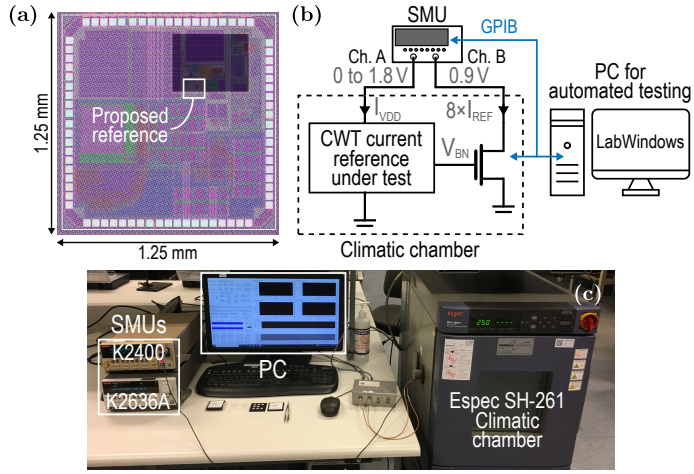

Fig. 3.19 (a) Chip microphotograph in GF 22-nm FD-SOI, with the proposed reference highlighted in white. (b) Conceptual and (c) actual measurement testbench for supply voltage and temperature dependence characterization.

large transistors. While the worst-case 8.3-s t_s could be critical, most applications require the reference to operate down to -40°C but not to start in the extreme SS -40°C corner, as nA-range current references are often always-on circuits. Nevertheless, this issue can be solved by widening M_{S2-S3} in Fig. 3.13(b), at the expense of a TC degradation in FF 85°C.

3.1.4 Measurement Results

In this section, we describe the testbench used to characterize the proposed current reference, fabricated in GF 22-nm FD-SOI as part of a 1.56-mm^2 microcontroller unit for biomedical applications codenamed ICare [Fig. 3.19(a)]. Then, we present the LS and TC measurements across the 20 dies in Figs. 3.20 and 3.21, before discussing the discrepancies with respect to post-layout simulations based on Figs. 3.22 and 3.23.

3.1.4.1 Measurement Testbench

Conceptual and actual views of the testbench are shown in Figs. 3.19(b) and (c). Supply voltage dependence is characterized using a two-channel Keithley K2636A source measurement unit (SMU), providing the supply voltage to the reference on channel A, and a 0.9-V V_{DS} to the output nMOS transistor on channel B. The supply current I_{VDD} and the output current, equal to $8 \times I_{REF}$, are measured by the K2636A, while a K2400 supplies the I/O voltage [Fig. 3.19(c)]. Supply voltage is then swept from 0 to 1.8 V in 25-mV steps. Then, temperature dependence is characterized using an Espec SH-261 climatic chamber which sweeps temperature from

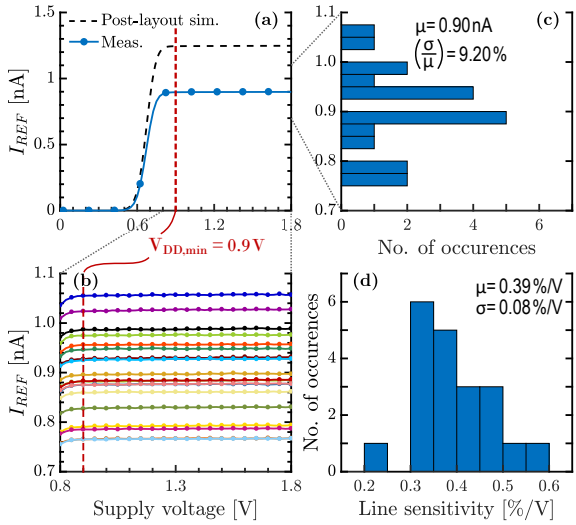

Fig. 3.20 (a) Post-layout-simulated and measured average I_{REF}, with (b) details of the 20 dies. Measured histograms of (c) I_{REF} at 1.8 V and (d) LS from 0.9 to 1.8 V. All figures are obtained at a temperature of 25°C.

-40 to 85°C in 5°C steps. Both equipments are connected in GPIB to a PC running a testing routine in LabWindows. Lastly, LS and TC are computed across the 20 dies according to (1.2) and (1.4).

3.1.4.2 *Supply Voltage and Temperature Dependence*

Firstly, Fig. 3.20 quantifies the LS and variability of I_{REF} obtained in measurement at 25°C. Fig. 3.20(a) describes the supply voltage dependence of I_{REF} for post-layout simulations in TT and for the measurements average. The measured $V_{DD,\text{min}}$ remains about 0.9 V as expected from simulation, but I_{REF} shrinks from 1.25 to 0.9 nA. This difference cannot be explained by the mismatch of the mirror between I_{REF} and the output current, as the current ratio has a limited 1.5-% (σ/μ) evaluated from 10^3 MC simulations. As hypothesized in [155] and confirmed in this work, this reduction is linked to global process variations and more specifically to skewed process corners of the ULL and LVT I/O devices M_8 and M_9 constituting the body / back-gate generator, as illustrated in Figs. 3.22(a) and 3.23(a). Details of the 20 dies are depicted in Fig. 3.20(b), and histograms of I_{REF} at 1.8 V and LS from 0.9 to 1.8 V are respectively presented in Figs. 3.20(c) and (d). Fig. 3.20(c) features a 9.20-% (σ/μ) larger than the 6.66-% value obtained in Section 3.1.3.3, which takes both mismatch and statistical process variations into account. Assuming the mean has been perfectly estimated, the 99-% confidence interval (CI) for the variance gives a CI for (σ/μ) equal to [7.3 %; 15.3 %], meaning that the limited sample size cannot explain the (σ/μ) discrepancy. The lower I_{REF} and higher (σ/μ) are rather explained by a CWT offset ΔV_T lower than its nominal value [Figs. 3.22(a) and (c)],

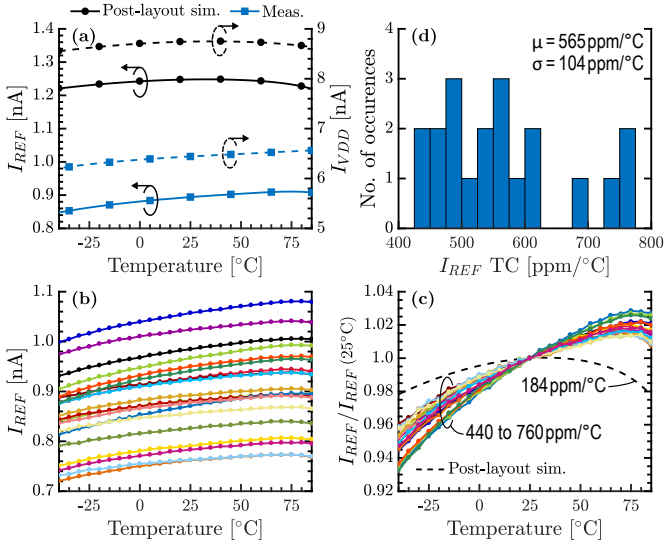

Fig. 3.21 (a) Post-layout-simulated and measured temperature dependence of the average I_{REF} and I_{VDD}. Measured temperature dependence of I_{REF} (b) without and (c) with normalization by the value at 25°C, for the 20 dies. (d) Measured histogram of I_{REF} TC from -40 to 85°C. All figures are obtained for a supply voltage of 1.8 V.

the larger variability being linked to an increased sensitivity $S_{I_{REF}}$ as M_{1-2}'s inversion level is reduced. Finally, Fig. 3.20(d) reveals that the measured LS is around 0.39 %/V, which is close to the 0.26 %/V obtained in post-layout simulation.

Furthermore, Fig. 3.21 gauges the temperature dependence of I_{VDD} and I_{REF} at 1.8 V. Fig. 3.21(a) highlights the second order behavior of I_{REF} in simulation and measurement, as well as a slighly PTAT trend observed in measurement only. I_{VDD} amounts to 8.8 nA in simulation (resp. 6.4 nA in measurement), leading to a 7.8-nW (resp. 5.8-nW) power consumption at 0.9 V. Details of the 20 dies are portrayed in absolute value in Fig. 3.21(b), and normalized by the value of I_{REF} at 25°C in Fig. 3.21(c). The measured TC is comprised between 440 and 760 ppm/°C, with an average of 565 ppm/°C [Fig. 3.21(d)]. Skewed process variations of ULL and LVT I/O devices reliably explain the TC deterioration, as a decreased (resp. increased) ΔV_T compared to its nominal value results in a slightly PTAT (resp. CTAT) behavior [Figs. 3.22(b) and (c)]. Besides, Fig. 3.23 depicts the process corners showing the closest agreement with the measurements in terms of I_{REF} and TC, with TCs of 446 and 557 ppm/°C observed in the (TT, SF, typ.) and (FS, TT, typ.) process corners, respectively [Fig. 3.23(a)]. These results much better coincide with the measured 565-ppm/°C TC than the nominal corner [Fig. 3.23(b)]. Finally, Fig. 3.23 suggests that the measurements are better explained by a minimum process for the parasitic nwell/psub diode D_{VX} than by a typical process.

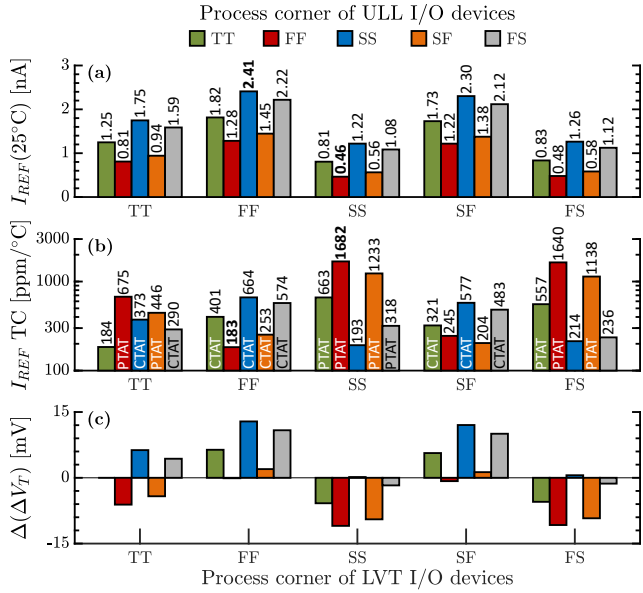

Fig. 3.22 Skewed process corners of ULL and LVT I/O devices have an impact on (a) I_{REF} at 25°C and (b) I_{REF} TC from -40 to 85°C, due to (c) changes in the CWT offset ΔV_T with respect to its nominal value. All results are obtained for a supply voltage of 1.8 V and a typical process for parasitic nwell/psub diodes.

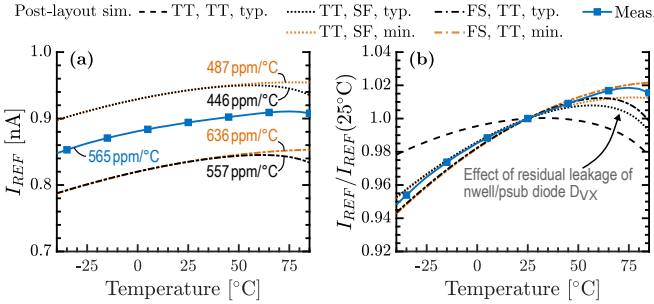

Fig. 3.23 Post-layout-simulated and measured temperature dependence of I_{REF} at 1.8 V (a) without and (b) with normalization by the value at 25°C. Post-layout simulations correspond to skewed process corners for LVT I/O devices, ULL I/O devices, and parasitic nwell/psub diodes.

Table 3.2 Comparison table of temperature-independent nA-range current references.

	Huang [66]	Far [96]	Kim [64]	Cordova [89]	Santamaria [99]	Aminzadeh [133]	Kayahan [94]	Dong [93]	Ji [39]	Wang [67]	Wang [40]	Huang [41]	Lee [144]	**Lefebvre This work**		
Publication	ISCAS	ROPEC	ISCAS	ISCAS	ISCAS	AEU	TCAS-I	ESSCIRC	ISSCC	VLSI-DAT	TCAS-I	TCAS-II	JSSC	JSSC		
Year	2010	2015	2016	2017	2019	2022	2013	2017	2017	2019	2019	2020	2020	2022		
Type of work	**Simulations**						**Silicon measurements**							**Sim.**	**Sim.**	**Meas.**
Number of samples	N/A	N/A	N/A	N/A	N/A	N/A	90	32*	10	10	16	10	10	N/A	N/A	20
Technology	0.18μm	0.18μm	0.13μm	0.18μm	0.18μm	0.18μm	0.35μm	0.18μm	0.18μm	0.18μm	0.18μm	0.18μm	0.18μm	65nm	22nm FD-SOI	
I_{REF} [nA]	2.05	14	27	10.86	2.66	6.7	25	35.02	6.64	6.46	9.77	11.6	1	1.10	1.25	0.9
Power [nW]	5.1 @0.85V	150 @1V	N/A	30.5 @0.9V	26 @2V	51 @1.1V	28500 @5V	1.02 @1.5V	9.3 @N/A	15.8 @0.85V	28 @0.7V	48.64 @0.8V	4.5/14▷ @1.5V	5.41 @0.7V	7.84 @0.9V	5.81
Area [mm^2]	N/A	**0.0102**	N/A	**0.01**	**0.0093**	**0.46**	**0.0053**	0.0169	**0.055**	**0.062**	**0.055**	**0.054**	**0.332**	**0.0021**	**0.0132**	
Supply range [V]	0.85 – 2.2	1 – 3.3	1.2	0.9 – 1.8	2 – 3.3◇	1.1 – 1.8	5	1.5 – 2.5	1.3 – 1.8	0.85 – 2	0.7 – 1.2	0.8 – 2	1.5 – 2	0.7 – 1.2	0.9 – 1.8	
LS [%/V]	1.35	**0.1**	N/A	**0.54**	**11**◇	**0.03**	**150**	3	1.16	4.15	**0.6**	1.08	1.4	**0.69**	**0.26**	**0.39**◁
Temperature range [°C]	0 – 150	0 – 70	-30 – 150	-20 – 120	-40 – 125	-40 – 120	0 – 80	-40 – 120	0 – 110	-10 – 100	-40 – 125	-40 – 120	-20 – 80	-40 – 85	-40 – 85	
TC [ppm/°C]	**91**	**20**	327	**108**	**182**	**40.33**	**128**/250*	282	680/283‡	**138**‡	**149.8**	**169**	289/265▷	**213**	**203**	565◁
I_{REF} var. (process) [%]	7.5	N/A	3.7	15.8/11.6‡	N/A	N/A	8/1.22*	4.7	N/A	N/A	+11.7/-8.7◇	+17.6/-10.3◇	N/A	+19.1/-7.2	+9.9/-9.5	N/A
I_{REF} var. (mismatch) [%]	N/A	**5.8**	N/A	N/A	**20.30**	**0.70**	**1.4** (sim.)	**1.6**	4.07/**1.19***	3.33	**1.6**	4.3	**1.26**/**0.25**‡	2.92	**6.39**	**9.20**
Trimming	No	No	No	Yes (6b)	No	No	No	No	Yes	No	Yes (5b)	Yes (6b)	Yes (27b)	No	No	No
Special components	No	No	Res.	Native	No	Res., **BJT**	No	Res., **BJT**	No	Res.	Res.,	Res.	No	No	No	No

* 16 dies for the TT process corner and 4 dies for each of the FF, SS, SF and FS process corners. * Simulated and measured values. ‡ Before and after trimming.
‡ Best TC, the average one is not reported. ◇ Estimated from figures. ◁ Mean measured value across the 20 dies. ▷ For 25 and 2.5 minutes between two calibrations.

3.1.5 Comparison to the State of the Art

This section compares our work to the state of the art of current references through some important trade-offs, illustrated in Fig. 3.24, and focuses on nA-range CWT references in Table 3.2. We report post-layout simulation results in 65-nm bulk and 22-nm FD-SOI, and measurement results in 22-nm FD-SOI, coresponding to the three orange markers in Fig. 3.24. Firstly, the 65-nm design surpasses all references in Table 3.2, simulated or fabricated, with a 0.0021-mm^2 area, and offers a 25$\times$ reduction compared to prior art of fabricated references. Then, the 0.0132-mm^2 silicon area in 22 nm outperforms all other fabricated references in Table 3.2 by at least a factor 4$\times$, except for [94] whose 28.5-μW power consumption is prohibitive in most applications. Fig. 3.24(a) further demonstrates that the proposed references are almost unchallenged in terms of silicon area among nA-range CWT references, and lie beyond the trade-off of conventional references. Only [99] is competitive in terms of silicon area with a 0.0093-mm^2 design, as it relies on diode-connected and zero-V_{GS} transistors as voltage-to-current converter. However, it suffers from a strong degradation of other FoMs with a 2-V $V_{DD,\text{min}}$, an 11-%/V LS and a 20.3-% (σ/μ). The low area overhead of the proposed reference is linked to the fact that it relies solely on transistors, contrary to other references which include area-hungry resistors. Besides, the implementation in advanced technology nodes further helps reducing the absolute area overhead. They reach the lowest reference current among CWT references at the exception of gate-leakage-based ones, which could be modified to reach a nA-range current but only at the cost of a 10^2-to-$10^3\times$ larger area.

In Table 3.2, power consumption and minimum supply voltage are on par with the state of the art, while LS is among the best for nA-range references with a sub-1-%/V value obtained by low-voltage cascoding for both implementations, and backed by a large intrinsic gain g_m/g_d in FD-SOI [37]. Next, in terms of TC, the 213- and 203-ppm/°C simulated values obtained for the proposed 65- and 22-nm designs are faintly larger than the TC of other fabricated references [Table 3.2 and Fig. 3.24(b)]. However, the design proposed in [40, 66] relies on a temperature exponent of carrier mobility close to two and cannot be ported to most technologies, whereas [40, 41, 39] are area-hungry due to the use of resistors and/or OTAs, and [144] due to the use of a current DAC and a low-TC reference. The TC degradation of the proposed 22-nm design to 565 ppm/°C in measurement calls for a TC calibration mechanism, extensively used by fabricated references in Table 3.2 [40, 41, 39, 144], to retrieve quasi simulation-level performance. Possible implementations could for example tune the current ratio between M_5 and M_4 using a binary-weighted mirror [41] to change K_{PTAT}, or the number of transistors connected in series to implement M_1 [30] to change α. In Fig. 3.24(c), the proposed references fare quite well against prior art but can simply not compete against gate-leakage-based (resp. resistor-based) references in the pA (resp. μA) range. Finally,

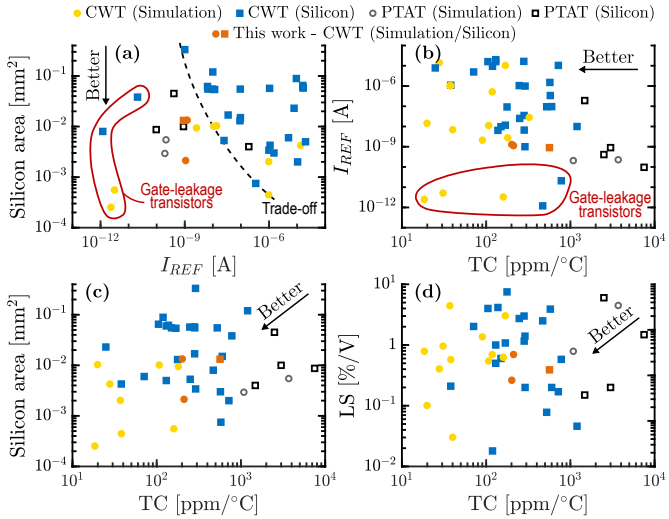

Fig. 3.24 Trade-offs between (a) area and I_{REF}, (b) I_{REF} and TC, (c) area and TC, and (d) LS and TC, based on the state of the art of current references.

Fig. 3.24(d) demonstrates that the proposed designs are competitive with most existing references in terms of LS and TC. The main drawback of the proposed 22-nm design is its large sensitivity to mismatch and process variations, with a 9.20-% (σ/μ) due to a large $S_{I_{REF}}$, which could be improved by increasing the sizes of M_{6-7}, or by increasing ΔV_T as it is done in the 65-nm design, whose simulated variability scales down to 2.92 %.

3.1.6 Conclusion

In this first part of Chapter 3, we demonstrated a CWT current reference operating in the nA range. It relies on an SCM biased by a PTAT voltage with a CWT offset voltage, which stems from the V_T difference between transistors of the same V_T type, one of them being forward body-biased, through its body in bulk or back-gate in FD-SOI. Then, we presented a comprehensive methodology for sizing the proposed reference based on the ACM model and validated it through post-layout simulations in 65-nm bulk and 22-nm FD-SOI. The 65-nm reference produces a 1.1-nA current with an LS of 0.69 %/V and a TC of 213 ppm/°C, and power and area overheads of 5.4 nW and 0.0021 mm^2. Lastly, the 22-nm FD-SOI design was fabricated and generates a 0.9-nA current with a 0.39-%/V LS and a 565-ppm/°C TC, while consuming 5.8 nW and occupying a silicon area of 0.0132 mm^2. The TC degradation from simulation to measurement, together with the large 9.20-% variability due to mismatch and process variations, ask for a TC calibration scheme to be explored in further work.

3.2 A Resistor-Based Peaking Current Reference

This second part of Chapter 3 proposes a nA-range CWT peaking current reference (PCR), in which the threshold voltage difference between two subthreshold transistors of the same V_T type, denoted as ΔV_T, biases a resistor. This ΔV_T results from the forward body biasing (FBB) of one of the transistors by a two-transistor (2T) ULP voltage reference, leading to a reduced bias voltage and thus, to a reduced resistance and area. The proposed design includes a leakage suppression circuit to mitigate the impact of parasitic diodes at high temperature, as well as trimming mechanisms for the reference current and its TC to maintain performance across process corners. As the proposed reference relies on the body effect, it has been validated with post-layout simulations in a 0.11-μm bulk and a 22-nm fully-depleted silicon-on-insulator (FD-SOI) to demonstrate feasibility in these two technology types. In addition, the proposed reference has been fabricated in 22-nm FD-SOI, yielding a 1.5-nA current with an 89-ppm/°C TC and a 0.51-%/V line sensitivity (LS), while consuming 2.87 nW at 0.75 V and occupying a record silicon area of 0.00214 mm^2. This section is organized as follows. First, Section 3.2.1 presents the operation principle of the proposed reference and discusses its sizing. Section 3.2.2 details architectural optimizations, while Sections 3.2.3 and 3.2.4 respectively present simulation and measurement results. Finally, Section 3.2.5 compares this work to the state of the art, while Section 3.2.6 offers perspectives for future works.

3.2.1 Operation Principle and Sizing

The main objective of this section is to respectively remind the operation principle of the conventional proportional-to-absolute-temperature (PTAT) PCR, and explain the one of the proposed CWT PCR, based on their governing equations in Sections 3.2.1.1 and 3.2.1.2. Then, Section 3.2.1.3 discusses the design and sizing methodology of the proposed CWT PCR in 0.11-μm bulk and 22-nm FD-SOI technologies.

Before getting into the heart of the governing equations, we need to remind two important concepts. First, the equations of a transistor in subthreshold are reminded in Appendix A.1. The second important concept to be introduced is the body effect, which is captured by

$$\Delta V_T = V_T - V_{T0} = \gamma_b \left(\sqrt{2\phi_{fp} - V_{BS}} - \sqrt{2\phi_{fp}} \right) \approx -\gamma_b^* V_{BS} \tag{3.22}$$

in a bulk technology, where γ_b is the body factor, γ_b^* its linearization around $V_{BS} = 0$, and ϕ_{fp} Fermi's potential. Note that in bulk, γ_b and γ_b^* are temperature-dependent.

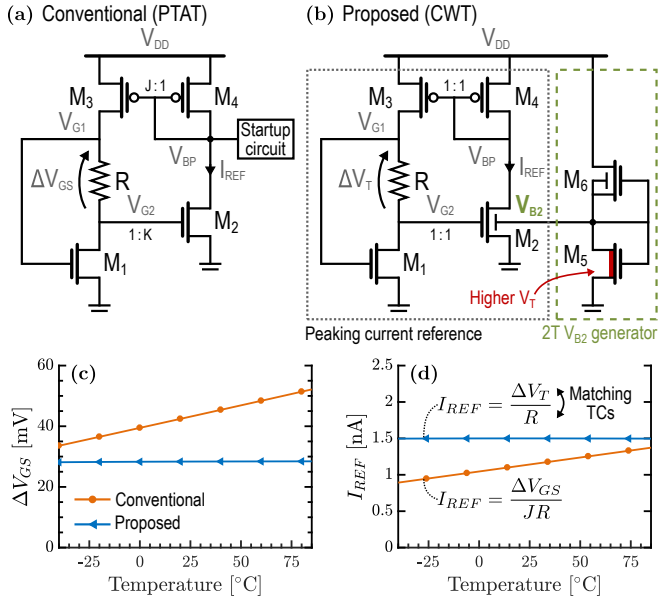

Fig. 3.25 Schematic of (a) the conventional PTAT peaking current reference and (b) the simplified proposed CWT one, which relies on the threshold voltage difference ΔV_T between M_{1-2}, obtained by forward body biasing M_2 with a 2T voltage reference (M_{5-6}). The term *peaking* comes from the fact that the relationship between the currents of M_{1-2} forming a Nagata current source, i.e., $I_{DS2} = f(I_{DS1})$, presents a peak. Operation principle illustrated with pre-layout simulations of (c) ΔV_{GS} and (d) I_{REF} in 22-nm FD-SOI, for the conventional design with $J = K = 2$, and the proposed one.

In an FD-SOI technology, the body effect can be modeled as

$$\Delta V_T = V_T - V_{T0} = -\gamma_b^* V_{BS} \tag{3.23}$$

where γ_b^* is CWT at first order [158].

3.2.1.1 *Conventional PTAT Peaking Current Reference*

In the conventional PTAT architecture [Fig. 3.25(a)], we consider that M_{1-2} have the same technological parameters and do not use any kind of body biasing, i.e., $V_{T01} = V_{T02} = V_T$ and $n_1 = n_2 = n$, excluding mismatch. In addition, the current mirror ratios J and/or K need to be larger than one, to have a positive voltage drop across resistor R. This results in

$$\Delta V_{GS} = V_{GS1} - V_{GS2} = nU_T \log(JK), \tag{3.24}$$

and

$$I_{REF} = \frac{\Delta V_{GS}}{JR} = \frac{nU_T \log(JK)}{JR}. \tag{3.25}$$

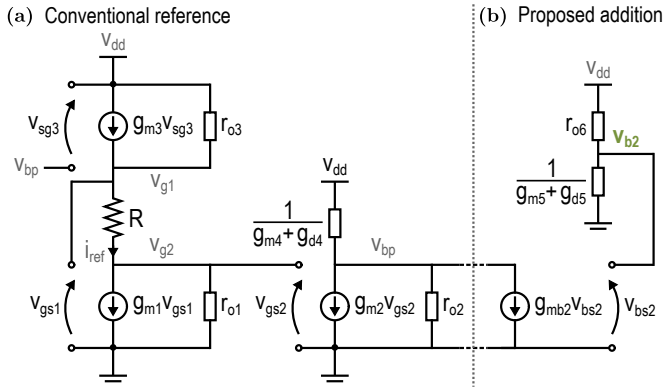

Fig. 3.26 Small-signal schematic of (a) the conventional PTAT PCR and (b) the proposed FBB addition to obtain a CWT reference current.

The TC of I_{REF} at a given temperature can be computed as

$$\mathrm{TC} = \frac{1}{I_{REF}}\frac{dI_{REF}}{dT} = -\frac{1}{R}\frac{dR}{dT} + \frac{1}{T}. \tag{3.26}$$

Eq. (3.26) shows that the TC of I_{REF} cannot be equal to zero unless the temperature coefficient of resistance (TCR) is equal to $1/T$. But in practice, the TCR is always smaller than $1/T$ and the TC of I_{REF} is thus positive. In Figs. 3.25(c) and (d), we observe that the PTAT behavior of ΔV_{GS} results in a PTAT behavior of I_{REF}, which is consistent with the positive TC.

Another quantity of interest is the LS of I_{REF}, which can be computed from a small-signal analysis of the PCR. Based on the small-signal schematic in Fig. 3.26(a), we find that

$$v_{bp} = \frac{(g_{m4}+g_{d4})v_{dd} - g_{m2}v_{g2}}{g_{m4}+g_{d4}+g_{d2}} \approx v_{dd} - \left(\frac{g_{m2}}{g_{m4}}\right)v_{g2} \tag{3.27}$$

with the simplification $g_m \gg g_d$, and we can thus compute the LS of I_{REF} as

$$\frac{i_{ref}}{v_{dd}} = \frac{1}{R}\,\frac{g_{d3}}{\left(g_{m2} + \left(\frac{g_{d1}+g_{d3}}{g_{m1}}\right)\frac{1}{R}\right)} \approx \frac{1}{R}\,\frac{g_{d3}}{g_{m2}}, \tag{3.28}$$

to be evaluated around the operation point of the current reference. Interestingly, the LS can be related to the inverse of resistance R and of the intrinsic gain (g_m/g_d).

3.2.1.2 *Proposed CWT Peaking Current Reference*

In the proposed CWT PCR [Fig. 3.25(b)], M_1 has its body connected to its source and is therefore not impacted by the body effect, hence $V_{T1} = V_{T01}$, while M_2 is biased with $V_{BS2} > 0$ and undergoes a forward body biasing lowering its thresh-

old voltage, i.e., $V_{T2} < V_{T1}$. In addition, unitary current mirror ratios $J = K = 1$ are used. In this architecture, the body voltage of M_2 is generated by the 2T voltage reference formed by M_{5-6}, in which the equilibrium of subthreshold currents $I_{DS5} = I_{DS6}$ leads to

$$V_{B2} = \left(V_{T05} - \frac{n_5}{n_6} V_{T06}\right) + n_5 U_T \log\left(\frac{I_{SQ6} S_6}{I_{SQ5} S_5}\right) \tag{3.29}$$

using (A.1), with n the subthreshold slope factor. The voltage drop across resistor R is therefore equal to the difference of threshold voltages between M_1 and M_2

$$\Delta V_{GS} = \Delta V_T = V_{T01} - V_{T2} \approx \gamma_b^* V_{B2}, \tag{3.30}$$

and results in a reference current

$$I_{REF} = \frac{\Delta V_T}{R} = \frac{\gamma_b^* V_{B2}}{R}. \tag{3.31}$$

The TC of I_{REF} at a given temperature can be computed as

$$\mathrm{TC} = \frac{1}{I_{REF}} \frac{dI_{REF}}{dT} = -\frac{1}{R}\frac{dR}{dT} + \frac{1}{\gamma_b^*}\frac{d\gamma_b^*}{dT} + \frac{1}{V_{B2}}\frac{dV_{B2}}{dT}. \tag{3.32}$$

Contrary to (3.26), in which there is no tuning knob to set the TC of I_{REF}, the proposed architecture allows to zero out the TC by properly selecting the TC of V_{B2}, which will compensate for the temperature dependence of R and γ_b^*. V_{B2} TC can indeed be tuned by changing the ratio of aspect ratios S_6/S_5 in (3.29), which will be the basis for the TC trimming circuit later discussed in Section 3.2.2.2. In Figs. 3.25(c) and (d), we notice that a close-to-CWT ΔV_{GS} gives a CWT I_{REF}, by matching the TC of ΔV_{GS} with the TCR. Hence, the operation principle of the proposed reference is to bias the resistor with the ΔV_T between two subthreshold transistors of the same V_T type, one of them being forward body biased to create a V_T imbalance. Interestingly, no startup circuit is required as the 2T voltage reference is unstable at zero I_{REF}. Other CWT PCRs employing slightly different ideas exist in the literature, such as [82, 33], biasing the resistor with the ΔV_T between transistors of the same V_T type but different lengths, and [161], making use of an additional degeneration resistor to achieve temperature compensation. Yet, these works are either limited to simulations and/or generate a larger I_{REF}.

Similarly to the conventional PCR, the LS can be obtained from a small-signal analysis. Based on the small-signal schematic in Figs. 3.26(a) and (b), we first find

$$v_{b2} = \frac{g_{d6}}{g_{m5} + g_{d5} + g_{d6}} v_{dd} \approx \frac{g_{d6}}{g_{m5}} v_{dd}, \tag{3.33}$$

Table 3.3 Resistor properties in 0.11-μm bulk and 22-nm FD-SOI. The density is measured at 25°C and the TCR is characterized from -40 to 85°C, and both characteristics are normalized to the lowest obtained value. All the resistors have a width and length of 0.5 μm and 1 μm in 0.11 μm, and 0.36 μm and 0.4 μm in 22 nm.

Techno.	Properties	N+			P+		
		diff.	poly.	poly. (high res.)	diff.	poly.	poly. (high res.)
0.11 μm	Normalized density	**1**	1.28	-	1.06	2.88	**4.12**
	Normalized TCR	**14.98**	1.69	-	7.87	**1**	5.34
22 nm	Normalized density	1.13	2.51	3.98/**4.07**	**1**	-	-
	Normalized TCR	5.55	**1**	1.36/1.12	**5.72**	-	-

and consequently,

$$v_{bp} = \frac{\left(g_{m4} + g_{d4} - g_{mb2}\left(\frac{g_{d6}}{g_{m5}}\right)\right) v_{dd} - g_{m2} v_{g2}}{g_{m4} + g_{d4} + g_{d2}}, \tag{3.34}$$

which simplifies to the same expression as (3.27) with $g_m \gg g_d$. The 2T bias generator thus only marginally affects the LS of I_{REF}, which can still be given by (3.28).

3.2.1.3 *Design and Sizing Methodology*

The design and sizing methodology of the proposed CWT PCR can be brought down to three main steps:

1) The selection of the resistor, based on its density in $\Omega/\square$ and its TCR in ppm/°C.
2) The sizing of the 2T body bias generator, which consists in selecting the transistor type and dimensions for M_{5-6}.
3) The sizing of all remaining transistors M_{1-4}, focusing on maintaining these transistors saturated in all PVT corners, and keeping mismatch-induced variability under an acceptable threshold.

First, step 1) relies on Table 3.3 to select an appropriate resistor type. We notice that diffusion resistors are typically a poor choice for nA-range CWT current references, as they present both a low density and a large TCR. High-resistivity (high-res.) polysilicon (poly) resistors are a better fit as they usually have a large density and a low TCR. In 22-nm FD-SOI, the high-res. poly resistor can even have its width narrowed down to 150 and 40 nm, thereby effectively increasing its density by 2.4 and 9× compared to the values shown in Table 3.3. In 0.11 μm, a P+ high-res. poly resistor is selected, while in 22 nm, an N+ high-res. narrow poly resistor is chosen. Because this work focuses on area reduction, we select the resistor with the highest density, but a better TC could potentially be attained by selecting the resistor with the lowest TCR. Section 3.2.3 however demonstrates that a sub-100-ppm/°C TC can be reached with the proposed choice.

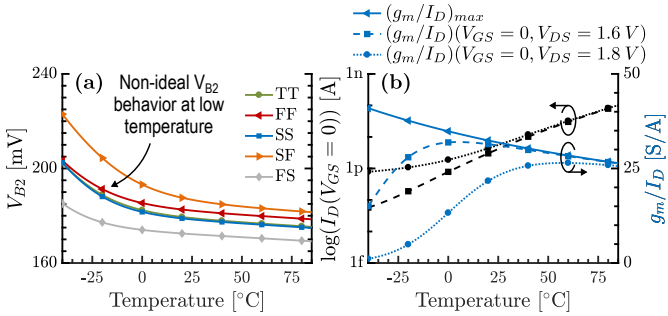

Fig. 3.27 The 2T voltage reference presents a nonideal behavior at low temperature, due to gate leakage, or to GIDL at high V_{DS}. All figures correspond to 22-nm FD-SOI. Temperature dependence of (a) V_{B2} in all process corners for a 2T voltage reference supplied at 1.8 V and implemented with 1-μm-long I/O nMOS, and (b) $\log(I_D)$ and (g_m/I_D) at V_{GS} = 0, and $(g_m/I_D)_{\max}$, for two different V_{DS} and for an I/O SLVT nMOS with W = 3.89 μm and L = 1 μm in the SS process corner.

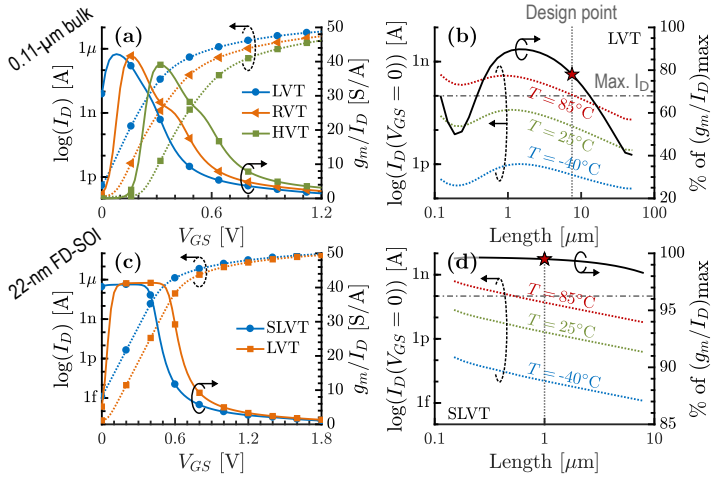

Fig. 3.28 All figures correspond to the SS process corner with a fixed $V_{DS} = V_{GS,\max}/2$. $\log(I_D)$, g_m/I_D vs. V_{GS} curves at T = -40°C (a) in 0.11 μm for core LVT, RVT and HVT nMOS with W = 0.5 μm and L = 10.45 μm, and (c) in 22 nm for I/O SLVT and LVT nMOS with W = 2 μm and L = 8 μm. $\log(I_D)$ at V_{GS} = 0 and at -40, 25 and 85°C, and g_m/I_D at V_{GS} = 0 as a percentage of $(g_m/I_D)_{\max}$ (b) in 0.11 μm for a core LVT nMOS with W = 0.5 μm and L ranging from 0.12 to 50 μm, and (d) in 22 nm for an I/O SLVT nMOS with W = 2 μm and L ranging from 0.15 to 8 μm.

Next, step 2) is presented in Figs. 3.27 to 3.30. The main problem that can appear in an inappropriately-sized 2T body bias generator is a divergence of the generated V_{B2} from its ideal behavior at low temperature, as depicted in Fig. 3.27(a). This discrepancy either stems from gate leakage, or from gate-induced drain leakage (GIDL), whose relative impact is exacerbated at low temperature due to an increased V_T. In the considered technologies, gate leakage is unlikely as 0.11-μm

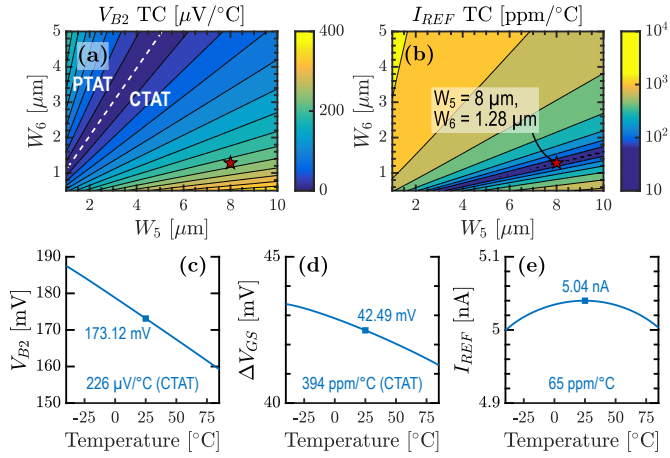

Fig. 3.29 In bulk technologies such as 0.11-μm, a CTAT V_{B2} is required to achieve a CWT I_{REF} due to the temperature dependence of the linearized body factor γ_b^*. Temperature coefficient of (a) V_{B2} and (b) I_{REF}, as a function of transistor widths W_5 and W_6. Temperature dependence of (c) V_{B2}, (d) ΔV_{GS} and (e) I_{REF} at the chosen design point.

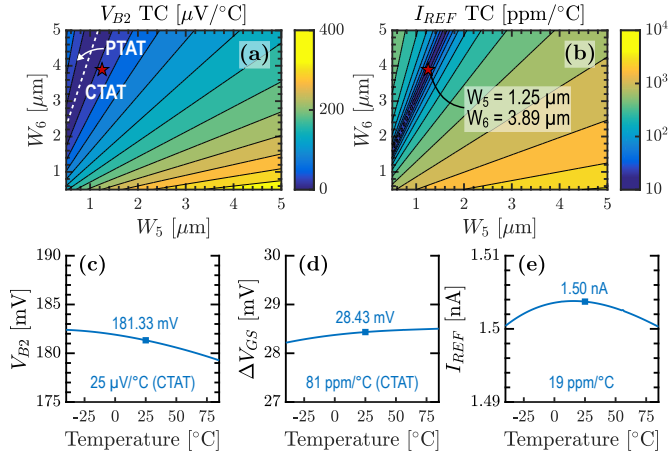

Fig. 3.30 In FD-SOI technologies such as 22-nm, a close-to-CWT V_{B2} is required to achieve a CWT I_{REF} due to the first-order temperature independence of the body factor γ_b^*. Temperature coefficient of (a) V_{B2} and (b) I_{REF}, as a function of transistor widths W_5 and W_6. Temperature dependence of (c) V_{B2}, (d) ΔV_{GS} and (e) I_{REF} at the chosen design point.

core devices still have a relatively thick oxide, and the devices used in 22 nm are I/O ones. Fig. 3.27(b) reveals that, at low temperature, I_{DS} at $V_{GS} = 0$ flattens instead of decreasing exponentially, while (g_m/I_D) at $V_{GS} = 0$, i.e., the slope of the $\log(I_D)$ vs. V_{GS} curve at $V_{GS} = 0$, plummets. This sharp drop is even more pronounced for a high V_{DS}, which is consistent with the fact that GIDL is exacerbated at high V_{DS}. This issue can nevertheless be alleviated by properly selecting the

transistor type and length of the transistors used in the 2T body bias generator, as shown in Fig. 3.28. In 0.11 μm, a low-V_T (LVT) transistor is preferable to a regular- or high-V_T (RVT or HVT) one, as these latter types present a strong degradation of (g_m/I_D) at V_{GS} = 0 [Fig. 3.28(a)]. Regarding the transistor length, L = 7.5 μm is selected, thereby yielding a (g_m/I_D) at V_{GS} = 0 equal to 78.1 % of $(g_m/I_D)_{\max}$, and a 107.9-pA leakage per transistor in the SS 85°C corner which is close to the selected 100-pA target [Fig. 3.28(b)]. In 22 nm, super-low-V_T (SLVT) I/O transistors are selected as they feature a nearly-perfect behavior at V_{GS} = 0 [Fig. 3.28(c)]. A length of 1 μm is chosen, leading to a (g_m/I_D) at V_{GS} = 0 equal to 99.5 % of $(g_m/I_D)_{\max}$, and a 50.7-pA leakage per transistor in SS 85°C. Note that, as the supply voltage can go up to 1.8 V thanks to the use of I/O devices, an additional zero-V_{GS} transistor M_7 identical of M_6 is added on top of it in Fig. 3.35(b) to reduce the V_{DS} to values similar to Fig. 3.28, thereby limiting the impact of GIDL while simultaneously improving LS. Now that the transistor types and lengths have been selected, a two-dimensional sweep of W_{5-6} allows to determine the ratio S_6/S_5 leading to a CWT I_{REF}, as represented in Figs. 3.29 and 3.30 for the 0.11-μm and 22-nm designs, respectively. In 0.11 μm, a complementary-to-absolute-temperature (CTAT) V_{B2} is required to compensate the temperature dependence of γ_b^* in bulk [Fig. 3.29(a)]. The chosen design point corresponds to W_5 = 8 μm and W_6 = 1.28 μm [Fig. 3.29(b)], and leads to a 226-μV/°C CTAT slope for V_{B2} [Fig. 3.29(c)] and a 65-ppm/°C TC for I_{REF} [Fig. 3.29(e)]. In 22 nm, a close-to-CWT V_{B2} is required because of the first-order temperature independence of γ_b^* in FD-SOI [158] [Fig. 3.30(a)]. The chosen design point corresponds to W_5 = 1.25 μm and W_6 = 3.89 μm [Fig. 3.30(b)], and leads to a 25-μV/°C CTAT slope for V_{B2} [Fig. 3.30(c)] and a 19-ppm/°C TC for I_{REF} [Fig. 3.30(e)].

Finally, step 3) must ensure that M_{1-4} remain saturated across PVT corners, and that variability constraints are met. On the one hand, M_{1-2} are operated in weak inversion and their aspect ratio S_{1-2} must be chosen so that $V_{GS2} = V_{DS1} > 4U_T$ in the FF 85°C corner. M_{3-4} should be biased in moderate inversion to minimize the current mirror mismatch within a reasonable silicon area, and their aspect ratio S_{3-4} must be such that $V_{GS4} = V_{DS4} > 4U_T$. In practice, this limit on V_{GS4} should be larger than $4U_T$ because of the operation in moderate inversion. On the other hand, variability considerations can also come into play, but this requires to establish an analytical expression linking the variability of I_{REF} to the transistor dimensions. To do so, we can rely on Pelgrom's law [162], and, under the assumption that the dominant source of mismatch is the threshold voltage, which is a common assumption in weak/moderate inversion [163], on the I_{DS} mismatch between two transistors taken from [154]. To compute the variability of I_{REF} due to mismatch, we employ the following expression

$$I_{REF} = \frac{(V_{T01} - V_{T02}) + \gamma_b^* V_{B2} + nU_T \log\left(1 + \frac{\Delta I_{DS}}{I_{DS}}\right)}{R}, \tag{3.35}$$

which is a more accurate version of (3.31) taking into account the difference of V_{T0} and the current imbalance between M_{1-2}. Considering R, γ_b^*, n and U_T as constants, the variance of I_{REF} in the proposed CWT PCR can be computed as

$$\sigma^2(I_{REF}) = \frac{\sigma^2\left(\Delta V_{T0,1-2}\right)}{R^2} + \left(\frac{\gamma_b^*}{R}\right)^2 \sigma^2\left(V_{B2}\right) + \left(\frac{nU_T}{R}\right)^2 \sigma^2\left(\log\left(1+\frac{\Delta I}{I}\right)\right), \tag{3.36}$$

with

$$\sigma^2(\Delta V_{T0,1-2}) = \frac{2A_{V_{Tn}}}{W_1 L_1}, \tag{3.37}$$

$$\sigma^2(V_{B2}) = A_{V_{Tn}}\left[\frac{1}{W_5 L_5} + \left(\frac{n_5}{n_6}\right)^2 \frac{1}{W_6 L_6}\right]. \tag{3.38}$$

The random variable $X = \left(1+\frac{\Delta I}{I}\right)$ has a normal distribution with an expected value of one and a variance $\sigma^2(\Delta I/I)$ given by [154]. The third term in (3.36) can thus be obtained as the variance of a log-normal distribution expressed as

$$\sigma^2\left(\log\left(X\right)\right) = \left[\exp\left(\sigma^2\left(\frac{\Delta I}{I}\right)\right) - 1\right]\exp\left(2+\sigma^2\left(\frac{\Delta I}{I}\right)\right), \tag{3.39}$$

using the common expression linking $\sigma^2\left(\log\left(X\right)\right)$ to the parameters of the normal distribution X, and simplifies to

$$\sigma^2\left(\log\left(X\right)\right) \approx \sigma^2\left(\frac{\Delta I}{I}\right)\exp(2) \tag{3.40}$$

as $\sigma^2(\Delta I/I) \ll 1$. Eq. (3.36) informs us that the variability of I_{REF} stems from the V_T mismatch between the transistor pairs M_{1-2} and M_{5-6}, as well as the current imbalance between M_{3-4}, the latter being the dominant source of mismatch as later discussed in Section 3.2.3. Special care must therefore be taken in sizing the pMOS current mirror.

3.2.2 Architectural Optimizations

This section details the features added to the simplified design in Fig. 3.25(b), namely a circuit to mitigate the impact of parasitic diode leakage in Section 3.2.2.1, and another to trim I_{REF} and its TC in Section 3.2.2.2. Then, all the details regarding the final implementation of the proposed PCR in 0.11-μm bulk and 22-nm FD-SOI are provided in Section 3.2.2.3.

3.2.2.1 Parasitic Diode Leakage Mitigation

The remaining issue with the 2T voltage reference is related to parasitic diode leakage, which becomes significant at high temperature and leads to a distortion of

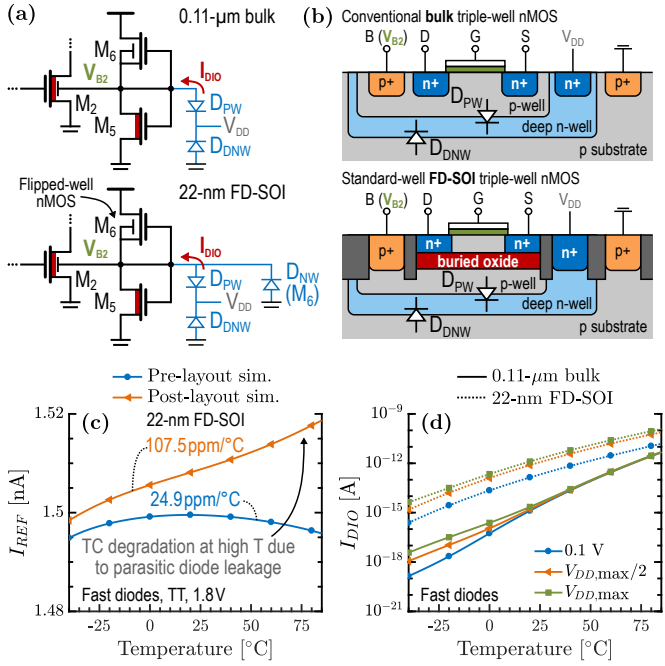

Fig. 3.31 I_{REF} **TC is degraded by the leakage of the parasitic p-well/deep n-well diode** D_{PW}**.** All figures are for 0.11-μm and 22-nm technologies except for (c). (a) Schematic of the 2T body bias generator with parasitic diodes. (b) Cross-section of triple-well nMOS devices. (c) Temperature dependence of I_{REF} in TT 1.8 V and fast diodes, based on pre- and post-layout simulations in 22-nm. (d) p-well/deep n-well diode leakage in a fast corner, as a function of temperature, for different reverse voltages, and for a diode area of 968 μm^2 in 0.11 μm (resp. 370 μm^2 in 22 nm).

V_{B2}, consequently impacting the TC of I_{REF}. It stems from the fact that the 2T voltage reference biases the body of the nMOS transistor M_2 with a voltage $V_{B2} > 0$ [Fig. 3.31(a)]. Therefore, M_2 needs to be implemented as a triple-well device, whose cross-section is represented for bulk and FD-SOI technologies in Fig. 3.31(b). Its p-well is biased at $V_{B2} > 0$, while its deep n-well and p-substrate are respectively connected to V_{DD} and ground. The connections of the parasitic diodes resulting from this triple-well implantation are shown in Fig. 3.31(a), and these parasitic diodes are located in the cross-section in Fig. 3.31(b). The leakage of the parasitic p-well/deep n-well diode leads to a current I_{DIO} flowing from V_{DD} to V_{B2}. Fig. 3.31(c) displays the degradation of I_{REF} TC from 107.5 to 24.9 ppm/°C between pre- and post-layout simulations in 22-nm FD-SOI. Furthermore, Fig. 3.31(d) reveals that this leakage increases exponentially with temperature and is also impacted by the reverse voltage drop V_D across the diode, with a higher V_D inducing a higher leakage. At 85°C, for a p-well corresponding to the dimensions of M_2 with its surrounding dummies, I_{DIO} is around 4.8 pA in 0.11 μm, and ranges from 15.4 to 120.4 pA in

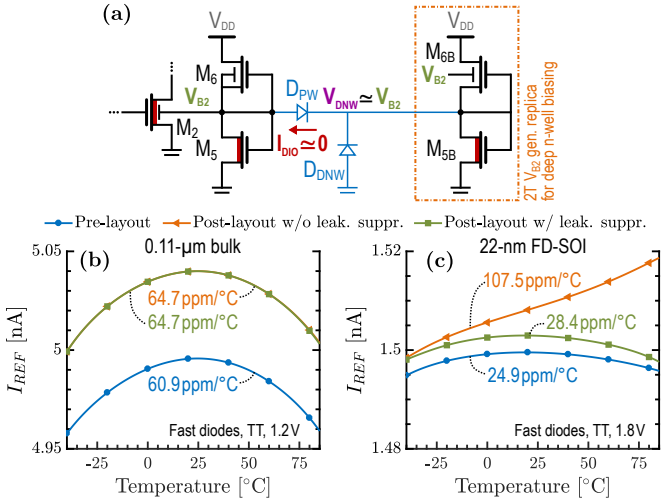

Fig. 3.32 **I_{REF} TC degradation is mitigated by leakage suppression, relying on a replica of the 2T body bias generator to bias the deep n-well.** (a) Schematic of the 2T body bias generator with parasitic diodes and a replica for leakage suppression. This schematic is accurate from an electrical standpoint, as it accounts for all parasitic diodes including the ones due to the replica. Temperature dependence of I_{REF}, based on pre-layout simulations, and post-layout simulations without and with leakage suppression, (b) in 0.11-μm bulk and (c) in 22-nm FD-SOI.

22 nm. These results suggest that I_{DIO} is largely underestimated in 0.11-μm models, as at 25°C and V_D = 0.1 V, the leakage per unit area is 2.83 aA/μm^2 in 0.11 μm compared to 565.96 aA/μm^2 in 22 nm, so a 200-× difference. At 85°C, this difference narrows down to 8.9×, with a leakage per unit area worth 4.70 fA/μm^2 in 0.11 μm and 41.73 fA/μm^2 in 22 nm. If we compare the leakage in 0.11 μm bulk to the dark current of a P+/n-well photodiode in 0.18 μm bulk at 25°C [164], the measured value is 7.16 fA for a 20×20-μm^2 diode, corresponding to a 17.9-aA/μm^2 leakage per unit area 6.3× larger than the simulated value in Fig. 3.31(d).

The proposed solution to mitigate the impact of this leakage, referred to as *leakage suppression*, consists in zeroing out the leakage by biasing the parasitic p-well/deep n-well diode with a reverse voltage V_D close to zero.This is achieved by biasing the deep n-well with a voltage V_{DNW} close to V_{B2}, generated by a replica of the 2T body bias generator, as shown in Fig. 3.32(a). This replica has the same S_6/S_5 ratio as the body bias generator, but not necessarily the same widths W_{5-6}, thereby allowing to adjust its power consumption. The leakage suppression technique was initially proposed in the context of voltage references [25], and mentioned as a possible solution for current references in [165]. For the 0.11-μm design in Fig. 3.32(b), because the parasitic diode model underestimates the leakage, we observe no significant degradation of I_{REF} TC between pre- and post-layout simulations, and the leakage suppression circuit therefore has no impact on the post-layout behavior.

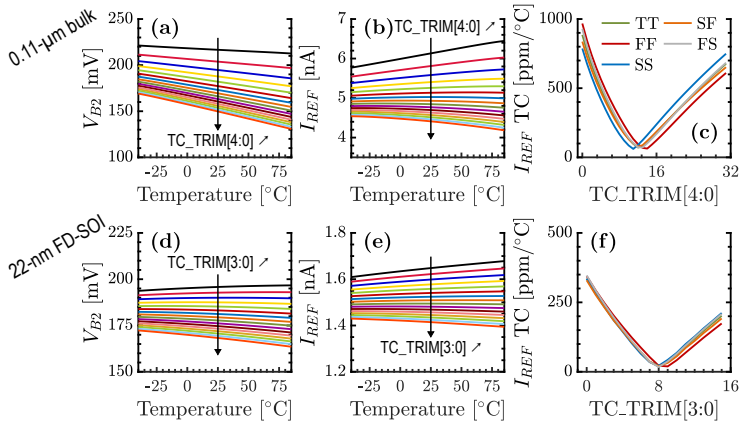

Fig. 3.33 I_{REF} **TC is trimmed by changing the effective width of** M_5 **in the 2T body bias generator.** In TT 1.2 V (resp. 1.8 V), temperature dependence of V_{B2} [(a) and (d)] and I_{REF} [(b) and (e)] as a function of the trimming code in 0.11 μm (resp. 22 nm). (c)(f) I_{REF} TC as a function of the trimming code in conventional process corners.

For the 22-nm design in Fig. 3.32(c), I_{REF} TC is degraded from 24.9 to 107.5 ppm/°C due to the parasitic diode leakage, but this degradation is nearly entirely recovered by the leakage suppression circuit, leading to a post-layout 28.4-ppm/°C TC. In the complete schematic in Fig. 3.35, the careful reader may notice that in 0.11-μm bulk, M_{6-6B} have their body connected to V_{B2} [Fig. 3.35(a)] and are located in the same p-well as M_2. On the contrary, in 22-nm FD-SOI, M_{6-6B} have their body connected to V_{DNW} [Fig. 3.35(b)], because they are implemented with SLVT flipped-well devices required to have a lower V_T than M_{5-5B}. They are thus located in an n-well, which is biased by the replica to keep the leakage of diode D_{NW} [Fig. 3.31(a)] from impacting V_{B2}.

3.2.2.2 *Temperature Coefficient and Reference Current Trimming*

Depending on the application, it might be necessary to calibrate the TC of I_{REF} and/or I_{REF} itself, to maintain performance across process corners. The proposed design includes two trimming circuits fulfilling this function. First, the TC trimming circuit is presented in Figs. 3.33 and 3.35, and relies on a change of S_6/S_5 in (3.29) to tune the TC of V_{B2}, and therefore, the TC of I_{REF}. It is implemented by changing the effective width of M_5 using binary-weighted branches connected in parallel. The switches are either located on top of or below transistors M_{5Vi}. We find more effective to place switches below M_{5Vi} in technologies with a large n as it results in a low I_{on}/I_{off} ratio. This switch arrangement alleviates the problem by providing a larger V_{GS} and therefore I_{DS} when the switch is on. Figs. 3.33(a) to (c) illustrate the effect of this trimming circuit in 0.11 μm, whereas Figs. 3.33(d) to (f) depict it in 22 nm. We observe in Figs. 3.33(a) and (d) that the change in V_{B2} TC allows to make I_{REF} either PTAT or CTAT [Figs. 3.33(b) and (e)] across the trimming

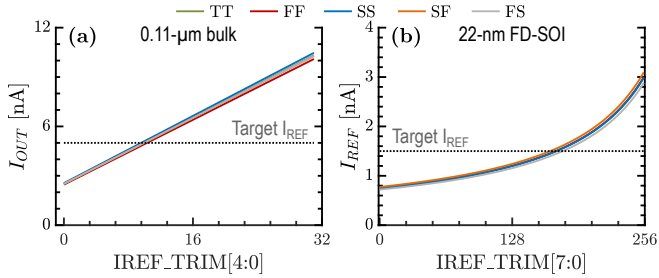

Fig. 3.34 I_{OUT} **is trimmed by means of a binary-weighted current mirror in bulk, and** I_{REF} **by a trimmable binary-weighted resistance in FD-SOI.** At 1.2 V (resp. 1.8 V), trimmed current at 25°C as a function of the trimming code in (a) 0.11 μm and (b) 22 nm.

range, and that the minimum I_{REF} TC is easily reached in the five conventional process corners [Figs. 3.33(c) and (f)]. Section 3.2.3.1 will later highlight that skewed process corners, i.e., different process corners for the devices of different V_T types used for M_5 and M_6, are more critical and should be adequately considered when defining the trimming range.

Moreover, a trimming of I_{REF} can be required in applications relying on an accurate value of I_{REF}. In 0.11 μm, this trimming is performed by a 5-bit binary-weighted current mirror [Fig. 3.35(a)], allowing for a linear control of the output current I_{OUT} [Fig. 3.34(a)]. Besides, 3.3-V I/O devices are used for the mirror formed by M_3, M_4 and $M_{4BF-4BVi}$, and for the switches $M_{SWBF-SWBVi}$, as they feature a lower I_{off} than core devices. In 22 nm, the I_{REF} trimming circuit is integrated inside the reference, and is implemented by eight binary-weighted resistors which can be shorted by nMOS switches [Fig. 3.35(b)]. This trimming scheme is possible as the I_{on}/I_{off} ratio is larger in 22 nm than in 0.11 μm thanks to a lower n, and is also more power-efficient as it avoids the overhead associated with I_{OUT}. In addition, it enables a finer trimming resolution, but leads to a nonlinear relationship between the calibration code and I_{REF} as it changes the value of resistor R in (3.31) [Fig. 3.34(b)].

3.2.2.3 *Final Implementation*

Two current references, respectively without trimming, and with TC and I_{REF} trimming, have been implemented in each of the 0.11-μm bulk and 22-nm FD-SOI technologies. The complete schematic of the proposed reference with leakage suppression, and TC and I_{REF} trimming, is presented in Fig. 3.35, while the layout and sizing of the four proposed references can be found in Fig. 3.36 and Table 3.4, respectively. Interestingly, Fig. 3.36 reveals that the area overhead of the trimming circuit, with respect to the area of the reference without trimming, corresponds to 23.5 % in 0.11 μm and can be attributed equally to the TC and I_{REF} trimming circuits, while it is only 9.1 % in 22 nm and is predominantly due to the binary-weighted resistors used to trim I_{REF}.

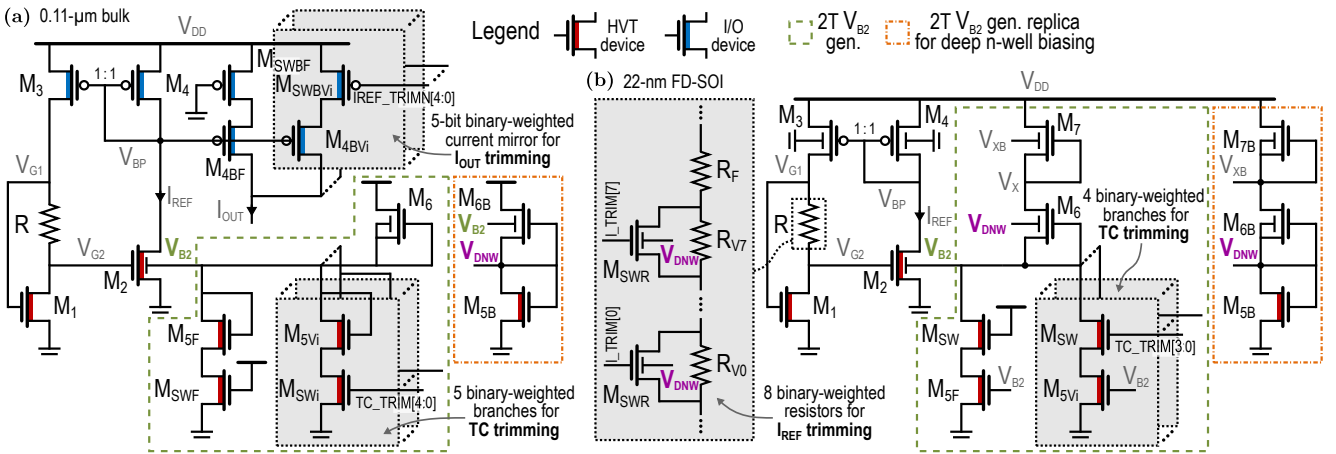

Fig. 3.35 Complete schematic of the proposed nA-range CWT reference in (a) 0.11-μm bulk and (b) 22-nm FD-SOI. The schematic includes trimming circuits for TC and I_{REF}, as well as a replica of the 2T body bias generator to suppress the leakage of the parasitic p-well/deep n-well diode.

Table 3.4 Sizing of the proposed nA-range CWT current references.

	0.11-μm bulk*							22-nm FD-SOI					
	w/o trimming			w/ TC and I_{REF} trimming				w/o trimming			w/ TC and I_{REF} trimming		
	Type*	W [μm]	L [μm]	Type*	W [μm]	L [μm]		Type*	W [μm]	L [μm]	Type*	W [μm]	L [μm]
M_{1-2}	LL	2×8	4×5	LL	2×8	4×5	M_{1-2}	LVT	8	4×8	LVT	8	4×8
M_{3-4}	HS	2×2	2×25	I/O	20×2.5	5	M_{3-4}	SLVT	0.32	10×8	SLVT	0.32	10×8
M_5	LL	16×4	7.5	-	-	-	M_5	LVT	8×1.25	1	-	-	-
M_{6-7}	HS	8×1.28	7.5	HS	8×1.28	7.5	M_{6-7}	SLVT	8×3.89	1	SLVT	8×3.9	1
M_{5B}	LL	4×4	7.5	LL	4×4	7.5	M_{5B}	LVT	8×1.25	1	LVT	16×0.625	1
M_{6B-7B}	HS	2×1.28	7.5	HS	2×1.28	7.5	M_{6B-7B}	SLVT	8×3.89	1	SLVT	8×3.9	1
R	P+ poly (high res.)	0.5	256×15.565	P+ poly (high res.)	0.5	212×18.705	R	N+ poly (high res.)	0.04	100×9.765	-	-	-
M_{5F}	-	-	-	LL	4×4	7.5	M_{5F}	-	-	-	LVT	8×0.625	1
M_{5Vi}	-	-	-	LL	1 to 16×4	7.5	M_{5Vi}	-	-	-	LVT	1 to 8×0.625	1
M_{SWF}	-	-	-	LL	4×0.25	2	M_{SW}	-	-	-	LVT	0.16	8
M_{SWVi}	-	-	-	LL	1 to 16×0.25	2	M_{SWR}	-	-	-	SLVT	10	0.15
M_{4BF}	-	-	-	I/O	10×2.5	5	R_F	-	-	-	N+ poly (high res.)	0.04	85×5.634
M_{4BVi}	-	-	-	I/O	1 to 16×2.5	5							
M_{SWBF}	-	-	-	I/O	10×0.25	1.25	R_{Vi}	-	-	-	N+ poly (high res.)	0.04	1 to 128×5.634
M_{SWBVi}	-	-	-	I/O	1 to 16×0.25	1.25							

* Dimensions reported for 0.11-μm bulk are pre-shrink ones, and must be scaled by a factor 0.9× to obtain silicon dimensions. * In 0.11 μm, HS refers to high-speed, i.e., LVT, and LL to low-leakage, i.e., HVT. In 22 nm, SLVT refers to super-low-V_T, and LVT to low-V_T.

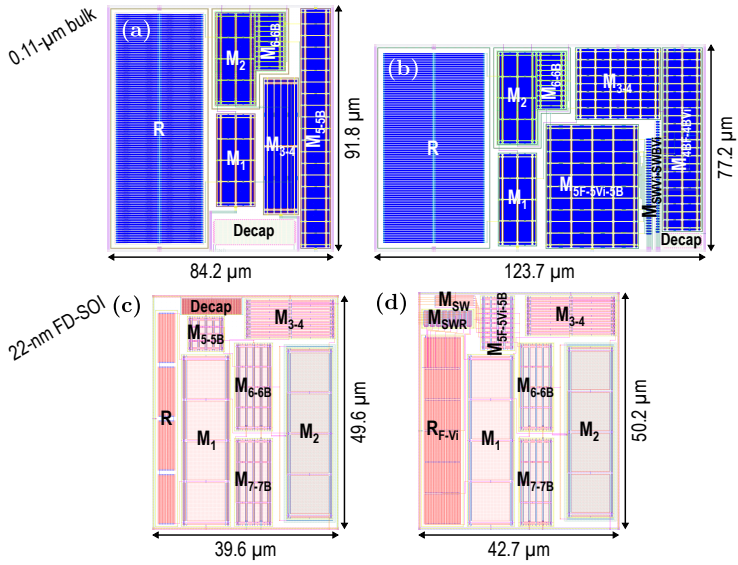

Fig. 3.36 Layout of the proposed reference (a)(c) without and (b)(d) with TC and I_{REF} trimming, in 0.11-μm bulk and 22-nm FD-SOI.

Table 3.5 Summary of the simulated and measured performance of the proposed nA-range CWT references. LS is lower in the 22-nm design than in the 0.11-μm one due to the larger intrinsic gain (g_m/g_d) in FD-SOI compared to bulk [37], as well as a greater $L/L_{\min}$ ratio. TC is also lower in 22 nm thanks to a more limited second-order behavior of the temperature dependence of I_{REF}.

	0.11-μm bulk		22-nm FD-SOI		
	w/o trimming Sim.	w/ trimming Sim.	w/o trimming Sim.	w/ trimming Sim.	w/ trimming **Meas.**
I_{REF} [nA]	5.04	5.03	1.50	1.50	1.21/1.50[†]
Power [nW]	5.03 @0.45V	13.88 @0.85V	2.04 @0.65V	2.35 @0.75V	2.87 @0.75V
Area [mm^2]	0.00773	0.00954	0.00197	0.00214	
Supply range [V]	0.45 – 1.2	0.85 – 1.2	0.65 – 1.8	0.75 – 1.8	
LS [%/V]	2.22	2.84	0.44	0.41	0.51
Temp. range [°C]	-40 – 85	-40 – 85	-40 – 85	-40 – 85	
TC [ppm/°C]	121.3	64.3	52.2	21.7	168.0/89.2[†]
I_{REF} var. (process) [%]	11.60	9.05	10.48	9.88	4.10/0.61[†]
I_{REF} var. (mismatch) [%]	0.71	1.32	2.55	2.98	
t_{start} [ms]	0.65	1.82	0.96	1.05	11.96

[†] Before and after trimming.

3.2.3 Post-Layout Simulation Results

In this section, we discuss the post-layout simulation results of the four references in Section 3.2.2.3. More specifically, the temperature dependence is discussed in conventional and skewed process corners, and for Monte-Carlo (MC) simulations. Additionally, for the design with TC and I_{REF} trimming, we characterize the supply voltage dependence and startup. Table 3.5 summarizes the performance of the designs.

3.2.3.1 Designs in 0.11-μm Bulk CMOS Technology

The temperature dependence of V_{B2} and I_{REF} is shown in Fig. 3.37. In the design without trimming, there is a slight change of V_{B2} [Fig. 3.37(a)], hence deteriorating I_{REF} TC in FF and SS to 90 and 99 ppm/°C, compared to 65 ppm/°C in TT [Fig. 3.37(b)]. Trimming the TC and I_{REF} modifies the CTAT slope of V_{B2} [Fig. 3.37(c)], and thereby reduces the TC to at most 78 ppm/°C in SF [Fig. 3.37(d)]. While the trimming mechanism in Fig. 3.37 may not yield obvious benefits in conventional process corners, its interest in dealing with different process corners for the two V_T types employed for M_{5-6} is paramount, as will be discussed herebelow in relation to Fig. 3.39. Next, the supply voltage dependence is depicted in Fig. 3.38, with the minimum supply voltage given by

$$V_{DD,\min} \approx 4U_T + \max\left(V_{GS1}, V_{SG4}, V_{B2}\right). \tag{3.41}$$

For this design, $V_{DD,\min}$ is limited to 0.85 V by the large V_{SG4} due to the use of I/O devices in the pMOS current mirror. Yet, the 2T body bias generator already produces a valid V_{B2} above 0.4 V, explaining why the design without trimming can operate down to 0.45 V in Table 3.5. V_{B2} LS is comprised between 1.42 and 1.57 mV/V from 0.85 to 1.2 V [Fig. 3.38(a)], while I_{REF} LS ranges from 2.67 to 3.52 %/V [Fig. 3.38(b)]. Eq. (3.28) indicates that this LS predominantly stems from the variation of M_3 V_{DS}. In addition, Fig. 3.39 considers the impact of HS/LL skewed process corners, i.e., different process corners for the high-speed (HS) and low-leakage (LL) core devices used for M_{5-6}. Fig. 3.39(a) shows that, without trimming, I_{REF} ranges from 7.42 nA in (FF, SS) down to 2.62 nA in (SS, FF), resulting in process variations of +47.2% / -48.0%. The remaining variations after trimming are +3.6% / -1.4%, related to the finite resolution of the trimming circuit. Regarding I_{REF} TC [Fig. 3.39(b)], it lies between 65 and 1283 ppm/°C without trimming, and is reduced to a range from 31 to 110 ppm/°C after trimming. Moreover, I_{REF} TC is below 100 ppm/°C in all process corners except (FF, SS), which would necessitate a slightly larger TC trimming range. The effect of the TC trimming scheme is to increase the CTAT slope of V_{B2} in fast nMOS HS corners, and to diminish it in slow ones, on top of smaller variations related to the LL corner [Fig. 3.39(c)]. Then, MC simulations highlight that, without trimming [Fig. 3.40(a)], the impact of mismatch is limited, with a (σ/μ) of 0.71 %.This value is relatively close to the

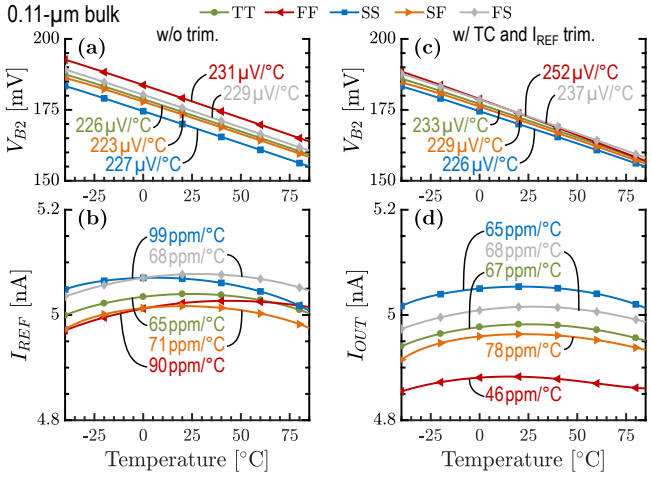

Fig. 3.37 In 0.11-μm bulk, post-layout simulation of the temperature dependence of V_{B2} and I_{REF}, in all process corners and at 1.2 V, without trimming [(a) and (b)], and with TC and I_{REF} trimming [(c) and (d)].

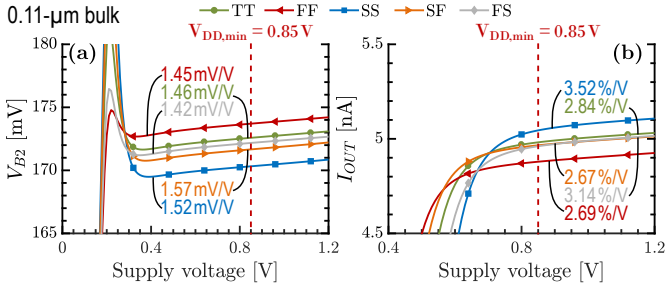

Fig. 3.38 In 0.11-μm bulk, post-layout simulation of the supply voltage dependence of V_{B2} and I_{REF} in all process corners and at 25°C, with TC and I_{REF} trimming.

1.18 % predicted by (3.36), from which 1% can be attributed to the mismatch of the pMOS mirror. The impact of process variations is more significant, with a (σ/μ) of 11.60 %, as a result of the process variations of M_{5-6} but more critically, of the resistance. In Fig. 3.40(b), the distribution of the TC due to local mismatch presents a 68-ppm/°C median and an 84-ppm/°C 99th percentile, while global process and combined effects both have a 122-ppm/°C median, with 99th percentiles at 422 and 446 ppm/°C. With TC trimming and no I_{REF} trimming, I_{REF} (σ/μ) slightly rises to 1.32 % with mismatch and shrinks to 9.05 % with process variations [Fig. 3.40(c)], due to a different sizing and to the trimming itself. In terms of TC, the median is cut down to 65 ppm/°C, with a 99th percentile at 75 ppm/°C for mismatch, and 80 ppm/°C for process and combined effects [Fig. 3.40(d)]. Finally, the x-% startup time corresponds to the time at which I_{REF} remains within (100-x) % of its steady-state value. The nominal 99-% startup time is equal to 1.83 ms in Fig. 3.41(a), and

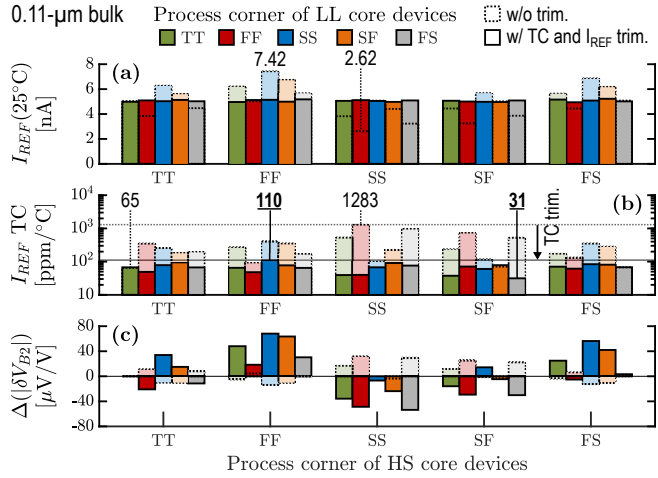

Fig. 3.39 In 0.11-μm bulk and at 1.2 V, post-layout simulation of (a) I_{REF} at 25°C, (b) I_{REF} TC from -40 to 85°C, and (c) the change in CTAT slope of V_{B2}, denoted as δV_{B2}, with respect to its nominal value, without trimming, and with TC and I_{REF} trimming.

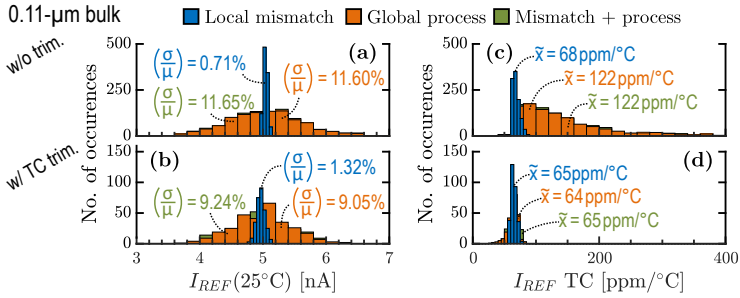

Fig. 3.40 In 0.11-μm bulk, for post-layout MC simulations (10^3 without trimming, and 3×10^2 with TC trimming) in TT at 1.2 V, histograms of I_{REF} at 25°C [(a) and (b)] and of I_{REF} TC from -40 to 85°C [(c) and (d)], without trimming [(a) and (c)], and with TC trimming [(b) and (d)]. $\tilde{x}$ denotes the median of the distribution.

ranges from 0.12 to 390.8 ms in the best- and worst-case corners, respectively FF 85°C and SS -40°C. This startup time is acceptable for a nA-range current reference which is most likely going to be used as an always-on block.

3.2.3.2 *Designs in 22-nm FD-SOI CMOS Technology*

In Fig. 3.42, depicting the temperature dependence of I_{REF}, the design without trimming shows slim variations of V_{B2} CTAT slope between 24.4 and 25.4 μV/°C [Fig. 3.42(a)], translating into negligible variations of I_{REF} TC from 19 to 24 ppm/°C [Fig. 3.42(b)]. After trimming, V_{B2} and its TC are slightly different [Fig. 3.42(c)], yet I_{REF} TC remains in a range similar to the design without trimming, comprised between 17 and 22 ppm/°C, while a clear effect of the I_{REF} trimming can be ob-

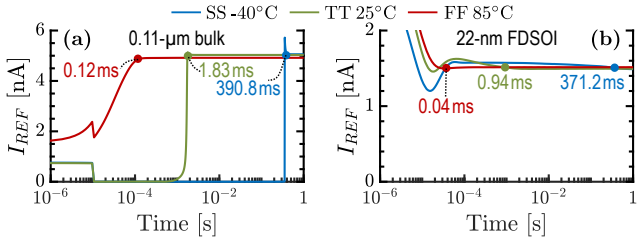

Fig. 3.41 Post-layout startup waveforms of the reference with TC and I_{REF} trimming, in the fastest (FF 85°C), typical (TT 25°C), and slowest (SS -40°C) corners, (a) at 1.2 V in 0.11-μm bulk and (b) at 1.8 V in 22-nm FD-SOI, using a voltage source with a 100-μs rise time.

served [Fig. 3.42(d)]. Then, regarding the supply voltage dependence in Fig. 3.43, $V_{DD,\text{min}}$ is equal to 0.75 V and is not dominated by V_{SG4} as in 0.11 μm, but rather by the minimum V_{DD} required by the switches in the I_{REF} trimming circuit to avoid distortion. Fig. 3.43(a) reveals that V_{B2} is generated at 0.5 V, and presents an LS around 230 μV/V. In Fig. 3.43(b), I_{REF} features an LS between 0.37 and 0.57 %/V, which is a reduction of nearly 6× compared to the 0.11-μm design, thanks to the larger (g_m/g_d) in FD-SOI. Moreover, Fig. 3.44 illustrates the variations in SLVT/LVT skewed process corners, i.e., different process corners for the SLVT and LVT I/O devices used for M_{5-6}. Fig. 3.44(a) displays that I_{REF} spans from 2.02 nA in (FF, SF) to 1.02 nA in (SS, FS) without trimming, leading to process variations of +34.1% / -33.4%. However, trimming reduces variations to +0.2% / -0.3%, approximately 10× better than in 0.11 μm, which is consistent with the fact that the 22-nm design uses three additional calibration bits for I_{REF}. Adding more bits to the 0.11-μm design would be possible, but only at the expense of significant area overhead for the binary-weighted current mirror. Then, regarding the TC, it ranges from 19 to 210 ppm/°C without trimming, and is reduced from 14 to 36 ppm/°C after it, while being below 50 ppm/°C in all corners [Fig. 3.44(b)]. The effect of the TC trimming is to bring V_{B2} CTAT slope closer to its value in the SLVT TT corner, with slightly larger (resp. lower) values in the fast (resp. slow) nMOS LVT corners [Fig. 3.44(c)]. Next, considering MC simulations, without trimming, mismatch leads to a (σ/μ) of 2.55 % which is 3× larger than in 0.11 μm due to the smaller dimensions of the pMOS current mirror. Eq. (3.36) indeed predicts a variability of 3.78 % from which 3.65 % come from the mirror mismatch. Process variations lead to a (σ/μ) of 10.70 % similar to 0.11 μm [Fig. 3.45(a)]. I_{REF} TC suffers most from mismatch, with a 49-ppm/°C median and a 172-ppm/°C 99th percentile, than from process variations, with a 28-ppm/°C median and a 62-ppm/°C 99th percentile [Fig. 3.45(c)]. After TC trimming and no I_{REF} trimming, I_{REF} (σ/μ) slightly increases while process variations are reduced, in the same fashion as in 0.11 μm [Fig. 3.45(b)]. The TC now has a median around 22 ppm/°C in all simulation types, with 99th percentiles at 33, 28, and 42 ppm/°C, for mismatch, process, and combined effects. Lastly, Fig. 3.41(b) highlights a nominal 99-% startup time of 0.94 ms, which spans from 0.04 and 371.2 ms in extreme corners. Similarly to the 0.11-μm

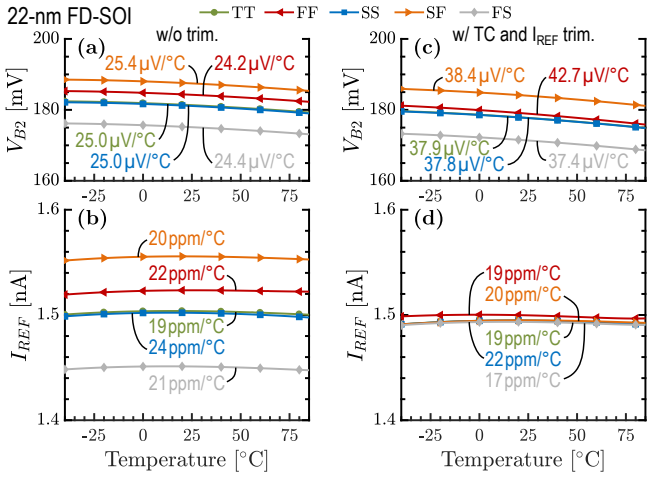

Fig. 3.42 In 22-nm FD-SOI, post-layout simulation of the temperature dependence of V_{B2} and I_{REF}, in all process corners and at 1.8 V, without trimming [(a) and (b)], and with TC and I_{REF} trimming [(c) and (d)].

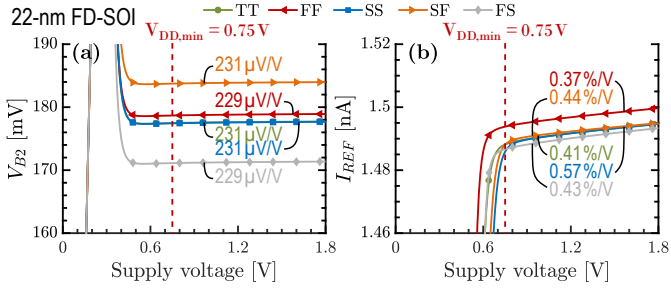

Fig. 3.43 In 22-nm FD-SOI, post-layout simulation of the supply voltage dependence of V_{B2} and I_{REF} in all process corners and at 25°C, with TC and I_{REF} trimming.

design, this startup time is acceptable for a nA-range current reference destined to be used as an always-on block.

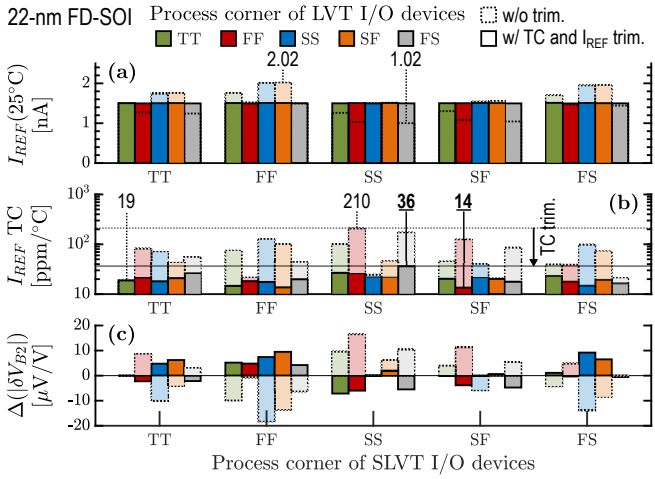

Fig. 3.44 In 22-nm FD-SOI and at 1.8 V, post-layout simulation of (a) I_{REF} at 25°C, (b) I_{REF} TC from -40 to 85°C, and (c) the change in PTAT slope of V_{B2}, denoted as δV_{B2}, with respect to its nominal value, without trimming, and with TC and I_{REF} trimming.

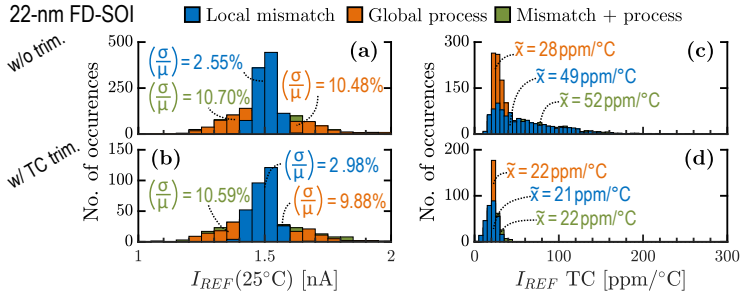

Fig. 3.45 In 22-nm FD-SOI, for post-layout MC simulations (10^3 without trimming, and 3×10^2 with TC trimming) in TT at 1.8 V, histograms of I_{REF} at 25°C [(a) and (b)] and of I_{REF} TC from -40 to 85°C [(c) and (d)], without trimming [(a) and (c)], and with TC and I_{REF} trimming [(b) and (d)]. $\tilde{x}$ denotes the median of the distribution.

3.2.4 Measurement Results

3.2.4.1 *Measurement Testbench*

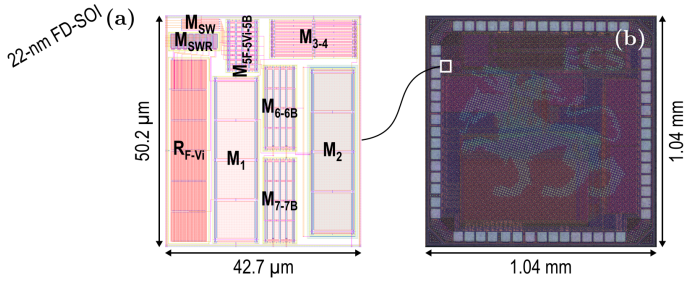

Fig. 3.46 In 22-nm FD-SOI, (a) layout of the proposed nA-range CWT current reference and (b) chip microphotograph with overlaid layout of the 1.08-mm^2 CERBERUS MCU.

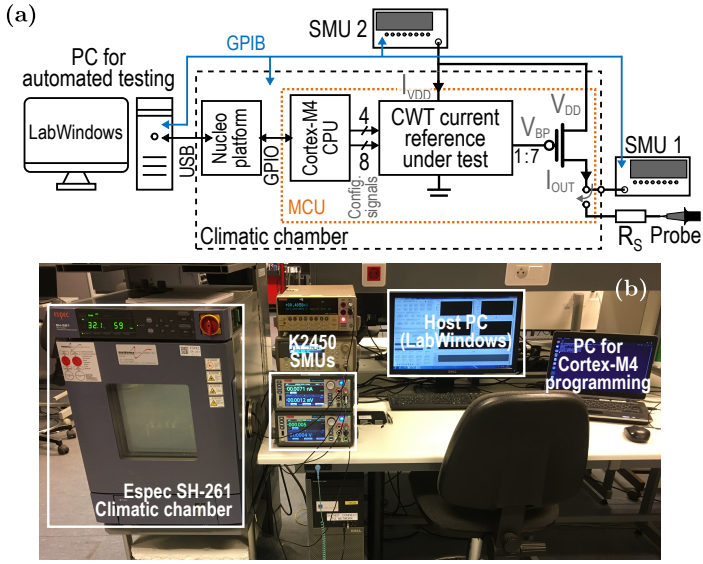

Fig. 3.47 Measurement testbench for the characterization of the dependence to supply voltage and temperature, as well as the startup time.

Out of the four designs in Section 3.2.2.3, the 22-nm design with TC and I_{REF} trimming has been fabricated as part of the CERBERUS microcontroller unit (MCU) [Fig. 3.46(b)]. Eleven dies have been measured, using the setup shown in Fig. 3.47. It consists of a host PC controlling an Espec SH-261 climatic chamber for the tem-

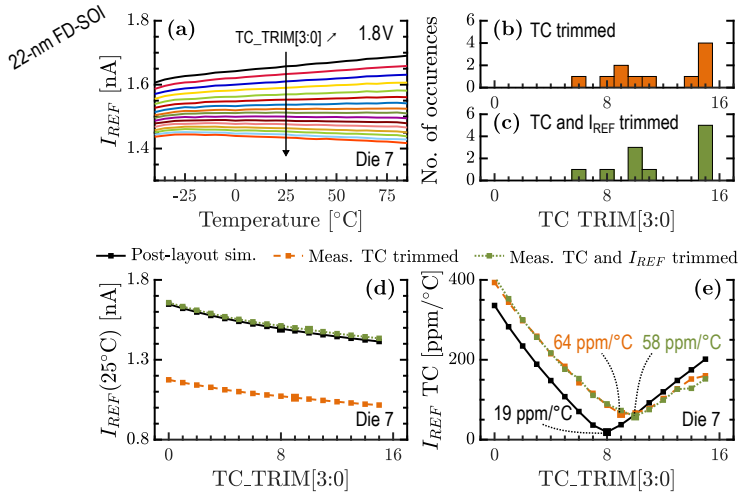

Fig. 3.48 In 22-nm FD-SOI, (a) measured temperature dependence of I_{REF} at 1.8 V for all trimming codes, with I_{REF} already trimmed. Histograms of the trimming code giving the minimum TC (b) before and (c) after I_{REF} trimming. Impact of the TC trimming (d) on I_{REF} at 25°C and (e) on I_{REF} TC. (b)(c) are for the 11 dies while (a)(d)(e) are for die 7.

perature sweep, and two Keithley K2540 source measure units (SMUs) for the supply voltage sweep. On the one hand, SMU 1 measures $I_{OUT} = 7I_{REF}$ with V_{SD} = 0.9 V, and the current mirror producing I_{OUT} only slightly increases I_{REF} (σ/μ) by 0.36 %. On the other hand, SMU 2 measures the sum of I_{OUT} and the supply current I_{VDD}. Besides, the calibration bits are managed by an on-chip Cortex-M4, interacting through GPIO with a Nucleo-64 platform piloted by the host PC. To measure the startup time, SMU 1 is replaced by an 82-MΩ resistance R_S, in series with the 1-MΩ input resistance of the probe.

3.2.4.2 *Measurement of the 22-nm FD-SOI Design*

Fig. 3.48(a) illustrates that the temperature dependence of I_{REF}, with I_{REF} already trimmed, changes from PTAT to CTAT for different TC trimming codes. Figs. 3.48(b) and (c) show the histogram of the optimal code before and after I_{REF} trimming, revealing only marginal changes and thereby confirming that trimming I_{REF} does not impact its TC. However, trimming the TC slightly modifies I_{REF} [Fig. 3.48(d)]. The TC should thus be trimmed first, and I_{REF} consequently adjusted to reach the target value. For the die showing the best TC, a minimum TC of 58 ppm/°C is reached for a code of 0xA, compared to 19 ppm/°C for 0x8 in the TT post-layout simulation. This gap originates from the behavior of I_{REF} below -20°C, as shown in Fig. 3.49(b). Next, the temperature dependence of I_{REF} is studied in Fig. 3.49 at the three stages of the trimming process, with Figs. 3.49(a) and (b) representing the I_{REF} vs. T curves for the 11 dies without and with trimming, respectively. Before any trimming, I_{REF} is 1.12 nA on average, with a (σ/μ) of 4.1 % and a TC of

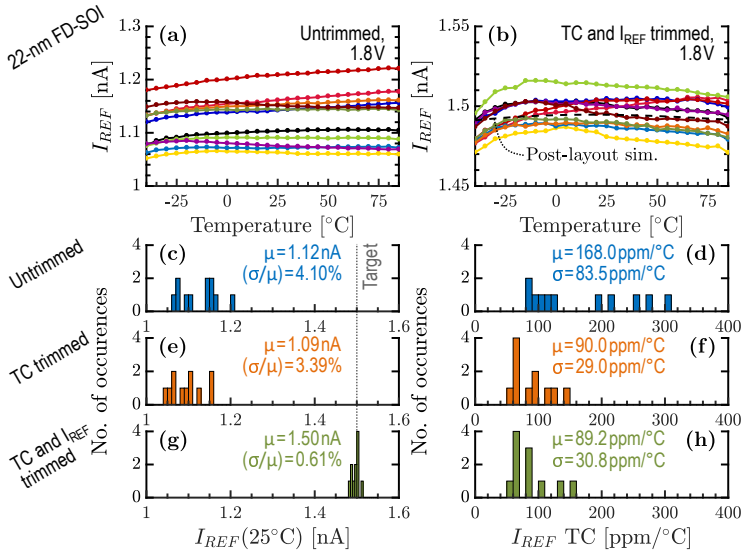

Fig. 3.49 In 22-nm FD-SOI and at 1.8 V, measured temperature dependence of I_{REF} (a) without trimming, and (b) with TC and I_{REF} trimming. Measured histograms of I_{REF} at 25°C [(c), (e) and (g)] and of I_{REF} TC from -40 to 85°C [(d), (f) and (h)], for the reference without trimming, with TC trimming, and with TC and I_{REF} trimming.

168 ppm/°C [Figs. 3.49(c) and (d)], suggesting that the dies might originate from a slow SLVT and fast LVT nMOS process corner [Fig. 3.45(a)]. After trimming the TC, (σ/μ) diminishes to 3.39 % while the TC decreases to 90 ppm/°C, with a standard deviation cut from 83.5 to 29 ppm/°C [Figs. 3.49(e) and (f)]. Finally, after complete trimming, I_{REF} is close to the 1.5-nA design point, with a (σ/μ) reduced to 0.61 % and an 89.2-ppm/°C average TC [Figs. 3.49(g) and (h)]. It should be noted that these results correspond to a trimming based on the complete temperature profile between -40 and 85°C, but a two-point trimming at -35 and 65°C gives comparable results and only slightly increases the mean TC from 89.2 to 89.4 ppm/°C, as depicted in Fig. C.3 in Appendix C. The TC differs from post-layout simulations due to the decrease of I_{REF} below -20°C, which is most likely due to the nMOS switches in the TC trimming circuit limiting the current flowing through M_{5Vi}. Moreover, Fig. 3.50(a) shows the supply voltage dependence of I_{REF} for the 11 trimmed dies, with $V_{DD,\text{min}}$ = 0.75 V and a 0.51-%/V average LS [Fig. 3.50(b)] in line with the 0.41-%/V simulated value.

Then, I_{REF} temperature dependence is characterized at various supply voltages, revealing a consistent behavior, albeit the TC is slightly degraded from 58 to 92.3 ppm/°C as V_{DD} is reduced from 1.8 to 0.9 V [Fig. 3.50(c)]. Additionally, Fig. 3.50(d) characterizes the supply voltage dependence of I_{REF} at different temperatures, and indicates that a $V_{DD,\text{min}}$ of 0.9 V would be required to operate down to -40°C, but also that the LS deteriorates from 0.58 to 0.96 %/V as temperature

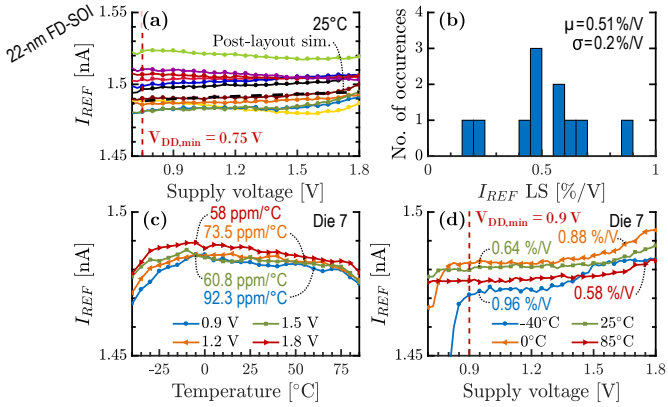

Fig. 3.50 In 22-nm FD-SOI and with TC and I_{REF} trimmed, (a) measured supply voltage dependence at 25°C and (b) histogram of LS from 0.75 to 1.8 V. For die 7, measured (c) temperature dependence at different supply voltages and (d) supply voltage dependence at different temperatures.

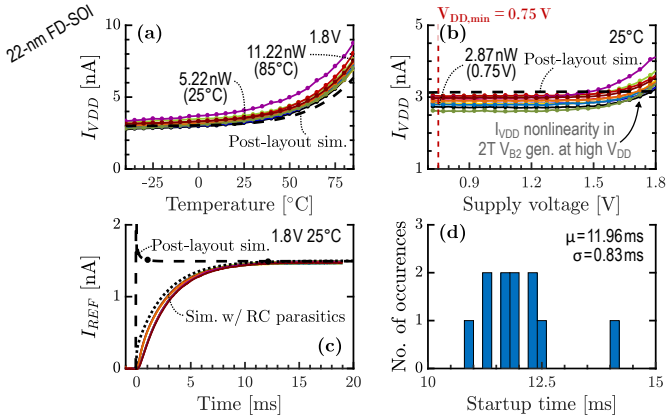

Fig. 3.51 In 22-nm FD-SOI, measured dependence of the supply current (a) to temperature at 1.8 V, and (b) to supply voltage at 25°C. (c) Measured startup waveforms and (d) histogram of the 99-% startup time at 1.8 V 25°C.

decreases from 85 to -40°C. These curves highlight an increase of I_{REF} above 1.5 V, which could be linked to drain-induced barrier lowering (DIBL). Moreover, the current consumption I_{VDD} in Fig. 3.51(a) is $2I_{REF}$ = 3 nA at low temperature as it is dominated by the PCR, but increases exponentially with temperature when the 2T body bias generator and its replica start to prevail, leading to a 2.1-× increase from 25 to 85°C. The dependence of I_{VDD} to the supply voltage in Fig. 3.51(b) presents a sharper increase at high V_{DD} compared to I_{REF}, likely originating from the 2T body bias generator. An average power consumption of 2.87 nW is reached at 0.75 V and 25°C. At last, regarding the 99-% startup time, an average value of 11.96 ms 11.4× larger than the simulated value is obtained [Fig. 3.51(d)]. In simulation, when con-

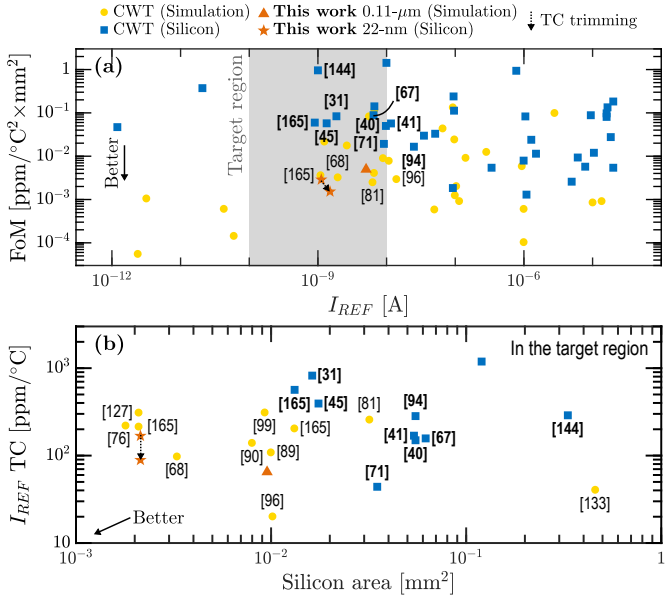

Fig. 3.52 (a) Figure of merit combining temperature dependence and silicon area as a function of I_{REF}, and (b) trade-off between TC and area in the target region, based on the state of the art of current references.

sidering a 33-pF capacitance at the drain of the pMOS transistor generating I_{OUT}, in parallel with the 82-MΩ resistance of R_S, a startup time of 12.15 ms is reached [Fig. 3.51(c)], confirming that PCB parasitics are the source of the observed discrepancy.

3.2.5 Comparison to the State of the Art

In this section, we compare our work to the state of the art of simulated and fabricated nA-range CWT current references, detailed in Table 3.6 and illustrated in Fig. 3.52 using the FoM defined in (1.12). In our comparison, we focus on fabricated current references, and hence limit our discussion to the proposed 22-nm design. Besides, we do not normalize the silicon area to the technology node as a fair normalization is not straightforward for analog circuits. First, Fig. 3.52(a) indicates that trimming the TC of I_{REF} improves the FoM of our 22-nm design by 1.9× thanks to a TC reduction from 168 to 89 ppm/°C. Compared to the closest fabricated competitor [71], our design offers a 12.9× FoM reduction explained by a 16.4× area reduction and an increased temperature range, despite a 2× larger TC. Moreover, [67, 40, 41] achieve an acceptable TC around 150 ppm/°C within a silicon area above 0.05 mm^2, due to the use of large subthreshold transistors [67] or resistors [40, 41]. [45, 31, 165] exhibit areas between 0.01 and 0.02 mm^2, dominated

by gate-leakage transistors [45], resistors [31], or a subthreshold β-multiplier [165]. Nevertheless, their area efficiency is counterbalanced by their relatively large TC above 400 ppm/°C. [94] uses a pMOS with a V_G tracking V_T, and a source degeneration resistor to achieve temperature compensation. It occupies a 0.0053-mm^2 area but consumes 28.5 μW, thereby limiting its interest. [144] employs a current DAC periodically trimmed by a high-precision duty-cycled current reference. It achieves a 265 ppm/°C TC, but at the expense of a significant 0.332-mm^2 silicon footprint.

3.2.6 Conclusion

In this second part of Chapter 3, we presented a nA-range CWT peaking current reference, biasing a resistor with the ΔV_T between two subhtreshold transistors, one of them being forward body biased to decrease its V_T. The body bias is generated by a 2T voltage reference, with a replica to suppress the leakage of parasitic diodes at high temperature. In addition, the proposed reference does not require a startup circuit as it is unstable at zero I_{REF}, and includes two simple mechanisms to trim I_{REF} and its TC, so as to maintain performance across process corners. Then, we proposed a thorough sizing methodology and validated the reference with post-layout simulations in a bulk and an FD-SOI technology, to demonstrate that the body effect can indeed be employed in both of these technologies. Finally, we fabricated the proposed reference in 22-nm FD-SOI, and measured a 1.5-nA current across 11 dies with average TC and LS of 89 ppm/°C and 0.51 %/V, respectively. It consumes 2.87 nW at 0.75 V and occupies an area of 0.00214 mm^2. This results in a 12.9× FoM improvement compared to the closest fabricated competitor in the nA range. Further work could focus on extending the temperature range to 125°C while avoiding a sharp increase of the power consumed by the 2T voltage reference.

Table 3.6 Comparison table of temperature-independent nA-range current references.

	Far [96]	Cordova [89]	Santamaria [99]	Agarwal [81]	Aminzadeh [133]	Mahmoudi [127]	Bruni [76]	Huang [90]	Yang [68]	De Vita [71]	Kayahan [94]	Ji [39]	Wang [67]	Wang [40]	Huang [41]	Lee [144]	Chang [45]	Shetty [31]	Lefebvre [165]	**Lefebvre This work**	
Publication	ROPEC	ISCAS	ISCAS	TCAS-II	AEU		CAE	AEU	AEU	ISCAS	TCAS-I	ISSCC	VLSI-DAT	TCAS-I	TCAS-II	JSSC	JJAP	TCAS-I	JSSC	JSSC	
Year	2015	2017	2019	2022	2022	2022	2023	2023	2023	2007	2013	2017	2019	2019	2020	2020	2022	2022	2023	2024	
Type of work	**Simulations**									**Silicon measurements**										**Sim.**	**Meas.**
Samples	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	20	90	10	10	16	10	10	3	10	20	N/A	11
Technology	0.18μm	0.18μm	0.18μm	0.18μm	0.18μm	0.13μm	0.18μm	0.18μm	0.18μm	0.35μm	0.35μm	0.18μm	0.18μm	0.18μm	0.18μm	0.18μm	90nm	0.13μm	22nm	0.11μm	22nm
I_{REF} [nA]	14	10.9	2.7	5.6	6.7	6.6	6.3	8.9	1.96	9.1	25	6.7	6.5	9.8	11.6	1	1.3	1.9	1.25/0.9*	5.03	1.12/1.50†
Power [nW]	150	30.5	26	9.5	51	3.7	3.3	0.05	9.2	54.8	28500	9.3	15.8	28	48.6	4.5/14	8.6	10.2	7.8/5.8*	13.88	2.87
	@1V	@0.9V	@2V	@0.55V	@1V	@0.4V	@0.6V	@0.8V	@0.55V	@1.5V	@5V	@N/A	@0.85V	@0.7V	@0.8V	@1.5V	@0.75V	@0.85V	@0.9V	@0.85V	@0.75V
Area [mm^2]	**0.0102**	**0.01**	**0.0093**	0.032	**0.46**	**0.0021**	**0.0018**	**0.008**	**0.0033**	0.035	**0.0053**	**0.055**	**0.062**	**0.055**	**0.054**	**0.332**	0.0175	0.0163	0.0132	**0.00954**	**0.00214**
Supply range [V]	1 – 3.3	0.9 – 1.8	2 – 3.63◇	0.55 – 1.9	1.1 – 1.8	0.4 – 1.6	0.6 – 1.8	0.8 – 1.8	0.55 – 1.8	1.5 – 4	N/A	1.3 – 1.8	0.85 – 2	0.7 – 1.2	0.8 – 2	1.5 – 2	0.75 – 1.55	0.85 – 2	0.9 – 1.8	0.85 – 1.2	0.75 – 1.8
LS [%/V]	**0.1**	**0.54**	**8.9**◇	**0.022**	**0.03**	2.7	**12.1**	1.39	**0.2**	**0.57**	**150**	1.16	4.15	**0.6**	1.08	1.4	**0.15**	4	**0.26**/**0.39**†	2.84	**0.51**
Temp. range [°C]	0 – 70	-20 – 120	-40 – 125	-30 – 70	-40 – 120	-40 – 120	-40 – 120	0 – 125	0 – 100	0 – 80	0 – 80	0 – 110	-10 – 100	-40 – 125	-40 – 120	-20 – 80	0 – 120	-40 – 120	-40 – 85	-40 – 85	-40 – 85
TC [ppm/°C]	**20**	**108**	309	256	**40.3**	308	219	**139**	**96.8**	**44**	**128**/250*	**680**/283†	**157**	**150**	**169**	289/265◇	**53**/394*	530/**822***	**203**/565*	**65**	168/**89**†
TC type	Typ.	μ	μ	μ	μ	μ	Typ.	μ	μ	μ	N/A	μ	μ	μ	μ	μ	μ	μ	μ	$\tilde{x}$	μ
I_{REF} var. (process) [%]	N/A	15.8 / 11.6†	N/A	+55.4 / -28.5◇	N/A	N/A	+129.1 / -61.8◇	+2.8 / -13.9◇	8.7	2.16	8/1.22*	N/A	N/A	+11.7 / -8.7◇	+17.6 / -10.3◇	N/A	21.1	N/A	+9.9 / -9.5	+3.64 / -1.41◁	+0.21 / -0.54◁
I_{REF} var. (mismatch) [%]	5.8	N/A	**20.3**	**10.4**	**0.7**	**6.1**	N/A	2.6	1.7		1.4	4.07/1.19*	3.33	1.6	4.3	1.26/**0.25**†		**15.6**	**6.39**/**9.20***	1.32	4.10/**0.61**†
Trimming	No	Yes	No	No	No	Yes	No	Yes	No	No	No	Yes	No	Yes	Yes	Yes	Yes	Yes	No	Yes	Yes
Spec. components	No	Native	No	Res.	Res., **BJT**	No	No	No	No	No	No	Res., **BJT**	No	Res.	Res.	No	No	Res.	No	Res.	Res.
FoM [ppm/°C^2×mm^2]	**0.0029**	**0.0077**	0.0174	0.0819	0.1159	**0.0040**	**0.0025**	**0.0089**	**0.0032**	0.0193	0.0166	0.1415	0.0887	0.0499	0.0570	0.9595	0.0575	0.0835	0.0597	**0.0050**	**0.0015**

* Simulated and measured values. † Before and after trimming. ◇ Estimated from figures. ▷ For 25 and 2.5 minutes between two calibrations. ◁ After trimming.

3.3 Take-Away Messages

In this chapter, we presented two ideas to modify $\Delta V_{GS}/R$ current references in order to generate a CWT nA-range current, which is well-suited to the requirements of IoT sensor nodes. Both ideas rely on the ΔV_T between two weak-inversion transistors of the same V_T type, one of them being forward body-biased, either through its body in a bulk technology or through its back-gate in an FD-SOI one. The first idea is to bias an SCM using a β-multiplier structure, generating a PTAT voltage with a CWT offset voltage obtained by FBB. In this first current reference, the body bias is generated by an SCM constituted of transistors with different V_T types and self-biased by the generated current. In addition, this reference does not include any trimming circuitry and requires a startup circuit. Then, the second idea is to bias a resistor with a voltage generated by a peaking current reference and also obtained by FBB. In this second current reference, the body bias is generated by a 2T voltage reference. Furthermore, this reference includes a leakage suppression mechanism at high temperature based on a replica of the 2T voltage reference and two simple trimming mechanisms for I_{REF} and its TC, but does not require any startup circuit due to the 2T voltage reference. Both proposed ideas thus rely on a $\Delta V_{GS}/R$ structure to bias a V-to-I converter, either a β-multiplier biasing an SCM in Section 3.1, or a peaking current reference biasing a resistor in Section 3.2. They also include FBB to obtain the ΔV_T between two weak-inversion transistors.

Furthermore, both ideas were validated through silicon measurements of fabricated references in 22-nm FD-SOI. The first reference is measured across 20 dies and presents a 0.9-nA current with a 0.39-%/V LS and a 565-ppm/°C TC. It consumes a minimum power of 5.8 nW at 0.9 V and 25°C, and occupies a silicon area of 0.0132 mm^2. The main issue of this reference is the large TC degradation from simulation (203 ppm/°C) to measurement (565 ppm/°C), which calls for a TC calibration scheme, and the large 9.20-% variability due to mismatch and process variations despite the relatively large area for this technology node, which requires additional design tuning knobs to reach a more favorable design point. The second reference is measured across 11 dies and features a 1.5-nA current with average LS and TC of 0.51 %/V and 89 ppm/°C, respectively. It consumes 2.87 nW at 0.75 V and occupies a silicon area of 0.00214 mm^2. It manages to reach a lower TC than an SCM-based reference by relying on a resistor, whose temperature dependence is much more linear than that of an SCM. The only drawback of this reference is that its power consumption strongly increases at high temperature, as the power consumption of the 2T voltage reference is proportional to the subthreshold leakage, which increases exponentially with temperature. Finally, the references were respectively simulated post-layout in TSMC 65 nm and 0.11 μm, to demonstrate feasibility in bulk technologies as they rely on the body effect.

Based on these results, we identify two claims which will be further detailed in the conclusion of this thesis:

1. *A self-cascode MOSFET (SCM) can generate a CWT nA-range current when biased by a PTAT voltage with a CWT offset voltage, leading to a CTAT inversion level which compensates the PTAT behavior of the specific current.*
2. *Trimming is necessary to obtain the best TC from MOS-based CWT current references and to ensure that this TC can be maintained across process corners.*

4

V/R Current References Based on Two-Transistor Voltage References

Every solution to every problem is simple.
It is the distance between the two where the mystery lies.
– Derek Landy

CONSTANT-WITH-TEMPERATURE (CWT) current references based on the ratio between a reference voltage and the equivalent resistance of a voltage-to-current (V-to-I) converter, referred to as V/R references in Chapter 1, generally rely on a bandgap voltage reference biasing the V-to-I converter through a feedback loop employing an operational transconductance amplifier (OTA). However, this conventional way of generating a reference current has evolved in recent years. On the one hand, the last two decades have seen the development of two-transistor (2T) voltage references with an ultra-low power consumption [22, 23, 24, 25], down to a few pW at ambient temperature, which otherwise do not significantly degrade performance metrics such as the line sensitivity (LS) and the temperature coefficient (TC) but generally require a calibration of V_{REF} and/or its TC. On the other hand, the OTA-based feedback loop can be suitably replaced by a single-transistor (1T) buffer [29, 30], thereby facilitating the design of the reference. Both of these enhancements allow to substantially reduce the silicon area occupied by V/R current references, making them attractive to implement area-efficient references with

a low TC, which are ideally-suited to the needs of Internet-of-Things (IoT) sensor nodes, as discussed in Chapter 2. Similarly to Chapter 3, the objective of this chapter is to examine potential solutions to the research question

"How can we practically modify existing current references to meet the specific requirements of the IoT ?",

established in the introduction of this thesis. Hence, this chapter presents three current references based on the idea of a 2T voltage reference generating a bias voltage for a V-to-I converter, with the buffering implemented by a single transistor. First, Section 4.1 presents a CWT μA-range and a proportional-to-absolute-temperature (PTAT) nA-range current references based on a 2T voltage reference, respectively relying on a resistor and a self-cascode MOSFET (SCM). The CWT μA-range reference biases the resistor with a quasi-CWT reference voltage matching the temperature coefficient of resistance (TCR) and generated by a 2T voltage reference consisting of transistors with different V_T types. In addition, it includes a calibration circuit for the TC of I_{REF} based on a change of transistor's aspect ratio in the voltage reference. In contrast, the PTAT nA-range reference biases an SCM with a PTAT voltage to generate a reference current proportional to the specific sheet current I_{SQ} and thus to T^{2-m}, where m is the temperature exponent of mobility comprised between 1.2 and 2 [49], thus yielding a direct dependence to absolute temperature T. Contrary to the CWT reference, the bias voltage is here obtained from a 2T voltage reference constituted of transistors of the same V_T type but with different widths. Then, Section 4.2 combines ideas from Sections 3.1 and 4.1, as it generates a CWT current by biasing an SCM using a PTAT voltage with a CWT offset voltage (Section 3.1), but replaces the β-multiplier by a four-transistor (4T) voltage reference buffered by a single transistor (Section 4.1), thereby solving all the limitations of the architecture previously discussed in Section 3.1. The 4T voltage reference employs forward body biasing (FBB) to generate the CWT offset voltage, and integrates a calibration circuit of the TC of I_{REF} based on a change of either the PTAT slope or CWT offset voltage of the generated voltage, using a change of transistor's aspect ratio in the voltage reference. All the references proposed in this chapter present two notable features. First, they do not require any startup circuit as they are unstable when the reference current is equal to zero, contrary to most existing current references. Second, they use a very limited number of transistors and are strikingly more simple than most references in the state of the art providing the same performance in terms of TC. At last, Section 4.3 closes this chapter with some concluding remarks.

4.1 A Family of Current References

In this first part of Chapter 4, we build upon [29, 30] to create a family of simple current references without startup circuit sharing two key principles: (i) the generation of a voltage reference by a 2T ULP structure and (ii) its buffering by a single transistor onto a voltage-to-current (V-to-I) converter. Compared with [29, 30], we substitute the gate-leakage transistor by either a self-cascode MOSFET (SCM) or a resistor, respectively resulting in a nA- and μA-range current. This leads to two novel current reference topologies, fabricated in a 0.18-μm partially-depleted silicon-on-insulator (PD-SOI) process. First, a proportional-to-absolute-temperature (PTAT) current reference built by applying a PTAT voltage to an SCM, which is similar to[27, 28] but with a different PTAT voltage generation. This reference could bias subthreshold operational amplifiers found in ULP sensor nodes with a constant g_m. The measured 0.096-nA current has a line sensitivity (LS) of 1.48 %/V, a temperature coefficient (TC) of 0.75 %/°C and a (σ/μ) of 1.66 %, while the current reference consumes down to 0.28 nW at 25°C. It consists of seven transistors and occupies a silicon area of 8700 μm^2. Second, a constant-with-temperature (CWT) current reference is obtained by the ratio of a voltage and a resistance with matched TCs. It provides a measured 0.99-μA current with an LS of 0.20 %/V, a TC of 290 ppm/°C, and a (σ/μ) of 0.65 %, and could be used as a reference for current-steering DACs. It consumes down to 0.64 μW at 25°C, and is made of four transistors and a polysilicon resistor, occupying a total silicon area of 3410 μm^2. Another version with a 4-bit TC calibration reduces temperature dependence down to 38 ppm/°C, and provides a 1.09-μA current within a 4270-μm^2 silicon area.

The remainder of this section is organized as follows. Section 4.1.1 highlights the principles shared by both proposed PTAT and CWT topologies, whose sizing is detailed in Section 4.1.2. Next, simulation and measurement results are discussed in Section 4.1.3. We address additional design considerations for an implementation in scaled technologies in Section 4.1.4. Finally, Section 4.1.5 compares our work to the state of the art and Section 4.1.6 offers some concluding remarks.

4.1.1 A Family of Current References

Fig. 4.1 presents the proposed family of current references, which share the same current generation principle. A reference voltage V_{REF} is generated by the 2T ULP structure formed by M_{1-2}, and then buffered onto a V-to-I converter by transistor M_3. The range and temperature dependence of the reference current, denoted as I_{REF}, are conditioned by the type of transistors used in the voltage reference and the chosen V-to-I converter. First, the current reference in Fig. 4.1(a) relies on a CWT voltage reference biasing a gate-leakage transistor or a resistor. The gate-leakage

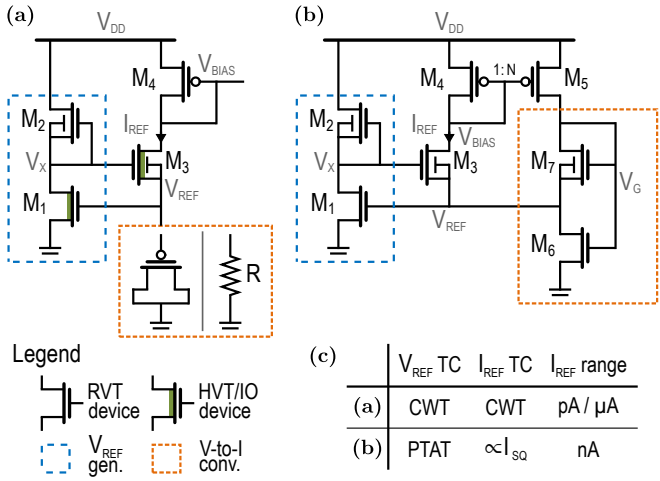

Fig. 4.1 Overview of the family of current references, generating a reference voltage V_{REF} with a 2T ULP structure and converting it into a current by single-transistor buffering onto (a) a gate-leakage transistor [29, 30] or a resistor, and (b) an SCM, generating a pA-, μA- and nA-range current, respectively. Finally, (c) summarizes the TC of V_{REF}, as well as the TC and range of I_{REF} across the different architectures.

transistor acts as a resistance in the order of GΩ. This structure was proposed in [29, 30] and generates a CWT reference current in the pA range. Alternatively, this current reference can rely on a quasi-CWT voltage reference biasing a resistor and compensating for its temperature dependence. It then generates a temperature-independent current in the μA range. Second, the current reference in Fig. 4.1(b) relies on a PTAT voltage reference biasing an SCM and generates a nA-range reference current proportional to the specific sheet current of M_{6-7} [27, 28]. Fig. 4.1(c) summarizes the characteristics of the three references described hereabove, with the I_{REF} range corresponding to the current level that is best suited to each reference, i.e., that leads to a reasonable silicon area. For example, the μA-range reference could generate a nA-range current, but only at the cost of significant silicon area due to the resistor. In the remainder of this section, we focus on the nA- and μA-range current reference topologies, as the pA-range one has already been proposed in prior art [29, 30].

The topology brought forward in this section offers three main advantages. First, it requires a small number of transistors, thus reducing the design time by restraining the number of degrees of freedom and potentially resulting in a low area footprint, even though considerations related to local mismatch will limit the area savings. Second, the voltage reference draws a supply current in the pA-to-nA range, resulting in a low power consumption compared to a β-multiplier or bandgap voltage reference. Third, it does not require any startup circuit as the reference has a unique stable operation point corresponding to a non-zero current,

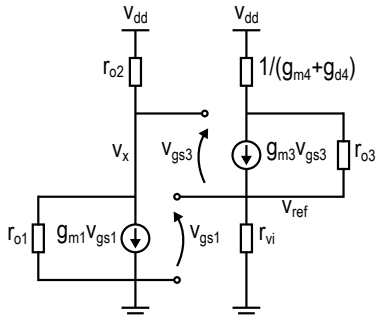

Fig. 4.2 Small signal schematic of the voltage reference, abstracting the V-to-I converter as an equivalent resistance r_{vi}.

leading to further area savings.

4.1.1.1 2T ULP Voltage Reference

The 2T ULP voltage reference used in this work was proposed in [29, 30] in the context of current references and shares the same operation principle as [22, 23, 24]. It relies on the balance of the subthreshold currents in transistors M_{1-2} to generate a reference voltage. There are three main assumptions underlying the reasoning that follows: (i) for the sake of generality, M_{1-2} have distinct characteristics, (ii) both transistors operate in weak inversion, and (iii) the drain-to-source voltage V_{DS} is larger than $4U_T$, where U_T is the thermal voltage, so the transistors are saturated. Applying (A.2) to M_{1-2} and solving for the reference voltage yields a unique solution

$$V_{REF} = n_1 U_T \log\left(\frac{I_{SQ2}}{I_{SQ1}}\frac{S_2}{S_1}\right) + \left(\frac{n_2 V_{T01} - n_1 V_{T02}}{n_2}\right). \tag{4.1}$$

This can be explained by the fact that M_2 acts as a current source biasing M_1 and leads to $V_{REF} > 0$ without requiring a startup circuit. For the μA-range reference, M_1 is chosen to have a larger threshold voltage than M_2, i.e., $V_{T01} > V_{T02}$, and the ratio S_2/S_1 can be used to tune the reference voltage's TC, whereas for the nA-range current reference, the same transistor type is used for M_{1-2} and (4.1) simplifies to a purely PTAT voltage

$$V_{REF} = nU_T \log\left(\frac{S_2}{S_1}\right), \tag{4.2}$$

assuming no mismatch between M_{1-2}. The LS of the reference voltage is computed from the small signal schematic in Fig. 4.2, where r_{vi} denotes the output resistance of the V-to-I converter. First, assuming that $g_{m3} \gg g_{d3}$ and $g_{m4} \gg \frac{1}{r_{vi}}$, the transfer function between v_x and v_{ref} is given by (4.3). Then, if $g_{m3} \gg \frac{1}{r_{vi}}$, this expression further simplifies to one, which is in line with the common-drain configuration of

M_3.

$$\frac{v_x}{v_{ref}} \simeq \frac{g_{m3} + g_{d3} + \frac{1}{r_{vi}}}{g_{m3}} \simeq 1 \tag{4.3}$$

$$\frac{v_{ref}}{v_{dd}} = \frac{g_{d2}}{g_{m1} + \frac{v_x}{v_{ref}}(g_{d1} + g_{d2})} \simeq \frac{g_{d2}}{g_{m1}} \tag{4.4}$$

Second, the supply dependence of V_{REF}, i.e., v_{ref}/v_{dd}, is given by (4.4) and simplifies to g_{d2}/g_{m1} for $g_m \gg g_d$.

4.1.1.2 nA-Range PTAT Current Reference

To generate a current proportional to the specific sheet current I_{SQ}, the nA-range reference relies on a moderate-inversion SCM formed by M_{6-7} and biased by a PTAT voltage, as in [27]. The use of moderate inversion requires the advanced compact MOSFET (ACM) model [156] to describe the transistor I-V relation, as presented in Appendix A.2. The ACM equations are applied to the SCM structure in Appendix B.
Moreover, the line sensitivity and mismatch of the reference current are directly related to the characteristics of the voltage reference, through the sensitivity $S_{I_{REF}}$. It is expressed based on (B.8). The line sensitivity and mismatch of the reference current can thus be expressed as

$$\frac{1}{I_{REF}}\frac{\partial I_{REF}}{\partial V_{DD}} = S_{I_{REF}}\frac{g_{d2}}{g_{m1}}, \tag{4.5}$$

$$\left(\frac{\sigma}{\mu}\right)_{I_{REF}} = S_{I_{REF}}\sigma_{V_{REF}}, \tag{4.6}$$

and depend on both the characteristics of the voltage reference and the sizing of the SCM. Lastly, the minimum supply voltage is given by

$$V_{DD,\min} = 4U_T + \max(V_{REF} + V_{GS3}, V_{REF} + V_{SG4}, V_G), \tag{4.7}$$

with each expression in the max function corresponding to one of the branches of the reference depicted in Fig. 4.1(b).

4.1.1.3 μA-Range CWT Current Reference

To generate a temperature-independent reference current, the μA-range current reference relies on a resistor biased by a CWT reference voltage. The reference current is thus given by $I_{REF} = V_{REF}/R$. Assuming that the threshold voltage of transistor M_i, denoted as V_{T0i}, decreases linearly with temperature T following $V_{T0i}(T) = V_{T0i}(T_0) - \alpha_{V_{T0i}}(T - T_0)$, and that the resistance temperature variation

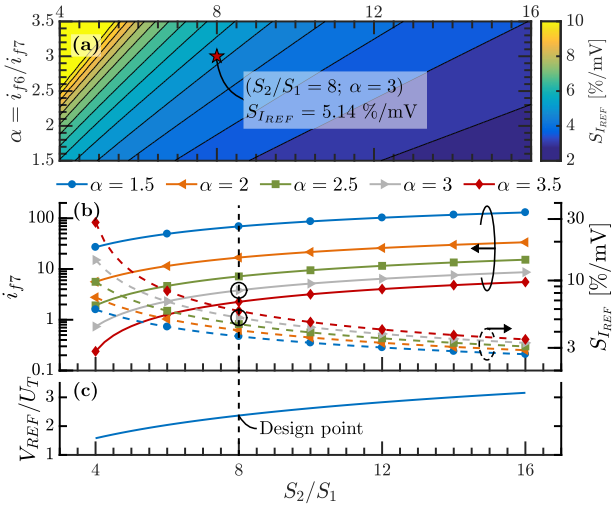

Fig. 4.3 (a) $S_{I_{REF}}$ is dependent on two key design parameters, namely S_2/S_1, related to the 2T ULP voltage reference, and $\alpha = i_{f6}/i_{f7}$, related to the SCM. The red star indicates the chosen design point. (b) Inversion level i_{f7} and sensitivity $S_{I_{REF}}$, for different values of α and (c) reference voltage V_{REF}, normalized by the thermal voltage U_T, as a function of S_2/S_1.

is captured by $\frac{\partial R}{\partial T}$, the temperature variation of I_{REF} is given by

$$\frac{\partial I_{REF}}{\partial T} = \frac{1}{R}\left(\frac{nk}{q}\log\left(\frac{I_{SQ2}S_2}{I_{SQ1}S_1}\right) + (\alpha_{V_{T01}} - \alpha_{V_{T02}})\right) - \frac{1}{R^2}\left(U_T \log\left(\frac{I_{SQ2}S_2}{I_{SQ1}S_1}\right) + (V_{T01} - V_{T02})\right)\frac{\partial R}{\partial T}. \tag{4.8}$$

Therefore, the ratio S_2/S_1 leading to zero temperature variation of the reference current at $T = T_0$ is

$$\frac{I_{SQ1}}{I_{SQ2}} \exp\left(\frac{q}{nk}\frac{(V_{T01} - V_{T02})\,\frac{1}{R}\frac{\partial R}{\partial T} + (\alpha_{V_{T01}} - \alpha_{V_{T02}})}{1 - \frac{T_0}{R}\frac{\partial R}{\partial T}}\right). \tag{4.9}$$

Similarly to the PTAT current reference, the line sensitivity and mismatch are expressed by (4.5) and (4.6), where $S_{I_{REF}}$ is expressed as $1/V_{REF}$. Interestingly, these quantities only depend on the characteristics of the voltage reference. Finally, the minimum supply voltage is given by (4.7) excluding V_G.

4.1.2 Circuit Design and Sizing Methodology

In this section, we explain the design choices and detail the steps of the sizing methodology used to implement the proposed references in the XFAB 0.18-μm PD-SOI technology.

4.1.2.1 nA-Range PTAT Current Reference

The sizing of the PTAT current reference illustrated in Fig. 4.1(b) has a twofold objective: minimizing the LS and variability of I_{REF}, while achieving the reference current target in nominal conditions (TT process, 25°C). Four main parameters can be tuned to achieve this objective:

1. S_2/S_1, the ratio of M_{1-2} aspect ratios, which amounts to W_2/W_1 if these transistors have the same length;
2. m, the multiplier or number of parallel devices used to implement both M_1 and M_2;
3. $\alpha = i_{f6}/i_{f7}$, the ratio of M_6 and M_7 inversion levels;
4. N, the multiplicative factor in the current mirror formed by M_4 and M_5.

The first two degrees of freedom are linked to the 2T voltage reference, while the two latter ones are related to the SCM. We will first explain the sizing of the V-to-I converter, i.e., the SCM, and will then turn to the 2T voltage reference. Besides, low-V_T (LVT) devices are selected to implement the proposed reference, as they lead to a lower minimum supply voltage than regular-V_T (RVT) devices and ensure the proper operation of the 2T voltage reference at low temperature, as will be discussed in Section 4.1.4.1. Then, we choose to invert the topology shown in Fig. 4.1(b), i.e., nMOS and pMOS devices are swapped, as well as ground and supply connections. This change makes it easier to reach a low reference current and avoids using several pwell voltages, requiring deep trench isolation (DTI) in PD-SOI or triple-well devices in bulk. Finally, the sizing of the SCM and its current mirror is similar to [27, 28], and performed at 25°C. It consists of the following steps:

1. Compute V_{REF} using (4.2);
2. Determine the inversion level of M_7 by solving (B.7) for i_{f7}. By definition, the inversion level of M_6 is computed as $i_{f6} = \alpha i_{f7}$, and the sensitivity $S_{I_{REF}}$ is calculated using (B.8);
3. Compute the aspect ratio and width of transistors M_6 and M_7, forming the SCM. S_7 is computed as
$$S_7 = \frac{N I_{REF}}{I_{SQ7} i_{f7}} \tag{4.10}$$
based on (A.4), while S_6 is calculated from (B.6);
4. Compute the aspect ratio and width of M_{3-5} using (A.4).

This methodology is implemented in Matlab, and the transistor properties, summarized in Table 4.1, are computed from DC SPICE simulations following [157]. Contrary to [27, 28], we do not limit ourselves to the methodology detailed hereabove, but we provide guidelines on how to select the main design parameters required by this methodology, namely S_2/S_1, α and N. Steps 1) and 2) are mostly technology-agnostic, as only the subthreshold slope factor n is required at this stage. Indeed,

Table 4.1 Properties of maximum-length 25-μm transistors in the XFAB 0.18-μm PD-SOI technology, at 25°C. I_{SQ} is determined in the sense of the ACM model.

Transistor type	n	I_{SQ} [nA]	V_{T0} [V]
LVT nMOS	1.21	99.63	0.433
LVT pMOS	1.14	23.98	-0.383
RVT nMOS	1.29	67.10	0.668
RVT pMOS	1.41	29.26	-0.749

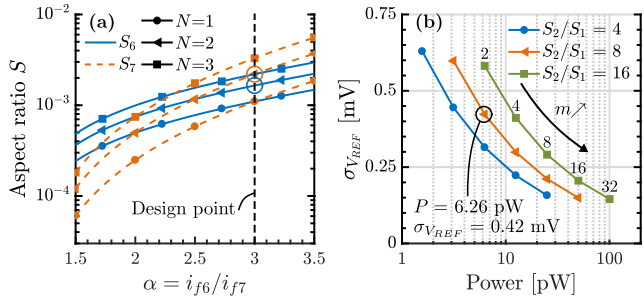

Fig. 4.4 (a) Aspect ratio of transistors M_{6-7} as a function of α, for different values of N, and for $S_2/S_1 = 8$, assuming the use of LVT pMOS devices for the SCM. (b) Trade-off between reference voltage mismatch, obtained from 10^4 Monte-Carlo runs, and power consumption in nominal conditions (TT, 1.2 V, 25°C), as a function of m and for different values of S_2/S_1. The unitary device is an LVT pMOS with a 1-μm width and 20-μm length.

Table 4.2 Sizing of the nA-range PTAT current reference in XFAB 0.18-μm PD-SOI.

		Sizing algorithm output			Final implementation	
	Type	W [μm]	L [μm]	i_f	W [μm]	L [μm]
M_1	LVT pMOS	4×1	20	-	4×1	20
M_2	LVT pMOS	32×1	20	-	32×1	20
M_3	LVT pMOS	0.34	10	0.12	0.35	10
M_4	LVT nMOS	1.03	2×25	0.05	2×0.5	2×25
M_5	LVT nMOS	2.06	2×25	0.05	4×0.5	2×25
M_6	LVT pMOS	0.82	20×25	11.41	**0.64**	20×25
M_7	LVT pMOS	1.10	20×25	3.80	**0.86**	20×25

the two other parameters coming into play are S_2/S_1 and α, which do not depend on the technology choice. Fig. 4.3(a) depicts sensitivity $S_{I_{REF}}$ as a function of these two parameters, and allows to select a couple $(S_2/S_1; \alpha)$ close to the target value for $S_{I_{REF}}$, here arbitrarily set to 5 %/mV. The chosen design point ($S_2/S_1 = 8$; $\alpha = 3$) is marked by a red star in Fig. 4.3(a) and yields a sensitivity of 5.14 %/mV. Furthermore, the trends observed in Fig. 4.3(a) are better understood by looking at Figs. 4.3(b) and (c). Increasing S_2/S_1 pushes M_{6-7} into moderate inversion, as evidenced by the increase of i_{f7} [Fig. 4.3(b)], due to the higher reference voltage V_{REF} applied to the SCM [Fig. 4.3(c)]. It should be noted that, for a fixed α, the sensitivity approximately improves as $1/i_{f7}$, as indicated by the first term in (B.12). Then, decreasing α provides a second tuning knob for improving $S_{I_{REF}}$, by pushing M_7 even further into moderate inversion [Fig. 4.3(b)]. Next, the results of step 3) are

technology-dependent, because they rely on (i) the specific sheet current (Table 4.1) and (ii) the I_{REF} target, here set to 0.1 nA. Fig. 4.4(a) represents the aspect ratio of M_{6-7} as a function of α, for different values of N and for a fixed voltage reference corresponding to $S_2/S_1 = 8$. Similarly to Fig. 4.3(b), decreasing α pushes M_{6-7} into moderate inversion, thus decreasing their aspect ratio at constant current. Besides, higher values of the multiplicative factor N increase S_{6-7}, as expected from (B.6) and (4.10), facilitating the implementation of these transistors at the cost of a higher power consumption. Here, we select $N = 2$, which gives $S_6 = 1.65 \times 10^{-3}$ and $S_7 = 2.20 \times 10^{-3}$. The very low values obtained for these aspect ratios cannot be achieved with a single device, but will be implemented as a composite transistor, i.e., the series connection of several devices. Step 4) is straightforward as it is a direct consequence of previous choices.

Finally, let us consider the sizing of the 2T voltage reference. As mentioned earlier, LVT pMOS devices are selected to ensure a proper operation in all process corners down to -40°C, as will be explained in Section 4.1.4.1. In addition, a length of 20 μm is chosen to reduce the output conductance of M_2 and improve the LS, as captured by (4.5). M_{1-2} are then sized based on Fig. 4.4(b), illustrating the trade-off between the standard deviation of the reference voltage due to local mismatch, denoted as $\sigma_{V_{REF}}$, and its power in nominal conditions. First, S_2/S_1 marginally impacts mismatch, as it is dominated by the threshold voltage variations of the smallest device, here M_1, whose sizes do not change with S_2/S_1. Consequently, increasing S_2/S_1 only results in a linear increase of the power consumption, shifting the curve to the right of Fig. 4.4(b). Second, the multiplier m improves mismatch as $1/\sqrt{m}$, following Pelgrom's law, while increasing power as m. A multiplier $m = 4$ is selected, in addition to the previously chosen $S_2/S_1 = 8$, and gives a power of 6.26 pW and a standard deviation of 0.42 mV.

The transistor sizes output by the sizing algorithm are summarized in Table 4.2. Two main changes are applied for the final implementation: (i) M_{4-5} are split into parallel devices to enable a common centroid layout, and (ii) M_{6-7} are narrowed based on simulation results to match the 0.1-nA I_{REF} target in nominal conditions. It should be noted that α, and therefore S_6/S_7, must remain constant during this upscaling, to preserve the reference behavior.

4.1.2.2 μA-Range CWT Current Reference

The sizing of the CWT current reference shown in Fig. 4.1(a) focuses on minimizing the TC of I_{REF} while achieving the current reference target, here set to 1 μA. The sizing methodology boils down to three steps:

1. Select a resistor with a low temperature coefficient of resistance (TCR);
2. Size transistors M_{1-2} to minimize the TC of I_{REF};
3. Tune R to reach the current reference target in TT.

Note that, similarly to the PTAT current reference, we choose to invert the topology depicted in Fig. 4.1(a). First, at step 1), selecting a resistor with a low TCR

Table 4.3 Resistor properties in the XFAB 0.18-μm PD-SOI technology. Density is measured at 25°C and TC is characterized over the -40-to-125°C temperature range, and both characteristics are normalized to the lowest obtained value. All the resistors have a width of 2 μm and a length of 10 μm.

Resistor type	N+			P+		
	diff.	poly.	poly. (high res.)	diff.	poly.	poly. (high res.)
Normalized density	**1**	5.22	**100.98**	1.23	4.54	16.28
Normalized TCR	13.61	12.77	**34.92**	39.58	**1**	7.86

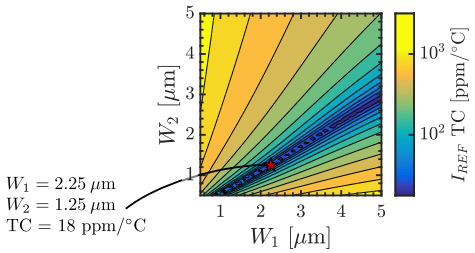

Fig. 4.5 Current reference TC in the -40-to-125°C range, as a function of transistor widths W_1 and W_2. The red star indicates the chosen design point. TC is computed as explained in Section 4.1.3.

is desirable to avoid the 2T voltage reference from compensating large and highly nonlinear resistance variations, which would lead to a poor TC of I_{REF}. Table 4.3 summarizes the properties of the available resistors, namely their density and their TCR, computed as

$$\text{TCR} = \frac{(R_{\max} - R_{\min})}{R(25°\text{C})\,(T_{\max} - T_{\min})}. \tag{4.11}$$

P+ poly resistors, i.e., poly over a p-type-doped substrate, present the lowest normalized TCR values, with 1 and 7.86 for the regular and high resistance flavors, respectively. A regular P+ poly resistor (`rpp1`) is selected for its low TCR, despite its modest normalized density of 4.54. Next, the objective of step 2) is to size M_{1-2} to minimize the TC of I_{REF}. For the 2T voltage reference to operate properly, (4.1) highlights the need for M_1 to have a larger threshold voltage than M_2, which is why an RVT and LVT pMOS are chosen. The length of both transistors being fixed to 5 μm to reach a competitive LS, Fig. 4.5 demonstrates that the TC of I_{REF} is minimized by a W_2/W_1 ratio of 0.56, as suggested by (4.9). Widths of 2.25 and 1.25 μm are selected for M_1 and M_2, on the grounds of variability, giving a TC of 18 ppm/°C. Finally, step 3) simply consists in tuning the value of the resistance to reach the 1-μA target. Transistors M_{3-4} can be easily sized, with the main limitations being that in all PVT corners, M_3 must ensure that M_1 remains saturated, and V_{SG4} must be larger than $4U_T$ for the current mirror to operate properly.

Nevertheless, the ratio W_2/W_1 leading to the minimum TC is process-dependent. A calibration mechanism, represented in Fig. 4.6, is consequently implemented by

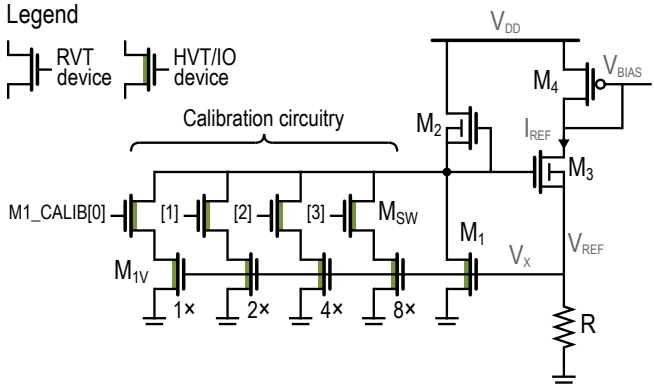

Fig. 4.6 A 4-bit TC calibration scheme is implemented by changing the width of M_1 and thus the ratio W_2/W_1.

Table 4.4 Sizing of the μA-range CWT current reference, without and with TC calibration, in XFAB 0.18-μm PD-SOI.

		w/o TC calib.		w/ TC calib.	
	Type	W [μm]	L [μm]	W [μm]	L [μm]
M_1	RVT pMOS	4×2.25	5	12×0.8	5
M_{1V}	RVT pMOS	/	/	1 - 8×0.8	5
M_{SW}	RVT pMOS	/	/	0.22	5
M_2	LVT pMOS	4×1.25	5	4×2	5
M_3	LVT pMOS	10×10	1	10×10	1
M_4	LVT nMOS	10×10	1	10×10	1
R	P+ poly.	0.45	26×13.1	0.45	26×11.9

tuning the width of M_1 with a 4-bit control signal. This allows to change W_2/W_1 from 0.37 to 0.83, leading to a TC for I_{REF} in the 10-to-30-ppm/°C range in most process corners, as will be shown in Section 4.1.3.2. To conclude, the chosen transistor sizes for the CWT current reference without and with calibration are summed up in Table 4.4.

4.1.3 Simulation and Measurement Results

This section presents the simulation and measurement results for the three current references fabricated in XFAB 0.18-μm PD-SOI, which behaves like a conventional bulk technology because it does not suffer from floating-body effects. Their layouts are shown in Fig. 4.7, together with the chip microphotograph. Simulations are performed post-layout, to account for non-idealities due to layout effects and parasitic diodes. Current measurements are carried out with a Keithley 2636A source meter, connected to the PCB including the chip through triaxial cables. The PCB is placed in an Espec SH-261 climatic chamber, in which temperature is swept from -40 to 85°C by steps of 5°C while leaving humidity uncontrolled. Temperature is limited

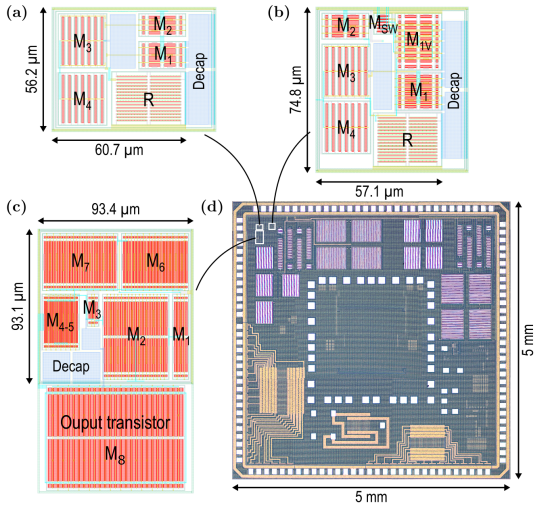

Fig. 4.7 Chip microphotograph and layout of the current references in XFAB 0.18-μm PD-SOI: μA-range CWT current reference (a) without and (b) with calibration, (c) nA-range PTAT current reference and (d) 25-mm^2 0.18-μm PD-SOI chip microphotograph.

to 85°C as some pieces of equipment cannot withstand higher temperatures.

In what follows, the LS and TC are computed using the box method following (1.2) and (1.4), as discussed in Chapter 1.

4.1.3.1 nA-Range PTAT Current Reference

Post-layout simulation results are represented in Figs. 4.8 and 4.9. First, as discussed in Section 4.1.1.1, the LS can be predicted by (4.5). With $S_{I_{REF}} = 5.14$ %/mV given by the design point and the LS of V_{REF} equal to 0.37 mV/V, as shown in Fig. 4.8(b), (4.5) predicts an LS of 1.90 %/V. Figs. 4.8(a) and (b) display that $V_{DD,min}$ is around 0.55 V and is limited by the minimum voltage required to bias the 2T voltage reference. The LS is 2.21 %/V from 0.55 to 1.8 V in TT, which is larger than the 1.90-%/V prediction as it does not account for the supply voltage dependence coming from the current mirror biasing the SCM. In addition, LS is relatively stable among process corners and is mainly impacted by process variations of I_{REF}, i.e., +14.5 % in FF and -11.6 % in SS. Thus, the worst-case LS is 2.93 %/V in FS. Next, the variability of I_{REF} can be linked to $\sigma_{V_{REF}} = 0.42$ mV through (4.6), giving a prediction of 2.16 %. Again, this value is lower than the simulation result of 2.78 % exhibited in Figs. 4.8(c) and (d), as the local mismatch in the SCM and the current mirror has not been accounted for. Finally, Fig. 4.9 depicts the temperature dependence of the PTAT current reference. Fig. 4.9(a) highlights that I_{REF} is approximetaly linear with temperature up to 100°C in TT. Above it, nonlinearities induced by leakage in parasitic nwell/psub diodes appear. This translates to a 0.92-%/°C TC for I_{REF} between -40 and 125°C in TT. Fig. 4.9(b) confirms the PTAT behavior of

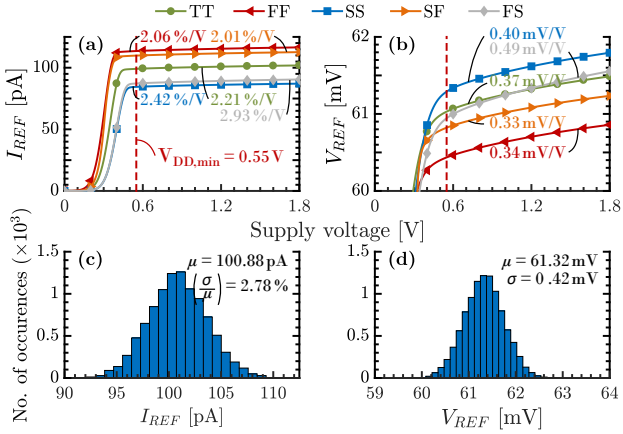

Fig. 4.8 Simulated nA-range PTAT current reference (a) I_{REF} and (b) V_{REF} as a function of supply voltage, in all process corners and at 25°C. Histograms of (c) I_{REF} and (d) V_{REF} for 10^4 Monte-Carlo runs in nominal conditions, i.e., in TT, at 1.2 V and 25°C.

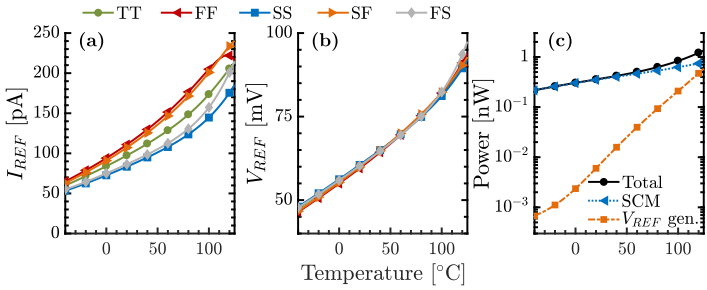

Fig. 4.9 Simulated temperature dependence of (a) I_{REF} and (b) V_{REF} in all process corners and at 1.2 V. (c) Power breakdown between the SCM and the 2T voltage reference in TT, as a function of temperature.

V_{REF}. Fig. 4.9(c) demonstrates that power consumption is linear with temperature below 60°C, and is dominated by the SCM which draws a current proportional to I_{REF}. Then, power increases exponentially with temperature due to the 2T voltage reference, whose power consumption scales with drain-to-source leakage. Finally, the startup time in typical conditions is 238 ms [Fig. 4.18(a)].

Measurement results are presented in Figs. 4.10 and 4.11. In what follows, the reference current is measured as the drain current of M_8 [Fig. 4.7(c)], divided by a fixed ratio of 36.4, obtained from nominal simulations. Firstly, Fig. 4.10(a) shows the average I_{REF} as a function of V_{DD}, and only differs from post-layout simulations by a small overshoot at 0.5 V. Regarding power consumption [Fig. 4.10(c)], the measured value is larger than the simulated one by roughly 2× due to additional leakage in the 2T voltage reference, but a minimum power of 0.28 nW is reached at 0.55 V. Moreover, details of the 10 measured dies are provided in Figs. 4.10(b)

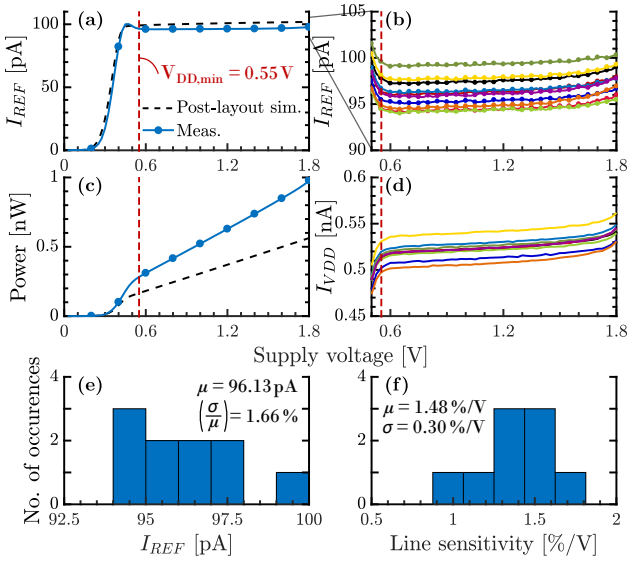

Fig. 4.10 Measured average (a) I_{REF} and (c) power consumption vs. V_{DD} at 25°C, with (b)-(d) details of the 10 dies, for the nA-range current reference. Histograms of (e) I_{REF} and (f) LS across the 10 dies.

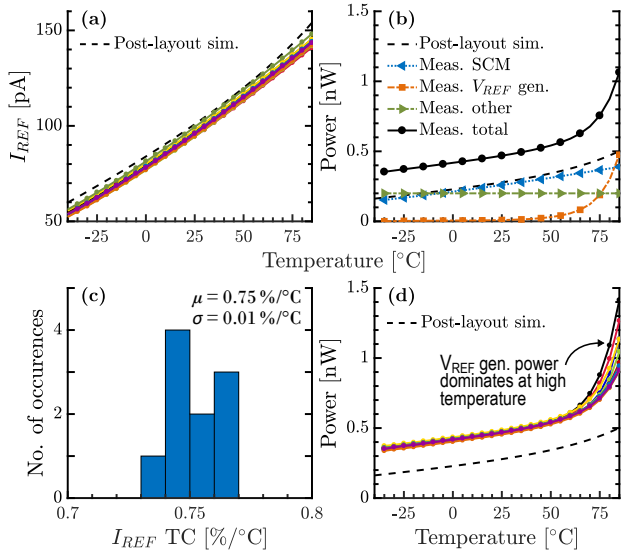

Fig. 4.11 Measured temperature dependence of (a) I_{REF} and (d) power consumption at 0.9 V, for all 10 dies. (b) Power breakdown between the SCM and the 2T voltage reference. (d) Histogram of TC across the 10 dies.

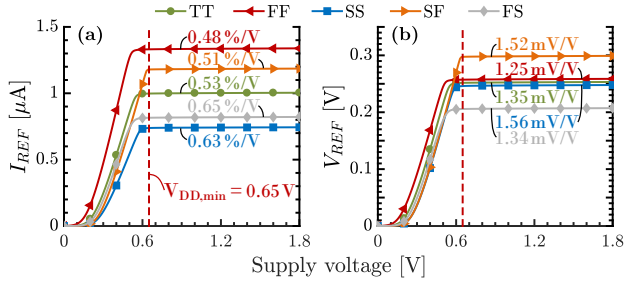

Fig. 4.12 Simulated µA-range CWT current reference (a) I_{REF} and (b) V_{REF}, as a function of supply voltage, in all process corners and at 25°C.

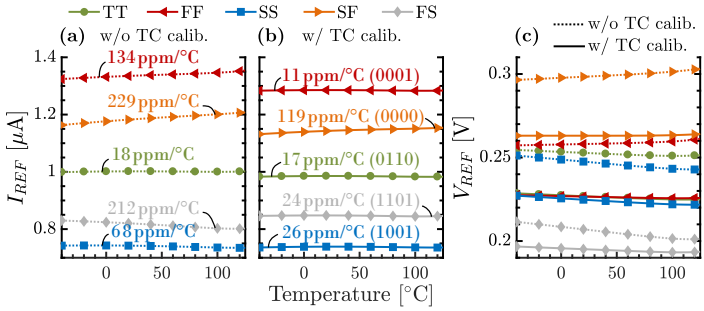

Fig. 4.13 Simulated temperature dependence of I_{REF} (a) without and (b) with TC calibration, and (c) V_{REF}, in all process corners and at 1.2 V.

and (d). Then, the variability of I_{REF} across the 10 dies is depicted in Fig. 4.10(e), with an average and (σ/μ) equal to 0.096 nA and 1.66 %, compared to 0.101 nA and 2.78 % in simulation. Given that in Fig. 4.10(f), the average LS (1.48 %/V) is also lower than in simulation (2.21 %/V), we hypothesize that both observations are explained by a lower-than-expected sensitivity $S_{I_{REF}}$. Finally, Fig. 4.11(a) illustrates the temperature dependence of I_{REF} for all 10 dies, which closely matches the post-layout simulations. The measured average TC is 0.75 %/°C from -40 to 85°C [Fig. 4.11(c)], with a standard deviation of 0.01 %/°C. Regarding power consumption, Fig. 4.11(b) highlights that the increase from simulation to measurement comes from a temperature-independent current, which could possibly originate from the 2T voltage reference. Furthermore, we observe in Fig. 4.11(d) that the 2T voltage reference power becomes dominant above 60°C, and leads to a larger growth than in TT simulations.

4.1.3.2 µA-Range CWT Current Reference

Post-layout simulation results are shown in Figs. 4.12 to 4.14. First, Figs. 4.12(a) and (b) depict I_{REF} and V_{REF} as a function of V_{DD}. Similarly to the PTAT reference, they highlight that $V_{DD,min}$ is limited by the 2T voltage reference and is equal to 0.65 V. From (4.5), we know that LS is inversely proportional to the intrinsic gain

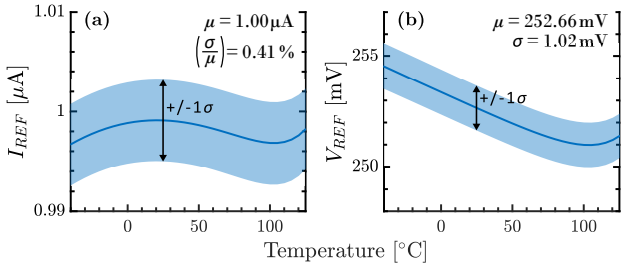

Fig. 4.14 Simulated temperature dependence of (a) I_{REF} and (b) V_{REF} with $\pm 1\sigma$, for 10^4 Monte-Carlo runs in TT and at 1.2 V.

g_m/g_d. Given the large g_m/g_d in this technology [166], an LS of 0.53 %/V is reached in TT from 0.65 to 1.8 V, with the worst-case LS corresponding to 0.65 %/V in FS. Besides, I_{REF} is strongly impacted by process variations, with +33.3 % in FF and -25.6 % in SS. Furthermore, the temperature dependence of I_{REF} and V_{REF} is represented in Fig. 4.13 without and with TC calibration. Fig. 4.13(a) illustrates that without TC calibration, an excellent TC of 18 ppm/°C is obtained in TT, but it degrades in skewed corners with 229 ppm/°C PTAT in SF and 212 ppm/°C CTAT in FS, due to a change of temperature dependence of V_{REF} [Fig. 4.13(c)]. Nevertheless, Fig. 4.13(b) demonstrates that a simple 4-bit calibration of the W_2/W_1 width ratio [Fig. 4.6] can reduce the TC below 30 ppm/°C in all process corners except for SF, in which the 119 ppm/°C PTAT TC would require a slightly larger tuning range. Lastly, in Fig. 4.14(a), I_{REF} presents a 2nd order temperature dependence below 100°C, and leakage leads to a current increase above this limit. Moreover, the (σ/μ)'s of I_{REF} and V_{REF} are equal, as stated by (4.6), and amount to 0.41 % [Figs. 4.14(a) and (b)], featuring a perfect match between theory and simulations. Regarding I_{REF}, its average value is 1 μA at 25°C, and its average TC reaches 14.9 ppm/°C, with a variability of 2.14 %. Lastly, the startup time is 5 ms in typical conditions [Fig. 4.18(b)]. This is a limitation of the proposed reference as a μA-range current would likely need to be shut down in sleep mode, and a 5-ms startup time does not allow for duty cycling to be used in all applicative contexts. The startup time of the reference is limited by the transient behavior of the 2T voltage generator, and the proposed architecture does not allow to keep it always on while shutting down the current generation structure due to the feedback loop between both structures through source-follower transistor M_3.

Measurement results are summarized in Figs. 4.15 to 4.17. As the TC of I_{REF} is mostly impacted by process variations rather than local mismatch, we select the optimal code by sweeping all 16 calibration codes on a single die from -40 to 85°C, as shown in Fig. 4.15(a). Alternatively, a two-point calibration at 0 and 85°C would yield a similar result, as illustrated in Fig. C.1 in Appendix C. Because we are using a voltage reference with pMOS devices for M_{1-2} and the control switches, increasing the calibration code decreases the actual W_1, thus reducing the PTAT part of

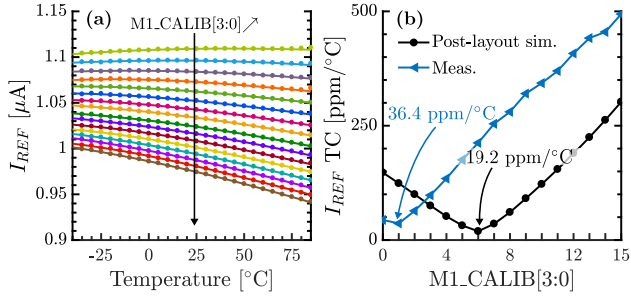

Fig. 4.15 Measured (a) temperature dependence of I_{REF} at 0.9 V, for all 16 calibration codes on a single die, for the μA-range current reference. (b) I_{REF} TC obtained for each calibration code, in TT post-layout simulations and in measurement.

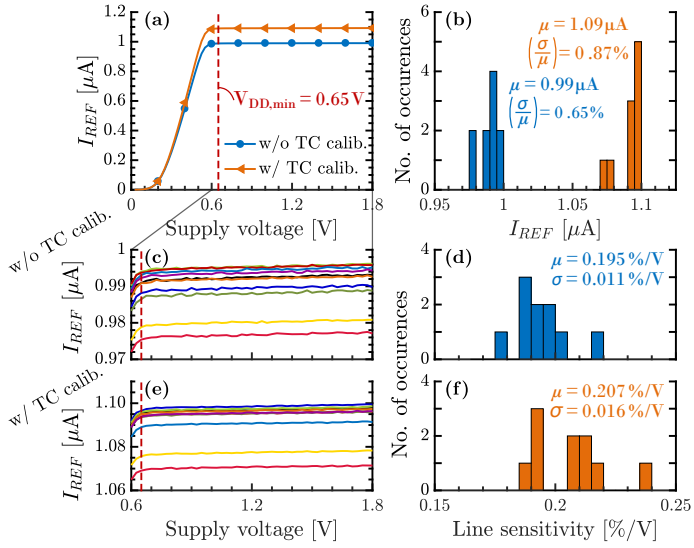

Fig. 4.16 Measured (a) average I_{REF} vs. V_{DD}, and details of the 10 dies (c) without and (e) with TC calibration, at 25°C. Histograms of (b) I_{REF} and LS (d) without and (f) with TC calibration, across the 10 dies.

V_{REF} and boosting the CTAT behavior of I_{REF}. Based on Fig. 4.15(b), we select a code of 0x0001 with a 36.4-ppm/°C TC, which is different from the simulated one, here 0x0110 with a 19.2-ppm/°C TC, likely due to process variations. Next, Fig. 4.16(a) shows the average I_{REF} behavior with supply voltage, with a $V_{DD,min}$ at 0.65 V and a slight increase of I_{REF} from 0.99 to 1.09 μA due to TC calibration [Fig. 4.17(b)]. In both cases, the average LS is around 0.20 %/V, which represents a 2.7× reduction compared to simulations and could result from a larger g_m/g_d. Variability reaches 0.65 % and 0.87 % without and with TC calibration [Fig. 4.16(b)]. The larger value compared to 0.41 % in simulation likely comes from the yellow and

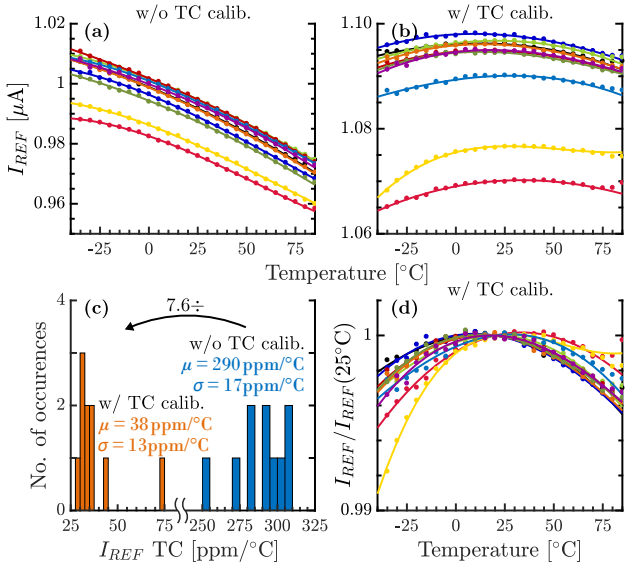

Fig. 4.17 Measured temperature dependence of I_{REF} (a) without TC calibration, (b) with TC calibration and (d) with TC calibration and normalization, at 0.9 V. (c) Histogram of I_{REF} TC across the 10 dies.

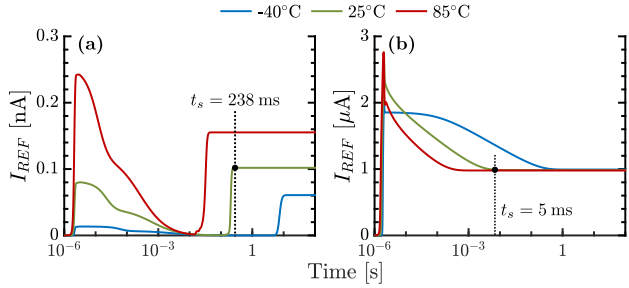

Fig. 4.18 Simulated startup waveforms of the (a) PTAT nA-range and (b) CWT μA-range current references in the TT process, with a 1.8-V and 1-μs rise time supply voltage.

red curves on the bottom of Figs. 4.16(c) and (e), which appear to be outliers leading to an overestimation of (σ/μ). To conclude, the temperature dependence of I_{REF} is represented in Figs. 4.17(a) and (b). On one side, without calibration, I_{REF} presents a CTAT behavior leading to a TC of 290 ppm/°C in the -40-to-85°C range. On the other side, with calibration, the TC reduces down to 38 ppm/°C, corresponding to a 7.6× improvement. In Figs. 4.17(b) and (d), we observe a 2nd order temperature dependence below 70°C, as predicted by simulations. A small current surge above this limit comes from the power consumption of the 2T voltage reference, which is measured together with the reference current, but is not taken into account in the TC.

4.1.4 Implementation in Scaled Technologies

Novel current references are often developed in the 0.18-μm technology node or above. However, their portability to common scaled technologies such as 65-nm bulk, 28-nm fully-depleted SOI (FD-SOI), or 14-nm FinFET, is hardly discussed and poses a series of challenges. This section details these challenges and how they can be overcome for the proposed family of current references by focusing on the implementation of the 2T voltage reference.

4.1.4.1 Leakage-Induced Non-Idealities

A PTAT voltage reference, implemented with pMOS devices in 65-nm bulk, is used to highlight the non-idealities of the 2T voltage reference. In Fig. 4.19(a), we note an increase of the reference voltage below 0°C in the slow pMOS process corners (SS and FS). A similar yet weaker behavior can be observed below -20°C in TT. Fig. 4.19(b) depicts the transconductance efficiency g_m/I_D and the ratio between gate and drain currents I_G/I_D, for a zero-V_{GS} pMOS in SS, as a function of temperature. The non-ideal behavior noticed in Fig. 4.19(a) coincides with a drop in g_m/I_D, which should increase at low temperature as the transconductance efficiency in deep subthreshold is proportional to $(g_m/I_D)_{max} = 1/(nU_T)$. As gate leakage has increased by several orders of magnitude from 0.18-μm to 65-nm [36, 167], this drop can be explained by an increased I_G/I_D ratio, coming from the fact that the current flowing in the 2T voltage reference is a drain-to-source leakage, decreasing exponentially with a temperature reduction, while the gate leakage remains approximately constant with temperature. I_G thus becomes non-negligible, reaching 6.5 % of I_D at 0°C in SS. Two tuning knobs can be used to mitigate this non-ideal behavior: the transistor type and sizes. First, Fig. 4.20(a) illustrates the impact of the transistor type using the same kind of curves as Fig. 4.19(b). It points out that increasing the threshold voltage from LVT to high-V_T (HVT) degrades the voltage reference behavior by shifting the point at which g_m/I_D drops, corresponding to an I_G/I_D around 1 to 5 %, to higher temperature. LVT devices are thus selected to implement the voltage reference, to ensure functionality at low temperature at the cost of an increased power consumption at high temperature. Second, Fig. 4.20(b) depicts the evolution with the transistor sizes of the ratio between g_m/I_D at zero V_{GS} and $(g_m/I_D)_{max}$. A length increase degrades this ratio, as it linearly increases I_G by expanding the gate area, while simultaneously decreasing I_D as $1/L$. A width increase has a limited impact, because at first order, I_G and I_D both increase linearly with it. Nevertheless, Fig. 4.20(b) shows that 2$^{\text{nd}}$ order effects also come into play. Based on this figure, we select a design point with a g_m/I_D at zero V_{GS} equal to 91.2 % of $(g_m/I_D)_{max}$, corresponding to $W = 0.3\,\mu$m and $L = 6\,\mu$m. We could select a shorter length to further mitigate the non-ideal behavior of the voltage reference, but only at the cost of a larger LS and power consumption.

Moreover, we argue that the g_m/I_D drop is a useful technology indicator for

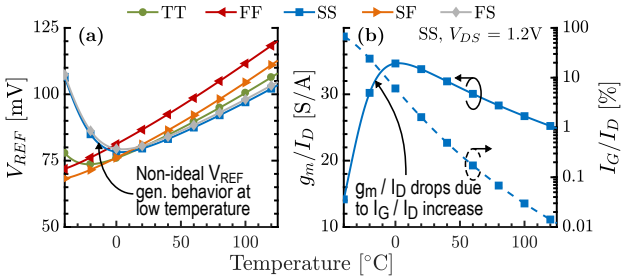

Fig. 4.19 Temperature dependence of (a) a PTAT voltage reference implemented with pMOS devices in 65-nm bulk and (b) the g_m/I_D and I_G/I_D of a zero-V_{GS} pMOS transistor in the SS process corner with $V_{DS} = 1.2$ V.

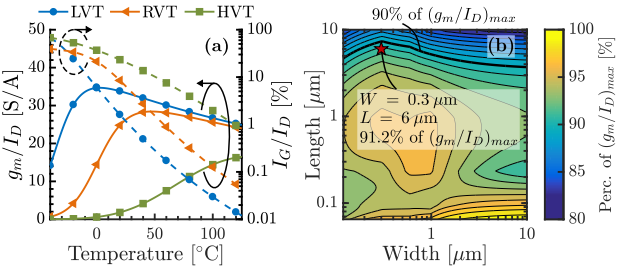

Fig. 4.20 For a 65-nm zero-V_{GS} pMOS in SS, (a) impact of the transistor flavor on the g_m/I_D and I_G/I_D curves vs. temperature, and (b) at 0°C, fraction of $(g_m/I_D)_{max}$ obtained at zero V_{GS} depending on the transistor sizes, with $(g_m/I_D)_{max}$ the maximum of the g_m/I_D vs. V_{GS} curve.

design as it captures various leakage sources degrading the voltage reference behavior. Indeed, in 65-nm bulk, the drop can be explained by the impact of gate leakage. Yet, in 0.18-μm PD-SOI and 28-nm FD-SOI, gate-induced drain leakage (GIDL) prevails, as the gate leakage is limited by the use of thick oxide and high-κ gates, respectively. Monitoring the g_m/I_D drop allows to capture any such effects, regardless of their origin, and makes it possible to size the voltage reference without thoroughly investigating them.

4.1.4.2 *Line Sensitivity Enhancement Techniques*

As stated in (4.4), the LS of the reference voltage is inversely proportional to the intrinsic gain, which is getting worse with each technology node as a result of increased output conductance [166]. In addition, the problem posed by gate leakage and GIDL at low temperature does not allow to select a maximum-length transistor, which would have lead to a large g_m/g_d and thus a lower LS. While this issue is not critical in 28-nm FD-SOI, as the intrinsic gain is larger than in bulk technologies [37], it significantly degrades the LS in 65-nm bulk. Therefore, several LS enhancement techniques are proposed in Fig. 4.21: (a) stacking, (b) stacking with a shared body bias (SBB), and (c) hybrid stacking. These techniques are illustrated for nMOS

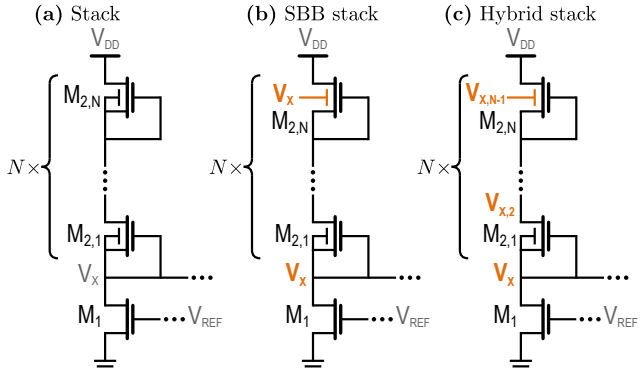

Fig. 4.21 Line sensitivity enhancement techniques, illustrated here for nMOS topologies, using (a) stacking, (b) stacking with a shared body bias (SBB), and (c) hybrid stacking. The different body voltages in (b) and (c) are self-generated by the stack.

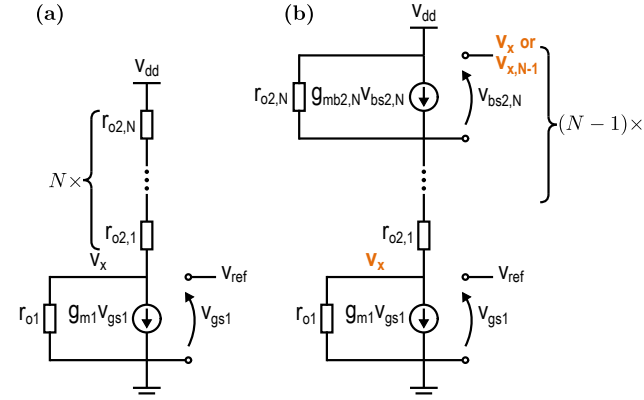

Fig. 4.22 Small signal schematics of the LS enhancement circuits depicted in Fig. 4.21, based on (a) stacking and (b) SBB/hybrid stacking.

topologies, albeit subsequent simulation results correspond to pMOS implementations, which limit the area overhead of using different body voltages by relying on nwells rather than on DTI or triple-well devices. Fig. 4.23 compares the various LS enhancement techniques to the basic solution, using a single transistor for M_2 and reaching an LS of 8.5 mV/V. First, employing a stack of N devices with their body tied to their source [Figs. 4.21(a) and 4.22(a)], the LS is expressed as

$$\frac{v_{ref}}{v_{dd}} = \frac{\frac{g_{d2,1}}{N}}{g_{m1} + g_{d1} + \frac{g_{d2,1}}{N}} \simeq \frac{g_{d2,1}}{g_{m1}} \frac{1}{N}, \tag{4.12}$$

under the assumptions that $g_{m1} \gg g_{d1}$, $g_{d2,1}$ and $v_x = v_{ref}$. The LS decrease does not exactly scale as $1/N$, because the small signal parameters are impacted by the change of operation point due to stacking. Nevertheless, Fig. 4.23 shows an im-

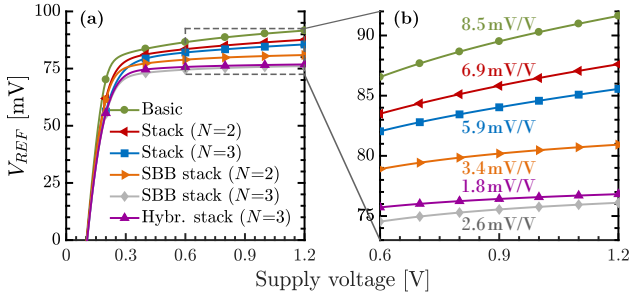

Fig. 4.23 Comparison of the various LS enhancement techniques for a PTAT voltage reference implemented with 6-μm-length LVT pMOS devices in 65-nm bulk. The LS is measured from 0.6 to 1.2 V at 25°C.

proved LS of 6.9 and 5.9 mV/V for a stacking of $N = 2$ and 3 devices. Second, the LS using SBB stacking [Figs. 4.21(b) and 4.22(b)], i.e., all bodies tied to V_X, or hybrid stacking [Figs. 4.21(c) and 4.22(b)], i.e., the body of $M_{2,n}$ tied to the source of $M_{2,n-1}$, is expressed as

$$\frac{v_{ref}}{v_{dd}} \simeq \frac{g_{d2,1}}{g_{m1}+g_{d1}} \frac{g_{d2,2}}{g_{mb2,2}+g_{d2,1}+g_{d2,2}},$$
$$\frac{v_{ref}}{v_{dd}} \simeq \frac{g_{d2,1}}{g_{m1}+g_{d1}} \frac{g_{d2,2}}{g_{mb2,2}+g_{d2,1}+g_{d2,2}} \frac{g_{d2,3}}{g_{mb2,3}+g_{d2,3}},$$

for stacks of $N = 2$ and 3 devices, respectively. SBB and hybrid are equivalent for $N = 2$ and lead to an LS of 3.4 mV/V, thanks to the second factor related to the body effect of $M_{2,2}$. Then, SBB and hybrid differ for $N = 3$, reaching a 2.6- and 1.8-mV/V LS, respectively. This difference comes from increased $g_{d2,1}$ and $g_{d2,2}$ in the SBB stack, arising from a V_{DS} lower than $4U_T$ for both $M_{2,1}$ and $M_{2,2}$. On the other hand, $M_{2,2}$ is saturated in the hybrid stack, lowering $g_{d2,2}$ and improving the LS. An hybrid stack with three devices is thus selected to implement the voltage reference.

Table 4.5 Comparison table of CWT (left) and PTAT (right, with TC highlighted in green) nA-range current references.

	Cordova [89]	Dong [93]	Far [96]	Hirose [100]	Huang [66]	Huang [41]	Ji [39]	Kayahan [94]	Kim [64]	Wang [67]	Wang [40]	Camacho [27]	Camacho [28]	**Lefebvre This work**		
Publication	ISCAS	ESSCIRC	ROPEC	ESSCIRC	ISCAS	TCAS-II	ISSCC	TCAS-I	ISCAS	VLSI-DAT	TCAS-I	TCAS-II	ISCAS	TCAS-I		
Year	2017	2017	2015	2010	2010	2020	2017	2013	2016	2019	2019	2005	2008	2022		
Type of work	Sim.	Silicon	Sim.	Silicon	Sim.	Silicon	Silicon	Silicon	Sim.	Silicon	Silicon	Silicon	Silicon	Silicon	Sim.◂	Sim.◂
Number of samples	N/A	32†	N/A	15	N/A	10	10	90	N/A	10	16	10	30	10	N/A	N/A
Technology	0.18μm	0.18μm	0.18μm	0.35μm	0.18μm	0.18μm	0.18μm	0.35μm	0.13μm	0.18μm	0.18μm	1.5μm	0.18μm	0.18μm PD-SOI	65nm	28nm FD-SOI
I_{REF} [nA]	10.86	35.02	14	9.95	2.05	11.6	6.64	25	27	6.46	9.77	0.41	0.9	0.096	0.22	0.2
Power [nW]	30.5 @0.9V	1.02 @1.5V	150 @1V	88.53 @1.3V	5.1 @0.85V	48.64 @0.8V	9.3 @N/A	28500 @5V	N/A	15.8 @0.85V	28 @0.7V	2 @1.1V	2.34 @0.65V	0.282 @0.55V	0.80 @0.7V	0.68 @0.74V
Area [mm^2]	0.01	0.0169	0.0102	**0.12**	N/A	0.054	0.055	**0.0053**	N/A	0.062	0.055	0.045	0.01	**0.0087**	**0.0054**	**0.0029**
Supply range [V]	0.9 – 1.8	**1.5** – 2.5	1 – 3.3	**1.3** – 3	0.85 – 2.2	0.8 – 2	**1.3** – 1.8	N/A	1.2	0.85 – 2	**0.7** – 1.2	1.1 – 3	**0.65** – 2	**0.55** – 1.8	**0.7** – 1.2	**0.74** – 1.8
LS [%/V]	**0.54**	3	**0.1**	**0.046**	1.35	1.08	1.16	**150**	N/A	**4.15**	**0.6**	3.5/**6***	**0.2**	1.48	**4.43**	**0.78**
Temperature range [°C]	-20 – 120	-40 – 120	0 – 70	-20 – 80	0 – 150	-40 – 120	0 – 110	0 – 80	-30 – 150	-10 – 100	-40 – 125	-20 – 70	-70 – 130	-40 – 85	0 – 85	-20 – 85
TC [ppm/°C]	108	282	**20**	1200	**91**	169 ‡	680/283◁	128 (sim.)	327	138▷	149.8	470/**2500***	**3000**	**7500**	**2930**	**1095**
I_{REF} var. (process) [%]	15.8	4.7	N/A	N/A	7.5	+17.6/-10.3◇	N/A	8/1.22*	3.7	N/A	+11.7/-8.7	N/A	N/A	+14.5/-14.6	+25.1/-2.0	+5.3/6.3
I_{REF} var. (mismatch) [%]	**11.6***	**1.6**	5.8	**14.1**	N/A	4.3	4.07/**1.19***	**1.4** (sim.)	N/A	3.33	**1.6**	**10**	2.67	**1.66**	2.59	4.06
Trimming type	6b for V_S gen.	N/A	N/A	3b for I_N/I_P sub.	N/A	6b for TC/V_{REF}	N/A	N/A	N/A	N/A	5b for SCM width	N/A	N/A	N/A	N/A	N/A
Complexity	25T	>**4T+2C**	31T	**52T**	**10T**	**23T+4C+2R**	>18T+1R	11T+1R	**7T+1R**	12T	**23T+2C+2R**	**10T**	16T+1C	**7T**	**9T**	**8T**
Special components	Native	No	No	No	No	Res.	Res., **1BJT**	Res.	Res.	No	Res.	No	No	No	No	No

* Simulation and measurement results. ⋆ Variability is due to the combined effects of process and mismatch variations. It is equal to 15.8 % for the untrimmed current reference and 11.6 % for the trimmed one. † 16 dies for the TT process corner and 4 dies for each of the FF, SS, SF and FS process corners.
‡ Average of the measurement results. ◇ Estimated from Fig. 3 of [41]. ◁ Untrimmed and trimmed results. ▷ Minimum of the measurement results.
◂ In this work, simulations refer to post-layout simulations including parasitic diodes.

Table 4.6 Comparison table of μA-range temperature-independent current references.

	Azcona [57]	Bendali [83]	Crupi [91]	Eslampanah [168]	Fiori [63]	Lee [134]	Liu [114]	Osipov [60]	Serrano [129]	Wang [35]	Wu [106]	Yang [105]	Yoo [95]	**Lefebvre This work**		
Publication	ISCAS	TCAS-I		ISCAS	TCAS-II	JSSC	ISCAS	TCAS-I	JSSC	TVLSI	CICC	ASSCC		TCAS-I		
Year	2014	2007	2017	2017	2005	2012	2010	2019	2008	2017	2015	2009	2007	2022		
Type of work	Sim.	Silicon	Silicon	Silicon	Sim.	Silicon	Sim.	Silicon	Silicon	Silicon	Silicon	Silicon	Silicon	Silicon	Sim.[▷]	Sim.[▷]
Number of samples	N/A	19	45	5	N/A	10	N/A	10	N/A	12	N/A	N/A	N/A	10	N/A	N/A
Technology	0.18μm	0.18μm	0.18μm	0.18μm	0.35μm BiCMOS	0.18μm	0.18μm	0.35μm	0.5μm	65nm	0.18μm	0.35μm	0.25μm	0.18μm PD-SOI	65nm	28nm FD-SOI
I_{REF} [μA]	0.5	144.3	0.34	1.5	13.65	7.81	10	1.05	16 – 50	9.42	20	16.5	10.45	0.99 / 1.09	1	1
Power [μW]	1.98 @1.2V	83 @1V	0.21 @0.45V	1.38 @0.8V	68.25 @2.5V	1.4 @1V	80 @2V	3.8 @2V	N/A	7.18 @1.4V	48 @2.4V	N/A	77 @1.1V	0.64 / 0.71 @0.65V	0.68 @0.7V	0.80 @0.8V
Area [mm^2]	N/A	**0.213**[⋆]	**0.00075**	0.003	0.0042	0.023	N/A	0.057	0.06[◁]	**0.089**	0.005	0.0576	**0.002**	0.0034 / 0.0043	**0.002**	**0.00044**
Supply range [V]	1.2 – 3	1	**0.45** – 1.8	**0.8** – 2	**2.5**	1 – 1.2	2 – 3	2 – 3.6	**2.3** – 3.3	1.3 – 2.5	**2.4** – 3	2 – 3.3	1.1 – 3	**0.65** – 1.8	**0.7** – 1.2	**0.8** – 1.8
LS [%/V]	0.69	N/A	**3.9**	N/A	**0.4**	N/A[◇]	3	2.73	<1	**0.018**	0.5	N/A	**0.17**	**0.20 / 0.21**	**4.38**	0.57
Temperature range [°C]	-40 – 120	0 – 100	0 – 80	-40 – 110	-30 – 100	0 – 100	-20 – 120	-45 – 125	0 – 80	-30 – 90	-40 – 80	-20 – 100	0 – 120	-40 – 85	0 – 125	-40 – 125
TC [ppm/°C]	119	185	**578**	**571**	**28**	**24.9**	170	143 (min.) 247 (avg.)	<130	**86 (min.)** 119 (avg.)	130	280[⋆]	**720**	290 / **38**[◀]	**37.33**[▶]	**38.42**[▶]
I_{REF} var. (process) [%]	1.3[⋆]	7[†]	N/A	8.5	N/A	4.5	2.14[‡]	N/A	N/A	5.13	N/A	0.52[⋆]	N/A	+33.3/-25.9	+46.7/-22.6	+9.8/-10.1
I_{REF} var. (mismatch) [%]	N/A		2.7[‡]	N/A	N/A	N/A		3.9	**<0.02**	**0.4**	**14**	N/A	N/A	**0.65 / 0.87**	**0.68**	**0.85**
Trimming type	2b for TC 2b for I_{REF}	N/A	4b for TC 4b for I_{REF}	N/A	N/A	N/A	N/A	N/A	Floating charge for TC, I_{REF}	N/A	N/A	10b for TC 8b for I_{REF}	N/A	4b for TC	N/A	N/A
Complexity	**39T+2R**	**30T+2C+5R**	**2T**	**4T+2R**	**5T+2R**	12T+1C+2R	38T	**5T+1R**	**>26T+5C+4R**	>28T+3R	15T+2R	27T+2R	18T+3R	**4/12T+1R**	**5T+1R**	**4T+1R**
Special components	Res.	Res., **2BJT**	No	Res.	Res.	Res.	**3BJT**	Res.	Res.	Res.	Res., **2BJT**	Res., **5BJT**	Res.	Res.	Res.	Res.

[⋆] After trimming. [⋆] Estimated from the microphotograph in Fig. 6 of [83]. [†] Variability is due to the combined effects of process and mismatch variations.
[‡] Before trimming. [◇] Line sensitivity is not measured because the current reference is supplied by a bandgap reference (BGR). [◁] The total area is split between the current reference (0.015 mm^2) and the charge pumps (0.045 mm^2). [▷] In this work, simulations refer to post-layout simulations including parasitic diodes. [◀] Average of the measurement results over 10 samples.
[▶] Median of 10^4 local mismatch Monte-Carlo runs.

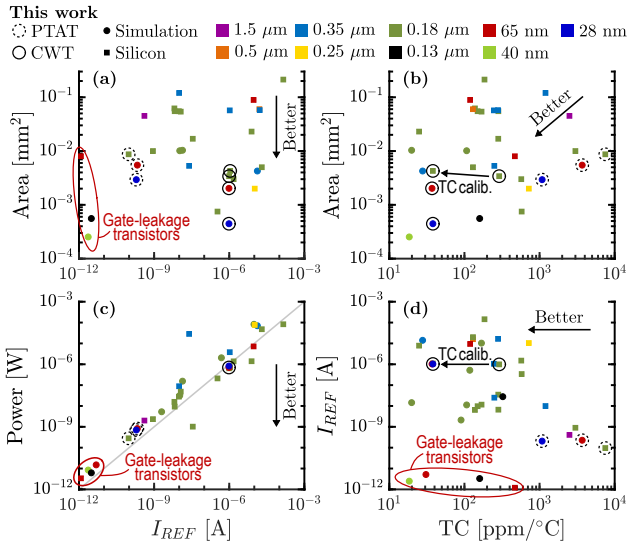

Fig. 4.24 Illustration of the trade-offs between (a) area and I_{REF}, (b) area and TC, (c) power and I_{REF}, and (d) I_{REF} and TC, based on the state of the art of nA- and μA-range current references and a few additional references.

4.1.5 Comparison to the State of the Art

This section compares our work to the state of the art of nA-range current references in Table 4.5, and μA-range temperature-independent ones in Table 4.6. These tables are complemented by Fig. 4.24, representing some of the most important trade-offs for current references. For both PTAT and CWT designs, measurements are reported for the 0.18-μm PD-SOI references. In addition, we present post-layout simulations in 0.18-μm PD-SOI, 65-nm bulk and 28-nm FD-SOI, while the vast majority of other works limit themselves to older technology nodes, typically 0.18-μm or above.

First, our PTAT design reaches the lowest current and power among nA-range references (Table 4.5), as depicted in Fig. 4.24(c), and is only outperformed by references using gate-leakage transistors. For the 0.18-μm reference, this corresponds to a 4.3× current and 7.1× power reduction compared to [27], respectively, enabled by a cut of $V_{DD,min}$ from 1.1 to 0.55 V. I_{REF} is slightly larger for the 65- and 28-nm references (0.2 / 0.22 nA), with a power consumption of 0.8 / 0.88 nW due to the larger I_{REF} and $V_{DD,min}$. Moreover, our 0.18-μm reference has the lowest $V_{DD,min}$ (0.55 V) among references in the nA range, followed by [28], [40] and our 65- and 28-nm designs in the 0.65-to-0.75-V range. Regarding LS, our 0.18-μm and 28-nm designs reach competitive values of 1.48 %/V and 0.78 %/V allowed by a large intrinsic gain in these technologies, while the 65-nm one exhibits a 4.43-%/V LS. Nonetheless, LS is significantly reduced from above 15 %/V down to 4.43 %/V as

a result of using an hybrid stack of three devices (Section 4.1.4.2). Then, the proposed topology is strikingly simple compared to other works, with only seven to nine transistors: two to four for the voltage reference and five for the SCM. Furthermore, it can be implemented with a single transistor type, and does not require any BJTs, startup circuit or trimming, thus resulting in a low silicon area ranging from 8700 μm^2 in 0.18-μm down to 2900 μm^2 in 28-nm [Fig. 4.24(a)]. Only [93] and [64] use simpler structures, but either occupy a 1.9$\times$ larger or unreported area. Speaking of area, [94] is the closest competitor, but it suffers from a prohibitive power of 28.5 μW for a reference current of 25 nA. As far as temperature range is concerned, the lower limit in 65- and 28-nm designs is due to gate leakage and GIDL, respectively, while the upper limit of 85°C shared by all designs originates from the leakage in parasitic nwell/psub diodes at high temperature. The temperature dependence of all three proposed references follows the specific sheet current, meaning that TC is not a relevant comparison criterion, but also that the main drawback of the proposed topology is that it suffers from process variations, although additional I_{REF} calibration is possible. Regarding the variability due to local mismatch, it is limited to 1.66 % in the 0.18-μm reference, which is among the lowest values reported in Table 4.5, while 65- and 28-nm references exhibit a larger variability due to a larger standard deviation of V_{REF}.

Second, our CWT current references (Table 4.6) also present a simple structure, consisting of a single resistor and four to five transistors, depending on the voltage reference implementation. Therefore, the silicon area is modest compared to other μA-range references [Fig. 4.24(a)], with 3410 / 4270 μm^2 in 0.18-μm, down to a best-in-class 440-μm^2 area in 28-nm. [91] has both a small 750-μm^2 area and a simple structure, as it relies on a 2T voltage reference to bias a transistor gate, but it suffers from degraded LS and TC, and has a limited 0-to-80°C temperature range. [168], [63] and [60] rely on a handful of components, but [168] has a large 0.003-mm^2 area, and [63, 60] require a substantial supply voltage above 2 V to operate. [95] occupies a limited 2000-μm^2 area, but its 720-ppm/°C TC is relatively poor, and the 18T+3R structure will likely lead to prohibitive variability due to local mismatch. Regarding TC, our three references feature a very low 38-ppm/°C TC for this current level [Fig. 4.24(d)], and offer one of the best trade-offs between TC and silicon area [Fig. 4.24(b)]. Other works in Table 4.6 present a low TC, such as [63] with 28 ppm/°C, which requires a 2.5-V supply voltage and consumes a considerable 68.3-μW power, and [134] with 25 ppm/°C, which necessitates a bandgap reference voltage to have a decent LS and occupies 5.3$\times$ more area than our largest design. As for other metrics, LS amounts to 0.2 %/V and 0.57 %/V in 0.18-μm and 28-nm, but increases up to 4.38 %/V in 65-nm, despite the use of an SBB stack of two devices. On one side, the lower temperature limit is -40°C, except in 65-nm where it rises to 0°C due to gate leakage. On the other side, the upper limit is 125°C, except in 0.18-μm where it is limited to 85°C by the measurement equipment. Similarly to their PTAT counterparts, our CWT references are significantly

affected by process variations, an issue that can be alleviated through a calibration of I_{REF}. Nevertheless, variability due to local mismatch is comprised between 0.65 and 0.87 %, which is among the best in the state of the art. Finally, our CWT references avoid the disadvantages of gate-leakage ones, which generate a pA-range current with limited power and area but can only be implemented in advanced technology nodes, suffer from a limited temperature range, and do not retain their area and power advantages for larger current levels.

4.1.6 Conclusion

In this first part of Chapter 4, we proposed two novel current reference topologies sharing two key ideas: (i) the generation of a voltage reference by a 2T ULP structure and (ii) its buffering onto a V-to-I converter by a single transistor. These references are fabricated in a 0.18-μm PD-SOI process. First, a nA-range PTAT current is obtained by biasing an SCM with a PTAT voltage. It generates a 0.096-nA current, the lowest to date for current references without gate-leakage transistors, while consuming only 0.28 nW at 0.55 V and 25°C. Second, a μA-range CWT current is obtained by biasing a polysilicon resistor with a matched-TC voltage. It generates either a 0.99-μA current with a 290-ppm/°C CTAT TC, or a 1.09-μA current with a 38-ppm/°C TC, using a 4-bit calibration of the 2T voltage reference width ratio. Both references exhibit a decent LS (1.48 / 0.21 %/V), a low $V_{DD,min}$ (0.55 / 0.65 V), a low variability due to local mismatch (1.66 / 0.87 %), while relying on simple 7T / 4T+1R structures without any startup circuit and occupying a limited silicon area of 8700 / 4270 μm^2. The main drawback of such architectures is their sensitivity to process variations. Furthermore, we discuss the challenges posed by gate leakage, GIDL, and declining intrinsic gain to the implementation of 2T voltages references in scaled 65- and 28-nm technologies. We demonstrate that a proper selection of the transistor type and sizes, together with the use of LS enhancement techniques, can mitigate these non-idealities.

4.2 An SCM-Based nA-Range Current Reference

In this second part of Chapter 4, we propose an area-efficient CWT current reference generating a current in the nA range and relying on an SCM biased by a four-transistor (4T) voltage reference through a 1T buffer. The 4T voltage reference provides the PTAT voltage with a CWT offset necessary to make the reference current CWT, includes a calibration mechanism to tune the TC in process corners, and removes the need for a startup circuit. Two prototypes have been fabricated in United Microelectronics Corporation (UMC) 0.11-μm bulk and GlobalFoundries (GF) 22-nm fully-depleted silicon-on-insulator (FD-SOI) CMOS technologies. The 0.11-μm (resp. 22-nm) design show a measured TC of 176 ppm/°C (resp. 82 ppm/°C) from -40 to 85°C, while occupying a silicon area of 0.0106 mm^2 (resp. 0.0026 mm^2). The rest of this section is structured as follows. Section 4.2.1 details the governing equations of the reference and presents its operation principle. Next, Section 4.2.2 discusses the design and sizing methodology, while Section 4.2.3 examines the simulation and measurement results. Finally, Section 4.2.4 compares this work to the literature while Section 4.2.5 delivers concluding remarks.

4.2.1 Governing Equations and Operating Principle

This section presents the equations governing the behavior of the two constitutive blocks of the proposed current reference, namely an SCM and a 4T voltage reference, depicted in Fig. 4.25(a) in its basic form, i.e., without calibration circuit and practical implementation details. It also details the operation principle of the reference, and explains how the limitations of our SCM-based β-multiplier reference [165] have been overcome in Section 4.2.1.3. Even though Sections 4.2.1.1 shares similarities with [165], the governing equations are slightly different due to the body connection of M_2 in Fig. 4.25(a), and we choose to detail them in this section. In what follows, the line sensitivity (LS) and TC are computed using the box method following (1.2) and (1.4), as discussed in Chapter 1.

4.2.1.1 Self-Cascode MOSFET

First, the SCM depicted in Fig. 4.25(b) relies on long-channel transistors in moderate inversion, for which a simplified model such as the analog compact MOSFET (ACM) model [156] is adequate to describe the transistor current-voltage (I-V) characteristics, with the detailed equations of this model provided in Appendix A.2. The reasoning related to the application of the ACM model to the SCM is described in Appendix B.

In existing SCM-based PTAT current references [27, 28, 169], the SCM is biased by a purely PTAT voltage V_X [Fig. 4.26(a)] and M_{1-2} operate at a fixed inversion level [Fig. 4.26(b)], thus making I_{REF} proportional to the specific sheet current I_{SQ}

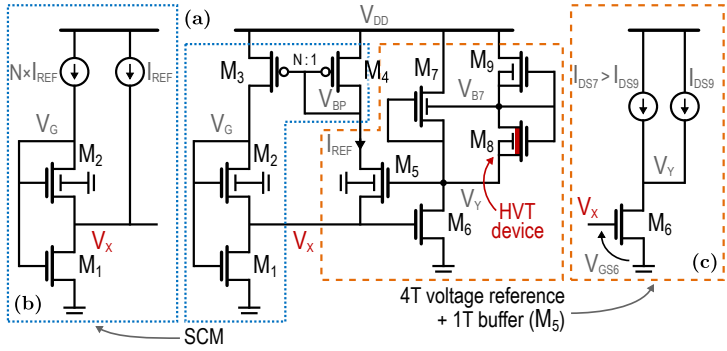

Fig. 4.25 (a) Basic schematic of the proposed current reference, which consists of (b) an SCM (M_{1-2}) biased by a pMOS current mirror (M_{3-4}), and (c) a 4T voltage reference (M_{6-9}) generating a PTAT voltage with a CWT offset, biasing the SCM through a 1T buffer (M_5).

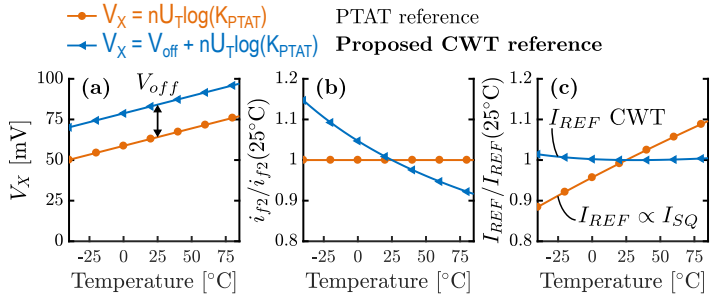

Fig. 4.26 Operation principle of PTAT references proposed in prior art [27, 28] (in orange) and of the proposed CWT reference (in blue). Analytical expression of (a) the voltage V_X applied to the SCM, (b) the inversion level of M_2, denoted as i_{f2}, and (c) the reference current I_{REF}, as a function of temperature and for V_{off} = 20 mV. Generic technological parameters n = 1.2 and m = 1.5 are selected. (b) and (c) are normalized to their value at 25°C. For the proposed CWT reference, the parameters leading to a minimum I_{REF} TC are $K_{PTAT} = 8$ and $\alpha = 1.5$.

(B.9). Therefore, I_{REF} presents a PTAT behavior dictated by T^{2-m} [Fig. 4.26(c)]. Nevertheless, to obtain an SCM-based CWT current reference such as [165], the SCM needs to be biased by a voltage of the form

$$V_X = V_{off} + nU_T \log\left(K_{PTAT}\right), \tag{4.13}$$

i.e., a PTAT voltage with a CWT offset as shown in Fig. 4.26(a), with which solving (B.7) gives an inversion level i_{f2} that decreases with temperature [Fig. 4.26(b)]. Eq. (B.9) indicates that, with a proper sizing of the SCM, the temperature dependence of I_{SQ} and i_{f2} can cancel each other out, eventually leading to a CWT reference current [Fig. 4.26(c)]. Therefore, the key principle leveraged in the proposed reference is that an SCM biased by a PTAT voltage with a CWT offset generates a temperature-independent reference current.

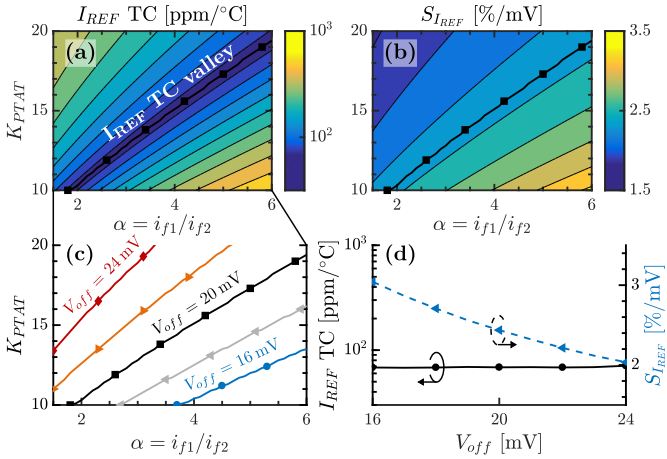

Fig. 4.27 Analytical expression of (a) the TC of I_{REF} and (b) the sensitivity $S_{I_{REF}}$, as a function of K_{PTAT} and α, for the same technological parameters as in Fig. 4.26 and V_{off} = 20 mV. (c) Location of the I_{REF} TC valley in the $(K_{PTAT}; \alpha)$ space, for V_{off} ranging from 16 to 24 mV. (d) I_{REF} TC and $S_{I_{REF}}$ as a function of V_{off}, for $\alpha = 4$ and the optimal value of K_{PTAT}.

Furthermore, Fig. 4.27 studies the impact of the bias voltage and parameter α of the SCM on I_{REF} TC and $S_{I_{REF}}$. More specifically, Figs. 4.27(a) and (b) are obtained by solving (B.7) for different values of K_{PTAT} and α, and a fixed V_{off} of 20 mV. Fig. 4.27(a) highlights that an I_{REF} TC valley is obtained for a linear relationship between K_{PTAT} and α, while Fig. 4.27(b) reveals that this valley also corresponds to an iso-$S_{I_{REF}}$ curve, meaning that sensitivity is fixed for a given CWT offset. Moreover, Fig. 4.27(c) illustrates that the location of this I_{REF} TC valley in the $(K_{PTAT}; \alpha)$ space is dependent on V_{off} and is shifted upwards for a larger offset. Finally, Fig. 4.27(d) shows that the optimal I_{REF} TC that can be reached is not dependent on V_{off}, albeit the sensitivity is improved at higher V_{off} as M_1 is biased closer to strong inversion. This improved sensitivity is however obtained at the cost of a potentially increased supply voltage.

4.2.1.2 4T Ultra-Low-Power Voltage Reference

To generate the PTAT voltage with a CWT offset required by the SCM, the proposed reference employs a novel 4T voltage reference architecture, inspired by decades of advances in 2T voltage references [22, 23, 24, 25], and sharing similarities with 4T structures introduced in [23, 90]. The transistors constituting this 4T voltage reference [Fig. 4.25(c)] operate in deep subthreshold, in which the drain-to-source current of an nMOS transistor can be described by (A.2). In addition, the proposed reference makes extensive use of the body effect, i.e., the change of threshold voltage due to a non-zero V_{BS} voltage, which is captured by

$$\Delta V_T = V_T - V_{T0} = \gamma_b \left(\sqrt{2\phi_{fp} - V_{BS}} - \sqrt{2\phi_{fp}} \right) \approx -\gamma_b^* V_{BS} \tag{4.14}$$

in a bulk technology, where γ_b is the body factor, γ_b^* its linearization around $V_{BS} = 0$, and ϕ_{fp} Fermi's potential, or by

$$\Delta V_T = V_T - V_{T0} = -\gamma_b^* V_{BS} \tag{4.15}$$

in an FD-SOI technology, for which γ_b^* is temperature-independent at first order [158]. In addition, it should be noted that in subthreshold, a common expression relating γ_b^* to the subthreshold slope factor n is given by

$$\gamma_b^* = n - 1. \tag{4.16}$$

A simple way to understand the proposed 4T voltage reference [Fig. 4.25(c)] is to see it as two drain-to-source leakage current sources, corresponding to transistors M_7 and M_9 connected with a zero V_{GS}, biasing M_6 to generate a reference voltage $V_X = V_{GS6}$. It should be noted that $I_{DS7} > I_{DS9}$ due to the 2T voltage reference formed by M_{8-9}, which leads to $V_{BS7} > 0$ and thus to a forward body biasing (FBB) of M_7, ultimately resulting in a reduction of V_{T7}. Applying Kirchhoff's current law at node V_Y gives $I_{DS6} = I_{DS7} + I_{DS9}$, and using (A.2), voltage V_X can be expressed as

$$V_X(T) = nU_T \log\left(\frac{S_9}{S_6} + \frac{S_7}{S_6}\exp\left(\frac{-\Delta V_{T7}}{nU_T}\right)\right), \tag{4.17}$$

where the decrease in threshold voltage $\Delta V_{T7} < 0$ results in a positive CWT offset V_{off}. Moreover, ΔV_{T7} can be related to M_7's body-to-source voltage through (4.14) or (4.15), with V_{BS7} found by equating the subthreshold currents $I_{DS8} = I_{DS9}$ in the 2T voltage reference formed by M_{8-9} based on (A.1), giving

$$V_{BS7} = \left(\frac{n_8}{n_9}V_{T08} - V_{T09}\right) + n_8 U_T \log\left(\frac{I_{SQ9}}{I_{SQ8}}\frac{S_9}{S_8}\right). \tag{4.18}$$

Different subthreshold factors are used for M_8 and M_9 as they can be of different V_T types. Next, the nonlinear expression of V_X given by (4.17) can be expressed as a voltage of the form (4.13) using a first-order Taylor series approximation of V_X around a temperature T_0, provided by

$$\begin{aligned} V_X(T) &\approx V_X(T_0) + \frac{dV_X(T_0)}{dT}(T - T_0), \\ &\approx V_{X0} + \delta_{V_X} T, \end{aligned} \tag{4.19}$$

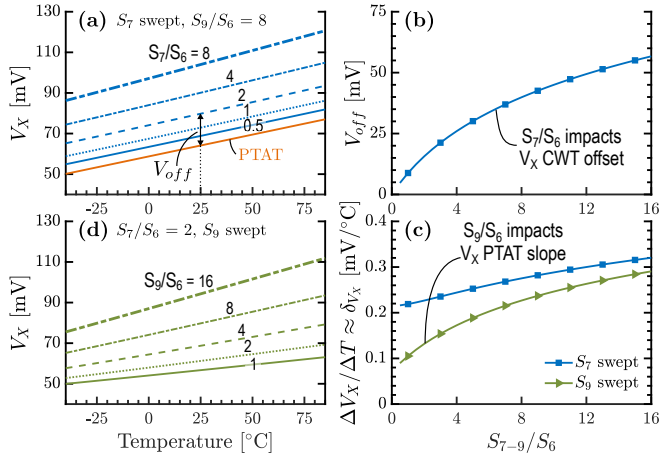

Fig. 4.28 All figures correspond to generic technological parameters $n = 1.2$, $\gamma_b^* = 0.15$, and $V_{BS7} = 0.2$ V, and rely on a body effect model corresponding to an FD-SOI technology. Temperature dependence of V_X for (a) a sweep of S_7 and a fixed $S_9/S_6 = 8$, and (d) a sweep of S_9 and a fixed $S_7/S_6 = 2$. (b) V_X CWT offset for the S_7 sweep in (a), and (c) V_X PTAT slope for the sweeps shown in (a) and (d), estimated as the variations of V_X across the temperature range divided by the temperature range.

with V_{X0} the voltage at zero absolute temperature and δ_{V_X} the PTAT slope of V_X. These two quantities are expressed as

$$V_{X0} = -\Delta V_{T7} \frac{S_7 \exp\left(\dfrac{-\Delta V_{T7}}{nU_{T0}}\right)}{S_9 + S_7 \exp\left(\dfrac{-\Delta V_{T7}}{nU_{T0}}\right)}, \tag{4.20}$$

$$\delta_{V_X} = \frac{dV_X(T_0)}{dT} = \frac{(V_X(T_0) - V_{X0})}{T_0}. \tag{4.21}$$

In practice, we find it more convenient to define quantities which can be extracted from simulation results. In what follows, the CWT offset of V_X, denoted as V_{off}, is thus defined as the difference between (4.17) and a purely PTAT reference voltage constituted solely of M_6 and M_9, at $T_0 = 25°C$, and expressed as

$$\begin{aligned} V_{off} &\triangleq V_X(T_0) - nU_{T0} \log\left(\frac{S_9}{S_6}\right), \\ &= nU_{T0} \log\left(1 + \frac{S_7}{S_9} \exp\left(\frac{-\Delta V_{T7}}{nU_{T0}}\right)\right). \end{aligned} \tag{4.22}$$

It is important to note that $V_{off} \neq V_{X0}$, even though they both represent an offset voltage. The PTAT slope of V_X is simply estimated as $\Delta V_X/\Delta T \simeq \delta_{V_X}$. Next, Fig. 4.28 illustrates the impact of changes of S_7/S_6 and S_9/S_6 on voltage V_X. First, an increase in S_7/S_6 for a fixed value of S_9/S_6 [Fig. 4.28(a)] results in an increased

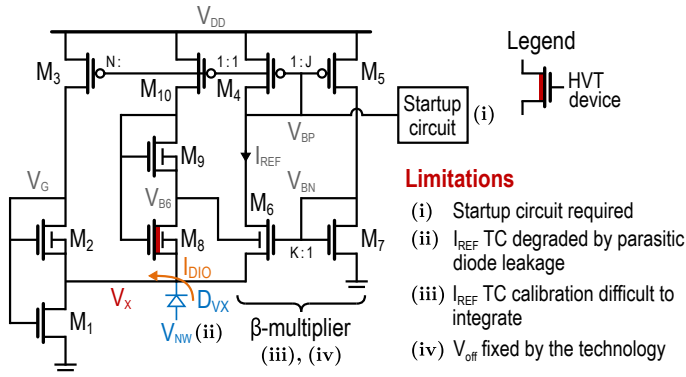

Fig. 4.29 Schematic of the SCM-based β-multiplier temperature-independent current reference proposed in [165] and its main limitations.

V_{off} ranging from 5 to 55 mV [Fig. 4.28(b)], while only slightly impacting the PTAT slope [Fig. 4.28(c)]. Next, an increase in S_9/S_7 for a fixed value of S_7/S_6 [Fig. 4.28(d)] strongly impacts the PTAT slope, with a variation from 0.1 to 0.3 mV/°C. Changing the ratios S_7/S_6 and S_9/S_6 therefore allows to tune the CWT offset and PTAT slope of V_X with a relative independence.

4.2.1.3 *Proposed Temperature-Independent Current Reference*

The proposed temperature-independent current reference combines the two key ideas described in Sections 4.2.1.1 and 4.2.1.2. Firstly, the idea of biasing an SCM using a PTAT voltage with a CWT offset to generate a CWT current, introduced in [165]. This concept shares some similarities with [77], in which the temperature dependence of the current in a deep-triode transistor is compensated with a temperature-dependent bias voltage. Then, the idea of using a ULP voltage reference whose output is buffered on a V-to-I converter, here an SCM, by a single transistor [29, 30, 169]. The main contributions of this work are thus to combine these two concepts and to propose a novel 4T voltage reference architecture to generate the PTAT voltage with a CWT offset required by the SCM. In addition, the proposed design corrects several limitations of our β-multiplier design [165], which was using a modified subthreshold β-multiplier to generate the SCM bias voltage, as shown in Fig. 4.29. The four following limitations have been corrected:

(i) A β-multiplier has two stable operating points and requires a startup circuit to ensure that it is biased around the non-zero one. However, this startup circuit requires extra silicon area and design time to ensure a proper functionality in all PVT corners without degrading the TC of I_{REF}. On the contrary, the proposed reference has a single non-zero operating point. Indeed, when I_{REF} is equal to zero, V_X and V_Y are ≈ 0, but this operating point is unstable as M_7 and M_9 are biasing M_6 with a non-zero current, thus leading to $V_{GS6} = V_X > 0$. This eliminates the need for a startup circuit;

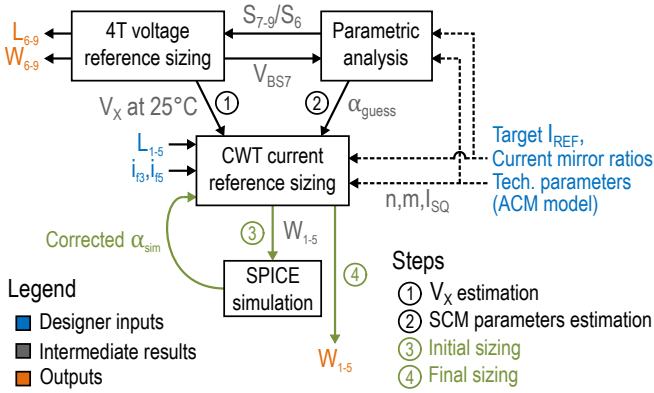

Fig. 4.30 Four-step flowchart of the design and sizing methodology.

(ii) The body / back-gate connection of M_2 and M_8 in Fig. 4.29 degrades I_{REF} TC due to the leakage through the parasitic p-well/deep n-well diode at node V_X. The proposed design solves this issue by connecting the body / back-gate of M_2 to ground, thus deleting this parasitic diode while only slightly changing the SCM's equations;

(iii) An I_{REF} TC calibration circuit, necessary to maintain an acceptable TC in all process corners, is difficult to integrate in the previous reference in Fig. 4.29 but is rather straightforward to add to the proposed reference by tuning the effective width of either M_7 or M_9 through a digital code. A complete explanation of this calibration is provided in Section 4.2.3.1;

(iv) The previous reference can only generate a fixed technology-dependent CWT offset related to the body factor and the ΔV_T between two transistors of different V_T types. There is consequently no degree of freedom to tune V_{off} apart from the transistor type. Yet, the proposed circuit allows to adjust V_{off} by simply changing the ratio S_7/S_6, as illustrated in Figs. 4.28(a) and (b), making it possible to optimize V_{off}.

The drawback of the proposed current reference is that the power consumption of the 4T voltage reference scales with the subthreshold I_{DS} leakage, and thus increases exponentially with temperature, leading to a larger power consumption than the β-multiplier-based reference at high temperature.

4.2.2 Design and Sizing Methodology

4.2.2.1 Overview of the Methodology

A flowchart of the sizing methodology is presented in Fig. 4.30. It is based on designer inputs such as the target reference current, the ratio of current mirrors, transistor lengths and inversion levels, as well as technological parameters estimated

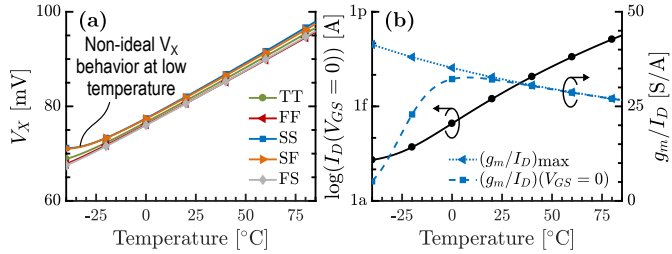

Fig. 4.31 The 4T voltage reference presents a non-ideal behavior at low temperature in slow nMOS process corners, due to gate leakage or GIDL. All figures correspond to GF 22-nm FD-SOI technology. Temperature dependence of (a) V_X in all process corners for a 4T voltage reference implemented with 8-μm-long I/O nMOS, and (b) $\log(I_D)$ at V_{GS} = 0, (g_m/I_D) at V_{GS} = 0, and $(g_m/I_D)_{\max}$, for an I/O LVT nMOS with W = 2 μm and L = 8 μm in the SS process corner.

by fitting the ACM model to g_m/I_D curves extracted from SPICE simulations, following the procedure described in [157]. This methodology outputs transistor dimensions and can be divided into four main steps, with steps 1) and 2) being more iterative than sequential.

Step 1) sizes the 4T voltage reference and provides an estimate of V_{BS7} after sizing W_{8-9} to make it CWT.

Step 2) provides an educated guess for the value of α that minimizes I_{REF} TC, denoted as α_{guess}, for a fixed S_7/S_6 and a given S_9/S_6, based on a parametric analysis similar to that described in Section 4.2.1.1 and Fig. 4.27.

Step 3) takes the estimated V_X at 25°C from step 1) and α_{guess} from step 2) to compute initial sizings of the current reference for a range of α values and fixed S_{7-9}/S_6 ratios. These sizings, characterized by different W_{1-2} values, are used to run pre-layout SPICE simulations to extract the correct optimal value of α, denoted as α_{sim}, taking into account the exact transistors' behavior.

Step 4) simply consists in running the sizing algorithm with $\alpha = \alpha_{\text{sim}}$, thereby generating the final current reference sizing.

4.2.2.2 4T Ultra-Low-Power Voltage Reference

The objectives of sizing the voltage reference, corresponding to step 1), are twofold. First, it aims at selecting a transistor type and length that limit the non-idealities of the voltage reference while minimizing power consumption. Second, it strives to make V_{BS7} CWT by properly sizing W_{8-9}.

First, Fig. 4.31(a) reveals that the 4T voltage reference can deviate from its ideal behavior at low temperature in the slow nMOS process corners. This behavior is explained by the fact that the subthreshold leakage ceases to decrease exponentially with temperature [Fig. 4.31(b)], either because of gate leakage becoming of the same order of magnitude as the I_{DS} one, or due to gate-induced drain leakage (GIDL), i.e., the increase of I_{DS} leakage at low V_{GS} and large V_{DS}. The second explanation is the most likely for the two technologies presented in this work as their gate leakage

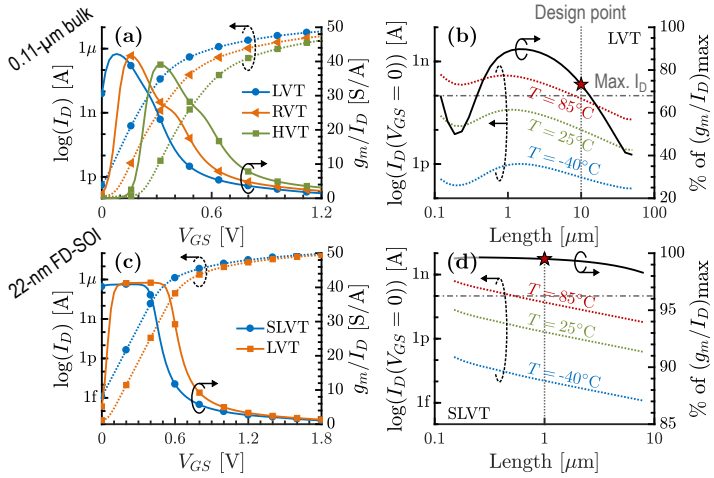

Fig. 4.32 All figures correspond to the SS process corner with a fixed $V_{DS} = V_{GS,\max}/2$. $\log(I_D)$, g_m/I_D vs. V_{GS} curves at T = -40°C (a) in 0.11 μm for core LVT, RVT and HVT nMOS with W = 0.5 μm and L = 10.45 μm, and (b) in 22 nm for I/O SLVT and LVT nMOS with W = 2 μm and L = 8 μm. $\log(I_D)$ at V_{GS} = 0 and at -40, 25 and 85°C, and g_m/I_D at V_{GS} = 0 as a percentage of $(g_m/I_D)_{\max}$ (b) in 0.11 μm for a core LVT nMOS with W = 0.5 μm and L ranging from 0.12 to 50 μm, and (d) in 22 nm for an I/O SLVT nMOS with W = 2 μm and L ranging from 0.15 to 8 μm.

is negligible. Indeed, 0.11-μm core devices still have a relatively thick oxide, while the devices used in 22 nm are I/O ones with high-κ gates. Both of these effects are nevertheless captured by a reduced g_m/I_D compared to $(g_m/I_D)_{\max} = 1/(nU_T)$ at V_{GS} = 0, as depicted in Fig. 4.31(b). Note that g_m/I_D is simply the slope of the $\log(I_D)$ vs. V_{GS} curve.

On the one hand, Figs. 4.32(a) and (c) depict the $\log(I_D)$ vs. V_{GS} curves in the SS process corner for different transistor types in 0.11 μm and 22 nm, together with the corresponding g_m/I_D vs. V_{GS} curves. On the other hand, Figs. 4.32(b) and (d) illustrate the trade-off between an ideal reference voltage behavior, coinciding with a g_m/I_D at V_{GS} = 0 close to $(g_m/I_D)_{\max}$, and a low power consumption, proportional to I_D at V_{GS} = 0. Here, we set a maximum leakage of 100 pA at 85°C for a unitary transistor, but harsher power constraints could be imposed. It should also be observed that the I_{DS} leakage current, and consequently the power consumption, grow exponentially with temperature. In 0.11 μm, core low-V_T (LVT) devices are preferred to regular- or high-V_T (RVT or HVT) ones as they are the only transistor type to have an acceptable g_m/I_D drop at V_{GS} = 0 [Fig. 4.32(a)]. A length of 10 μm is selected, leading to a g_m/I_D at V_{GS} = 0 and -40°C worth 73.2 % of $(g_m/I_D)_{\max}$, and a 10.1-pA I_D at 25°C [Fig. 4.32(b)]. In addition, short-channel effects are visible for small transistor lengths. In 22 nm, I/O super-low-V_T (SLVT) devices are picked as they present a perfect behavior at V_{GS} = 0, contrary to LVT ones [Fig. 4.32(c)]. A length of 1 μm is chosen, reaching a g_m/I_D at V_{GS} = 0 and

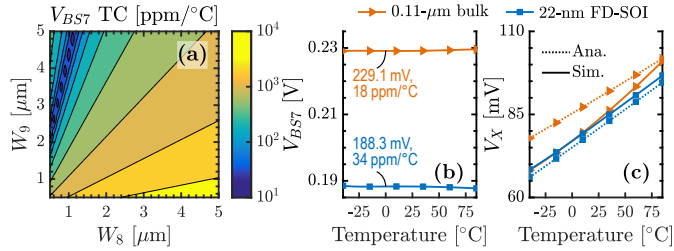

Fig. 4.33 ***V_{BS7}* is made CWT by tuning the ratio *S_9/S_8* in (4.18).** All figures correspond to the TT process corner. (a) V_{BS7} TC from -40 to 85°C in 22 nm at 1.8 V, for W_{8-9} swept from 0.5 to 5 μm and L_{8-9} = 1 μm. Temperature dependence of (b) V_{BS7} (simulated) and (c) V_X (analytical and simulated), in 0.11 μm at 1.2 V with S_7/S_6 = 4 and S_9/S_6 = 4, and in 22 nm at 1.8 V with S_7/S_6 = 2 and S_9/S_6 = 8.

-40°C of 99.5 % of $(g_m/I_D)_{\max}$ and a 2.08-pA I_D at 25°C [Fig. 4.32(d)].

Next, widths W_{8-9} are determined by a simple sweep, as exemplified in Fig. 4.33(a) for a 22-nm technology. This figure shows that an S_9/S_8 ratio of 4.38 leads to a CWT V_{BS7}, by having the TC of the second term in (4.18), which is proportional to U_T, compensate that of the difference of V_{T0}'s between M_{8-9}. The resulting pre-layout SPICE simulation results of V_{BS7} and V_X are shown in Figs. 4.33(b) and (c), together with analytical expression (4.17) for V_X. In 0.11 μm, M_8 and M_9 are respectively implemented with core HVT and LVT nMOS, yielding a 229-mV V_{BS7} with an 18-ppm/°C TC. Regarding V_X, the simulation presents a slightly larger PTAT slope than the analytical expression because of the temperature dependence of the body effect in bulk (4.14) leading to a non-zero ΔV_{T7} TC. In addition, the body factor γ_b^* is approximated using (4.16), thus leading to some discrepancies between the analytical expression and simulation. In 22 nm, M_8 and M_9 are respectively implemented with I/O LVT and SLVT nMOS, and a 188-mV V_{BS7} with a 34-ppm/°C TC is obtained. V_X's simulated behavior is close to the analytical expression, mostly because γ_b^* in FD-SOI is temperature-independent at first order [158], thus making ΔV_{T7} approximately CWT. The simulation only differs from the analytical expression by a 1.9-mV offset.

4.2.2.3 *Self-Cascode MOSFET*

The parametric analysis of step 2) yields Figs. 4.34(a) and (b), which are similar to Fig. 4.27 but with the difference that the y-axis corresponds to the ratio S_9/S_6 rather than to K_{PTAT}, and that parameters of GF 22-nm FD-SOI technology are used instead of generic ones. In Fig. 4.34(a), the I_{REF} TC valley corresponds to a quasi-linear relationship between S_9/S_6 and α. However, Fig. 4.34(b) illustrates that, contrary to Fig. 4.27, this valley is not an iso-$S_{I_{REF}}$ curve as the sizing is performed in the $(S_9/S_6;\ \alpha)$ space instead of the $(K_{PTAT};\ \alpha)$ one.

Furthermore, the sizing of the current reference shares similarities with the sizing methodologies proposed in [27, 165]. It consists of four main steps:

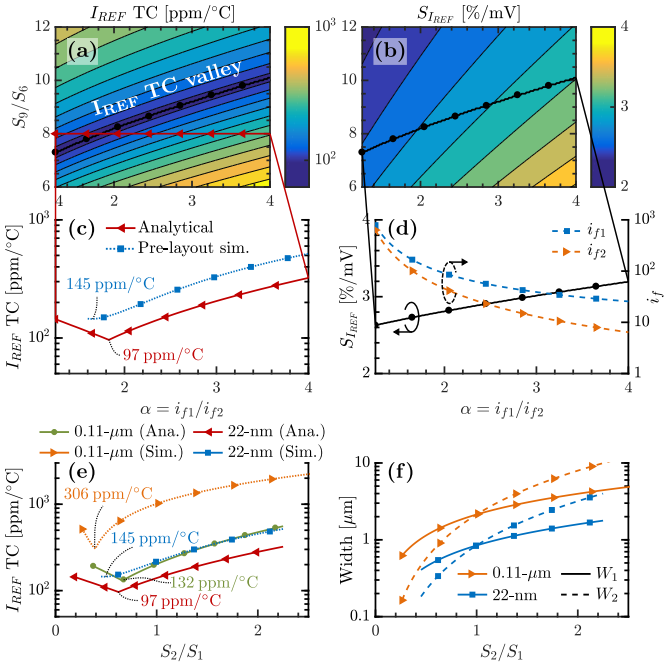

Fig. 4.34 **I_{REF} is made CWT by properly selecting S_9/S_6 and α, for a fixed S_7/S_6 corresponding to a given CWT offset V_{off}.** In 22 nm, (a) I_{REF} TC and (b) $S_{I_{REF}}$ for different values of $(S_9/S_6;\ \alpha)$, with $m = 1.63$, $n = 1.21$, and $S_7/S_6 = 2$, corresponding to $V_{off} = 17.3$ mV. (c) I_{REF} TC, (d) $S_{I_{REF}}$, and i_{f1-2}, as a function of α and computed from the analytical model and pre-layout simulations. In 0.11 μm and 22 nm and as a function of S_2/S_1, (e) I_{REF} TC for the analytical model and pre-layout simulations and (f) W_{1-2}.

1. Compute voltage V_X at 25°C using (4.17) or use the pre-layout simulation value obtained from step 1);
2. Solve (B.7) for i_{f2}, then calculate $i_{f1} = \alpha i_{f2}$, $S_{I_{REF}}$ from (B.12), S_2 from (A.4), and S_1 from (B.6);
3. Compute the aspect ratio of transistors M_{3-4} forming the pMOS current mirror using (A.4) while ensuring that $V_{SG4} > 4U_T$;
4. Compute the aspect ratio of M_5 using (A.4) while ensuring that $V_Y = V_X + V_{GS5} > 4U_T$.

Let us now have a closer look at the results of the sizing algorithm shown in Figs. 4.34(c) to (f). First, Fig. 4.34(d) illustrates that there is an interest in choosing small values of α as they result in a lower $S_{I_{REF}}$. This trend stems from the fact that M_{1-2} are biased in moderate ($i_f \in [1;\ 100]$) or strong ($i_f > 100$) inversion, at the cost of a larger minimum supply voltage. A design point corresponding to $(S_9/S_6;\ \alpha_{guess}) = (8; 1.825)$ is selected based on Figs. 4.34(a) and (c), yielding an I_{REF} TC = 96.7 ppm/°C and $S_{I_{REF}} = 2.77\ \%/V$. Pre-layout SPICE simulations in steps 3)

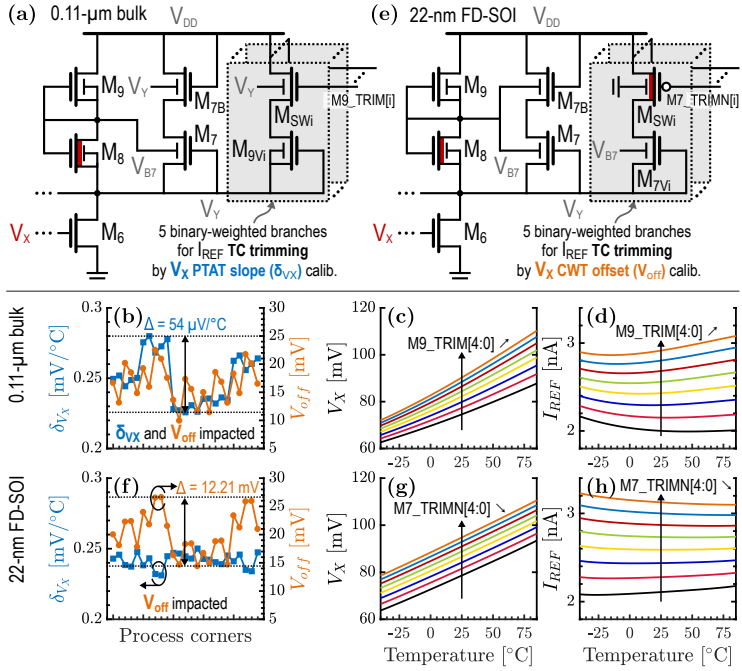

Fig. 4.35 ***I_{REF}*'s temperature independence can be maintained across process corners by tuning V_X PTAT slope (δ_{V_X}) in 0.11-μm bulk or V_X CWT offset (V_{off}) in 22-nm FD-SOI.** Schematic of the 4T voltage reference with I_{REF} TC calibration circuit in (a) 0.11 μm and (b) 22 nm. δ_{V_X} and V_{off} in process corners (considering skewed process corners of the nMOS of different V_T types used for M_{8-9}) in (b) 0.11 μm and (f) 22 nm. Temperature dependence of V_X and I_{REF} for different 5-bit calibration codes in (c)(d) 0.11 μm and (g)(h) 22 nm, in the TT process corner.

and 4) reveal that a 145-ppm/°C I_{REF} TC is eventually reached for $\alpha_{\text{sim}} = 1.65$, also corresponding to $S_{I_{REF}} = 2.73\ \%/V$. Fig. 4.34(e) depicts the same kind of results as Fig. 4.34(c), but as a function of S_2/S_1, used as a proxy for α and calculated from (B.6). In 0.11 μm, the difference between the 131.5-ppm/°C analytical optimum located at $S_2/S_1 = 0.66$ and the 306-ppm/°C pre-layout one obtained for $S_2/S_1 = 0.39$ originates from the temperature dependence of the body effect, which was not accounted for in the analytical model, as detailed in Section 4.2.2.2. In 22 nm, the 96.7-ppm/°C analytical optimum located at $S_2/S_1 = 0.62$ and the 145-ppm/°C pre-layout one obtained for $S_2/S_1 = 0.49$ are closer to each other but still differ due to inaccuracies of the ACM model, and more specifically, of the fitting of the temperature exponent of carrier mobility m. Finally, Fig. 4.34(f) demonstrates that W_{1-2} decrease with α as M_{1-2} are biased in stronger inversion while keeping L_{1-2} and I_{D1-2} fixed. In addition, the transistor widths are larger in 0.11 μm because M_{1-2} are chosen to be roughly 2× longer in this technology ($L = 40\times30\ \mu\text{m} = 1.2$ mm) than in 22 nm ($L = 64\times8\ \mu\text{m} = 512\ \mu$m).

Table 4.7 Sizing of the proposed nA-range CWT current references.

	UMC 0.11-μm bulk*						GF 22-nm FD-SOI					
		w/o I_{REF} TC calib.			w/ I_{REF} TC calib.			w/o I_{REF} TC calib.			w/ I_{REF} TC calib.	
	Type*	W [μm]	L [μm]	i_f	W [μm]	L [μm]	Type*	W [μm]	L [μm]	i_f	W [μm]	L [μm]
M_1	HS	**0.915**†	40×30	250.60	**0.915**†	40×30	SLVT	**0.44**†	64×8	165.82	**0.415**†	64×8
M_2	HS	**0.36**†	40×30	164.33	**0.36**†	40×30	SLVT	**0.215**†	64×8	100.50	**0.202**†	64×8
M_3	HS	6×1.25	5×10	1.43	6×1.25	5×10	LVT	6×5	5×1	0.02	6×5	5×1
M_4	HS	2×1.25	5×10	1.43	2×1.25	5×10	LVT	2×5	5×1	0.02	2×5	5×1
M_5	HS	1.2	10	0.10	1.2	10	SLVT	10	0.5	0.0007	10	0.5
M_6	HS	2×2	10	-	4×2	20	SLVT	2×5.47	1	-	2×5.6	1
M_7	HS	8×2	10	-	16×2	20	SLVT	4×5.47	1	-	10×1.12	1
M_{7B}	HS	-	-	-	0.16	25	SLVT	4×5.47	1	-	2×1.12	1
M_8	LL	8×2	10	-	2×2	20	LVT	16×1.25	1	-	18×1.28	1
M_9	HS	8×2	10	-	2×2	20	SLVT	16×5.47	1	-	18×5.6	1
M_{SWi}	HS	-	-	-	0.16	25	ULL	-	-	-	0.16	5×8
M_{7Vi}	-	-	-	-	-	-	SLVT	-	-	-	1 to 16×1.12	1
M_{9Vi}	HS	-	-	-	1 to 16×2	20	-	-	-	-	-	-

* Dimensions reported for UMC 0.11-μm bulk are pre-shrink ones, and must be scaled by a factor 0.9× to obtain silicon dimensions. * In 0.11 μm, HS refers to high-speed, i.e., LVT, and LL to low-leakage, i.e., HVT. In 22 nm, SLVT refers to super-low-V_T, LVT to low-V_T, and ULL to ultra-low-leakage, i.e., HVT.
† Widths fine-tuned based on the outputs of the sizing algorithm to obtain the target I_{REF}.

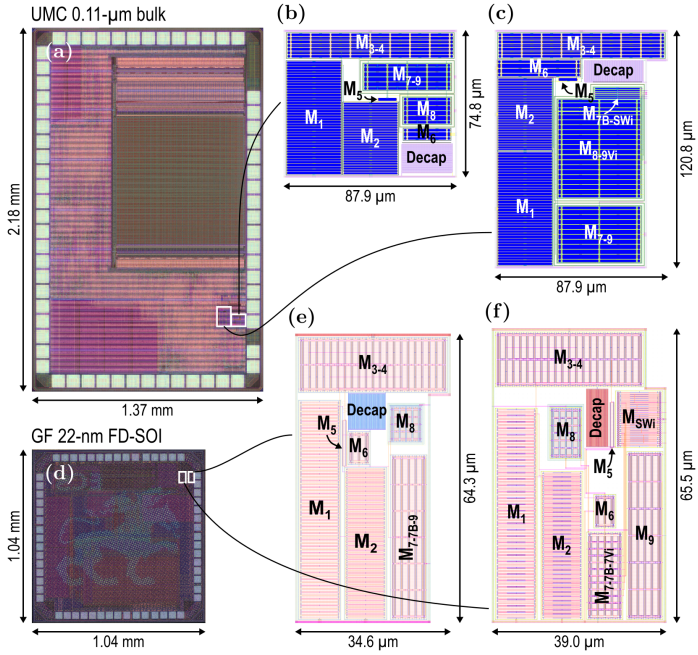

Fig. 4.36 Chip microphotographs with overlaid layout in (a) UMC 0.11-μm bulk (3 mm^2) and (d) GF 22-nm FD-SOI (1.08 mm^2). Layouts of the proposed nA-range CWT current references (b)(e) without and (c)(f) with I_{REF} TC calibration.

4.2.3 Simulation and Measurement Results

In this section, we present the I_{REF} TC calibration circuit implemented in the proposed reference, and provide an overview of the implemented current references and the measurement setup. Then, we discuss into details the post-layout simulations and measurements of the designs in 0.11-μm bulk and 22-nm FD-SOI, whose summary is provided in Table 4.8.

4.2.3.1 I_{REF} TC Calibration and Overview of the Designs

Fig. 4.35 shows the I_{REF} TC calibration mechanism implemented in the proposed current references. First, in 0.11-μm bulk, process variations (including skewed process corners of M_{8-9}) impact V_X PTAT slope (δ_{V_X}) and CWT offset (V_{off}), as shown in Fig. 4.35(b), with total variations of 54 μV/°C and 12.57 mV, respectively. When both quantities are impacted, we observe that calibrating δ_{V_X} is more effective than calibrating V_{off} in terms of number of components. Tuning the number of transistors placed in parallel to implement M_9 using a calibration code [Fig. 4.35(a)] modifies δ_{V_X} by changing the ratio S_9/S_6 in (4.17) [Fig. 4.35(c)], thus allowing to adjust the I_{REF} TC [Fig. 4.35(d)]. Then, in 22-nm FD-SOI, process variations mostly impact V_X CWT offset (V_{off}) with a total variation of 12.21 mV, and

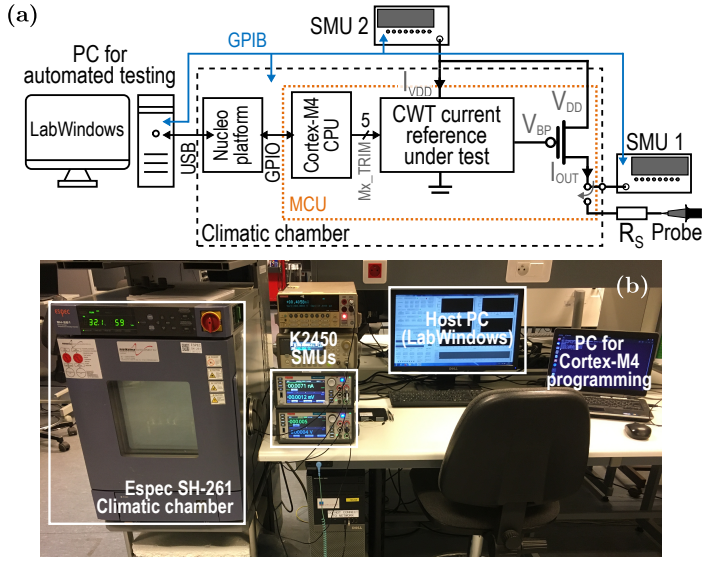

Fig. 4.37 (a) Conceptual and (b) actual measurement testbench for supply voltage and temperature dependence characterization.

have a lesser influence on δ_{V_X} than in 0.11 μm, as it only changes by 19 μV/°C [Fig. 4.35(f)]. It is then more effective to calibrate V_{off}. Tuning the number of transistors placed in parallel to implement M_7 using a calibration code [Fig. 4.35(e)] impacts V_{off} by changing the ratio S_7/S_6 in (4.17) [Fig. 4.35(g)], thus providing another way to calibrate the I_{REF} TC [Fig. 4.35(h)]. Two current references, respectively without and with I_{REF} TC calibration, have been fabricated in each of the UMC 0.11-μm bulk and GF 22-nm FD-SOI technology nodes. Chip microphotographs, layouts and final dimensions of these four current references can be found in Fig. 4.36 and Table 4.7, respectively. Based on these references, the area overhead of the the TC calibration circuit is estimated to be 61.5 % compared to the design without calibration in 0.11 μm, and 14.9 % in 22 nm. This gap in area overhead originates from the much-longer transistors used in the TC calibration circuit in 0.11 μm. Only the power consumption of the 4T voltage reference is affected by the calibration, and the power overhead is thus dependent on the calibration code.

4.2.3.2 *Measurement Testbench*

The measurement setup is schematized in Fig. 4.37(a) and shown in Fig. 4.37(b). The proposed current references are integrated in microcontroller units (MCUs), called (i) MANTIS in 0.11-μm bulk, intended for near-sensor image processing applications, and (ii) CERBERUS in 22-nm FD-SOI, intended for edge machine-learning applications and low-power wide-area network communication. Eleven

Table 4.8 Summary of the simulated and measured performance of the proposed nA-range CWT references.

	UMC 0.11-μm bulk				GF 22-nm FD-SOI			
	w/o TC calib.		w/ TC calib.		w/o TC calib.		w/ TC calib.	
	Sim.	Meas.	Sim.	Meas.	Sim.	Meas.	Sim.	Meas.
I_{REF} [nA]	2.49	2.74	2.40	2.30	2.48	2.32	2.50	2.54
Power [nW]	11.19 @0.8V	12.65 @0.8V	10.98 @0.8V	11.06 @0.8V	10.23 @1V	9.40 @1V	10.27 @1V	10.39 @1V
Area [mm^2]	0.00657		0.01061		0.00222		0.00255	
Supply range [V]	0.8 – 1.2		0.8 – 1.2		1 – 1.8		1 – 1.8	
LS [%/V]	2.94	2.60	2.07	2.23	0.21	1.47	0.26	1.53
Temp. range [°C]	-40 – 85		-40 – 85		-40 – 85		-40 – 85	
TC [ppm/°C]	330.7	529.5	290.6	176.0	137.5	360.6	101.5	81.5
I_{REF} var. (process) [%]	6.00	2.11	7.53	3.47	3.16	2.48	4.18	2.55
I_{REF} var. (mismatch) [%]	1.32		1.74		2.68		2.41	
t_{start} [ms]	15.25	17.53	16.21	18.22	3.29	11.56	3.26	11.20

dies have been measured in each technology node. Furthermore, the testing is controlled by a host PC controlling an Espec SH-261 climatic chamber for the temperature sweep, and two Keithley K2450 source measure units (SMUs) for the supply voltage sweep. SMU 1 measures the output current I_{OUT} with $V_{SD} = V_{DD,\max}/2$, respectively equal to 4× and 8×I_{REF} in 0.11 μm and 22 nm, and SMU 2, the sum of I_{OUT} and the supply current I_{VDD}. The pMOS current mirror generating I_{OUT} employs a common-centroid layout to accurately replicate I_{REF}, and only marginally augments I_{REF} (σ/μ) by 0.03 and 0.06 % in 0.11 μm and 22 nm, respectively. In addition, the host PC controls the TC calibration code through a Nucleo platform interacting with the on-chip Cortex-M4 central processing unit (CPU). At last, startup measurements are performed by replacing SMU 1 with an 82- / 47-MΩ resistor R_S in series with the 1-MΩ input resistance of the oscilloscope probe.

4.2.3.3 *Designs in 0.11-μm Bulk CMOS Technology*

First, we discuss the post-layout simulation results of the references. Fig. 4.38(a) reveals that, without TC calibration, δ_{V_X} spans from 232 to 288 μV/°C due to process variations of the subthreshold slope factor n. This results in a 739-ppm/°C CTAT to 720-ppm/°C PTAT I_{REF} TC in Fig. 4.38(b). With TC calibration, δ_{V_X} is adapted to each process corner [Fig. 4.38(c)], leading to an I_{REF} TC between 287 and 349 ppm/°C with a residual second order temperature dependence [Fig. 4.38(d)]. Then, Fig. 4.39 presents the supply voltage dependence of the reference with TC calibration, whose TC has been calibrated in each process corner. Fig. 4.39(a) shows that V_X LS lies between 0.9 and 1.05 mV/V from 0.8 to 1.2 V. The analytical expression of the minimum supply voltage is given by

$$V_{DD,\min} = 4U_T + \max(V_G,\ V_X + V_{SG4},\ V_X + V_{GS5} + V_{GS8}), \tag{4.23}$$

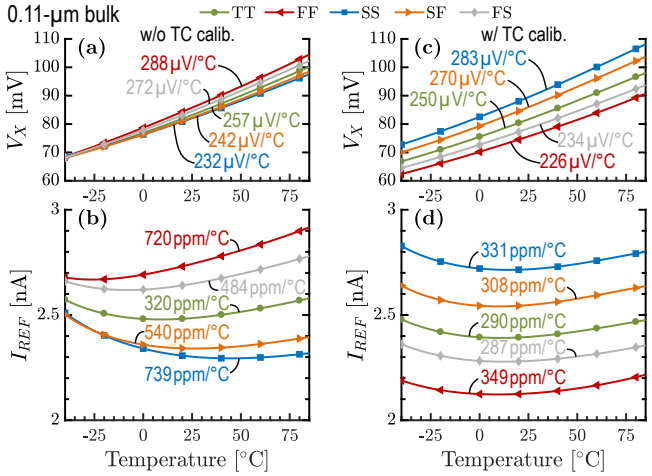

Fig. 4.38 In UMC 0.11-μm bulk, post-layout simulation of the temperature dependence of V_X and I_{REF}, in all process corners and at 1.2 V, without [(a) and (b)] and with I_{REF} TC calibration [(c) and (d)].

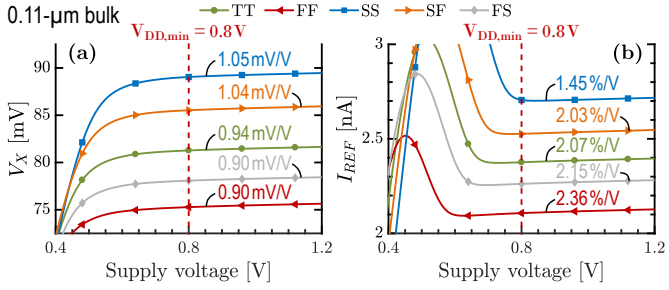

Fig. 4.39 In UMC 0.11-μm bulk, post-layout simulation of the supply voltage dependence of (a) V_X and (b) I_{REF} in all process corners and at 25°C, with I_{REF} TC calibration.

and $V_{DD,\text{min}}$ = 0.8 V is here limited by voltage V_G in the SCM. This translates into an LS of I_{REF} between 1.45 and 2.36 %/V in Fig. 4.39(b). Next, we consider skewed process corners of high-speed (HS), i.e., LVT, and low-leakage (LL), i.e., HVT, core devices in Fig. 4.40. The TC calibration moderately raises I_{REF} process variations from +26.4 % / -22.8 % to +29.2 % / -29.2 % in the (FF, SS) and (SS, FF) corners, respectively. This behavior stems from tuning δ_{V_X}, which affects the value of V_X itself [Fig. 4.40(a)]. Meanwhile, the calibration shifts the TC from 289 to 739 ppm/°C, down to 184 to 411 ppm/°C [Fig. 4.40(b)]. The calibration mechanism tends to harmonize δ_{V_X} for a given LL process corner, while δ_{V_X} was initially quite uniform in a given HS process corner [Fig. 4.40(c)]. Finally, Fig. 4.41(a) emphasizes that, without TC calibration, I_{REF} varies more significantly due to global process variations, with a 6-% (σ/μ), than from local mismatch, with a 1.32-% (σ/μ). The same conclusion can be drawn with TC calibration [Fig. 4.41(b)], with slightly larger (σ/μ)'s

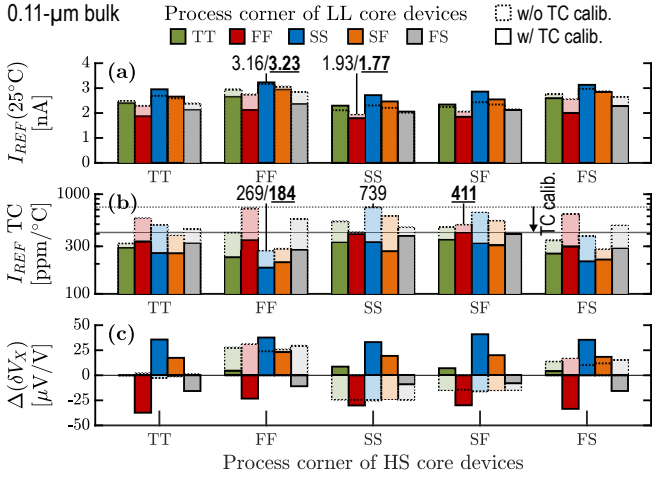

Fig. 4.40 In UMC 0.11-μm bulk and at 1.2 V, post-layout simulation of (a) I_{REF} at 25°C, (b) I_{REF} TC from -40 to 85°C, and (c) the change in PTAT slope of V_X with respect to its nominal value, without and with TC calibration. Skewed process corners of LL and HS core devices are considered.

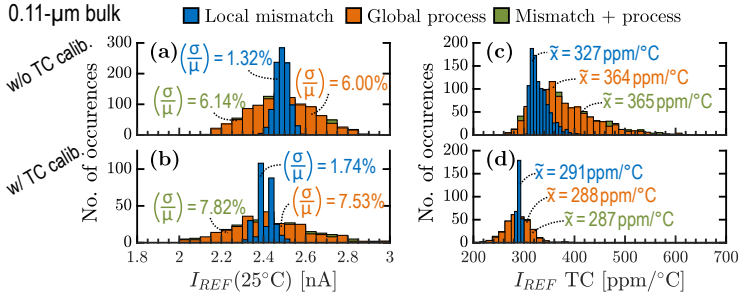

Fig. 4.41 In UMC 0.11-μm bulk, for 10^3 / 3×10^2 post-layout MC simulations in TT at 1.2 V, histograms of I_{REF} at 25°C [(a) and (b)] and of I_{REF} TC from -40 to 85°C [(c) and (d)], without [(a) and (c)] and with I_{REF} TC calibration [(b) and (d)]. $\tilde{x}$ denotes the median of a statistical distribution.

of 7.53 % and 1.74 % for process and mismatch, due to a different sizing of the 4T voltage reference to accommodate the TC calibration circuit, coupled with the tendency of this calibration scheme to accentuate I_{REF} variations.

Then, we present the measurement results of the 11 dies. The temperature dependence without and with TC calibration is shown in Figs. 4.42(a) and (b). We notice a drop of I_{REF} at high temperature which is due to the leakage of the electrostatic discharge (ESD) protection diodes in the I/O pad connected to SMU 1. In Figs. 4.42(c) and (d), average values of 2.74 and 2.30 nA are obtained, with (σ/μ)'s of 2.11 and 3.47 %. This variability is above the simulated one for local mismatch, suggesting that the measured dies originate from different process

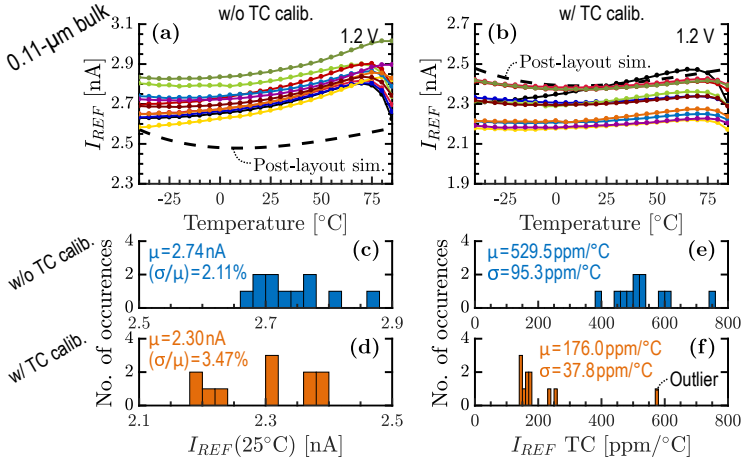

Fig. 4.42 In UMC 0.11-μm bulk and at 1.2 V, measured temperature dependence of I_{REF} (a) without and (b) with I_{REF} TC calibration. Measured histograms of I_{REF} at 25°C [(c) and (d)] and of I_{REF} TC from -40 to 85°C [(e) and (f)], without and with I_{REF} TC calibration.

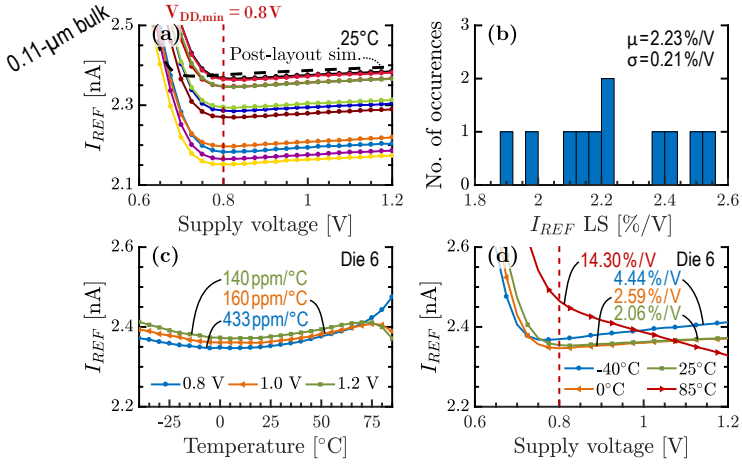

Fig. 4.43 In UMC 0.11-μm bulk and for the design with I_{REF} TC calibration, (a) measured supply voltage dependence at 25°C and (b) histogram of LS from 0.8 to 1.2 V. For die 6, measured (c) temperature dependence at different supply voltages and (d) supply voltage dependence at different temperatures.

batches. It should be noted that, if required by the applicative context, a calibration of I_{REF} could readily be implemented using a binary-weighted current mirror. Finally, the calibration improves the TC from 530 to 176 ppm/°C, and also reduces σ from 95 to 38 ppm/°C [Figs. 4.42(e) and (f)]. It should be noted that the 575-ppm/°C outlier in Fig. 4.42(f), corresponding to the black curve in Fig. 4.42(b), is not accounted for in the mean. These results are obtained with a complete knowledge of the temperature profile between -40 and 85°C, but a two-point calibration

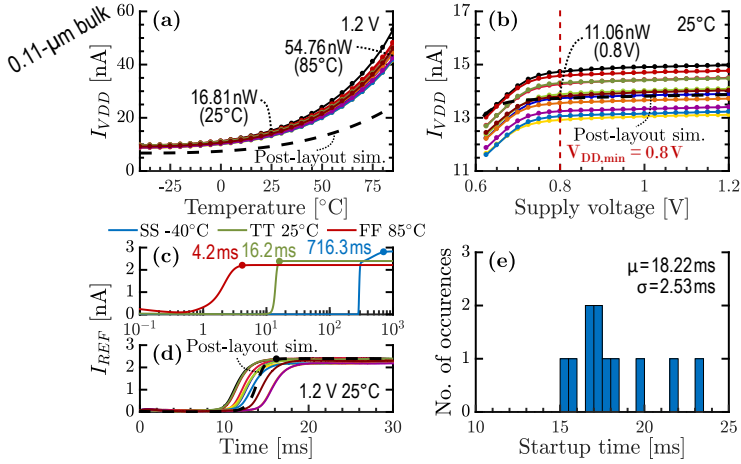

Fig. 4.44 In UMC 0.11-μm bulk, measured dependence of the supply current (a) to temperature at 1.2 V, and (b) to supply voltage at 25°C. (c) Post-layout-simulated RCC startup waveforms in extreme corners, and (d) measured startup waveforms and (e) histogram of 99-% startup time, at 1.2 V 25°C.

at -25 and 85°C yields similar results, with a mean TC marginally increased from 176 to 182 ppm/°C, as illustrated in Fig. C.5 in Appendix C. Moving on to the supply voltage dependence, the details of the 11 dies are shown in Fig. 4.43(a), and an average LS of 2.23 %/V is achieved in Fig. 4.43(b). This value is close to the 2.07 %/V obtained in TT post-layout simulation, which is not surprising given the good agreement between simulation and measurement in Fig. 4.43(a). Then, Fig. 4.43(c) highlights that the I_{REF} drop at high temperature transforms into an I_{REF} surge as supply voltage decreases. This behavior arises from the fact that, at 85°C, I_{REF} decreases with V_{DD} while it presents a normal supply voltage dependence at all other temperatures [Fig. 4.43(d)]. For a 0.8-V supply, the leakage of the ESD diodes between the pad and the supply voltages (core and I/O) dominates and increases the measured I_{OUT}, while at 1.2 V, the leakage of the diodes between the pad and ground is prevalent and decreases the measured I_{OUT}. Next, in Fig. 4.44(a), the supply current is around 10 nA at low temperature as it is dominated by the SCM which draws a current equal to $(N+1)I_{REF}$ with a current ratio $N = 3$, while at high temperature, it scales exponentially as the power consumption of the 4T voltage reference is proportional to the I_{DS} leakage. At 1.2 V, average power consumptions of 16.8 and 54.8 nW are reached at 25 and 85°C, respectively. The steeper supply current increase in measurement compared to the TT simulation indicates that the dies might be from a fast nMOS process corner. Fig. 4.44(b) shows that the drawn current does not substantially increase with the supply voltage, and that a minimum average power consumption of 11.1 nW is achieved at 0.8 V. Finally, the x-% startup time is computed as the time at which I_{REF} remains within (100-x) % of its steady-state value. The 99-% startup time has a simulated

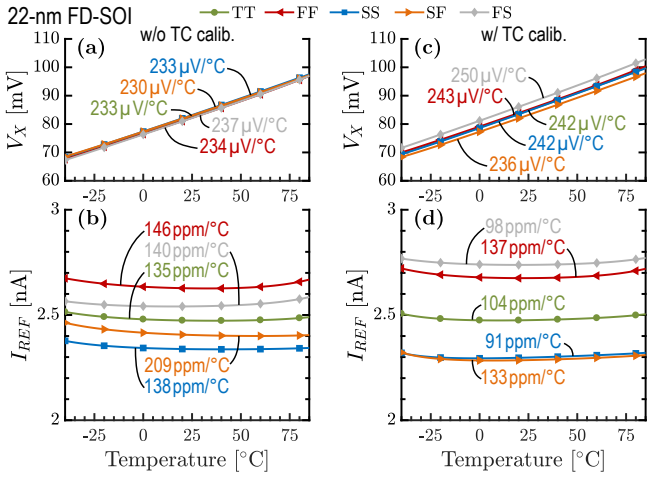

Fig. 4.45 In GF 22-nm FD-SOI, post-layout simulation of the temperature dependence of V_X and I_{REF}, in all process corners and at 1.8 V, without [(a) and (b)] and with I_{REF} TC calibration [(c) and (d)].

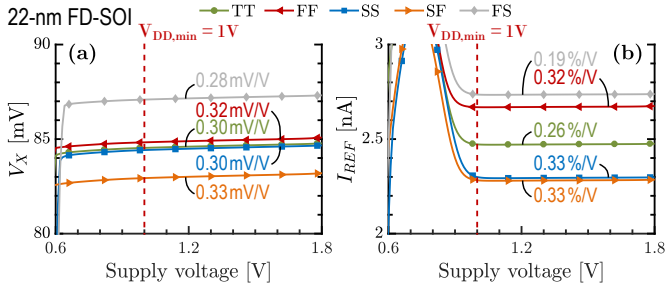

Fig. 4.46 In GF 22-nm FD-SOI, post-layout simulation of the supply voltage dependence of (a) V_X and (b) I_{REF} in all process corners and at 25°C, with I_{REF} TC calibration.

nominal value of 16.2 ms and a worst-case one of 716.3 ms in the SS -40°C corner [Fig. 4.44(c)]. At 1.2 V and 25°C, the measured startup time is 18.2 ms on average [Figs. 4.44(d) and (e)], and confirms the inutility of a startup circuit. This startup time is sufficiently low given the fact that a nA-range current reference will likely be employed as an always-on block.

4.2.3.4 *Designs in 22-nm FD-SOI CMOS Technology*

Similarly to the results in 0.11 μm, we first discuss the post-layout simulations results. Fig. 4.45(a) shows that, without TC calibration, δ_{V_X} is less process-dependent than in 0.11 μm, and takes lower values between 230 and 237 μV/°C. These two observations are linked to the subthreshold slope factor, which can be defined as $n = 1 + C_d/C_{ox}$. In bulk, C_d is the depletion layer capacitance, while in FD-SOI, C_d is the capacitance between the back-gate and the channel due to the buried oxide.

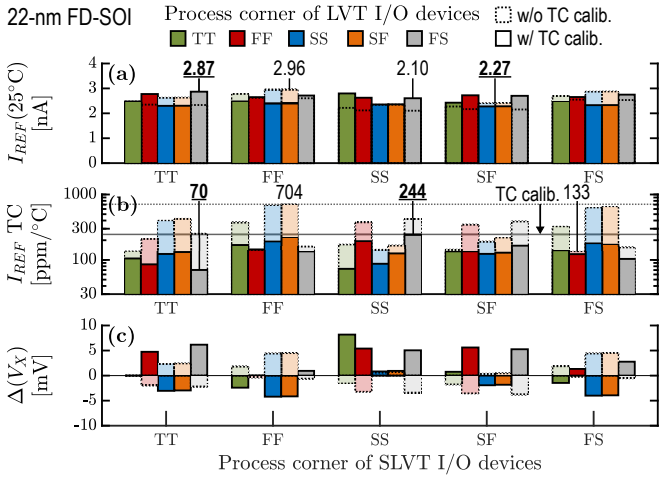

Fig. 4.47 In GF 22-nm FD-SOI and at 1.8 V, post-layout simulation of (a) I_{REF} at 25°C, (b) I_{REF} TC from -40 to 85°C, and (c) the change in PTAT slope of V_X with respect to its nominal value, without and with TC calibration. Skewed process corners of SLVT and LVT I/O devices are considered.

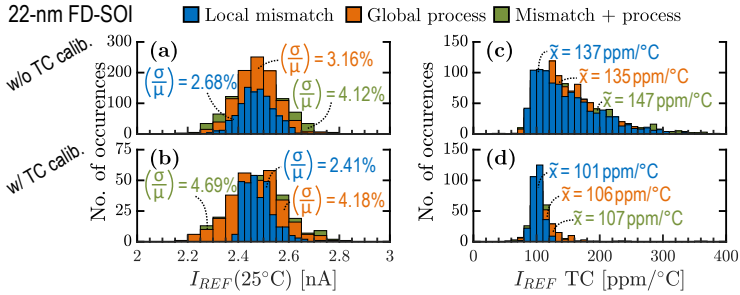

Fig. 4.48 In GF 22-nm FD-SOI, for 10^3 / 3×10^2 post-layout MC simulations in TT at 1.8 V, histograms of I_{REF} at 25°C [(a) and (b)] and of I_{REF} TC from -40 to 85°C [(c) and (d)], without [(a) and (c)] and with I_{REF} TC calibration [(b) and (d)]. $\tilde{x}$ denotes the median of a statistical distribution.

This capacitance is process-invariant at first order, and smaller than the depletion layer capacitance, thus explaining our observations. The resulting I_{REF} TC is comprised between 138 and 209 ppm/°C [Fig. 4.45(b)]. Regarding I_{REF} TC, calibration improves the median value $\tilde{x}$ by 40 to 80 ppm/°C, but most notably shortens the tail of the distribution, with a 99th percentile for combined process and mismatch reduced from 576 to 364 ppm/°C [Figs. 4.41(c) and (d)].

In 22 nm, the TC calibration changes V_{off} [Fig. 4.45(c)] and reduces I_{REF} TC between 91 to 137 ppm/°C [Fig. 4.45(d)]. The necessity of the TC calibration might not be obvious from the analysis of conventional process corners, but will become clear when discussing skewed process corners herebelow. Besides, Fig. 4.46 shows

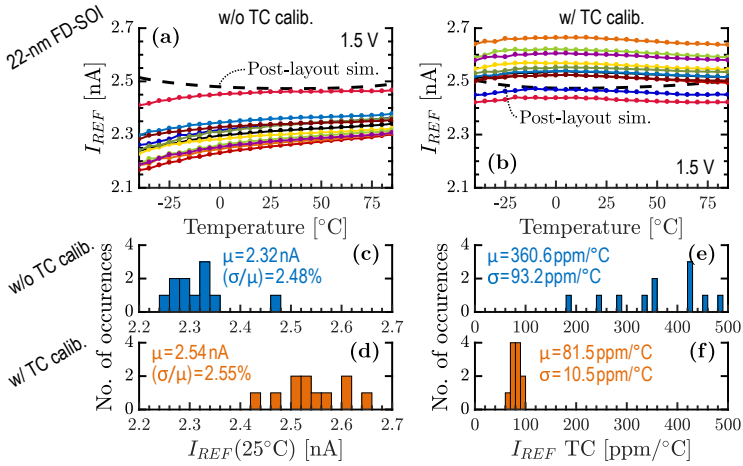

Fig. 4.49 In GF 22-nm FD-SOI and at 1.5 V, measured temperature dependence of I_{REF} (a) without and (b) with I_{REF} TC calibration. Measured histograms of I_{REF} at 25°C [(c) and (d)] and of I_{REF} TC from -40 to 85°C [(e) and (f)], without and with I_{REF} TC calibration.

that, for the reference with TC calibration, V_X LS is around 0.28 to 0.32 mV/V [Fig. 4.46(a)], which is more than 3× lower than in 0.11 μm thanks to the large intrinsic gain (g_m/g_d) in FD-SOI [37], thereby improving the LS, as it is usually proportional to (g_d/g_m). This translates into an I_{REF} LS between 0.19 and 0.33 %/V from 1 to 1.8 V, with $V_{DD,\text{min}}$ = 1 V limited by the SCM. Next, we consider skewed process variations of SLVT and LVT I/O devices in Fig. 4.47. Contrary to the 0.11-μm design, the TC calibration somewhat reduces I_{REF} process variations from +18.4 % / -16 % to +14.8 % / -9.2 % [Fig. 4.47(a)]. The max./min. values are however not attained in the same corners without and with TC calibration. I_{REF} TC is reduced from the 133-to-704-ppm/°C range down to the 70-to-204-ppm/°C one, pointing out the importance of this calibration to maintain performance across process corners [Fig. 4.47(b)]. We notice that the effect of the TC calibration is to slightly increase V_{off} in fast LVT nMOS corners, and to decrease it in slow LVT nMOS corners [Fig. 4.47(c)]. Regarding I_{REF} variability at 25°C, similarly to the 0.11-μm references, the impact of local mismatch is more limited than that of global process variations, but with values that are nonetheless closer from each other, with a 2.68-% and 3.16-% (σ/μ)'s for mismatch and process variations without TC calibration [Fig. 4.48(a)]. With TC calibration, the impact of mismatch is reduced to a 2.41-% (σ/μ), while the impact of process is a bit more significant, with a value of 4.18 % [Fig. 4.48(b)]. The median TC improves by roughly 40 ppm/°C when the TC is calibrated, and the tail of the distribution is also reduced, with the 99th percentile for combined mismatch and process diminished from 333 to 239 ppm/°C [Figs. 4.48(c) and (d)].

Continuing with the measurement results, Figs. 4.49(a) and (b) depict the temperature dependence without and with TC calibration for a supply voltage of 1.5 V,

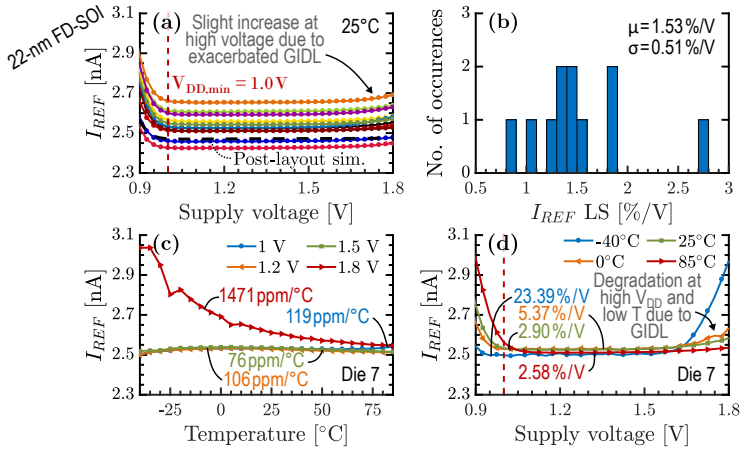

Fig. 4.50 In GF 22-nm FD-SOI and for the design with I_{REF} TC calibration, (a) measured supply voltage dependence at 25°C and (b) histogram of LS from 1 to 1.8 V. For die 7, measured (c) temperature dependence at different supply voltages and (d) supply voltage dependence at different temperatures.

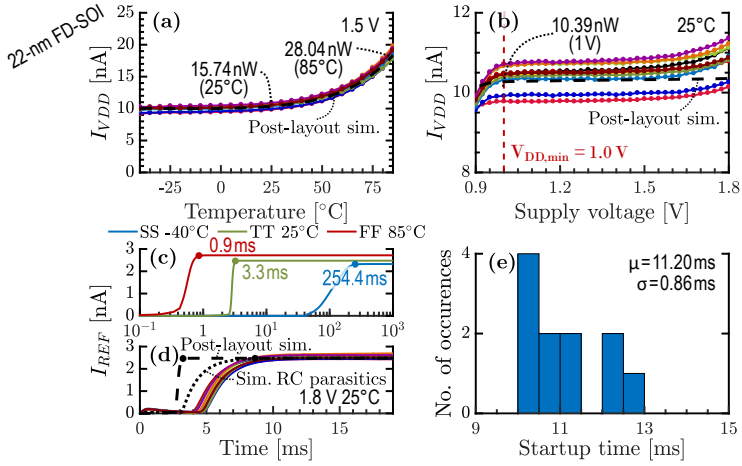

Fig. 4.51 In GF 22-nm FD-SOI, measured dependence of the supply current (a) to temperature at 1.5 V, and (b) to supply voltage at 25°C. (c) Post-layout-simulated RCC startup waveforms in extreme corners, and (d) measured startup waveforms and (e) histogram of 99-% startup time, at 1.8 V 25°C.

instead of 1.8 V in post-layout simulation results. This choice is related to non-idealities in the 4T voltage reference and will be explained later in this paragraph. Figs. 4.49(c) and (d) present 2.32- and 2.54-nA average values of I_{REF} without and with TC calibration, with (σ/μ)'s of 2.48 and 2.55 %. These results are in line with post-layout simulations and suggest that the measured dies come from the same process batch, as the variability has the same magnitude as the one due to local

mismatch in simulation. The TC calibration mechanism cuts the TC from 361 to 82 ppm/°C, with a sharp reduction of σ from 93 to 11 ppm/°C. In addition, it is interesting to note that all measured dies present a TC lower than 100 ppm/°C. Similarly to the 0.11-μm design, these results correspond to a calibration based on the complete temperature profile between -40 and 85°C, but a two-point calibration at -40 and 80°C gives comparable results and only slightly increases the mean TC from 81.5 to to 82.7 ppm/°C, as shown in Fig. C.7 in Appendix C. Furthermore, Fig. 4.50(a) reveals a modest rise of I_{REF} at high supply voltage, due to the exacerbated GIDL at high V_{DS} in the zero-V_{GS} transistors used as current sources in the 4T voltage reference. This results in an average LS of 1.53 %/V larger than the 0.26-%/V simulated value [Fig. 4.50(b)]. Besides, Fig. 4.50(c) illustrates that the TC is consistent across the supply voltage range, except at 1.8 V, for which I_{REF} soars due to the exacerbated GIDL of the zero-V_{GS} transistors, made worse by the increased V_{T0} at low temperature. This interpretation is supported by the measurements in Fig. 4.50(d), in which the distortion at high supply voltage is aggravated by the temperature reduction, and hints that nMOS devices might be in a slow process corner. Nevertheless, this problem could be solved by placing diode transistors in series with the zero-V_{GS} transistors M_{7Vi} to reduce their V_{DS}, without potentially impacting $V_{DD,\text{min}}$ as it is currently limited by voltage V_G in the SCM. Then, the supply current temperature dependence [Fig. 4.51(a)] is similar to the 0.11-μm design, with a prevalence of the SCM current equal to $4I_{REF} \approx 10$ nA at low temperature, and an increased share due to the 4T voltage reference as temperature rises. Average power consumptions of 15.8 and 28.0 nW are respectively attained at 25 and 85°C. Moreover, the supply voltage dependence of I_{VDD} is similar to that of I_{REF} [Fig. 4.51(b)], as the power consumption at 25°C is dominated by the SCM, and a minimum power consumption of 10.4 nW is obtained for $V_{DD,\text{min}}$ = 1 V. At last, the simulated 99-% startup time is 3.3 ms in typical conditions and 254.4 ms in the worst case [Fig. 4.51(c)], while the measured value is 11.2 ms on average [Figs. 4.51(d) and (e)]. On the one hand, this difference is explained by an nMOS process corner slightly slower than the typical one, which causes the shift to the right in Fig. 4.51(d) and corroborates the observations related to the temperature and supply voltage dependences. On the other hand, it is due to the RC time constant caused by the series resistance R_S and the 25-pF PCB parasitic capacitance, as illustrated in Fig. 4.51(d). These results again prove that the proposed reference does not require a startup circuit.

4.2.3.5 *Measured Calibration Results in Both Technologies*

This final section examines into more details the TC calibration results, based on post-layout simulations and measurements of all 11 dies. In UMC 0.11 μm, Fig. 4.52(a) highlights that the calibration range has been properly selected, as a TC around 300 ppm/°C can be attained in all five conventional process corners. The FF and SS process corners are the most critical, because they lie close to the

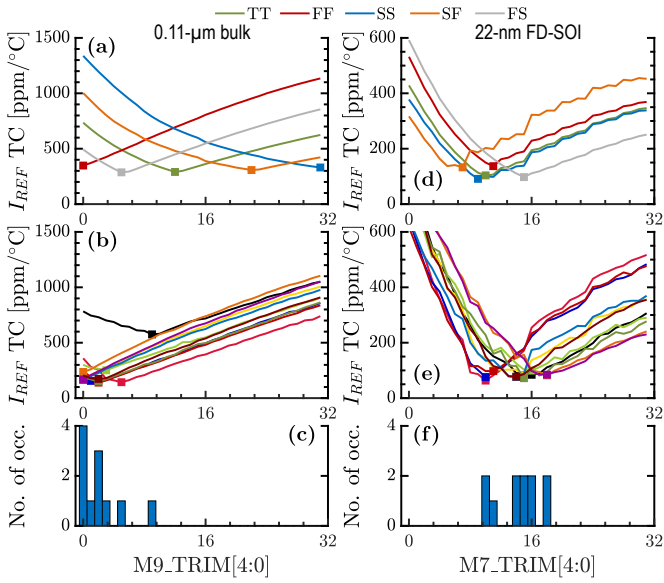

Fig. 4.52 In UMC 0.11-μm bulk and GF 22-nm FD-SOI, (a)(d) post-layout simulation in all process corners and (b)(e) measurement for all 11 dies of the TC of I_{REF} as a function of the calibration code, at 1.2 V in 0.11 μm and 1.8 V in 22 nm. (c)(f) Histogram of the measured calibration code yielding the best I_{REF} TC.

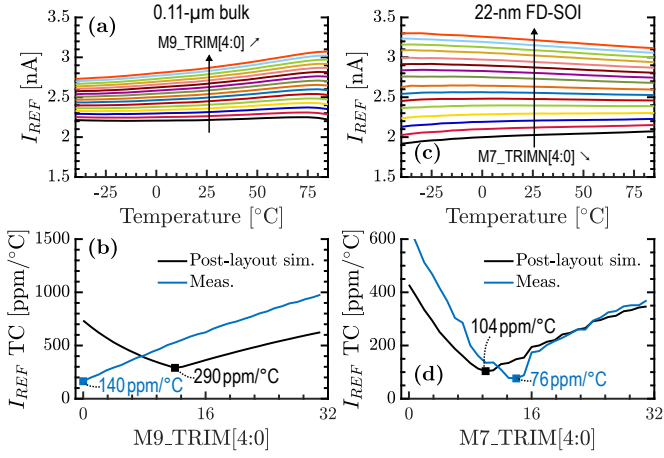

Fig. 4.53 In UMC 0.11-μm bulk and GF 22-nm FD-SOI, and for the die with the best TC, (a)(c) measurement of the temperature dependence I_{REF} for all calibration codes at 1.2 V in 0.11 μm and 1.8 V in 22 nm, and (b)(d) I_{REF} TC as a function of the calibration code in TT post-layout simulation and in measurement.

edges of the calibration range. Fig. 4.52(b), when compared to Fig. 4.52(a), indicates that the dies originate from a fast nMOS process corner, either FF or FS, as

already suggested by the larger power consumption at high temperature observed in Fig. 4.44(a). The die that fails to reach a TC around 200 ppm/°C as the others corresponds to the outlier in Fig. 4.42(f). Next, the histogram of the measured calibration code yielding the minimum I_{REF} TC in Fig. 4.52(c) shows that the optimal code lies between 0 and 4 for the batch of dies that has been measured, with the spread originating from local mismatch as well as global process variations. Finally, Figs. 4.53(a) and (b) reveal that, for the die with the best TC, I_{REF} predominantly presents a PTAT behavior [Fig. 4.53(a)], and attains a minimum TC of 140 ppm/°C compared to 290 ppm/°C in the TT post-layout simulation, likely due to the ESD diode leakage at high temperature.

In GF 22 nm, Fig. 4.52(d) shows that the optimal calibration codes in the five conventional process corners are less scattered than in 0.11 μm. In this technology, the calibration range is rather defined by skewed process corners, as discussed in Fig. 4.47. In measurements, the curves depicting the TC of I_{REF} vs. the calibration code in Fig. 4.52(e) are really close to post-layout simulations, and the optimal calibration code is comprised between 9 and 18 [Fig. 4.52(f)]. For the die with the best TC, the temperature dependence of I_{REF} can be either CTAT or PTAT [Fig. 4.53(c)], and the measured 76-ppm/°C TC is in close agreement with the 104-ppm/°C TT post-layout simulated value [Fig. 4.53(d)].

Table 4.9 Comparison table of temperature-independent nA-range current references.

	Far [96]	Cordova [89]	Santamaria [99]	Agarwal [81]	Aminzadeh [133]	Mahmoudi [127]	Bruni [76]	Huang [90]	Yang [68]	De Vita [71]	Kayahan [94]	Ji [39]	Wang [67]	Wang [40]	Huang [41]	Lee [144]	Chang [45]	Shetty [31]	Lefebvre [165]	**Lefebvre This work**	
Publication	ROPEC	ISCAS	ISCAS	TCAS-II	AEU		CAE	AEU	AEU	ISCAS	TCAS-I	ISSCC	VLSI-DAT	TCAS-I	TCAS-II	JSSC	JJAP	TCAS-I	JSSC	JSSC	
Year	2015	2017	2019	2022	2022	2022	2023	2023	2023	2007	2013	2017	2019	2019	2020	2020	2022	2022	2023	2024	
Type of work	**Simulations**									**Silicon measurements**											
Samples	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	20	90	10	10	16	10	10	3	10	20	11	11
Technology	0.18μm	0.18μm	0.18μm	0.18μm	0.18μm	0.13μm	0.18μm	0.18μm	0.18μm	0.35μm	0.35μm	0.18μm	0.18μm	0.18μm	0.18μm	0.18μm	90nm	0.13μm	22nm	0.11μm	22nm
I_{REF} [nA]	14	10.9	2.7	5.6	6.7	6.6	6.3	8.9	1.96	9.1	25	6.7	6.5	9.8	11.6	1	1.3	1.9	1.25/0.9*	2.4/2.3*	2.5/2.5*
Power [nW]	150	30.5	26	9.5	51	3.7	3.3	0.05	9.2	54.8	28500	9.3	15.8	28	48.6	4.5/14	8.6	10.2	7.8/5.8*	11.0/11.1*	10.3/10.4*
	@1V	@0.9V	@2V	@0.55V	@1V	@0.4V	@0.6V	@0.8V	@0.55V	@1.5V	@5V	@N/A	@0.85V	@0.7V	@0.8V	@1.5V	@0.75V	@0.85V	@0.9V	@0.8V	@1V
Area [mm^2]	**0.0102**	**0.01**	**0.0093**	0.032	**0.46**	**0.0021**	**0.0018**	**0.008**	**0.0033**	0.035	**0.0053**	**0.055**	**0.062**	**0.055**	**0.054**	**0.332**	0.0175	0.0163	0.0132	**0.0106**	**0.00255**
Supply range [V]	1 – 3.3	0.9 – 1.8	2 – 3.63◇	0.55 – 1.9	1.1 – 1.8	0.4 – 1.6	0.6 – 1.8	0.8 – 1.8	0.55 – 1.8	1.5 – 4	N/A	1.3 – 1.8	0.85 – 2	0.7 – 1.2	0.8 – 2	1.5 – 2	0.75 – 1.55	0.85 – 2	0.9 – 1.8	0.8 – 1.2	1 – 1.8
LS [%/V]	**0.1**	**0.54**	**8.9**◇	**0.022**	**0.03**	2.7	**12.1**	1.39	**0.2**	**0.57**	**150**	1.16	4.15	**0.6**	1.08	1.4	**0.15**	4	**0.26**/**0.39***	2.07/2.23*	**0.26**/1.53*
Temp. range [°C]	0 – 70	-20 – 120	-40 – 125	-30 – 70	-40 – 120	-40 – 120	-40 – 120	0 – 125	0 – 100	0 – 80	0 – 80	0 – 110	-10 – 100	-40 – 125	-40 – 120	-20 – 80	0 – 120	-40 – 120	-40 – 85	-40 – 85	-40 – 85
TC [ppm/°C]	**20**	**108**	309	256	**40.3**	308	219	**139**	**96.8**	**44**	**128**/250*	**680**/283†	**157**	**150**	**169**	289/265◇	**53**/394*	530/**822***	**203**/565*	290/**176***	**101**/**82***
TC type	Typ.	μ	μ	μ	μ	μ	Typ.	μ	μ	μ	N/A	μ	μ	μ	μ	μ	μ	μ	μ	μ	μ
I_{REF} var. (process) [%]	N/A	15.8 / 11.6†	N/A	+55.4 / -28.5◇	N/A	N/A	+129.1 / -61.8◇	+2.8 / -13.9◇	8.7	2.16	8/1.22*	N/A	N/A	+11.7 / -8.7◇	+17.6 / -10.3◇	N/A	21.1	N/A	+9.9 / -9.5	+34.8 / -25.9	+15.9 / -8.3
I_{REF} var. (mismatch) [%]	5.8	N/A	**20.3**	**10.4**	**0.7**	**6.1**	N/A	2.6	1.7		1.4	4.07/1.19*	3.33	1.6	4.3	1.26/**0.25**†		**15.6**	**6.39**/**9.20***	1.74/3.47*	2.41/2.55*
Trimming	No	Yes	No	No	No	Yes	No	Yes	No	No	No	Yes	No	Yes	Yes	Yes	Yes	Yes	No	Yes	Yes
Spec. components	No	Native	No	Res.	Res., **BJT**	No	No	No	No	No	No	Res., **BJT**	No	Res.	Res.	No	No	Res.	No	No	No
FoM [ppm/°C^2×mm^2]	**0.0029**	**0.0077**	0.0174	0.0819	0.1159	**0.0040**	**0.0025**	**0.0089**	**0.0032**	0.0193	0.0166	0.1415	0.0887	0.0499	0.0570	0.9595	0.0575	0.0835	0.0597	0.0149	**0.0017**

* Simulated and measured values. † Before and after trimming. ◇ Estimated from figures. ▷ For 25 and 2.5 minutes between two calibrations.

4.2.4 Comparison to the State of the Art

In this section, we compare our work to the state of the art of simulated and fabricated nA-range CWT current references. Table 4.9 summarizes the performance of each reference, while Fig. 4.54 provides a graphical representation of the temperature dependence and silicon area across different current levels, using the figure of merit (FoM) (1.12) introduced in Chapter 1 combining these two characteristics. This FoM shares some similarities with the one proposed in [24] in the context of voltage references, given by

$$\text{FoM}_2 = \frac{(T_{\max} - T_{\min})^2}{\text{TC} \times \text{Power} \times \text{Area}} \times \frac{1}{10^{21}} \left[^\circ\text{C}^3/(\text{W} \times \text{mm}^2)\right], \tag{4.24}$$

and later used for current references in [31]. However, the proposed FoM must be minimized instead of maximized, and removes the square on the temperature range as we do not believe it is relevant to put so much emphasis on this characteristic. First, the proposed designs uses more scaled technologies than in the state of the art, which predominantly features the 0.18-μm technology node. In practice, the reduction of Pelgrom's mismatch parameter A_{V_T} with the technology node [154] allows to reduce transistor dimensions and thus silicon area, while maintaining the same specification on variability. The use of FD-SOI also improves A_{V_T} compared to bulk by a factor between 1.5 and 1.7× [37]. Technologies with a subthreshold slope factor n close to unity are also beneficial, as the fast decrease of I_{DS} with V_{GS} in subthreshold allows to shorten transistors in the 4T voltage reference. Nonetheless, we did not normalize the silicon area to the technology node as (i) our 22-nm design is based on I/O devices whose 0.15-μm minimum length is comparable to a 0.18-μm technology, (ii) analog blocks do not benefit from scaling as much as digital ones, and (iii) this is not conventionally done in the literature and would be extremely complex to implement in a fair way. Besides, Fig. 4.54(a) highlights that calibrating I_{REF} TC improves the FoM of the proposed 0.11-μm and 22-nm designs by 1.9× and 3.8×, respectively, by reducing the TC while slightly increasing the silicon area [Fig. 4.54(b)]. Therefore, in what follows, we will focus on the designs with I_{REF} TC calibration as they present a better FoM value.

Next, compared to fabricated references in the literature, we obtain a 1.3× / 11.4× FoM reduction for the 0.11-μm and 22-nm designs compared to the closest measured competitor [71], achieving a 44-ppm/°C TC within a 0.035-mm^2 area. For both designs, the FoM improvement compared to [71] stems from the lower limit of the temperature range, decreased from 0 to -40°C, and the area reduction, as [71] relies on a somewhat-complex β-multiplier variant. Furthermore, [67, 40, 41] feature a TC around 150 ppm/°C that is competitive with the proposed designs, but exhibit a larger area above 0.05 mm^2, due to the use of resistors [40, 41] or massive transistors in deep subthreshold [67] as V-to-I converters. Finally, [165, 45, 31] occupy a silicon area between 0.01 and 0.02 mm^2 which is close to the proposed

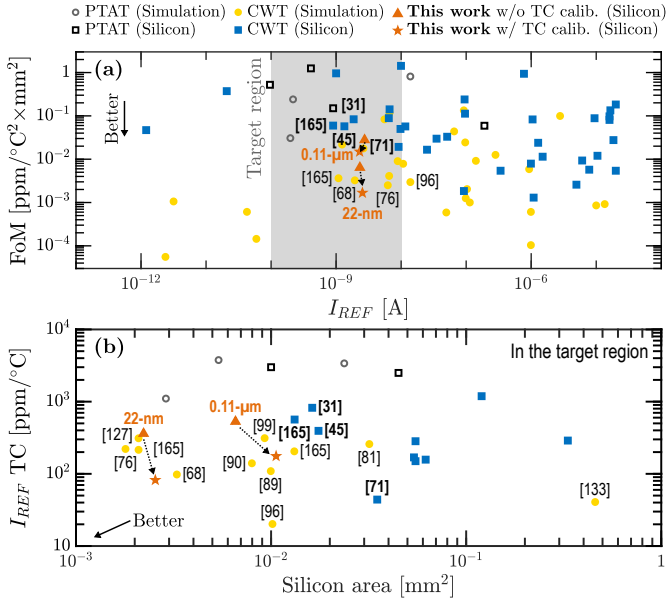

Fig. 4.54 (a) Figure of merit (1.12) combining temperature dependence and silicon area as a function of I_{REF}, and (b) trade-off between TC and area in the nA target region, based on the state of the art of current references.

designs, as [165] relies on an SCM biased by a modified β-multiplier, [45] on a gate-leakage transistor biased by a 6T voltage reference, and [31] on the weighted sum of PTAT and CTAT currents generated by BJT-based β-multipliers. Despite the area efficiency of these techniques, the I_{REF} TC is worse than in the proposed designs as these architectures do not embed any TC calibration circuit, whose addition would inevitably increase the area they occupy.

4.2.5 Conclusion

In this second part of Chapter 4, we demonstrated a nA-range CWT current reference based on an SCM biased by a PTAT voltage with a CWT offset. This bias voltage is generated by a 4T ULP voltage reference and buffered by a single transistor. This structure does not require a startup circuit, and can integrate two types of simple I_{REF} TC calibration circuits, which are key to maintain performance across process corners and to obtain a measured TC comparable with post-layout simulations. Then, we presented a methodology for sizing the proposed reference based on the ACM model and supported by post-layout simulations in 0.11-μm bulk and 22-nm FD-SOI. Lastly, we validated the proposed reference based on designs without and with I_{REF} TC calibration, fabricated in 0.11-μm bulk and 22-nm FD-SOI technologies, to prove that the body / back-gate effect can indeed be leveraged in

these two technology types. The designs with I_{REF} TC calibration achieve a 2.3-nA current with a 176-ppm/°C TC and a 2.23-%/V LS in 0.11-μm bulk, and a 2.5-nA current with a 82-ppm/°C TC and a 1.53-%/V LS in 22-nm FD-SOI. They demonstrate the high level of performance achieved by the proposed reference, as well as its portability to different technologies. In addition, the simplicity of the proposed architecture renders its sizing and implementation quite straightforward. Further work should however focus on reducing the power consumption of the 4T voltage reference at high temperature.

4.3 Take-Away Messages

In this chapter, we presented three V/R current reference topologies sharing the idea of generating a reference voltage using a simple 2T/4T ULP structure, whose output is buffered onto a V-to-I converter by a single transistor. It should be noted that, thanks to the use of this specific voltage reference topology, the proposed references present the advantage of being unstable at zero current, thereby suppressing the need for a startup circuit. The two first current references presented in Section 4.1 respectively use a resistor and an SCM as V-to-I converter, in order to generate a CWT μA-range and a PTAT nA-range currents. The μA-range reference biases a polysilicon resistor with a quasi-CWT voltage generated by a 2T voltage reference with different V_T types, and whose TC matches the TCR in order to reach temperature independence. It includes a 4-bit TC trimming circuit implemented by changing the effective width of a transistor in the 2T reference. In contrast, the nA-range reference biases an SCM with a purely PTAT voltage produced by a 2T voltage reference with the same V_T type but different widths, to obtain a PTAT current proportional to the specific sheet current I_{SQ}. This reference does not integrate any trimming mechanism. Next, the last of the three current references is detailed in Section 4.2 and combines the idea of employing an SCM biased by a PTAT voltage with a CWT offset voltage to generate a CWT current, introduced in Section 3.1, with the concept of using a few-transistor voltage reference buffered onto a V-to-I converter by a single transistor, presented in Section 4.1. It incorporates a 5-bit TC trimming circuit implemented by changing the effective width of a transistor in the 4T reference, thereby either changing the PTAT slope or the CWT offset voltage of the SCM's bias voltage.

These references were validated by silicon measurements in XFAB 0.18-μm PD-SOI for the two first references, and in UMC 0.11-μm bulk and GF 22-nm FD-SOI for the last reference. First, the CWT μA-range reference is measured across 10 dies and generates either a 0.99-μA current with a 0.20-%/V LS and a 290-ppm/°C CTAT TC without TC calibration, or a 1.09-μA current with a 0.21-%/V LS and 38-ppm/°C TC with TC calibration. They respectively consume 0.64 and 0.71 μW at 0.65 V and 25°C, while occupying silicon areas of 0.0034 and 0.0043 mm^2. The main drawback of this architecture is that the reference current can be significantly impacted by process variations of the transistors in the 2T voltage reference on one side and of the polysilicon resistor on the other side. A trimming circuit for I_{REF} might thus be necessary to achieve the required current. Second, the PTAT nA-range reference, also measured across 10 dies, generates a 0.096-nA current, the lowest to date for current references without gate-leakage transistors, while consuming only 0.28 nW at 0.55 V and 25°C. This reference current presents an LS of 1.48 %/V and has a footprint of 0.0087 mm^2. A potential problem with this architecture is to reach low temperatures without any nonideal behavior of the 2T

reference, due to the exacerbated impact of gate leakage and GIDL at these temperatures. In addition, it should be noted that the CWT μA-range and PTAT nA-range references were also validated through post-layout simulations in TSMC 65-nm bulk and STMicro 28-nm FD-SOI, to prove their portability to more scaled technologies, despite the analog non-idealities arising in these technology nodes. Finally, the CWT nA-range reference is measured across 11 dies in both 0.11-μm bulk and 22-nm FD-SOI, to prove that the body / back-gate effect can indeed be leveraged in these two technology types. The designs with I_{REF} TC calibration achieve a 2.3-nA current with a 176-ppm/°C TC and a 2.23-%/V LS in 0.11-μm bulk, and a 2.5-nA current with a 82-ppm/°C TC and a 1.53-%/V LS in 22-nm FD-SOI. They respectively consume 11.1 and 10.4 nW at 0.8 and 1 V, and at 25°C, with silicon areas of 0.0106 and 0.00255 mm^2.

In conclusion, the three proposed references are strikingly simple compared to existing references in the state of the art, especially given the level of performance they are able to achieve. This simplicity has two direct benefits: (i) the design time is reduced as a consequence of the lower design complexity and (ii) the silicon area can be significantly scaled down as the sub-circuits constituting the current reference are brought to their simplest form. However, the common drawback of all three proposed references is the steep power consumption increase at high temperature, resulting from the fact that the 2T voltage reference's power consumption is linked with the drain-to-source leakage. Mitigating the power consumption at high temperature is certainly a research direction worth investigating in future works.

Based on the results of this chapter and of the previous one, we identify two additional claims which will be detailed in the conclusion of this thesis:

1. *In the nA range, SCM-based references offer the best area efficiency and a TC of I_{REF} between 100 and 500 ppm/°C, while resistor-based references present a larger area than their SCM counterparts, but allow to reach a sub-100-ppm/°C TC.*
2. *V / R references implemented with a 2T voltage reference and a 1T buffer allow to generate a wide range of current levels and temperature behaviors, depending on the TC of the reference voltage and the choice of V-to-I converter.*

5

Discussion of the Applications of CWT Current References

Technology is so much fun but we can drown in our technology.
The fog of information can drive out knowledge.
– Daniel J. Boorstin

EVALUATING the relevance of a technical innovation with respect to its potential applications is an important step that is too often missing in the context of current references. Admittedly, this is not a simple task as it requires to better understand the analog circuits using these current references and the applicative context in which they are operating. In this chapter, we attempt to fill in this gap by discussing some leads of answers to the third research question laid out in the introduction of this thesis, namely

Do these improvements bring meaningful benefits to the applications of current references mentioned in the state of the art ?

To do so, we rely on the corpus of constant-with-temperature (CWT) current reference papers formed in Chapter 1, to first identify which applicative contexts and specific analog circuits are targeted by current references in Section 5.1, and to then analyze which analog circuits actually require a CWT reference current in

Section 5.2. This chapter does not aim at presenting an exhaustive view of all the applications of CWT current references, but rather to identify the main cases in which the generation of a CWT current can be beneficial. To conclude this chapter, Section 5.3 summarizes our observations and shares some conclusions regarding the considered research question.

5.1 Study of the Reduced Corpus

5.1.1 About the Reduced Corpus

This chapter uses a reduced version of the corpus, obtained by imposing more stringent constraints on the origin of the papers than for the original corpus. All journal papers are conserved, but conference papers which do not originate from major conferences of the IEEE societies dedicated to circuits and systems (CAS) and solid-state circuits (SSCS) are discarded. This results in a reduced corpus of 78 papers, compared to 114 papers for the original one. Fig. 5.1(a) indicates from which journal or conference the papers of the reduced corpus are coming from, but excludes journals and conferences which only appear once. This bar chart informs us that the overwhelming majority of the papers originates from the CAS society (47 papers), followed by the SSCS society (9 papers), and then by other editors.

5.1.2 Applicative Contexts of Current References

First, we try to identify the applications in which CWT current references are used, before commenting on the relevance of using such current references in these contexts. The bar chart in Fig. 5.1(b) summarizes the applications mentioned in the reduced corpus, which spans the years 2000 to 2023. It should be noted that a single paper can mention more than one applicative context. A first observation is that, during this time period, the main context to be mentioned is unsurprisingly the Internet of Things (IoT), with 27 papers, and the development of the wireless sensor nodes (WSNs) required to implement it, with 25 papers. Environmental monitoring, which can be seen as a more specific IoT application, is also quite popular with 9 papers. As already discussed in Chapter 2, the IoT is characterized by a diversity of applications with different specifications on supply voltage and temperature variations. IoT sensor nodes must therefore be able to cope with a wide range of conditions, and striving for the generation of a reference current with little sensitivity to temperature variations appears as a relevant target. The temperature range to be considered can either be the industrial temperature range, i.e., -40 to 85°C, or the extended temperature range, i.e., -40 to 125°C.

Then, another context which elicits the interest of current references' designers (22 papers) is biomedical devices, which include implantable medical devices (IMDs) such as pacemakers, cochlear implants, gastric simulators, etc, and wearable devices, such as fitness trackers and blood pressure, glucose and electrocardiogram (ECG) monitors. In the context of IMDs, targeting a CWT current does not make sense as the internal temperature of the body is regulated around 37°C with variations of less than 1°C. In contrast, wearables must be able to cope with a larger temperature range which is however limited by the fact that a person is wearing the device. A reduced range from -20 to 50°C is thus often sufficient, and large temperature ranges as the ones used for IoT devices are not of particular interest.

Finally, other applicative contexts include automative and aeronautics, for which a broad temperature range can be required due to extreme operating conditions, harsh environments, or heating effects from the engines or power electronic devices. For some circuits, a temperature range beyond the extended industrial range can be required. Furthermore, applications such as smartphones and smart homes are akin to wearable devices, as their operating conditions must often be withstandable by humans, leading to a limited temperature range.

In conclusion, the applicative contexts mentioned for current references can be divided into four categories. First, applications in which temperature variations are negligible, e.g., IMDs, and for which a CWT current reference is not necessary. Then, applications related to human activities, in which devices must be able to operate over a temperature range that can be withstood by a human being. Wearables, smartphones and smart homes fall into this category, and can operate with a relaxed constraint on the TC. Next, a third category corresponds to applications in which devices must operate over the conventional or extended industrial temperature range to collect information in conditions that a human cannot support. IoT applications are a good example of this category, as sensor nodes generally have to cope with a wide range of operating conditions. A final category gathers applications in which devices must withstand particularly harsh conditions, e.g., low temperatures in space applications, or high temperatures in contexts in which an engine or industrial machine generates a large amount of heat.

5.2 Analysis of Specific Analog Circuits

In this section, we focus on the analog circuits utilizing current references and determine which of them necessitate a CWT bias current. This analysis consists of two steps. First, to identify the analog blocks mentioned in the reduced corpus, and then, to analyze these specific blocks based on the papers referenced in the reduced corpus and additional resources, to understand if they require a CWT current or not. The first step is illustrated in Fig. 5.2, with Fig. 5.2(a) depicting a bar

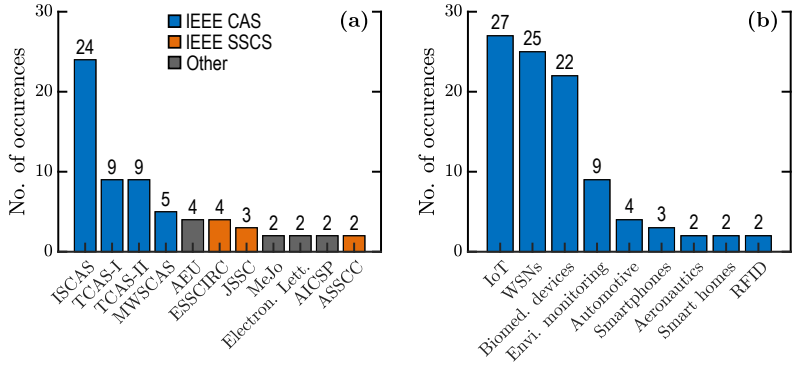

Fig. 5.1 Bar charts summarizing (a) the origin of the journal and conference papers considered in the reduced corpus, and (b) the applicative contexts mentioned for current references in the papers of the reduced corpus. The acronyms of the conferences and journals in (a) are the following: International Symposium on Circuits and Circuits (ISCAS), Transactions on Circuits and Systems I: Regular Papers (TCAS-I), Transactions on Circuits and Systems II: Express Briefs (TCAS-II), Midwest Symposium on Circuits and Systems (MWSCAS), AEU - International Journal of Electronics and Communications (AEU), European Conference on Solid-State Circuits (ESSCIRC), Journal of Solid-State Circuits (JSSC), Microelectronics Journal (MeJo), Analog Integrated Circuits and Signal Processing (AICSP), Asian Solid-State Circuits Conference (ASSCC).

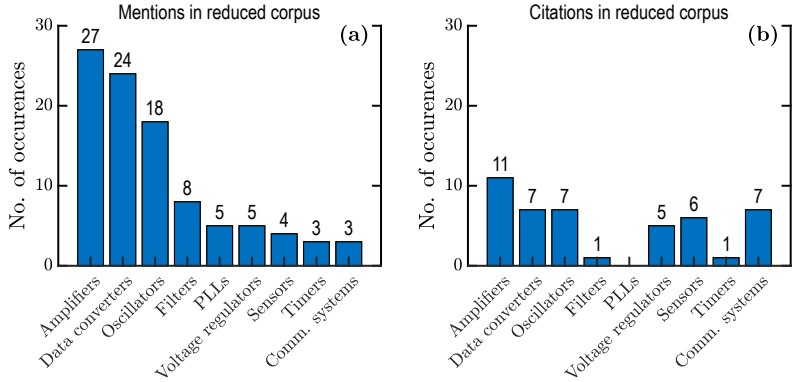

Fig. 5.2 Bar charts summarizing (a) the mentions to specific analog circuits and (b) the citations related to these specific analog circuits, in the reduced corpus.

chart of the analog circuit blocks mentioned to be using a CWT current reference. The three most mentioned analog circuits are amplifiers, data converters, and oscillators. Moreover, we examine the papers referenced in the reduced corpus. Only 29 papers of the reduced corpus cite some references related to applications or analog blocks using current references, leading to a total of 64 referenced papers. 19 of them do not focus on analog blocks, but rather on the applicative context, for example the IoT [170, 14, 15, 171, 17] or biomedical devices [172, 173, 174, 175], on energy harvesting [176, 177, 178, 17, 179], or on analog techniques for ultra-low-

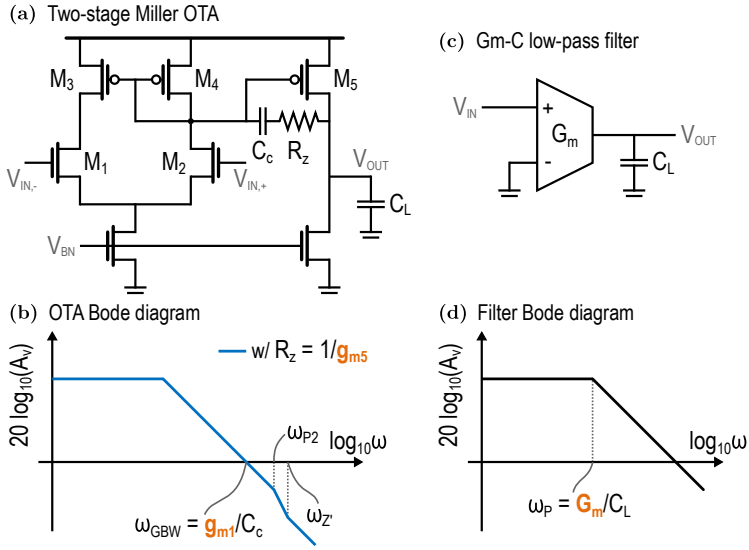

Fig. 5.3 (a) Conventional two-stage Miller OTA with Miller compensation capacitor C_c and nulling resistor R_z. (b) Frequency response of the Miller OTA with nulling resistor R_z, highlighting the fact that the gain-bandwidth (GBW) product is related to g_{m1}, and that the nulling resistor is usually chosen to be $R_z = 1/g_{m5}$, in order to push the zero at high frequency. In practice, it is often a more robust solution to push this zero at higher frequency. (c) Conventional G_m-C first-order low-pass filter and (d) its frequency response, featuring a pole linked to G_m.

power (ULP) operation [180, 181, 182, 183, 184]. Hence, they will not be discussed into details in this thesis. Fig. 5.2(b) summarizes the topics of the referenced papers related to specific analog blocks. The three most referenced topics are the same as in Fig. 5.2(a), but Fig. 5.2(b) also indicates the presence of several papers related to voltage regulators, sensors and sensor interfaces, and communication systems, as well as the quasi absence of papers related to filters, phase-locked loops (PLLs), and timers.

5.2.1 Amplifiers and Filters

Operational transconductance amplifiers (OTAs) are the backbone of analog circuits, and IoT sensor nodes are no exception to this. In the case of OTAs, such as the two-stage Miller OTA depicted in Fig. 5.3(a), the performance that needs to be made CWT is the gain-bandwidth (GBW) product, sometimes also called the transition frequency. For the two-stage Miller OTA, which will be used as an example, the GBW is given by $\omega_{\text{GBW}} = g_{m1}/C_c$, as illustrated in the frequency response in Fig. 5.3(b), where g_{m1} is the transconductance of the differential pair and C_c is the Miller compensation capacitor. As capacitance presents negligible

dependence to temperature, a constant-bandwidth OTA is obtained by biasing it with a current providing a constant g_m. As already discussed in Chapter 1, when OTAs are operated in weak inversion, the transconductance is given by $g_m = I_{DS}/(nU_T)$, where I_{DS} is the drain-to-source current, n is the subthreshold slope factor, and U_T is the thermal voltage. Therefore, a temperature-independent g_m is obtained when biasing weak-inversion transistors with a proportional-to-absolute-temperature (PTAT) current reference, which is why such current references are also referred to as constant-g_m references. In addition, some frequency compensation techniques rely on the value of the g_m, such as the nulling resistor $R_z = 1/g_{m5}$ employed in Figs. 5.3(a) and (b) used to push the unstable zero of the Miller OTA to high frequency. Among the papers referenced in the reduced corpus, several of them present OTAs [185, 186, 187, 188, 189, 147, 190]. They feature a bandwidth in the kHz range, lying between 0.25 and 307 kHz, and a nW-range power consumption, comprised between 2.4 nW and 1.57 μW, compatible with the power constraints of IoT sensor nodes. A handful of papers also discuss biopotential amplifiers for electrocardiogram (ECG) or electroencephalogram (EEG) applications [148, 191, 192], characterized by a larger power consumption compared to conventional OTAs as they are designed with much more stringent constraints on intrinsic noise to properly sense the biopotential signals.

Two other types of analog circuits also require a PTAT or constant-g_m biasing. First, continous-time voltage comparators need their delay to be made CWT. However, when the comparator is biased by a CWT current, this delay typically presents a PTAT dependence. Biasing the comparator with a PTAT current solves this issue and renders the delay approximately CWT. Nevertheless, the example of comparators referenced in the reduced corpus, namely [193], is not a relevant application of current references as it consists of digital standard cells and hence does not require any reference current. Second, analog continuous-time filters often rely on a G_m-C implementation, as illustrated in Fig. 5.3(c) for a basic first-order low-pass filter (LPF). This case can be assimilated to the case of an OTA, as the poles are also directly related to the G_m. An example of such a filter is provided in the context of biomedical applications in [194].

5.2.2 Data Converters

Another category of analog circuits that can be found in a wide variety of electronic systems is data converters, which can be divided into analog-to-digital converters (ADCs) [195, 196, 197, 198] and digital-to-analog converters (DACs) [199, 200, 201]. The papers referenced in our reduced corpus are far from encompassing the numerous architectures that have been proposed over the years, but rather highlight some data converter topologies potentially necessitating a CWT reference current. Let us start this discussion with the DAC topologies illustrated in Figs. 5.4(a) and (b). A topology which obviously requires a reference current is the current-steering

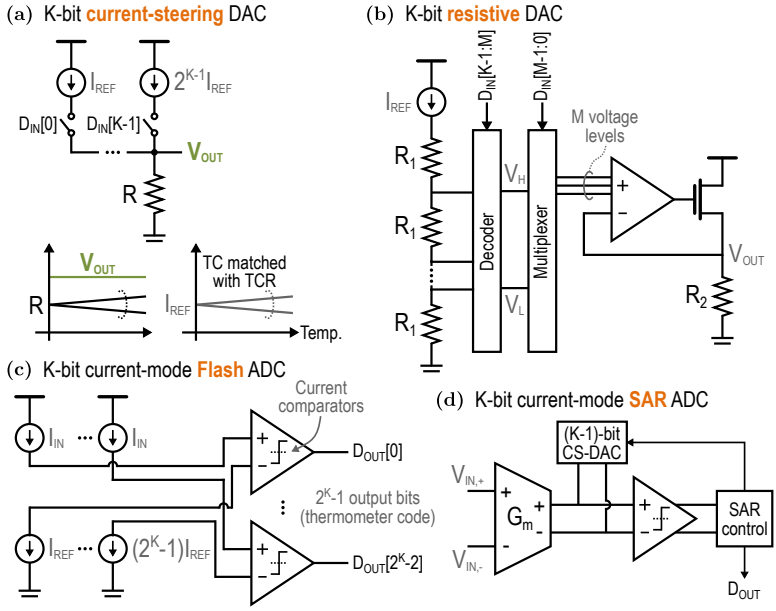

Fig. 5.4 Digital-to-analog converters (DACs) utilizing a reference current I_{REF}, either (a) in a current-steering (CS) DAC or (b) in a resistive DAC. Current-mode analog-to-digital converters (ADCs) using I_{REF} in (c) a Flash ADC or (d) a successive approximation (SAR) ADC.

(CS) DAC [Fig. 5.4(a)], in which a current controlled by a K-bit digital input D_{IN} flows through a resistor to generate an analog output voltage V_{OUT} [199, 200]. The control signal used to tune the current can either be binary [199] or, in less frequent instances, ternary [200]. In this topology, a reference current whose TC matches the temperature coefficient of resistance (TCR) is required to produce a CWT V_{OUT}, rather than a truly CWT current. Another possible option is to make the resistance CWT by using the series connection of two different resistor types with opposite TCs, in which case I_{REF} also needs to be CWT. The same conclusion holds true for the resistive DAC topology shown in Fig. 5.4(b), in which the output voltage is coarsely tuned by $(K - M)$ bits in the voltage decoder, and finely tuned by M bits in the multiplexer, thereby defining M voltage levels passed to a resistance interpolation stage at the input of the OTA [201].

Moving on to ADC topologies, the current-mode Flash ADC [195] depicted in Fig. 5.4(c) evidently requires a reference current, as its operation is based on the direct comparison between an input current I_{IN} and a reference current I_{REF}. Multiplications by factors ranging from 1 to $2^K - 1$ are required in order to generate a thermometer-code digital output D_{OUT} consisting of $2^K - 1$ bits, produced by the same number of current comparators. In this topology, the temperature dependence of the ADC is only as good as the TC of I_{REF}, thus making it a critical requirement. Similarly, a current-mode successive approximation (SAR) ADC [196]

similar to the one shown in Fig. 5.4(d) can also benefit from a CWT current as it relies on a current-steering DAC to offset the differential input current, in order to conduct the binary search algorithm generating the digital output. Finally, [197] presents a 10-bit single-slope (SS) ADC making use of a current ramp, generated by a 20-nA I_{REF} from a bandgap reference. In this case, the TC of I_{REF} need to match the TC of the frequency used in the counter, so we hypothesize that a CWT current would be the simplest solution, despite the fact that temperature variations are not considered in this work. Even though the performance of the ADCs in [195, 196] are not aligned with the constraints of IoT sensor nodes, respectively with sampling rates of 3.3 GS/s and 50 MS/s and power consumptions of 1.3 and 6 mW, their operation principle remains valid for IoT nodes. The technical performance achieved by the 12-bit SAR-assisted digital-slope ADC presented in [198] is better suited to the needs of IoT sensor nodes, with a sampling rate of 20 kS/s and a power consumption of 330 nW, albeit this architecture does not require a reference current.

5.2.3 Oscillators

In the context of IoT sensor nodes, low-frequency oscillators are often used for real-time clock (RTC) generators or wake-up timers, and two main architectures are considered to implement oscillators on chip: current-starved ring oscillators (CSROs) and relaxation oscillators. Crystal-based and LC oscillators are not discussed here as the former require a quartz crystal as external component, and the latter consume too much power for an IoT sensor node. Besides, jitter is usually a concern in the context of oscillators, but this aspect will not be detailed here. In the papers referenced in the reduced corpus, only [202] and [203] are mentioned in relationship with CSROs, but they do not present a specific architecture. They instead compare existing CSRO architectures [202], and discuss the benefits of back-bias-controlled oscillators (BBCOs) with respect to CSROs. At first order, the frequency of a CSRO can be made CWT by using a CWT reference current, as demonstrated in [204], which features a 1.44-MHz clock with a 269-ppm/°C TC from -20 to 70°C, where a 27-nA I_{REF} with a 15.1-ppm/°C TC is obtained by the weighted sum of PTAT and complementary-to-absolute-temperature (CTAT) currents.

Nonetheless, the vast majority of oscillators employed by IoT sensor nodes are relaxation oscillators. [206, 205, 207, 208, 149] are referenced in the reduced corpus, while [209, 210, 150, 211, 212, 213, 214, 215] are added to refine our analysis, and the main techniques are shown in Fig. 5.5. First, a typical relaxation oscillator [Fig. 5.5(a)] is based on the charge of a capacitor C by a reference current I_{REF}. The comparison threshold for the comparator is obtained as the voltage drop V_{REF} generated by letting I_{REF} flow through a resistor R. In this topology, the TC of I_{REF} in itself does not matter, as the temperature dependence of the frequency originates from the temperature variations of the RC time constant and hence from the

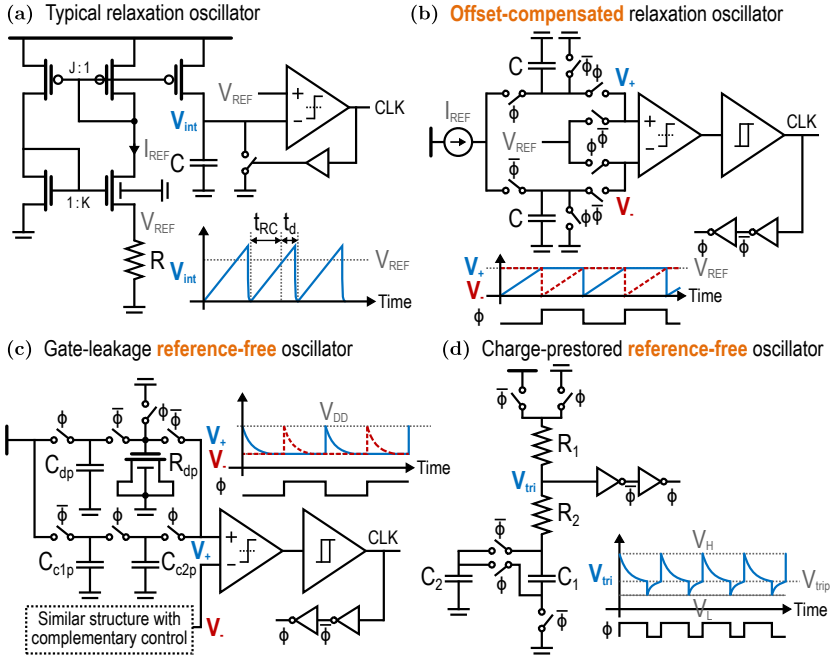

Fig. 5.5 (a) Typical relaxation oscillator based on a reference current I_{REF} charging a capacitor, with a threshold V_{REF} generated by letting I_{REF} flow through a resistor. The oscillation period is consequently related to the RC time constant. (b) Offset-compensated relaxation oscillator [205] which can either rely on CWT V_{REF} and I_{REF}, or on V_{REF} and I_{REF} with matched TCs. (c) Reference-free oscillator based on the discharge of a capacitor C_{dp} by a large equivalent resistance R_{dp}, implemented as a gate-leakage transistor. (d) Reference-free charge-prestored oscillator based on capacitors and temperature-compensated resistors.

TCR, given the temperature stability of capacitances. A first possibility to generate a temperature-independent frequency is thus to implement R with a temperature-compensated resistance. An alternative proposed in [206] consists in letting the PTAT behavior of the RC time constant t_{RC}, due to the use of a PTAT polysilicon (poly) resistor, compensate the CTAT behavior of the comparator's delay t_d, thereby making the frequency CWT. Another popular architecture presenting the benefit of compensating the comparator's offset [Fig. 5.5(b)] is proposed in [205]. In [205], a PTAT I_{REF} generated by a conventional β-multiplier structure is employed to charge the capacitors, to generate a reference voltage V_{REF} using a resistor, and to bias the comparator to make its delay CWT. [149] uses the same structure as [205], but instead produces independent CWT I_{REF} and V_{REF}, resulting in a 9.3-Hz clock frequency with a 1000-ppm/°C TC from -40 to 120°C. [150, 211] are variants of this architecture based on two comparators, both of them generating V_{REF} from I_{REF} using a temperature-compensated resistor, with a CWT I_{REF} even though not really necessary in [150], and a PTAT I_{REF} in [211]. The key idea in comparator-

based relaxation oscillators is therefore to use I_{REF} and V_{REF} with matched TCs, by generating V_{REF} from I_{REF} using a temperature-compensated resistance, as also observed in other relaxation oscillators such as [212, 213, 214, 209]. Using a CWT reference current is therefore not a strict requirement, as some oscillators based on a PTAT reference current have demonstrated a TC below 100 ppm/°C. Yet, this is a convenient choice as the same PTAT current can be used to bias the continuous-time comparator, hence featuring a CWT delay.

At last, reference-free oscillators, i.e., oscillators which can operate without any current nor voltage references, have emerged as an alternative to existing architectures. The topology introduced in [122, 42] is shown in Fig. 5.5(c) and uses a differential structure leveraging the discharge time of a capacitor $C_{dp/n}$ by a large equivalent resistance $R_{dp/n}$, implemented as a gate-leakage transistor. In addition, while a first structure connected to the positive input of the comparator implements this discharge, a non-zero threshold is generated at the negative input by a second structure with complementary control signals, using charge sharing between capacitors $C_{c1p/n}$ and $C_{c2p/n}$. During the opposite clock polarity, the roles of the two structures are exchanged. A 2.8-Hz clock with a 500-ppm/°C TC from -40 to 60°C is obtained using this technique. Another reference-free architecture proposed in [215] [Fig. 5.5(d)] exploits a charge-prestored oscillator based on time constants fixed by two capacitors and two temperature-compensated resistors. In this case, the clock frequency is much higher, with a 21.2-MHz oscillation frequency which only varies by 15.2 ppm/°C from -30 to 125°C.

5.2.4 Sensors and Interfaces

The reduced corpus references various types of sensors and interfaces. Firstly, [216] proposes an analog front-end (AFE) for ECG, EEG, and electromyogram (EMG) applications, based on an AC-coupled instrumentation amplifier (IA) with a current feedback. This work uses an on-chip bias current generator, likely a constant-g_m one, to maintain a constant bandwidth in the IA across the temperature range, as previously discussed in the context of OTAs. Second, [217] describes a sensor designed to detect the presence of leukaemic blood cells based on a frequency difference between two relaxation oscillators due to a change in capacitance. Following the discussion of relaxation oscillators hereabove, we can assert that this sensor likely requires a PTAT reference current to achieve a CWT comparator's delay. At last, [218] presents a sensor to monitor perishable goods based on the temperature characteristics of the current in weak-inversion MOSFETs. This sensor relies on the ratio between two weak-inversion currents computed by a translinear divider, which necessitates a CWT reference current as it outputs a current $I_{OUT} = I_{REF} \times (I_{D2}/I_{D1})$. Most of these sensors and interfaces thus require a constant-g_m reference as they make use of amplifiers or comparators.

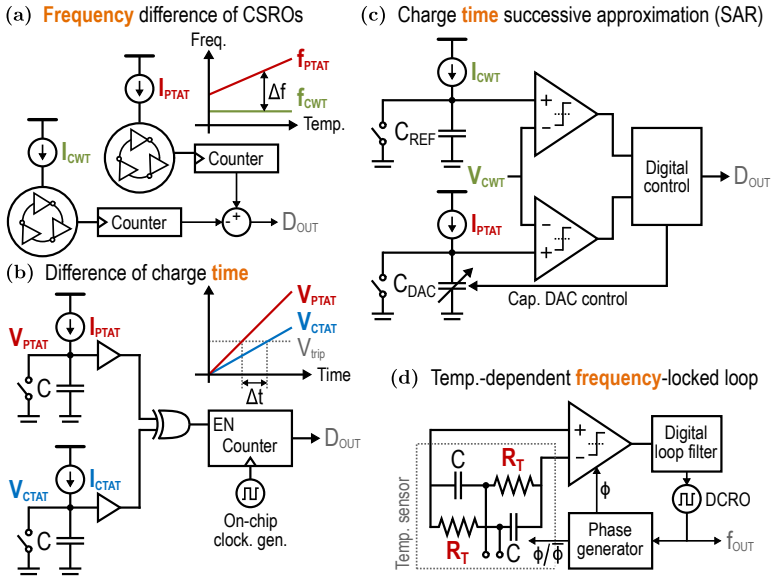

Fig. 5.6 Temperature sensors based (a) on the frequency difference of oscillation frequencies of current-starved ring oscillators (CSROs), (b) on the difference of charge time of capacitors, (c) on the successive approximation of the charge time of capacitors through a capacitive DAC, and (d) on the output of a temperature-dependent frequency-locked loop (FLL) stemming from the temperature dependence of a polysilicon resistor R_T.

Another type of sensor which is well represented in the reduced corpus is temperature sensors [219, 151, 220]. We add several recent works on this topic [221, 222, 223, 224, 225, 152, 226] to the papers referenced in the reduced corpus, in order to better understand the operation principles of these sensors. The main techniques used in MOS-based temperature sensors are depicted in Fig. 5.6. We choose not to discuss BJT-based temperature sensors as none of them are referenced in the reduced corpus. A first possibility to measure temperature is to generate two currents, a PTAT and a CWT one, and to let these currents influence the frequency of ROs, as shown in Fig. 5.6(a). The frequency difference between these two ROs, denoted as Δf, hence presents a temperature dependence and is translated into a digital code by subtracting the outputs of two counters clocked by the ROs. Other works leverage the temperature dependence of a single RO operated in weak inversion [222], or using zero-V_{GS} transistors as bias current sources [223], which results in a PTAT temperature dependence of the RO frequency. The second approach, illustrated in Fig. 5.6(b), shares similarities with Fig. 5.6(a) in the sense that two currents with different TCs are used, but replaces the ROs with current-to-time converters [220]. It indeed relies on the difference of charge times Δt between two identical capacitors C, respectively charged by a PTAT and a CTAT current. The proposed structure generates a pulse of duration Δt connected to the enable signal

of a digital counter clocked by an on-chip generator, thus allowing to convert the time difference into a digital code. [221] also relies on a time difference as a mean to measure temperature, more specifically on the temperature-dependent delay of an inverter supplied by a PTAT current. Next, a third solution represented in Fig. 5.6(c) retains the two currents with different TCs and the current-to-time converters, but implements a successive approximation algorithm to even out the charge time of the capacitors by modifying the capacitance charged by the PTAT current through a capacitive DAC [152, 226]. In [152], pA-range CWT and PTAT currents are used in conjunction with a CWT reference voltage, while in [226], a single pA-range CWT current is used with CWT and PTAT reference voltages, as they can be easily generated from 3T ULP voltage references. A final approach proposed in [224] relies on a frequency-locked loop (FLL) whose temperature dependence stems from the PTAT behavior of the P+ poly resistors used to implement R_T in the temperature sensor [Fig. 5.6(d)]. In this case, no reference current is required as the comparator is a clocked one, and the other circuits do not need any bias current. Another approach which we do not cover into details here digitizes a PTAT voltage generated as the ΔV_{GS} of diode-connected pMOS devices using a zoom ADC [225]. Based on this overview of MOS-based temperature sensors, we can conclude that a CWT reference current is not necessarily needed, as some effective solutions rely on two reference currents with opposite TCs, potentially resulting in a larger sensitivity to temperature [220], or do not require any reference current at all, but rather rely on the temperature dependence of passive elements [224]. We are not arguing that a CWT reference current would be useless in this context, but rather that the state of the art has evolved to dispense with such a current.

5.2.5 Other Applications

Several other applications are referenced as of potential interest for CWT current references. First, voltage regulators, split between linear regulators, such a low-dropout (LDO) regulators [227], and switching regulators, such as charge pumps [228, 229, 230] and DC/DC converters [231]. Despite a careful analysis of these papers, we fail to see the interest of a CWT reference current in this applicative context. Then, moving on to communication systems, the related papers in the reduced corpus discuss wake-up receivers [232, 233, 234], demodulators for binary phase-shift keying (BPSK) [235, 236, 237], and transmitters [238]. The BPSK demodulator in [237] is based on a reference current charging capacitors, so a CWT current would make sense in this context. Furthermore, the transmitter in [238] uses a CSRO, whose output frequency can be made temperature-independent at first order using a CWT current. Unfortunately, the other papers either require a bias current whose TC is not specified, or do not require a bias current at all.

Then, some referenced papers are the only ones to mention a specific application. [239] presents a time reference, obtained by comparing the voltage across

a capacitor charged by the current of a strong-inversion MOSFET, to a reference voltage whose TC compensates the TC of carrier mobility. Next, [240] presents a frequency-to-voltage converter based on a CWT current charging a capacitor. [241, 242] respectively propose a physical unclonable function based on a 2T voltage divider, and current-starved cross-coupled inverter rings used to emulate chaotic and neural-like dynamics. In both of these applications, it is not clear whether temperature independence of a given performance is sought and how a CWT reference would be helpful in doing so.

5.3 Take-Away Messages

Based on this overview of the analog circuits employing current references, and the applicative contexts in which they are operating, we can pinpoint a series of observations. Regarding the analog blocks relying on current references, we can partition them in three groups: (i) circuits which do not require a CWT I_{REF}, (ii) circuits which can rely on a CWT I_{REF} but for which there exists effective alternatives allowing to cope with the absence of a CWT I_{REF}, and (iii) circuits which cannot work without a CWT I_{REF}. The first category primarily consists of amplifiers, comparators, and filters, for which a constant-g_m, i.e., a PTAT current, is required by weak-inversion implementations to achieve a temperature-independent bandwidth, to realize frequency compensation techniques based on the value of the transconductance g_m, or to achieve a CWT delay. All the circuits making extensive use of digital standard cells also fall into this category, as they do not even require a reference current. Then, the second category regroups MOS-based oscillators and temperature sensors, which can be based on a CWT I_{REF}, but for which recent advances allow to realize the same functionality without such a reference current. Examples of these alternatives examined in this thesis are reference-free relaxation oscillators [122, 42, 215], or temperature sensors based on PTAT and CTAT currents [220], or on the PTAT behavior of poly resistors [224]. We do not believe that a CWT I_{REF} is useless in this second category of circuits, but rather that the satisfactory performance attained by alternative architectures strongly reduces the incentives to conduct further research on architectures based on a CWT I_{REF}. Finally, the third category is constituted of circuits in which the reference current has a direct impact on the performance and, by that, on its temperature dependence. Current-mode ADCs are probably the best example of such circuits, as input currents are directly compared to the reference current to generate a digital output. Current-steering DACs do not require a CWT I_{REF} per se, but could be placed in this category as well, given that they require a quasi-CWT I_{REF} whose TC matches the TC of the resistance used to convert the current into an analog output voltage. Some other specific circuits, predominantly relying on a reference current charging

a capacitor, can be added to this category, but they belong to a wide variety of analog circuits. Therefore, a first important conclusion of this analysis is that the analog circuits requiring of CWT I_{REF} are far less numerous than traditionally claimed in the literature. This conclusion is rather surprising given that the referenced papers exclusively originate from works dealing with CWT current references.

Moving on with the applicative contexts typically mentioned for current references, temperature independence appears as a less critical feature in applications in which devices operate in close proximity with humans, such as wearables, smartphones, smart homes, etc, as they are usually characterized by a reduced temperature range compared to industrial applications. This statement is even more true in the context of IMDs, as they operate in a temperature-regulated environment. Yet, in the context of IoT sensor nodes, temperature independence of the circuit performance remains relevant, but could probably be alleviated if the applicative needs were better understood by circuit designers. A second conclusion of our analysis is thus that, in our opinion, applicative requirements are not sufficiently apprehended by circuit designers, who sometimes spend too much time on the development of new circuit architectures and techniques rather than on the context in which these circuits are going to be used. More specifically, we observe a mismatch between the claimed utility of the proposed circuit developments, and the actual benefits they could potentially deliver in their applicative context.

Conclusions and Perspectives

Science can amuse and fascinate us all,
but it is engineering that changes the world.
– Isaac Asimov

In this thesis, our objective was to develop novel current reference architectures that are better suited to the needs of Internet-of-Things (IoT) sensor nodes, either by improving existing architectures or by introducing some new concepts. To do so, we approached this objective by successively considering the following research questions, formulated in the introduction of this thesis and used throughout the chapters of this whole manuscript:

1. *What are the specific requirements for current references in the context of the IoT ?*
2. *How can we practically modify existing current references to meet the specific requirements of the IoT ?*
3. *Do these improvements bring meaningful benefits to the applications of current references mentioned in the state of the art ?*

First, we delved into the state of the art of constant-with-temperature (CWT) current references based on a corpus of 114 papers from the time period 2000-2023. This corpus allowed us to provide partial answers to the first research question in Chapters 1 and 2, and to the third one in Chapter 5. It also brought to light a few uncertainties and information that current reference designers should be aware of for further works, and which will be discussed in these conclusions. In addition, we dived into the design of several types of current references in Chapters 3 and 4, predominantly nA-range current references characterized by their simplicity, area efficiency, and low temperature coefficient (TC). We can now take a step back and provide several conclusions and guidelines regarding the design of such references, thereby providing several answers to the second research question.

Table 6.1 Summary of the applications, measured performance, and limitations of the current references proposed in this thesis.

Type	**CWT μA-range ref.**	**CWT nA-range ref.**				**PTAT nA-range ref.**
Applications	Constant-current biasing of IoT nodes in active mode	Biasing of size-constrained biomedical devices (untrimmed) Constant-current biasing of IoT nodes in sleep mode, or in active mode at the extreme edge - Untrimmed: Any mixed-signal circuit - Trimmed: Current-mode data converters, oscillators, temperature sensors, some sensor interfaces				Constant-g_m biasing of IoT nodes in sleep mode, or in active mode at the extreme edge
Publication	Section 4.1 TCAS-I	Section 3.2 JSSC	Section 3.1 ESSCIRC, JSSC	Section 4.2 JSSC		Section 4.1 TCAS-I
Year	2022	2024	2022, 2023	2024		2022
Number of samples	10	11	20	11	11	10
V-to-I converter Bias voltage	Resistor CWT	Resistor CWT	SCM PTAT with CWT offset	SCM PTAT with CWT offset	SCM PTAT with CWT offset	SCM PTAT
Technology	0.18 μm PD-SOI	22 nm FD-SOI	22 nm FD-SOI	0.11 μm bulk	22 nm FD-SOI	0.18 μm PD-SOI
I_{REF} [nA]	990 / 1090*	1.12 / 1.50†	0.9	2.74 / 2.30*	2.32 / 2.54*	0.096
Power [nW]	640 / 710* @0.65 V	2.87 @0.75 V	5.81 @0.9 V	12.65 / 11.06* @0.8 V	9.40 / 10.39* @1 V	0.282 @0.55 V
Area [mm^2]	0.0034 / 0.0043*	0.00214	0.0132	0.00657 / 0.01061*	0.00222 / 0.00255*	0.0087
Supply range [V]	0.65 – 1.8	0.75 – 1.8	0.9 – 1.8	0.8 – 1.2	1 – 1.8	0.55 – 1.8
LS [%/V]	0.20 / 0.21*	0.51	0.39	2.60 / 2.23*	1.47 / 1.53*	1.48
Temperature range [°C]	-40 – 85	-40 – 85	-40 – 85	-40 – 85	-40 – 85	-40 – 85
TC [ppm/°C]	290 / 38*	169 / 89†	565	530 / 176*	361 / 82*	7500
I_{REF} var. (process)◇ [%]	+33.3 / -25.9	+0.21 / -0.54	+9.9 / -9.5	+34.8 / -25.9	+15.9 / -8.3	+14.5 / -15.6
I_{REF} var. (mismatch) [%]	0.65 / 0.87*	4.10 / 0.61†	9.20	2.11 / 3.47*	2.48 / 2.55*	1.66
99-% startup time [ms]	5▷	11.96	456▷	17.53 / 18.22*	11.56 / 11.20*	238▷
Trimming	TC (4b)	TC (4b), I_{REF} (8b)	No	TC (5b)	TC (5b)	No
Special components	Resistor	Resistor	No	No	No	No
Limitations	- Large power consumption of the 2T voltage ref. at high temp. - Startup time impeding duty cycling - Costly two-point TC trimming per batch	- Large power consumption of the 2T voltage ref. at high temp. - Costly two-point TC trimming + one-point I_{REF} trimming of each ref.	- TC trimming necessary but difficult to integrate in this topology - Relatively long startup time, even for an always-on ref.	- Large power consumption of the 2T voltage ref. at high temp. - Costly two-point TC trimming of each ref.		- Large power consumption of the 2T voltage ref. at high temp. - Nonideal behavior at low temp. (gate leakage, GIDL)

* Current reference without and with TC trimming. † Before and after trimming. ◇ Post-layout simulation results in process corners. ▷ Post-layout RCC simulation results in typical corner (TT, 1.8 V, 25°C).

Establishing Current References' Specifications

Let us first focus on our analysis of the state of the art of CWT current references based on the corpus of papers from Chapter 1, and state our two major findings.

Claim 1 *Current references well-suited to the needs of IoT sensor nodes should produce a current in the nA range, as well as be temperature-independent and area-efficient.*

In Chapter 2, we established that the power budget available to sensor nodes with a 10-year lifetime for batteries and a 1-cm maximum dimension for energy harvesters was comprised between 0.1 and 100 μW. The lower end of the range consists of extreme-edge sensor nodes or millimeter-sized devices [14], and the upper end of the range, of devices such as ultra-low-power (ULP) micro-controller units (MCUs). In this context, there is an interest to generate a nA-range current to support analog functions either in sleep mode for devices with an upper-end power budget, or in active mode for devices with a lower-end power budget. Minimizing the area occupied by the reference is also important to reduce its economic cost as well as its direct environmental impacts, which can be directly related to silicon area [19]. Circuit designers should however be aware that, while reducing silicon area is fundamentally a good thing, there is a high risk of rebound effect, i.e., increasing the total direct environmental impacts despite a technological improvement, because more functionalities are added to a chip whose area remains the same, or more sensor nodes with a smaller individual size are deployed. This is an important pitfall in which the electronic industry has too often fallen, and that should therefore be considered in future developments. At last, Chapter 5 highlights that temperature independence is of particular interest in the context of IoT sensor nodes, which can be subject to large variations of their operating conditions, but that only a fraction of analog blocks actually benefit from a CWT current. This leads us to our second claim.

Claim 2 *Temperature independence of the reference current is not as widely relevant to applications and analog blocks than traditionally claimed in the literature.*

The main outcome of Chapter 5 is to realize that temperature independence is not necessary in several cases, that are nonetheless mentioned as being relevant to CWT current references in our corpus of papers. In terms of applications, biomedical devices do not benefit from a CWT current as much as other applications, because they either operate in a temperature-regulated environment, in the case of implantable medical devices, or over a temperature range that is reduced compared to the industrial range as it must be withstandable by a human, in the case of wearables. In applications such as the IoT, devices are usually expected to operate over the industrial range, while automotive and aeronautical applications usually require an extended temperature range given the harsh conditions in which

devices have to operate. In terms of analog and mixed-signal circuits, amplifiers and comparators typically require a constant-g_m bias current, i.e., a proportional-to-absolute-temperature (PTAT) current, to respectively maintain their bandwidth and delay constant with temperature. Temperature sensors, and oscillators employed by real-time clock generators and wake-up timers, can take advantage of a CWT current even though several alternative architectures that do not rely on a CWT current exist and provide a similar or better performance. A CWT current thus presents a limited interest for these circuits. Finally, current-mode data converters such a current-steering DACs and current-mode ADCs are probably one of the few type of circuits in which a CWT current is needed, with current-steering DACs requiring a quasi-CWT current compensating the TC of the resistance used to convert the digitally-controlled current in an output voltage, and current-mode ADCs proceeding to a direct comparison between their input current and a reference current.

A recommendation to circuit designers, which originates from these two conclusions but is not limited to the context of current references, is to spend more time considering how their circuit is going to impact the performance of the electronic system in which it operates, and to consider the implications beyond the scope of the electronic system itself. However, this can be difficult to do in practice as the complexity of electronic systems keeps increasing, and as circuit designers do not always have the knowledge necessary to properly understand the implications of their work beyond the electronic system.

Guidelines for the Design of Current References

Based on the current reference architectures proposed in Chapters 3 and 4, we can put forward several key concepts and observations. In addition, the applications, measured performance and limitations of the references proposed in this thesis are summarized in Table 6.1.

Claim 3 *A self-cascode MOSFET (SCM) can generate a CWT nA-range current when biased by a PTAT voltage with a CWT offset voltage, leading to a CTAT inversion level which compensates the PTAT behavior of the specific current.*
In Sections 3.1 and 4.2, we demonstrated that an SCM can be used to generate a CWT current in the nA range when it is biased by a PTAT voltage with a CWT offset voltage. Using this type of V-to-I converter greatly reduces the silicon area occupied by the current reference thanks to the area efficiency of the SCM at this current level. Our first prototype in Section 3.1 biases the SCM with the ΔV_{GS} of two weak-inversion MOSFETs generated by a β-multiplier. The CWT offset voltage

is implemented by forward body biasing (FBB) one of the two transistors to reduce its V_T, with the body voltage generated by a two-transistor (2T) SCM-based voltage reference with different V_T types. While this first prototype fabricated in 22-nm fully-depleted silicon-on-insulator (FD-SOI) reduced the silicon area compared to existing works down to 0.0132 mm^2, it featured a 0.9-nA current with a disappointing TC of 565 ppm/°C due to the lack of TC trimming circuit and the impossibility to tune the value of the CWT offset voltage in this first architecture. Our second prototype in Section 4.2 addressed all of these shortcomings by instead biasing the SCM with a 4T voltage reference buffered by a single transistor. In this structure, the CWT offset voltage is obtained by applying FBB to one of the zero-V_{GS} transistors in the 4T reference. It attained a much more competitive 0.00255-mm^2 silicon area while providing a 2.5-nA current with a 82-ppm/°C TC.

Claim 4 *In the nA range, SCM-based references offer the best area efficiency and a TC of I_{REF} between 100 and 500 ppm/°C, while resistor-based references present a larger area than their SCM counterparts, but allow to reach a sub-100-ppm/°C TC.*

SCM-based references, such as the one proposed in Section 4.2, are particularly area-efficient in the nA range, but usually result in a TC comprised between 100 and 500 ppm/°C. This can be explained by the fact that the nonlinear PTAT behavior of the specific current is compensated by the also nonlinear CTAT behavior of the inversion level. Section 4.2 featured two SCM-based designs, a first one in 0.11-μm bulk with a 2.3-nA 176-ppm/°C current occupying a silicon area of 0.01061 mm^2, and a second one in 22-nm FD-SOI with a 2.5-nA 82-ppm/°C current and a silicon area of 0.00255 mm^2. In contrast, resistor-based references such as the one proposed in Section 3.2, present a larger silicon area than their SCM-based counterparts because of the relatively large area occupied by the resistor at this current level. However, the temperature dependence of high-resistivity (high-res.) polysilicon (poly) resistors generally used in such references is mostly linear and typically results in a lower TC of I_{REF} below 100 ppm/°C. Section 3.2 presented two references demonstrating a 5-nA 65-ppm/°C current within a 0.00954-mm^2 area, simulated in 0.11-μm bulk, and a 1.5-nA 89-ppm/°C current within a 0.00214-mm^2 area, measured in 22-nm FD-SOI. At first glance, these results appear to be in contradiction with our claim, but the 0.11-μm resistor-based design presents a reference current which is twice as large as the SCM-based one, and would therefore require an increased silicon area to reach the same reference current. Besides, the 22-nm resistor-based design benefits from narrow high-res. poly resistors, which are denser than conventional high-res. poly ones but do not exist in most technologies. The silicon area would therefore be increased in most technologies. In addition, the 89-ppm/°C measured TC does not match the 22-ppm/°C simulated value, and a better understanding of second-order effects degrading the TC in measurement would be required to reduce this gap.

Claim 5 *V / R references implemented with a 2T voltage reference and a 1T buffer allow to generate a wide range of current levels and temperature behaviors, depending on the TC of the reference voltage and the choice of V-to-I converter.*

Chapter 4 introduced a family of current references based on a reference voltage generated by few transistors and biasing a V-to-I converter through a single-transistor (1T) buffer. Section 4.1 proposed two first variants, fabricated in 0.18-μm partially-depleted SOI (PD-SOI). The first one consists of a CWT reference voltage, generated by a 2T reference with different V_T types, biasing a resistor to generate a CWT μA-range current. This reference achieves a 1.09-μA current with a 38-ppm/°C TC and a silicon area of 0.0043 mm^2. The second variant consists of a PTAT reference voltage, generated by a 2T reference with the same V_T type but different transistor widths, biasing an SCM to produce a PTAT nA-range current. It generates a 96-pA PTAT current within a 0.0087-mm^2 silicon area. Then, Section 4.2 introduced a third variant, in which a 4T voltage reference with different V_T types generates a PTAT voltage with a CWT offset voltage, biasing an SCM to generate a CWT nA-range current. This last reference hence produces a 2.5-nA current with a 82-ppm/°C TC and a 0.00255-mm^2 silicon area. These current references present the advantage of not requiring any startup circuit, as the 2T voltage reference renders the current reference unstable at zero I_{REF}. Moreover, they allow to generate a wide range of reference currents, and are actually better aligned with the diversity of needs in mixed-signal circuits identified in Chapter 5 than CWT nA-range current references. However, as the power consumption of the 2T reference is proportional to the drain-to-source leakage of transistors, it scales exponentially with temperature, leading to a sharp increase of the current reference's power consumption at high temperature.

Claim 6 *Trimming is necessary to obtain the best TC from MOS-based CWT current references and to ensure that this TC can be maintained across process corners.*

Another finding of this thesis is that trimming is an essential ingredient of MOS-based CWT current references in order to maintain temperature independence in process corners. Most of our CWT current reference designs hence include some kind of trimming, and the improvements brought by trimming the TC, for example, are clearly visible in Figs. 6.1 and 6.2. In Chapter 4, we included a trimming of the TC by changing a width ratio in the 2T/4T voltage reference in both the CWT μA-range and nA-range references. For the CWT μA-range design, the measured TC is improved from 290 to 38 ppm/°C , while for the CWT nA-range designs, it is enhanced from 530 to 176 ppm/°C in 0.11-µm bulk and from 361 to 82 ppm/°C in 22-nm FD-SOI. Furthermore, the resistor-based nA-range reference presented in Section 3.2 includes a trimming of the TC based on a change of width ratio in the 2T body bias generator, as well as a trimming of I_{REF} based either on a binary-weighted current mirror in 0.11-μm bulk and on binary-weighted resistor segments in 22-nm FD-SOI. The TC and I_{REF} trimming mechanisms change the current from

1.12 nA with a 168-ppm/°C TC, to the 1.5-nA design target with a 89-ppm/°C TC. We chose to implement a trimming of I_{REF} in the resistor-based reference as process variations of the resistance alone modify the value I_{REF} by ±30 %, and add up to the process variations of transistors to reach a total variation of ±50 %.

Final Comparison to the State of the Art

At the end of the day, one might wonder if this thesis managed to answer the main research question defined in the introduction, i.e.,

How can current references be improved to better suit the needs of Internet-of-Things (IoT) sensor nodes ?

While it is not for us to judge if we were successful in that attempt, we can however say that we have developed several novel architectures of current references, namely CWT nA-range, CWT μA-range, and PTAT nA-range ones. Figs. 6.1 to 6.3 provide an overview of the extent to which our work has advanced the state of the art, by placing our results among the 114 papers of the corpus established in Chapter 1. Additional graphs are provided in Appendix D. First, our nA-range CWT references presented in Sections 3.2 and 4.2 present the best performance in terms of FoM_1, related to the TC and silicon area and defined in (1.12), and FoM_2, adding the normalized power consumption to FoM_1 and defined in (1.13), which they improve by at least 34.6× and 54.4× compared to references with a current close to 1 nA, and by at least 11.6× and 17.0× compared to references with a current closer to 10 nA [Figs. 6.1(a) and (b)]. Interestingly, the proposed measured references even beat all simulated references in the nA range in terms of FoM_1 [Fig. 6.1(a)]. These significant improvements stem from a reduction of the silicon area by at least 6.4× compared to the smallest measured current reference in the nA range, a sub-100-ppm/°C TC from -40 to 85°C [Fig. 6.2(a)], and a normalized power consumption between 2 and 4 [Fig. 6.2(b)]. Then, the CWT μA-range reference proposed in Section 4.1 achieves 8.7× and 12.3× reductions of FoM_1 and FoM_2 [Fig. 6.1(a) and (b)], obtained by the combination of a 0.0043-mm^2 area, a 38-ppm/°C TC [Fig. 6.2(c)], and a 0.7 normalized power consumption [Fig. 6.2(d)]. At last, the nA-range PTAT reference described in Section 4.1 achieves a 96-pA current, one of the lowest current to date for references which do not rely on gate-leakage transistors, with a 0.0087-mm^2 silicon area [Fig. 6.1(c)]. Another performance metric that we did not discuss as extensively as the TC in this thesis is the line sensitivity (LS) of I_{REF}. Fig. 6.3 compares the proposed references to the state of the art based on FoM_3 (1.14), combining the LS of I_{REF} and silicon area, and on the LS itself. Fig. 6.3(a) highlights that the performance attained by the proposed references is comparable with existing references in the nA range, thanks to a reduced silicon area and an LS on par with other fabricated works [Fig. 6.3(b)].

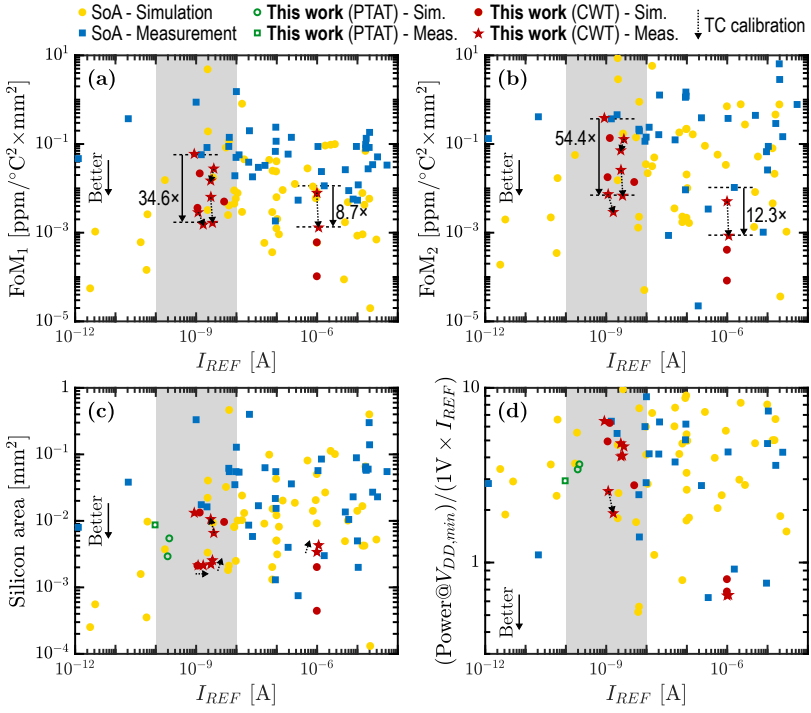

Fig. 6.1 Comparison of the current references proposed in this thesis to the state of the art of simulated and measured current references, presented as (a) FoM_1, (b) FoM_2, (c) silicon area, and (d) TC of I_{REF}, as a function of the reference current.

The proposed references featuring a sub-1-%/V LS either make use of long transistors in an FD-SOI technology, thus leading to a large intrinsic gain (g_m/g_d) and therefore, to a low LS, or rely on cascoding to improve the LS. In the μA range, a 0.2-%/V LS is obtained for the measured 0.18-μm design, again by employing the large intrinsic gain of long transistors in this old technology node, similarly to what is done in the nA range with an FD-SOI technology. An interesting conclusion is that cascoding or a feedback loop based on an operation transconductance amplifier (OTA) are not always necessary to obtain an acceptable LS in the nA and μA ranges, except in technology nodes presenting a particularly low intrinsic gain, such as 65-nm bulk. In addition, LS can generally be improved at the cost of an increased minimum supply voltage $V_{DD,\text{min}}$. Yet, in the proposed references, it is often the self-cascode MOSFET operating in moderate/strong inversion or the TC trimming circuit which limit $V_{DD,\text{min}}$. A low-voltage cascoding circuit or an OTA-based feedback loop could thus be integrated in some of the proposed designs without necessarily leading to an increased $V_{DD,\text{min}}$. In conclusion, it is safe to say that we have delivered on our claim of improving current references.

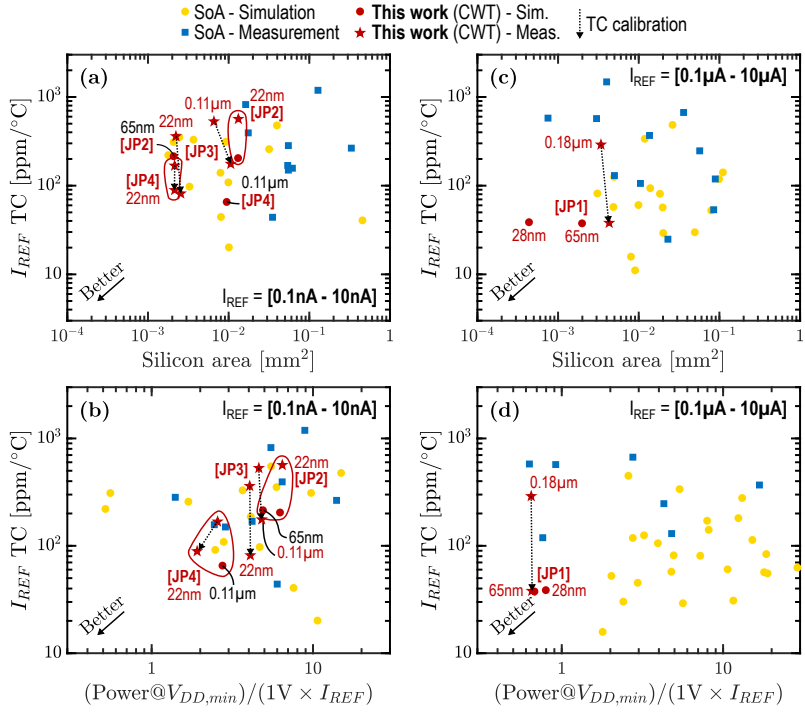

Fig. 6.2 Comparison of the current references proposed in this thesis to simulated and measured current references in the nA range [(a) and (b)] and the μA range [(c) and (d)]. TC of I_{REF} as a function of (a)(c) silicon area and (b)(d) normalized power consumption.

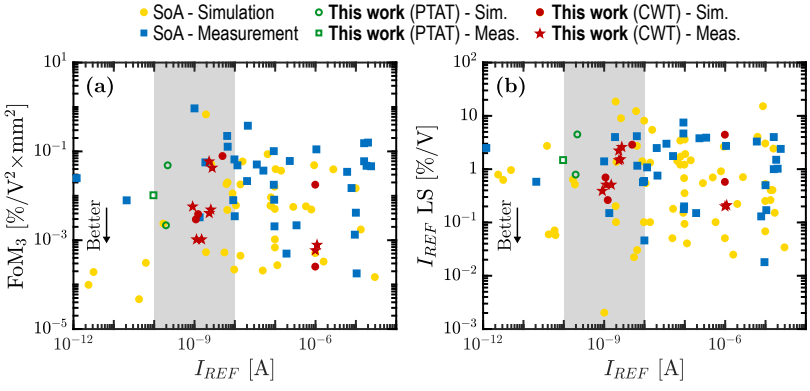

Fig. 6.3 Comparison of the current references proposed in this thesis to the state of the art of simulated and measured current references, presented as (a) FoM_3 and (b) LS of I_{REF}, as a function of the reference current.

The second part of our research question was related to the needs of the IoT, and this thesis has revealed in Chapters 2 and 5 that the temperature independence is not particularly relevant in applicative contexts with a limited temperature range, such as biomedical devices. But it remains of interest in the context of IoT sensor nodes facing large variations of their operating conditions, for example environmental monitoring. Yet, our analysis of the needs of specific analog and mixed-signal circuits in Chapter 5 emphasized that, while maintaining the performance of these circuits constant with temperature is critical, this characteristic is not necessarily achieved through a CWT current. Indeed, only a few circuits such as current-mode data converters require a CWT current, while amplifiers and comparators rather necessitate a constant-g_m biasing, and oscillators and temperature sensors have alternative architectures that can work without a CWT current. In our opinion, CWT current references should thus be regarded as a stepping stone towards other applications requiring a specific and controllable temperature dependence, rather than a goal in itself. Consequently, we cannot say with certainty that the proposed references correspond to the actual needs of IoT sensor nodes, despite the outstanding performance in terms of TC that they achieve. We rather believe that their main strength resides in their simplicity, i.e., the fact that they consist of a limited number of transistors and do not require a startup circuit, as well as in the detailed sizing methodology we provided for each of them. These two elements allow to reduce silicon area on one side, and to facilitate the sizing of the reference, thereby saving precious design time, on the other side.

Perspectives

Now that the contributions of this thesis have been discussed in ample details, let us take a first step back and discuss which directions further research on this topic should focus on, based on the limitations identified in Table 6.1.

Device Models

1. Parasitic diodes between n-well and p-substrate, or p-well and deep-nwell, have a significant impact on the behavior of the proposed references at high temperature, most notably on the 2T/4T ULP voltage references. However, these diodes are often poorly modeled as their impact is rather modest in the vast majority of analog circuits, thus limiting the interest to more accurately characterize their behavior. The development of accurate parasitic diode models would thus be an important step towards a more reliable design of the proposed current references. Some initiatives have already been launched in FD-SOI technologies, namely by ST in 28 nm and GF in 22 nm,

to offer a more detailed modeling of substrate effects in the context of RF designs. Interestingly, these improved models would also result in a more accurate DC behavior. Yet, such models could be further improved with a specific focus on the DC behavior, and are still lacking in bulk technologies;

2. Transistor models could probably also be improved with a focus on operating conditions corresponding to their utilization in ULP circuits. For example, the proposed current references rely on zero-V_{GS} transistors with a relatively large V_{DS}, for which a thorough characterization of gate-induced drain leakage (GIDL) is necessary, for example. A modeling of gate leakage in older technology nodes is also missing in most cases, and it is not clear whether it is not modeled because it is indeed negligible, or because it was not characterized when process development kits (PDKs) were created;
3. In the measurement of currents in the nA range and below, every source of leakage can negatively impact the measurements. The leakage of ESD protection diodes, even in analog pads, can significantly impact the measured current at high temperature, and is either poorly modeled due to overly-simple diode models, or in terms of electrical circuit, with some key parasitic diodes missing from the schematic. Designers working with ULP circuits must therefore keep in mind that simulations do not always accurately represent reality and thus do not guarantee a correct behavior in measurement.

Temperature Coefficient Trimming

1. A limitation of the current references proposed in this thesis is that they require a costly two-point trimming step with respect to temperature, so as to maintain their temperature independence across process corners. First, designers should check if the TC of the untrimmed referenced could be acceptable for the application in which the reference is being used. Then, an interesting research direction would also be to investigate if these references could perform the trimming autonomously [243], with the difficulty that temperature cannot be controlled by the chip, or be turned into trimming-less architectures [93, 244];
2. To allow for an acceptable TC trimming step in an industrial context, several possibilities can be envisioned. First, the impact of mismatch on the TC could be reduced by employing a different sizing, allowing to select the calibration code for a whole process batch based on measurements of a single chip. This is already the approach followed for the μA-range reference discussed in Section 4.1. Next, a current measurement circuit could be integrated on chip to facilitate the trimming step by providing a digital output rather than having to measure a current in the nA range. However, this solution increases the design complexity, and entails power and area overheads.

One must thus evaluate if the gain in performance is worth the cost of this additional circuit.

Circuit and System Design

1. The main problem of the 2T voltage reference used in most of the proposed references is that its power consumption is proportional to the drain-to-source leakage of transistors and hence increases exponentially with temperature. Several works have already proposed solutions to reduce the power consumption, but most of them have not yet been integrated in current references. [245] biases a 2T voltage reference structure with a PTAT current in the pA-range, generated by a β-multiplier structure in which the resistor is replaced by a gate-leakage transistor. This first idea allows the power consumption to increase linearly with temperature, rather than exponentially. Next, [46] relies on a 3T voltage reference in which a gate-leakage transistor is added inside the 3T structure to limit the bias current, also leading to a linear increase of the power consumption with temperature. The generated reference voltage is then used to bias a gate-leakage transistor and produce a reference current in the pA range. The important feature here is that the bias current employed in the voltage reference increases linearly with temperature, but not necessarily that this behavior would be implemented with a gate-leakage transistor. One potential problem with these two solutions is that the reduction of the bias current at high temperature might lead to a non-ideal behavior, as the leakage current of parasitic diodes and junction leakage could have a greater impact than the bias current. Finally, [246] proposes to use a temperature-dependent duty cycling of the 2T voltage reference, resulting in a quasi-linear power increase with temperature, but necessitating a clock and leading to some voltage ripple on the reference voltage. Nonetheless, these two categories of possible solutions lead us to believe that the power consumption problem is close to being solved in the context of current references. Besides, in our opinion, an element that needs to be refined to allow for a more reliable design of 2T voltage references is the quality of the parasitic diode leakage models, as already discussed hereabove, which are not critical in the overwhelming majority of circuits and have thus elicited little interest, but play a decisive role in 2T voltage references;
2. An interesting improvement which could be brought to the CWT μA-range current reference is to implement a sleep mode while providing a fast wake-up time, to be able to use this reference in an IoT node with duty cycling. This would require to power down the current generation structure while keeping the 2T voltage reference active, as its startup time would otherwise be too long to ensure a fast wake-up. However, doing so requires to momentarily decouple the 2T voltage reference from the current generation structure,

as the feedback loop implemented through the transistor in source-follower configuration does not allow to power down the current generation structure without also powering down the 2T voltage reference;

3. One might wonder if the proposed current references can be ported to the latest technology nodes, and more specifically to FinFET or gate-all-around (GAA) technologies. But as there is an extremely limited body effect in FinFET and no body effect in GAA, while we make extensive use of it in our references except for the ones presented in Section 4.1, the answer to this interrogation is clear: it is simply not possible. However, this creates new opportunities for current reference architectures which were discarded in bulk and FD-SOI technologies, precisely because they were negatively impacted by the presence of a body effect, to be revisited;
4. Based on the examples of systems-on-chip (SoCs) developed in our research group, in which we integrated the current references fabricated in this thesis, we can estimate their contribution to the area of the SoC, and thereby, to the economic cost and embodied carbon footprint. It corresponds to 0.84 % for the ICare SoC in Section 3.1, 0.20 and 0.23 % for the CERBERUS SoC in Sections 3.2 and 4.2, and 0.35 % for the MANTIS SoC in Section 4.2. It is thus clear that current references are not the main contributor to the cost and footprint of the SoC. This contribution could be more important in a use case in which several untrimmed references are used in the SoC, to avoid distributing the bias voltage across the chip. Nonetheless, it is not clear to us whether this use case would be realistic or not. More generally, we believe that the same effort of reducing the silicon area that we applied to our references needs to be extended to other analog blocks, the idea being that there are opportunities to simplify existing architectures to only retain the core elements providing functionality. Only if this effort is generalized to all analog blocks will we make a difference at the chip level;
5. A totally different application in which current references can be useful is for strain sensors implemented in a CMOS technology. [247, 248] rely on a conventional β-multiplier in which the resistor is replaced by a triode transistor. Strain sensing is performed by placing the two transistors forming the pMOS current mirror and the Widlar current source along orthogonal directions. Then, the impact of strain on the silicon substrate leads to a different change in mobility along the two directions and modifies the reference current generated by the β-multiplier. A similar approach could be applied to the PTAT current reference [27, 28], but with a reduced power consumption as the β-multiplier in [247, 248] generates a μA-range current, while [27, 28] is well-suited to the generation of a nA-range current and could hence reduce the power consumption by three to four orders of magnitude.

Let us eventually take a second step back, to reflect more broadly on circuit design and on the role of electronic engineers in the 21st century. In this thesis, we followed an innovation strategy which consists in improving figures of merit of specific analog and mixed-signal circuits, and is quite common in the circuit and systems community. However, our broader analysis revealed that the potential benefits of this optimization might not be as significant as we thought, as most of the circuits mentioned as requiring a CWT current in the literature did not in fact need it. In our opinion, this kind of bad surprises is symptomatic of the fact that circuit designers have become too focused on optimizing the performance of individual blocks and often lack time to take a step back and consider the higher-level requirements of the electronic system in which their block is operating. Three factors come to our mind to explain this shortage of time: (i) the fact that circuit design inherently requires a long implementation time in order to reliably make it work on silicon, (ii) the fact that electronic systems have grown so big in terms of scale and complexity that implementing them no longer requires a few people but large teams, while understanding all of their intricacies may not be as easy as it used to be, and (iii) the fact that, in our modern societies, technological innovation is generated at such a fast rate that we can hardly follow it and remain relevant. Consequently, we can only but encourage our fellow circuit designers to take more time to go up a few abstraction levels and understand how their circuit will impact the whole system, how complex it may be. In addition, the climate crisis that we are facing (among other crises), requires us to rethink the way the electronic ecosystem is working, by rejecting innovation for the sake of innovation, and by moving away from the needs, desires, and research directions that several prominent tech companies try to force upon us for their own profit. Related to this topic, it is impossible for us not to mention some particularly useless examples of IoT applications such as connected swimsuits, smart drinking bottles, smart contact lenses, and recording devices for kids placed in stuffed toys. The concept of smart glasses so widely advertised by Meta also comes to mind, as it raises serious concerns regarding the kind of society that we want to live in and regarding the material resources necessary to make this vision come true. In our opinion, the role of electronic engineers in the 21st century should therefore extend beyond technical considerations, and is to question the relevance of the proposed applications in the context of a world in which resources are finite and greenhouse gases (GhG) emissions need to be drastically reduced, so as to reach a sustainable future.

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Appendices

A Transistor Models

The objective of this appendix is to introduce the transistor models used in this thesis. More specifically, we first detail the equations of a transistor operating in weak inversion or subthreshold in Section A.1. Then, we describe various transistor models that remain valid across the inversion range in Section A.2, as these are of particular interest for designing the self-cascode MOSFETs used in several of our current references.

A.1 Transistor Model for Weak Inversion

In the weak inversion regime, also referred to as subthreshold, the drain-to-source current I_{DS} of the transistor is dominated by diffusion currents and can thus be expressed as

$$I_{DS} = I_{SQ} S \exp\left(\frac{V_{GS} - V_T}{n U_T}\right)\left(1 - \exp\left(\frac{-V_{DS}}{U_T}\right)\right), \tag{A.1}$$

where V_{GS} is the gate-to-source voltage, V_{DS} the drain-to-source voltage, $I_{SQ} = \mu C'_{ox}(n-1)U_T^2$ the specific sheet current, $S = W/L$ the transistor's aspect ratio, μ the carrier mobility, C'_{ox} the gate oxide capacitance per unit area, n the subthreshold slope factor, $U_T = k_B T/q$ the thermal voltage, and V_T the threshold voltage for any body-to-source voltage V_{BS}, as opposed to V_{T0}, the threshold voltage for a V_{BS} equal to zero.
The transistor is usually considered as being saturated when $V_{DS} > 4U_T$, which simplifies (A.1) to

$$I_{DS} = I_{SQ} S \exp\left(\frac{V_{GS} - V_T}{n U_T}\right), \tag{A.2}$$

and gives a gate-to-source voltage

$$V_{GS} = V_T + nU_T \log\left(\frac{I_{DS}}{I_{SQ}S}\right). \tag{A.3}$$

A.2 Transistor Models Valid Across the Inversion Range

First, the model used in this thesis to describe the operation of a transistor across the inversion range is the analog compact MOSFET (ACM) model proposed in [156] in 1998. In this model, the drain current is given by

$$I_D = I_{SQ}S\left(i_f - i_r\right), \tag{A.4}$$

where $I_{SQ} = \frac{1}{2}\mu C'_{ox} n U_T^2$ is a different definition of the specific sheet current compared to (A.1), and i_f, i_r are respectively the forward and reverse inversion levels. Next, the transistor current-voltage characteristics are captured by two equations,

$$V_P - V_S = U_T\left[\sqrt{1+i_f} - 2 + \log\left(\sqrt{1+i_f} - 1\right)\right], \tag{A.5}$$

where $V_P = (V_G - V_{T0})/n$ is the pinch-off voltage. An important comment regarding this equation is that all voltages are referred to the body of the transistor. The reverse inversion level i_r can be determined using a similar equation, obtained by replacing V_S by V_D are i_f by i_r in (A.5). However, i_r is only relevant when the transistor is not in saturation, otherwise, its impact is negligible. Besides, when the transistor is saturated, the limits between the three inversion regimes are defined as follows: (i) weak inversion for $i_f < 1$, (ii) moderate inversion for $i_f \in [1;\, 100]$, and (iii) strong inversion for $i_f > 100$.

To determine the parameters of this model, we can follow the methodology outlined by P. Jespers and B. Murmann in [157], which relies on the simplified Enz-Krummenacher-Vittoz (EKV) model. This model is very similar to the ACM one, but uses slightly different equations. In this model, the drain current is given by

$$I_D = I_{SQ}S\left[(q_S^2 + q_S) - (q_D^2 + q_D)\right], \tag{A.6}$$

where $I_{SQ} = 2\mu C'_{ox} n U_T^2$ is a definition of the specific sheet current similar to the one in the ACM model, but with a difference of a factor $4\times$, and q_S, q_D are respectively the normalized mobile charge densities at the source and drain, and are akin to the inversion levels i_f, i_r in the ACM model. Similarly to (A.5), the current-voltage characteristics is captured by

$$V_P - V_X = U_T\left[2(q_X - 1) + \log(q_X)\right]. \tag{A.7}$$

with q_D only relevant when the transistor is not saturated. Finally, when the transistor is in saturation, the limits between the three inversion regimes are the following: (i) weak inversion for $q_S < 0.2$, (ii) moderate inversion for $q_S \in [0.2; 5]$, and (iii) strong inversion for $q_S > 5$. In our opinion, this model is more intuitive than the ACM one in terms of how the limits between inversion regimes are defined, as $q_S = 1$ corresponds to drift and diffusion currents of the same magnitude.

B ACM Equations Applied to a Self-Cascode MOSFET

In this appendix, we apply the ACM equations (A.4) and (A.5) presented in Appendix A to the self-cascode MOSFET (SCM) structure illustrated in Fig. B.1. This development is similar to the one initially proposed in [27, 28] in the context of proportional-to-absolute-temperature (PTAT) current references employing an SCM as voltage-to-current converter, and was later extended to current references that are constant-with-temperature (CWT) in our works [169, 165].

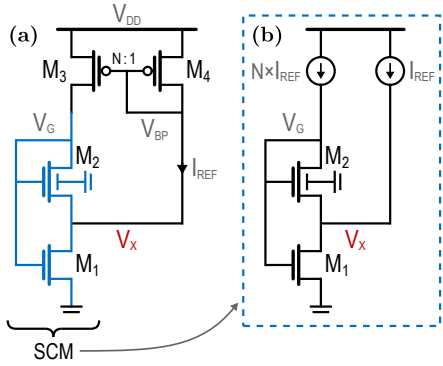

Fig. B.1 (a) Schematic of an nMOS SCM formed by M_{1-2} (in blue) and biased by a pMOS current mirror constituted of M_{3-4} and with a current mirror ratio N. This schematic is further simplified in (b).

Applying (A.4) to M_{1-2}, with the assumption that M_2 is saturated while M_1 is not, yields

$$I_{D1} = I_{SQ1} S_1 \left(i_{f1} - i_{r1} \right) = (N+1) I_{REF}, \tag{B.1}$$

$$\text{and} \quad I_{D2} = I_{SQ2} S_2 i_{f2} = N I_{REF}. \tag{B.2}$$

Then, we notice that V_P is the same for M_{1-2} as they share the same gate voltage V_G. Eq. (A.5) therefore provides us with

$$V_P = U_T \left[\sqrt{1+i_{f1}} - 2 + \log\left(\sqrt{1+i_{f1}} - 1 \right) \right], \tag{B.3}$$

$$V_P - V_X = U_T \left[\sqrt{1+i_{r1}} - 2 + \log\left(\sqrt{1+i_{r1}} - 1 \right) \right], \tag{B.4}$$

$$V_P - V_X = U_T \left[\sqrt{1+i_{f2}} - 2 + \log\left(\sqrt{1+i_{f2}} - 1 \right) \right]. \tag{B.5}$$

Eqs. (B.4) and (B.5) reveal that i_{r1} must be equal to i_{f2}. If we now define $i_{f1} \triangleq \alpha i_{f2}$,

with $\alpha > 1$, we can link S_1 and S_2 using (B.1) and (B.2), yielding

$$\frac{S_1}{S_2} = \frac{I_{SQ2}}{I_{SQ1}} \frac{1+N}{N} \frac{1}{\alpha}. \tag{B.6}$$

Additionally, we can relate i_{f2} to V_X based on (B.3) and (B.5), i.e.,

$$V_X = U_T \left[\left(\sqrt{1+\alpha i_{f2}} - \sqrt{1+i_{f2}} \right) + \log \left(\frac{\sqrt{1+\alpha i_{f2}} - 1}{\sqrt{1+i_{f2}} - 1} \right) \right]. \tag{B.7}$$

Solving this equation for i_{f2} with a given V_X provides us with a complete solution to the problem at hand. Interestingly, if V_X is a purely PTAT voltage as in [27, 28], then i_{f2} is temperature-independent, and the temperature dependence of I_{REF} only originates from the specific sheet current I_{SQ}, as can be seen from (B.9).

Another quantity of interest is the sensitivity of the reference current I_{REF} to voltage V_X, denote as $S_{I_{REF}}$, and computed as

$$S_{I_{REF}} = \frac{1}{I_{REF}} \frac{dI_{REF}}{dV_X} = \frac{1}{I_{REF}} \frac{dI_{REF}}{di_{f2}} \frac{di_{f2}}{dV_X} \tag{B.8}$$

using the chain rule. On the one hand, I_{REF} is expressed as

$$I_{REF} = \frac{I_{SQ2} S_2 i_{f2}}{N} \tag{B.9}$$

from (B.2), and dI_{REF}/di_{f2} is consequently computed as

$$\frac{dI_{REF}}{di_{f2}} = \frac{I_{SQ2} S_2}{N}. \tag{B.10}$$

On the other hand, di_{f2}/dV_X is calculated as the inverse of dV_X/di_{f2} based on (B.7), i.e.,

$$\frac{di_{f2}}{dV_X} = \left(\frac{dV_X}{di_{f2}} \right)^{-1} = \frac{2}{U_T} \left[\frac{\alpha}{\sqrt{1+\alpha i_{f2}} - 1} - \frac{1}{\sqrt{1+i_{f2}} - 1} \right]^{-1}. \tag{B.11}$$

The sensitivity $S_{I_{REF}}$ is finally obtained by substituting (B.10) and (B.11) in (B.8), yielding

$$S_{I_{REF}} = \frac{2}{i_{f2} U_T} \left[\frac{\alpha}{\sqrt{1+\alpha i_{f2}} - 1} - \frac{1}{\sqrt{1+i_{f2}} - 1} \right]^{-1}. \tag{B.12}$$

C Additional Temperature Coefficient Trimming Results

This appendix provides additional measurement results regarding the trimming of the TC of I_{REF} in all the references proposed in this thesis. The results described in the main body of text indeed correspond to a trimming based on the complete temperature profile between -40 and 85°C, and the objective of this appendix is thus to verify the feasibility of a conventional two-point trimming to select the optimal calibration code. First, for the resistor-based μA-range current reference presented in Section 4.1, Fig. C.1(b) illustrates that an estimation of the TC based on two temperature points at 0 and 80°C would lead to the selection of a calibration code equal to 0 instead of 1, thus only marginally increasing the TC from 36.3 to 44.0 ppm/°C. A two-point trimming would therefore be perfectly acceptable in the case of this first reference.

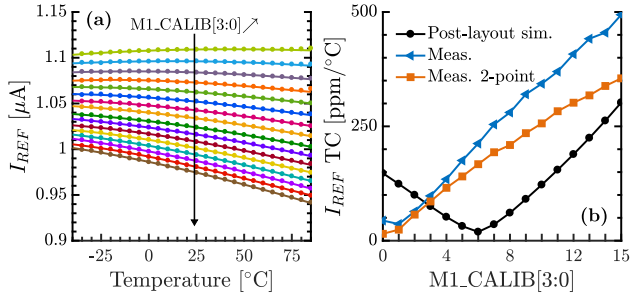

Fig. C.1 For the μA-range current reference in Section 4.1, measured (a) temperature dependence of I_{REF} at 0.9 V, for all 16 calibration codes on a single die. (b) I_{REF} TC obtained for each calibration code, in TT post-layout simulations and in measurement. An estimation of the TC based on two points, here 0 and 80°C, leads to a calibration code close to the optimal one.

Then, for the resistor-based nA-range reference proposed in Section 3.2, Fig. C.2 indicates that a trimming based on two points at -35 and 25°C (ambient temperature) leads to six different codes out of 11 compared to the optimal codes selected with a complete knowledge of the temperature profile, and to an average distance of 1.3 with respect to the optimal code [Figs. C.2(c) and (d)]. The average TC is hence degraded from 89.2 to 108.3 ppm/°C [Figs. C.2(e) and (f)]. Furthermore, Fig. C.3 highlights that if any two points can be selected, here -35 and 65°C, only one code out of 11 is different from the optimal ones, yielding an average distance of 0.1 from the optimal code [Figs. C.3(c) and (d)]. This translates to a negligible increase of the average TC from 89.2 to 89.4 ppm/°C [Figs. C.3(e) and (f)].

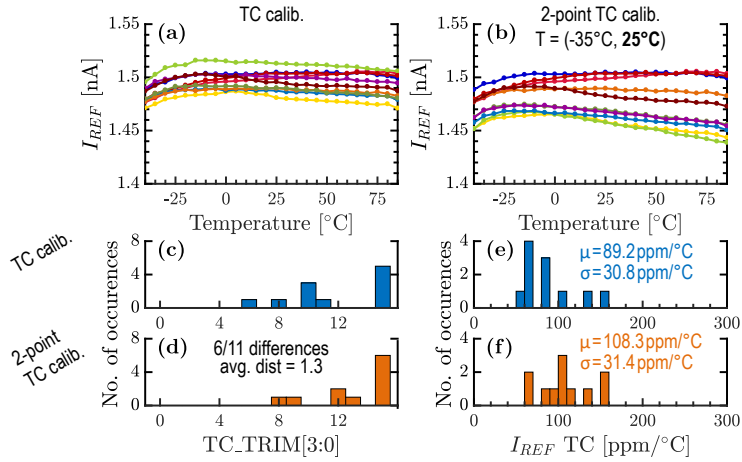

Fig. C.2 For the nA-range current reference in Section 3.2, implemented in 22-nm FD-SOI and at 1.8 V, measured temperature dependence of I_{REF} with TC trimming based on (a) the complete temperature profile and (b) two temperature points (-35 and 25°C). Histograms of the selected calibration code [(c) and (d)] and the corresponding I_{REF} TC [(e) and (f)] for a TC trimming based on the complete temperature profile or two temperature points.

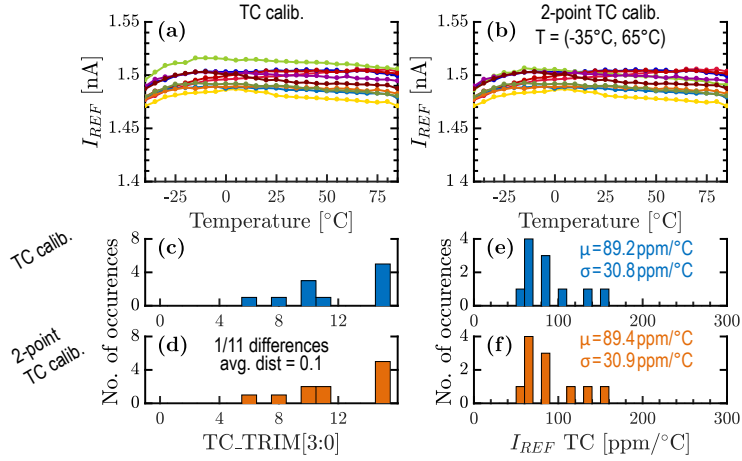

Fig. C.3 For the nA-range current reference in Section 3.2, implemented in 22-nm FD-SOI and at 1.8 V, measured temperature dependence of I_{REF} with TC trimming based on (a) the complete temperature profile and (b) two temperature points (-35 and 65°C). Histograms of the selected calibration code [(c) and (d)] and the corresponding I_{REF} TC [(e) and (f)] for a TC trimming based on the complete temperature profile or two temperature points.

Lastly, for the SCM-based nA-range reference proposed in Section 4.2 and implemented in two technologies, we repeat the same experiment as for the resistor-based reference. For the design in UMC 0.11-μm bulk, a trimming based on two temperature points at -10 and 25°C [Fig. C.4] leads to five different codes out of 10 compared to the optimal ones, and an average distance of 0.8 from the optimal code [Figs. C.4(c) and (d)]. This leads to a mild increase of the TC from 176 to 190 ppm/°C [Figs. C.4(e) and (f)]. Using trimming points at -25 and 85°C [Fig. C.5] reduces the number of different codes to four out of 10 and the average distance with respect to the optimal code to 0.5 [Figs. C.5(c) and (d)]. In terms of average TC, it is only slightly increased from 176 to 182 ppm/°C [Figs. C.5(e) and (f)]. For the design in GF 22-nm FD-SOI, a trimming based on two points at -20 and 25°C [Fig. C.6] yields five different codes out of 11 compared to the optimal codes, and an average distance of 0.5 with respect to the optimal code [Figs. C.6(c) and (d)]. This slightly augments the average TC from 81.5 to 88.2 ppm/°C [Figs. C.6(e) and (f)]. By changing the trimming points to -40 and 80°C [Fig. C.6], the number of different codes is reduced to two and the average distance to 0.3 [Figs. C.7(c) and (d)], while the average TC is negligibly increased from 81.5 to 82.7 ppm/°C [Figs. C.7(e) and (f)]. A general observation which is valid for all the references proposed in this thesis is that a two-point trimming intuitively provides sufficient information to trim the TC, as the temperature dependence of I_{REF} presents a clear second-order behavior.

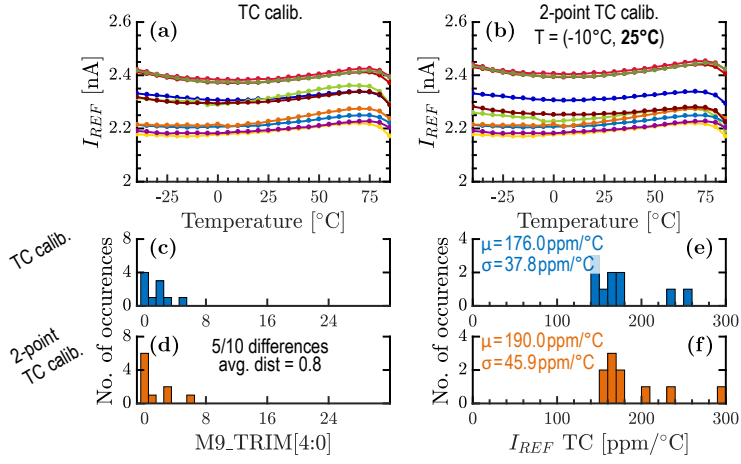

Fig. C.4 For the nA-range current reference in Section 4.2, implemented in UMC 0.11-μm bulk and at 1.2 V, measured temperature dependence of I_{REF} with TC trimming based on (a) the complete temperature profile and (b) two temperature points (-10 and 25°C). Histograms of the selected calibration code [(c) and (d)] and the corresponding I_{REF} TC [(e) and (f)] for a TC trimming based on the complete temperature profile or two temperature points.

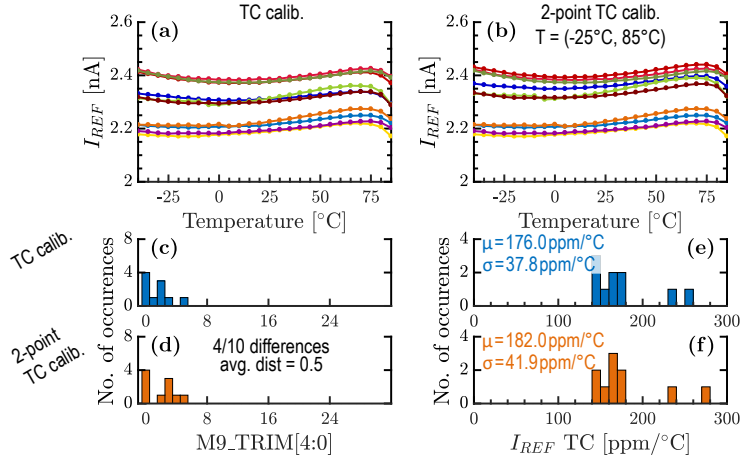

Fig. C.5 For the nA-range current reference in Section 4.2, implemented in UMC 0.11-μm bulk and at 1.2 V, measured temperature dependence of I_{REF} with TC trimming based on (a) the complete temperature profile and (b) two temperature points (-25 and 85°C). Histograms of the selected calibration code [(c) and (d)] and the corresponding I_{REF} TC [(e) and (f)] for a TC trimming based on the complete temperature profile or two temperature points.

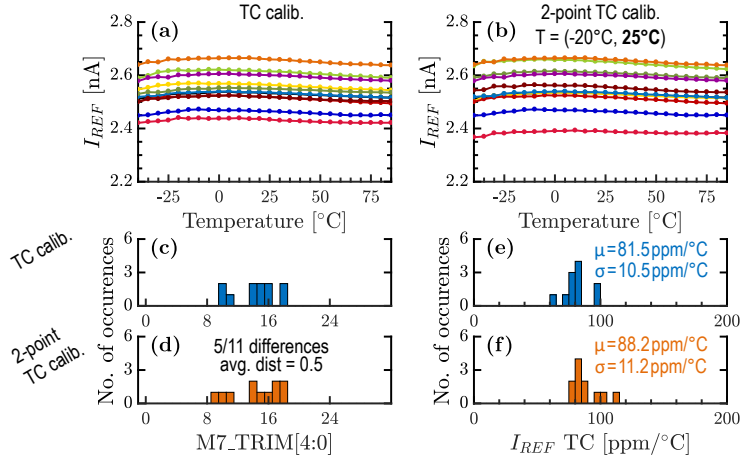

Fig. C.6 For the nA-range current reference in Section 4.2, implemented in GF 22-nm FD-SOI and at 1.8 V, measured temperature dependence of I_{REF} with TC trimming based on (a) the complete temperature profile and (b) two temperature points (-20 and 25°C). Histograms of the selected calibration code [(c) and (d)] and the corresponding I_{REF} TC [(e) and (f)] for a TC trimming based on the complete temperature profile or two temperature points.

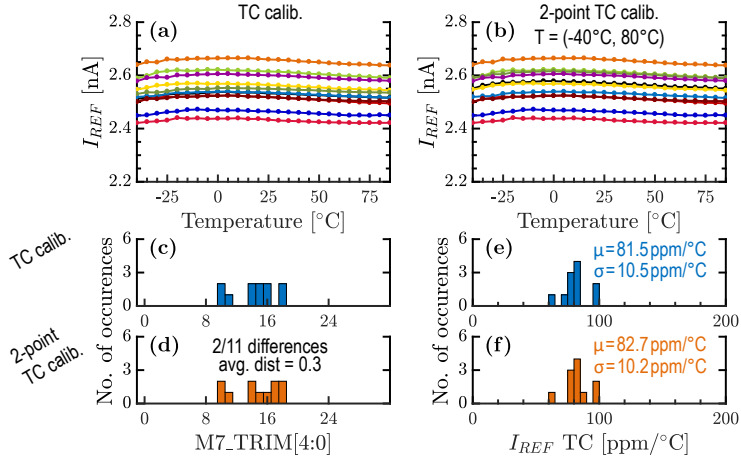

Fig. C.7 For the nA-range current reference in Section 4.2, implemented in GF 22-nm FD-SOI and at 1.8 V, measured temperature dependence of I_{REF} with TC trimming based on (a) the complete temperature profile and (b) two temperature points (-40 and 80°C). Histograms of the selected calibration code [(c) and (d)] and the corresponding I_{REF} TC [(e) and (f)] for a TC trimming based on the complete temperature profile or two temperature points.

D Comparison to the State of the Art

This appendix contains additional graphs positioning our contributions with respect to the state of the art of constant-with-temperature (CWT) current references, i.e., the corpus of papers formed in Chapter 1. Fig. D.1 illustrates FoM_1 (1.12), FoM_2 (1.13), silicon area, and normalized power consumption as a function of the reference current, and provides an overview of the performance of the proposed current references. Figs. D.2 and D.4 are identical to Fig. D.1 but limit themselves to simulated and fabricated references, respectively. Furthermore, Figs. D.3 and D.5 illustrate the trade-off between the temperature coefficient (TC) of I_{REF} and silicon area, and between the TC of I_{REF} and normalized power consumption, in the nA and μA ranges.

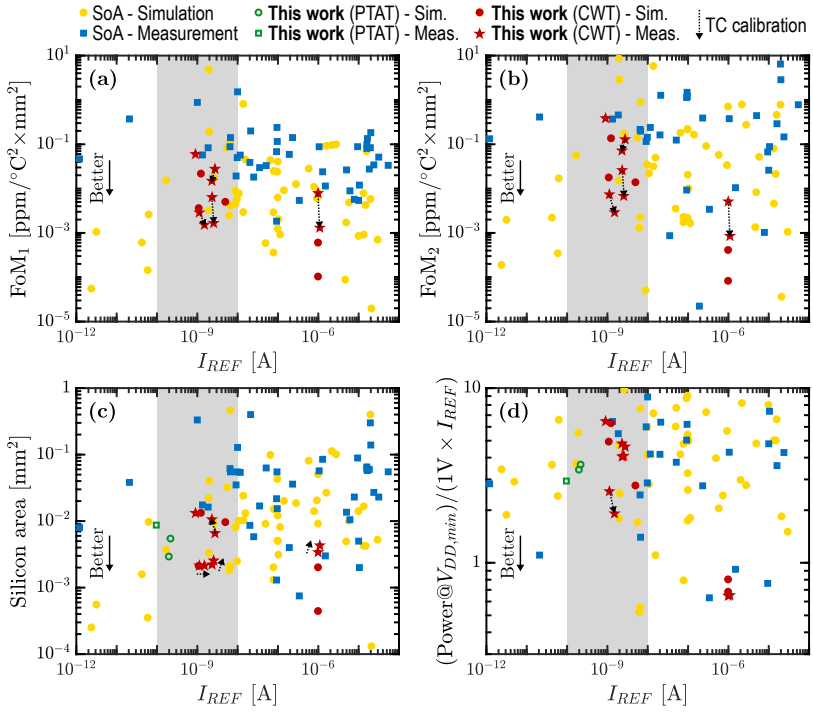

Fig. D.1 Comparison of the current references proposed in this thesis with the state of the art of simulated and measured CWT current references, presented as (a) FoM_1, (b) FoM_2, (c) silicon area, and (d) normalized power consumption, as a function of the reference current.

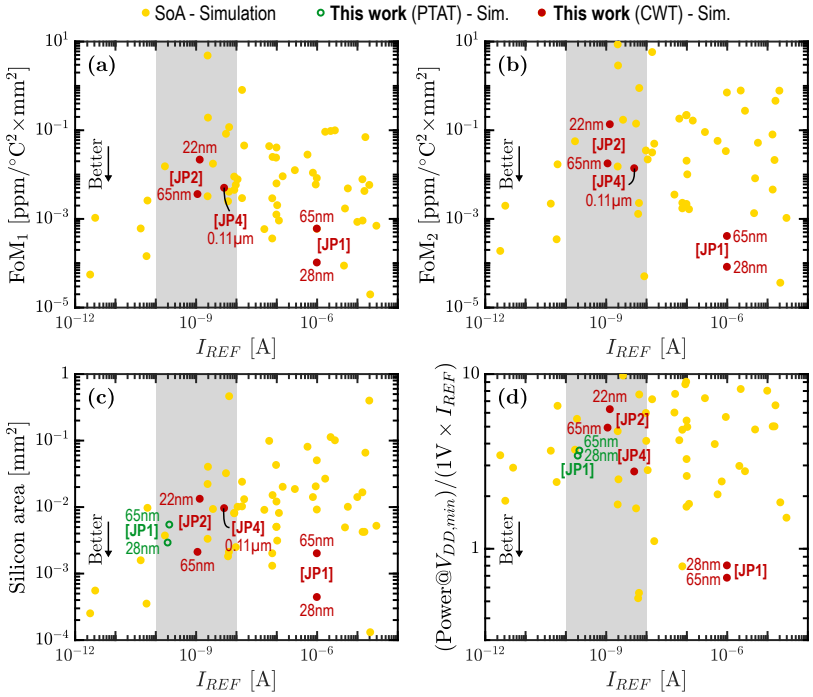

Fig. D.2 Comparison of the simulated current references proposed in this thesis with the state of the art of simulated CWT current references, presented as (a) FoM_1, (b) FoM_2, (c) silicon area, and (d) normalized power consumption, as a function of the reference current.

First, let us focus on CWT nA-range current references, corresponding to our journal papers [JP2, JP3, JP4]. [JP2] is presented in Section 3.1 and consists of a CWT current reference based on a self-cascode MOSFET (SCM) biased by a β-multiplier. This first prototype of SCM-based CWT current reference has been simulated post-layout in 65-nm bulk and 22-nm fully-depleted silicon-on-insulator (FD-SOI), and fabricated in 22-nm FD-SOI. Fig. D.2 highlights that the 65-nm design reaches figures of merit (FoMs) on par with existing simulated references, while the 22-nm design is slightly less effective [Figs. D.2(a) and (b)]. This difference originates from a larger 0.0132-mm^2 silicon area in 22 nm compared to 0.0021 mm^2 in 65 nm [Figs. D.2(c) and D.3(a)]. FoM_2 values are slightly less competitive than FoM_1 ones due to normalized power consumptions of 4.92 and 6.27 for the 65- and 22-nm designs [Figs. D.2(d) and D.3(b)], which originate from the relatively large number of branches drawing current from the supply voltage as well as their respective current mirror ratios. Regarding the 22-nm fabricated reference, Figs. D.2(a) and (b) show that both FoMs are deteriorated compared to post-layout simulations due to a degradation of the TC of I_{REF} from 203 ppm/°C in simulation to 565 ppm/°C in measurement [Fig. D.5(a)]. This issue stems from the fact that this design does

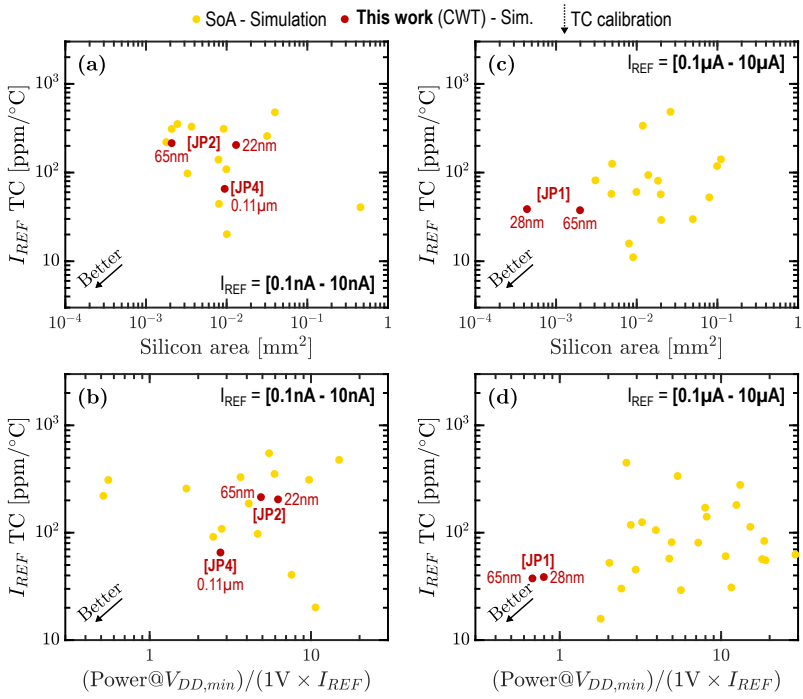

Fig. D.3 Comparison of the simulated current references proposed in this thesis with simulated CWT current references in the nA range [(a) and (b)] and the μA range [(c) and (d)]. TC of I_{REF} as a function of (a)(c) silicon area and (b)(d) normalized power consumption.

not include any TC calibration mechanism, a problem which has been solved in the second prototype introduced in [JP3].

The SCM-based current referenced proposed in [JP3] is detailed in Section 4.2 and solves all of the issues of the first prototype by replacing the β-multiplier with a four-transistor (4T) ultra-low-power (ULP) voltage reference. Only measurement results are discussed in this appendix for the sake of concision, as we have characterized designs without and with TC calibration circuits in two technologies, namely 0.11-μm bulk and 22-nm FD-SOI, thus totaling four measured references. Moreover, measurements are fairly close to post-layout simulations results except for some nonidealities such as gate-induced drain leakage (GIDL) and leakage current of electrostatic discharge (ESD) protection diodes, which could be alleviated in future works. As depicted in Fig. D.4(a), calibration significantly improves the TC at the cost of a somewhat expanded silicon area. In what follows, we will therefore focus on the designs with TC calibration. In terms of FoM_1 [Fig. D.4(a)], the 0.11-μm design is slightly better than all existing architectures in the nA range. In contrast, the 22-nm substantially improves FoM_1 by 34.6× and 11.6×, compared to references with a current close to 1 and 10 nA, respectively. The disparity between

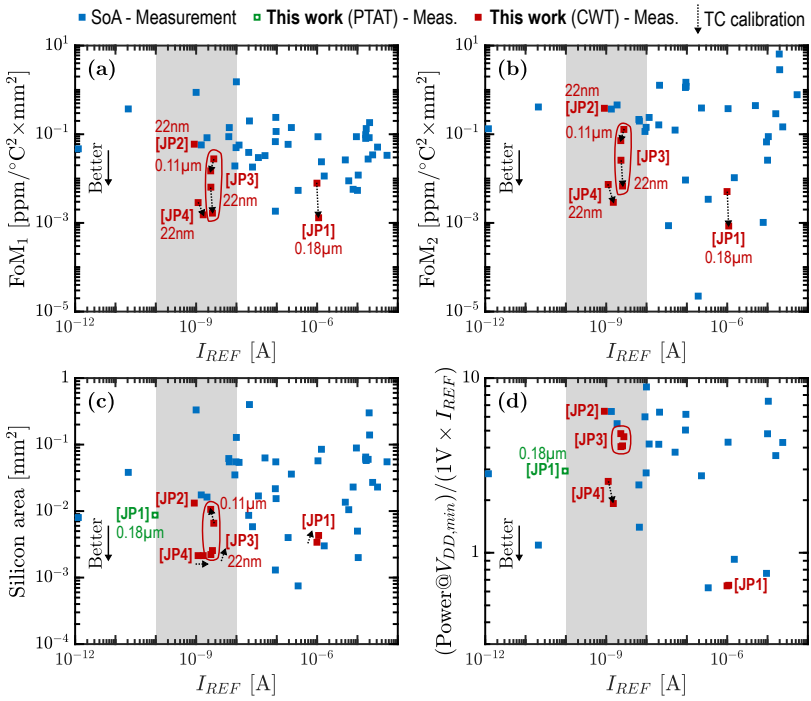

Fig. D.4 Comparison of the measured current references proposed in this thesis with the state of the art of measured CWT current references, presented as (a) FoM_1, (b) FoM_2, (c) silicon area, and (d) normalized power consumption, as a function of the reference current.

the two designs is predominantly explained by the difference in silicon area, with 0.01061 mm^2 in 0.11 μm and 0.00255 mm^2 in 22 nm [Fig. D.4(c)], and marginally by the difference in TC, with 176 ppm/°C in 0.11 μm and 82 ppm/°C in 22 nm [Fig. D.5(a)]. Then, Fig. D.4(b) reveals that FoM_2 is even better than FoM_1 compared to the state of the art, thanks to a normalized power consumption between 4.05 and 4.81 [Fig. D.4(d)]. This is an improvement in comparison with the 6.47 normalized power consumption in [JP2], obtained by drastically reducing the power consumption of the bias voltage generator by relying on a 4T ULP voltage reference. Therefore, the 22-nm design improves FoM_2 by 54.4× and 17.0× compared to references generating a 1- and 10-nA current, respectively.

At last, [JP4] presents a resistor-based peaking current reference (PCR) described in Section 3.2. This design was simulated in 0.11-μm bulk and measured in 22-nm FD-SOI. First, the 0.11-μm simulated design reaches a reasonable performance regarding FoM_1 [Fig. D.2(a)], thanks to a 65-ppm/°C TC and a 0.00954-mm^2 silicon area [Figs. D.2(c) and D.3(a)]. This performance is further improved by a normalized power consumption of 2.76, due to the fact that only two branches carrying I_{REF} are used in the proposed PCR structure, and in addition, that the two-

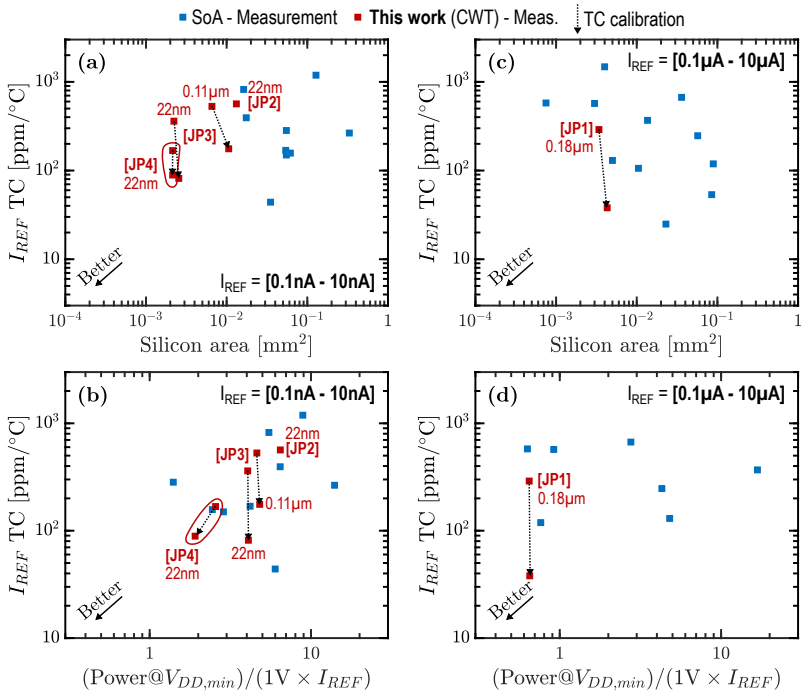

Fig. D.5 Comparison of the measured current references proposed in this thesis with measured CWT current references in the nA range [(a) and (b)] and the μA range [(c) and (d)]. TC of I_{REF} as a function of (a)(c) silicon area and (b)(d) normalized power consumption.

transistor (2T) bias voltage generator consumes negligible power at ambient temperature. This results in an FoM_2 superior to most references in Fig. D.2(b). Next, the 22-nm fabricated design presents the best performance of all references operating in the nA range. More precisely, it respectively improves the performance 1- and 10-nA current references by 37.7× and 12.6× for FoM_1, and by 126.9× and 39.6× for FoM_2. This outstanding performance can be explained by an 89-ppm/°C TC from -40 to 85°C, a 0.00214-mm^2 silicon area, and a 1.91 normalized power consumption [Figs. D.4(a) and (b)].

Next, let us consider the two type of references proposed in [JP1], namely a CWT μA-range and a proportional-to-absolute-temperature (PTAT) nA-range current references, discussed in Section 4.1. These two references are simulated in 65-nm bulk and 28-nm FD-SOI, and fabricated in 0.18-μm partially-depleted SOI (PD-SOI). Regarding the CWT μA-range reference, simulations present best-in-class results in terms of FoM_1 and FoM_2 [Figs. D.2(a) and (b)], especially in 28 nm, thanks to a 38-ppm/°C TC from -40 to 125°C, a 0.00044-mm^2 silicon area, and a 0.8 normalized power consumption [Figs D.3(c) and (d)]. Measurements in 0.18 μm achieve 8.7× and 12.3× reductions of FoM_1 and FoM_2 with respect to 1-μA references

[Figs D.4(a) and (b)], mostly through a 0.0043-mm^2 silicon area and a 0.65 normalized power consumption [Figs. D.5(c) and (d)]. Regarding the PTAT nA-range reference, a sub-1-nA current is achieved in simulations and measurements with a low silicon area ranging from 0.0029 mm^2 for the 28-nm simulated design to 0.0087 mm^2 for the 0.18-μm fabricated one [Figs. D.2(c) and D.4(c)], despite the fact that the proposed reference does not rely on gate-leakage transistors.