J Comput Electron (2013) 12:675–684
DOI 10.1007/s10825-013-0532-1

Multi-scale strategy for high-k/metal-gate UTBB-FDSOI devices modeling with emphasis on back bias impact on mobility

O. Nier · D. Rideau · Y.M. Niquet · F. Monsieur · V.H. Nguyen · F. Triozon · A. Cros · R. Clerc · J.C. Barbé · P. Palestri · D. Esseni · I. Duchemin · L. Smith · L. Silvestri · F. Nallet · C. Tavernier · H. Jaouen · L. Selmi

Published online: 28 November 2013

Abstract Mobility in high-k/metal-gate Ultra-Thin Body and Box Fully Depleted SOI devices has been extensively investigated by means of multi-scale simulations and experimental data. Split-CV mobility measurements have been performed for various Interfacial Layer Equivalent Oxide Thickness allowing an investigation of the physical mechanisms responsible for the mobility degradation at high-k/Interfacial layer interface. The impact of the back bias on transport properties is investigated and mobility enhancement in the reverse regime (back gate inversion) is studied. A multi-scale simulation strategy is ranging from quantum Non-equilibrium Green's Functions to semi-classical Kubo Greenwood approach. These advanced solvers made possible a throughout calibration of empirical TCAD mobility models.

Keywords UTBB-FDSOI devices · Split C-V mobility measurements · Back bias · NEGF · Multi-scale simulations · TCAD

O. Nier (✉) · D. Rideau · F. Monsieur · A. Cros · C. Tavernier · H. Jaouen
STMicroelectronics, 850, rue J. Monnet, BP. 16, 38921 Crolles, France
e-mail: olivier.nier@st.com

O. Nier
IMEP-LAHC, MINATEC, 3 Parvis Louis Néel, 38016 Grenoble, France

Y.M. Niquet · V.H. Nguyen · I. Duchemin
SP2M, UMR-E CEA/UJF-Grenoble 1, INAC, Grenoble, France

O. Nier · F. Triozon · J.C. Barbé
CEA-LETI, Campus MINATEC, 17 rue des Martyrs, 38054 Grenoble, France

O. Nier · P. Palestri · D. Esseni · L. Selmi
DIEGM, University of Udine, Via delle Scienze 208, 33100 Udine, Italy

L. Silvestri · F. Nallet
Synopsys, Thurgauerstrasse 40, 8050 Zürich, Switzerland

L. Smith
Synopsys, Inc., 700 E. Middlefield Rd., Mountain View, CA, USA

R. Clerc
Laboratoire Hubert Curien (UMR 5516), Institut d'Optique, 18 rue Benoît Lauras, 42000, Saint-Etienne, France

1 Introduction

Ultra-Thin Body and Box Fully Depleted SOI (UTBB-FDSOI) device is considered as one of the best alternative solution to overcome conventional planar Bulk CMOS limitations [1–3]. Thanks to an excellent electrostatic control and transport properties, this architecture is suitable to reach ITRS requirements for 14 nm technology node and beyond [4]. The threshold voltage can be easily adjusted by applying back biases (BB) and it has recently been demonstrated that the mobility can be enhanced in the reverse regime ($VB > 0$ V for nMOS and $VB < 0$ V for pMOS) [5]. The mobility in high-k UTBB-FDSOI devices is limited by a complex combination of scattering mechanisms: the presence of high-k dielectrics can induce mobility degradation through Remote Coulomb (RC) [6–10], Remote Phonon (RP) [27] and Remote Surface Roughness scatterings (RSR) [11]. Moreover, phonon and Surface Roughness (SR)-limited mobility are strongly dependent on the channel thickness (T_{Si}) [12]. Additionally, it has been demonstrated that mechanisms limiting the mobility can highly depend on the voltage applied on the front and the back gate [12, 13].

Technology Computer Aided Design (TCAD) support for UTBB-FDSOI technology development can reduce cost and development time but also secure technology choices. For efficient TCAD predictions, a preliminary identification of the mechanisms responsible for transport degradation, as well as a calibration of empirical TCAD transport models, is mandatory. TCAD models parameters calibration based on measurements only can bring to misleading conclusions. Indeed, TCAD solvers are based on empirical models that are developed for single scattering mechanism and the de-embedding of these mechanisms from measurements is often difficult. A more rigorous approach consists in fitting models parameters on advanced solvers such as Kubo-Greenwood (KG), Multi-subband Monte Carlo (MSMC) and quantum Non-Equilibrium Green's Functions (NEGF) solvers.

In this paper, we present a multi-scale simulation strategy for UTBB-FDSOI devices featuring high-k/metal-gate. Based on a large series of measurements in devices with various Equivalent Oxide Thicknesses (EOT), the effect of BB on the electrostatics and on the transport properties is presented in the first part of the paper. From split-CV measurements at various BB, we demonstrated that the mobility can be significantly improved, which is a direct consequence of back gate inversion at high Body Voltage (VB) [13]. In the second part of this paper, we present a direct comparison between NEGF and KG solvers in the view of obtaining reference mobility curves for TCAD model parameters calibration. By adapting the KG parameters for surface roughness and remote Coulomb, we show that KG solvers can reproduce the NEGF results and be used as a reference for TCAD mobility models parameters calibration. In the third part of the paper, TCAD mobility models are presented and their parameters determined using the previously mentioned KG reference simulations for the three main degradation mechanisms: (1) phonons, (2) surface roughness and (3) remote Coulomb scattering. Special care is paid to the impact of BB on mobility, as well as the EOT and the temperature dependencies of the mobility. We demonstrate that, once calibrated, TCAD tools efficiently predict device performances and therefore can be used to optimize device architectures.

2 Experimental observations and electrostatic calibration

Devices have been processed on 300 mm SOI wafers with a 25 nm thick BOX. The oxide stack is made of a 1.8 nm thick layer of high-k oxide (HfSiON) deposited on top of a SiON interfacial layer (IL) with various physical thicknesses (1.0 nm, 2.4 nm 3.5 nm and 4 nm). The final silicon channel thickness is 7.5 nm and the effective mobility was extracted using split-CV method on 0.9×0.9 µm^2 ($W \times L$) devices (corrected from access resistances $R_{\text{access}} = 2 \times 60$ Ω·µm).

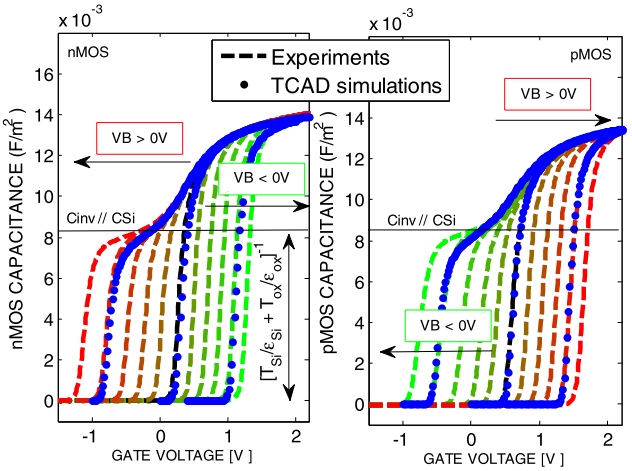

Fig. 1 Gate capacitance as a function of the gate voltage for various back biases ranging from −10 V to 10 V in steps of 2 V for n- (**a**) and p-MOS (**b**) devices. $T_{\text{inv}} = 2.65$ nm; $T_{\text{Si}} = 7.5$ nm; $T = 300$ K. TCAD calibration shown for $VB = -8$, 0 and 8 V

2.1 Impact of the back bias

The impact of voltage VB, applied at the back terminal, on the gate capacitance is shown in Fig. 1 for both n- and pMOS devices. As previously demonstrated in [14], in the reverse regime, the capacitance is distorted and reaches a first level whose magnitude is related to the active layer capacitance C_{Si} in series with the oxide one C_{inv}. Figure 2 shows the threshold voltage (VTH) variation with VB for n- and pMOS devices. As can be seen, the VTH can be shifted by −1.5 V to 1 V for VB ranging from −10 V to 10 V. The corresponding drain current measurement at various VB is shown in Fig. 3. We found out that the sub-threshold slopes remains almost unchanged with back bias ($\frac{\Delta S}{S} < 7$ %).

Using the variation of the capacitance (Fig. 1) and the variation of the threshold voltage with respect to VB (Fig. 2), we determined the physical IL thickness $T_{\text{IL}} = 2.4$ nm (for the device in Fig. 2), the channel thickness $T_{\text{Si}} = 7.5$ nm, the SiO_2 BOX thickness $T_{\text{BOX}} = 25$ nm as well as the material permittivity: $\epsilon_{\text{IL}} = 5.2\epsilon_0$, $\epsilon_{\text{high-k}} = 22\epsilon_0$ and $\epsilon_{\text{BOX}} = 3.9\epsilon_0$.

All simulations which follows are performed using these parameters excepted for the IL physical thickness which depends on the considered device (part II.B), and assuming a channel doping concentration of 1e15 cm^{-3} (undoped substrate) and a ground plane doping of 2e18 cm^{-3} (these latter results are obtained from TCAD process simulation).

The dependence of the mobility on inversion charge for various back biases for n- and pMOS is shown in Fig. 4. For a given inversion charge, an increase of the mobility is observed for $VB > 0$ V in nMOS and for $VB < 0$ V in pMOS devices. In reverse region, a non-monotonic behavior of the mobility is shown (not to be confused with the RC-limited

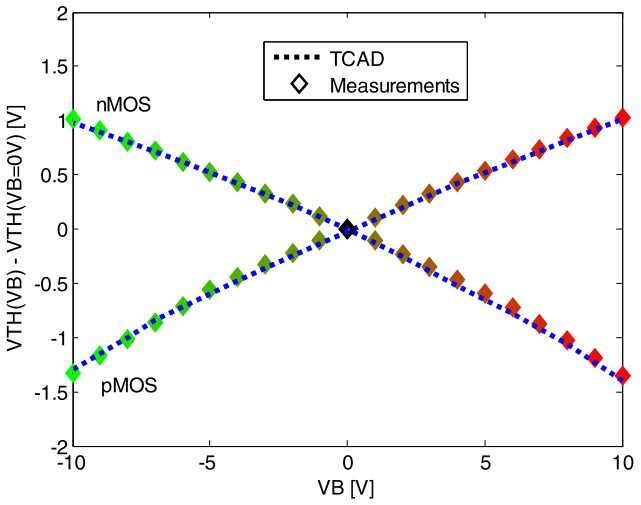

Fig. 2 Threshold voltage variation (reference at $VB = 0$ V) as a function of the back bias in n- and pMOS devices. $T_{inv} = 2.65$ nm; $T_{Si} = 7.5$ nm; $T = 300$ K

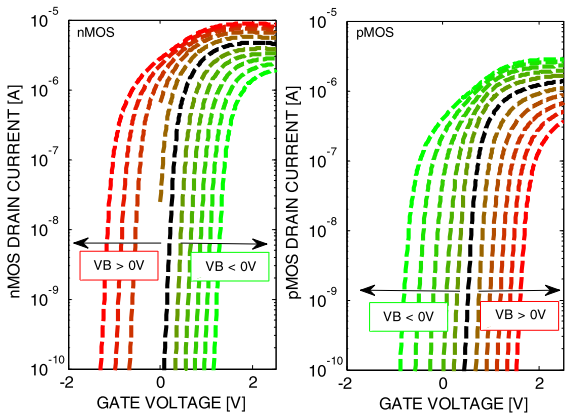

Fig. 3 Drain current as a function of the gate voltage for various back biases ranging from −10 V to 10 V in steps of 2 V) in n- (**a**) and pMOS devices (**b**). $T_{inv} = 2.65$ nm; $T_{Si} = 7.5$ nm; $T = 300$ K

contribution observed at lower density). This is further depicted in Fig. 5 which represents the mobility variation as a function of VB for fixed inversion charge for both devices.

Figure 6 shows the profile of the potential and the electron density in the channel simulated using Poisson-Schrödinger solver (PS) for three front and back gate voltage conditions specified in Fig. 5 ($N_{inv} = 1e13$ cm^{-2}). The application of a high positive BB induces a back gate inversion for nMOS devices. No clear "volume" inversion regime is however reached as the majority of carriers are still confined at front and back interfaces. This is expected since the silicon channel is too thick ($T_{Si} = 7.5$ nm) to reach this regime [15]. The mobility enhancement can be explained by the shift of the inversion charge centroid away from the front interface affecting surface-roughness and the screening of the coulombic effect at the high-k/IL interface [13, 16].

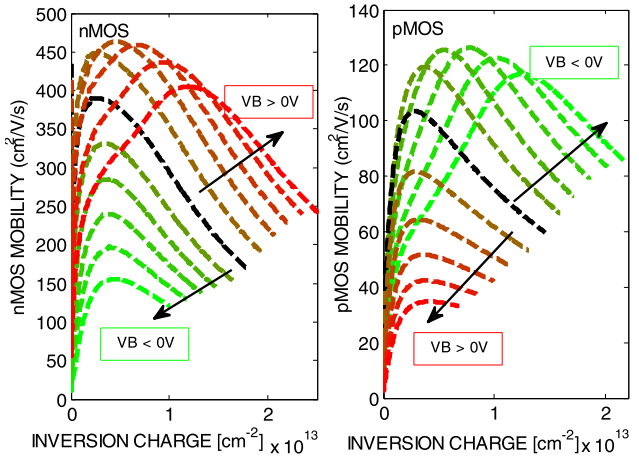

Fig. 4 Experimental effective mobility as a function of the inversion charge for various back biases ranging from −10 V to 10 V in steps of 2 V, in n- (**a**) and pMOS devices (**b**). $T_{inv} = 2.65$ nm; $T_{Si} = 7.5$ nm; $T = 300$ K. $R_{access} = 2 \times 60$ Ω·μm

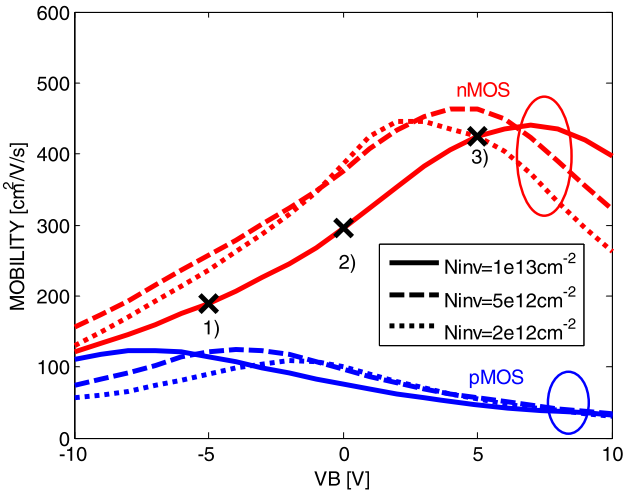

Fig. 5 Effective experimental mobility as a function of the back bias for various inversion densities: $N_{inv} = 1e13$, 5e12 and 2e12 cm^{-2}. $T_{inv} = 2.65$ nm; $T_{Si} = 7.5$ nm; $T = 300$ K. Symbols represent biases conditions whose density profiles are extracted in Fig. 6: (1) $VB = -5$ V, $VG = 2.0$ V; (2) $VB = 0$ V, $VG = 1.6$ V; (3) $VB = 5$ V, $VG = 1.2$ V. $R_{access} = 2 \times 60$ Ω·μm

2.2 Influence of the IL EOT

The gate capacitance for three devices with physical IL thicknesses of 2.4 nm, 3.5 nm and 4.0 nm is shown in Fig. 7. The mobility variation with respect to the inversion charge for four structures with different IL physical thickness (1.0, 2.4, 3.5 and 4.0 nm) is shown in Fig. 8. A significant degradation of the mobility is observed and can be attributed to the presence of interfacial charge at the high-k/IL interface. The degradation of the mobility in presence of high-k oxide is well known and can be attributed to remote Coulomb [6–10], remote phonon [27] or remote surface roughness scat-

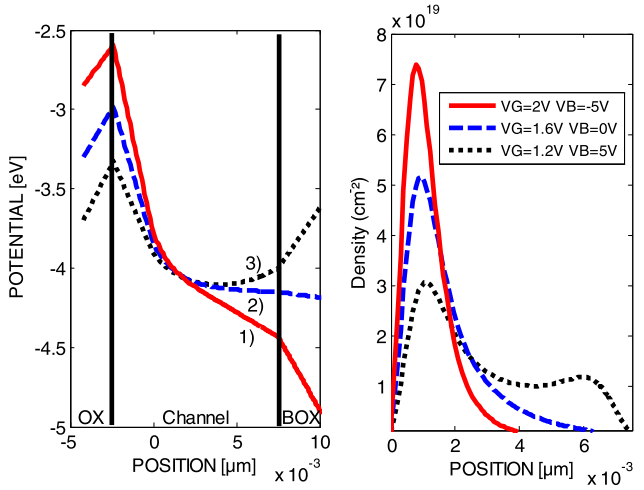

Fig. 6 Simulated profile of the potential (**a**) and the electron density (**b**) in the channel for various biases conditions using PS simulations: (1) $VB = -5$ V, $VG = 2.0$ V; (2) $VB = 0$ V, $VG = 1.6$ V; (3) $VB = 5$ V, $VG = 1.2$ V. nMOS device, $T_{inv} = 2.65$ nm. $T_{Si} = 7.5$ nm; $T = 300$ K

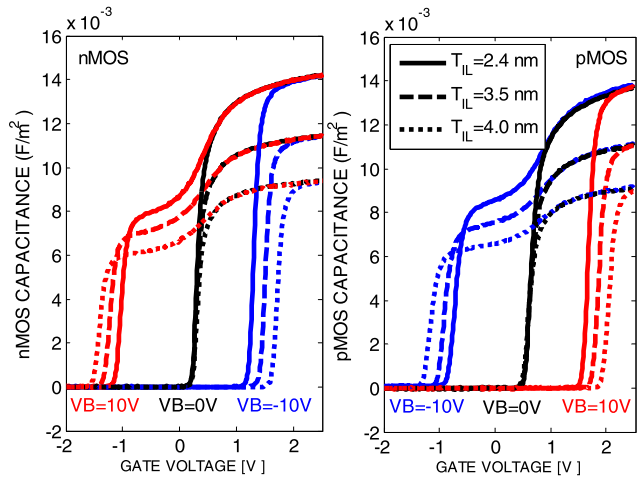

Fig. 7 Gate capacitance as a function of the gate voltage for various back biases (VB): $VB = -10$, 0 and 10 V. IL physical thicknesses of the devices: 2.4, 3.5 and 4.0 nm

tering [11]. However, it has been demonstrated in [10] that the remote phonon scattering mechanism is significant for IL EOT < 1 nm. Concerning remote surface roughness scattering, there is a controversial debate about its importance. Indeed, some groups suggest that it may degrade the mobility [18, 19] but there is no publication demonstrating it by means of experimental data. Moreover, for IL EOT > 1 nm, our simulations tend to demonstrate that RC is the main mechanisms responsible for the mobility degradation (variation of the mobility with the IL EOT is well reproduced by considering RC only). In this paper, since simulations targeted to reproduce devices with IL EOT > 1 nm, remote phonon and remote surface roughness have been neglected.

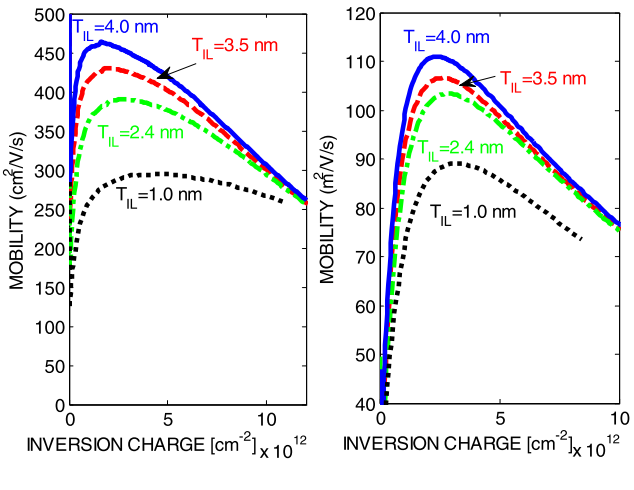

Fig. 8 n- (**a**) and pMOS (**b**) experimental effective mobility as a function of the inversion charge for structures with various IL physical thicknesses ($VB = 0$ V). $R_{access} = 2 \times 60\ \Omega{\cdot}\mu m$

3 Advanced solvers for reference mobility simulations

3.1 NEGF

It has been recently shown that fundamental mobility calculation in advanced high-k devices can be performed with NEGF solvers [12, 13, 16, 31]. NEGF mobility simulations have been performed [17] with a view of obtaining accurate and reliable references for RC-limited mobility and SR-limited mobility. The methodology presented in [16] is briefly summarized hereafter: either SR or RC-limited mobility is obtained by means of geometrical fluctuations of the SiO_2/Si front and back interfaces and the inclusion of random coulombic centers. Random samples of disorder with width $W = 20$ nm and length $L = 30$ nm are generated and then, we built devices made of these units repeated once, twice ($L = 60$ nm), and up to three times ($L = 90$ nm). One nanometer of SiON is included in the effective mass Hamiltonians on both sides of the film. We next computed the resistance of the devices in a mode space approach, including electron-phonon scattering. As expected, in a long channel device, the resistance of the devices is proportional to their length, allowing for an accurate extraction of the resistance of the disordered sample. We finally computed the phonon-limited mobility μ_{PH} in smooth films and extracted an "effective" mobility $\mu_{SR}^{-1} = \mu_{SR+PH}^{-1} - \mu_{PH}^{-1}$ (SR) or $\mu_{RCS}^{-1} = \mu_{RCS+PH}^{-1} - \mu_{PH}^{-1}$ (RC). Note that direct NEGF calculation of the SR or RC-limited mobility is not possible. Indeed, in absence of inelastic scattering such as the one with optical phonons, quantum transport cannot reduce in a conventional ohmic regime even in long channel device, because of extreme localization.

3.2 Semi-classical approach

Advanced and computationally efficient solvers based on Momentum Relaxation Time (MRT) approximation are often used to calculate the SR and RC-limited mobility [12, 13, 20]. In a previous study [12], we have compared KG and NEGF mobility calculations in SiO_2-based FDSOI device. We extend our comparisons to back biased devices featuring RC effects. In order to make relevant comparisons, we carefully choose identical parameters for both methods. As for NEGF, acoustic phonons are treated as an isotropic, elastic mechanism and inter-valley phonons as isotropic with fixed phonon energies. Surface roughness is treated as elastic, anisotropic mechanism within the generalized Prange-Nee model [22]. Coulomb scattering is treated as an intra-valley, elastic scattering mechanism and RC and SR matrix elements are screened using the scalar Lindhard approach [7].

3.3 Mobility extraction: discussion about the Matthiessen's rule

As mentioned, in NEGF simulations, the SR or RC-limited mobility cannot be extracted directly by turning off the phonon scattering mechanisms. An "effective" mobility μ_{M}, based on the Matthiessen's rule is defined and used for the comparison between the different solvers:

$$\mu_{\mathrm{M}}^{-1} = \mu_{\mathrm{A+PH}}^{-1} - \mu_{\mathrm{PH}}^{-1} \tag{1}$$

A is the considered scattering mechanism: SR or RCS in this paper.

The validity of the Matthiessen's rule has been recently questioned and quantitative errors have been evaluated using the following expression [23, 24]:

$$E = \frac{\mu_{\mathrm{M}} - \mu_{\mathrm{A}}}{\mu_{\mathrm{A}}} \tag{2}$$

With μ_{A} the mobility for mechanism A directly calculated using KG simulations.

An error ranging from -20 to -12 % is observed (Fig. 9) when extracting the SR-limited mobility using the Matthiessen's rule. This is consistent with simulations in [23]. Concerning RC scattering, the error can reach -80 % which is of the order of magnitude than the error found for local Coulomb scattering [23]. It is therefore important, for the solvers comparison, to use the same method to extract the mobility. The SR-limited mobility comparison between NEGF and KG is done by using Matthiessen's rule and, concerning RC-limited mobility, Phonon scatterings are included. Moreover, since TCAD mobility models use the Matthiessen's rule to combine all single mechanisms, parameters are calibrated on mobility extracted using the Matthiessen's rule.

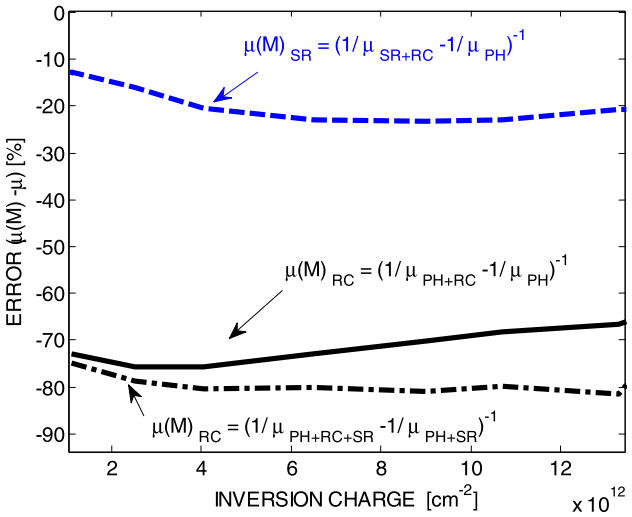

Fig. 9 Error E produced by the extraction of mobility components (surface roughness and remote Coulomb scattering) using the Matthiessen's rule

3.4 Results

Advanced solvers comparison has been performed for electrons using the effective mass approximation (purely parabolic band structure) with a Si/SiON barrier of 3.15 eV. In silicon, the longitudinal and transversal masses are $m_l^* = 0.916m_0$ and $m_t^* = 0.191m_0$ respectively and the effective mass in oxide is $m^* = 0.5m_0$. The gate stack of the device is made of 2 nm of HfO_2 ($\varepsilon = 22\varepsilon_0$) on top of 2.4 nm of SiON ($\varepsilon = 5.21\varepsilon_0$). The silicon channel and the BOX thicknesses are 7.5 nm and 25 nm respectively.

Following [12] which reports an overestimation of the SR-limited mobility when calculated with the KG solvers, the SR parameter Δ_{SR} is increased up to 0.62 nm using an exponential autocorrelation function with $\Lambda_{\mathrm{SR}} = 1.3$ nm (while in NEGF a more usual value $\Delta_{\mathrm{SR}} = 0.47$ nm is used with $\Lambda_{\mathrm{SR}} = 1.3$ nm). On the other hand, we found out that RC-limited mobility tends to be slightly underestimated (for $T_{\mathrm{IL}} = 2.4$ nm) with the KG simulations when compared to NEGF [13, 16]. Consequently, the charge density at the high-k/IL interface is adapted (3e13 cm^{-2} for KG and 5e13 cm^{-2} for NEGF). The difference can be due to the first order approximation of the Boltzmann Transport Equation when calculating the RC-limited mobility or the use of the Matthiessen's rule in the MRT-based approach. These approximations are well discussed in [28]. Once these parameters have been adjusted, a good correlation has been found as depicted in Figs. 10 and 11, for $VB = 0$ V and $VB = 8$ V. An interesting point can be noticed in comparing Figs. 10 and 11. While in an unbiased device, the RC contribution to the total mobility is large, in the back biased device, the RC contribution appears much weaker.

Considering the good agreement between the two solvers, an exhaustive series of simulations with the much more

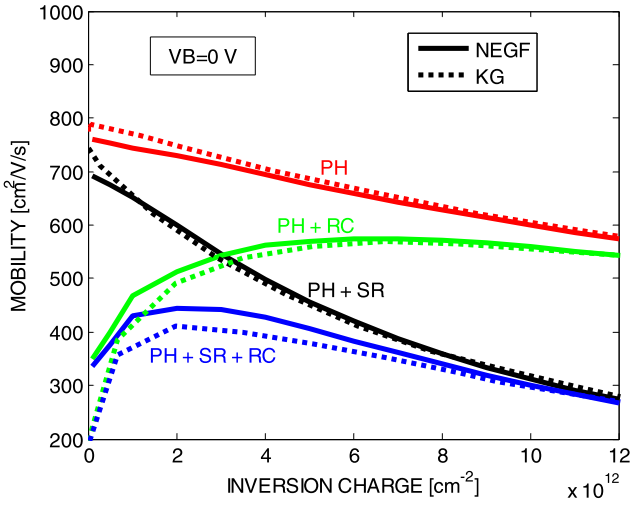

Fig. 10 nMOS effective mobility components (PH, SR and RC mobility) at $VB = 0$ V. Comparison between NEGF and KG results. Parameters for SR: exponential SR autocorrelation with $\Delta_{SR} = 0.47$ nm and $\Lambda = 1.3$ nm for NEGF and $\Delta_{SR} = 0.62$ nm and $\Lambda_{SR} = 1.3$ nm for KG. Charge density at high-k/IL interface: 3e13 cm^{-2} for KG and 5e13 cm^{-2} for NEGF

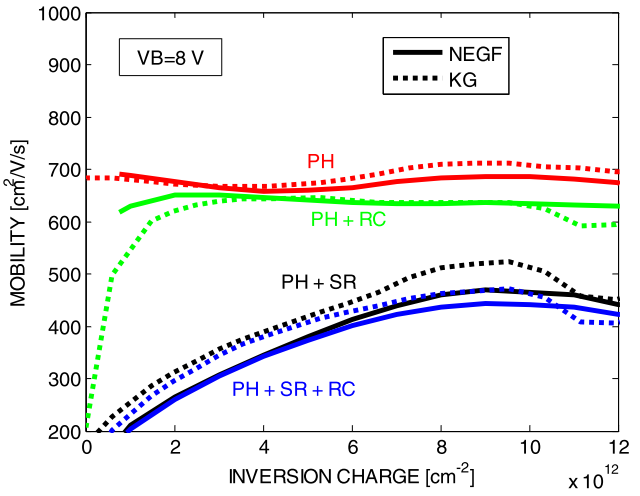

Fig. 11 nMOS effective mobility components (PH, SR and RC mobility) at $VB = 8$ V. Comparison between NEGF and KG results. Parameters for SR: exponential SR autocorrelation with $\Delta_{SR} = 0.47$ nm and $\Lambda_{SR} = 1.3$ nm for NEGF and $\Delta_{SR} = 0.62$ nm and $\Lambda_{SR} = 1.3$ nm for KG. Charge density at high-k/IL interface: 3e13 cm^{-2} for KG and 5e13 cm^{-2} for NEGF

CPU efficient KG solvers has been performed varying the IL thickness, the temperature, the interface charge density and the back bias (part IV). Unfortunately, direct hole mobility comparisons between NEGF and KG are still missing. Therefore, for the purpose of TCAD calibration in pMOS device, a series of 6k.p-based KG simulations [20] (with Luttinger-Kohn parameters: $\gamma_1 = 4.27$, $\gamma_2 = 0.315$ and $\gamma_3 = 1.387$ [30]) has been performed using the same $\Lambda_{SR} =$ 1.3 nm parameter as for nMOS while $\Delta_{SR} = 0.40$ nm has been adjusted on measurements.

4 TCAD models calibration

4.1 TCAD mobility models calibration

As already mentioned, mobility in TCAD software (all simulations shown here are performed with Sentaurus Device—Sdevice [21]) is determined using empirical models which depend on a series of unknown parameters that have to be calibrated. A recent model accounting for the mobility degradation in thin channel at both front and back interfaces has been developed in [25] (Eq. 297 in [26]). The parameters of this model have been carefully calibrated in [26] and therefore are used in the present study. Note nevertheless that a slight change of the SR parameters was mandatory to better reproduce measurements ($\delta = 2.5$e18 cm^2/V s, $\eta = 1$e50 V^2/cm/s for nMOS and $\delta = 4.10$e15 cm^2/V s, $\eta = 5.82$e31 V^2/cm/s for pMOS in Eq. (3)). The SR-limited mobility is given by:

$$\mu_{SR} = \left(\frac{(F_\perp / F_{ref})^{A^*}}{\delta} + \frac{F_\perp^3}{\eta} \right)^{-1} \tag{3}$$

The RC-limited mobility was modeled using the following equation [26]:

$$\mu_C = \frac{\mu_1 (1 + (c/c_{trans})^v)}{(\frac{N_C}{N_0})^{\eta_2} . D} \tag{4}$$

With $D = \exp(-\frac{x}{l_{crit}})$, x is the distance from high-k/IL interface, N_c is the negative or positive interface charge density, c is the local carrier concentration in the channel and the other terms are fitting parameters. The mobility variation with the temperature can be expressed for each scattering mechanisms through the law $\mu\alpha(\frac{T}{300\text{ K}})^\gamma$. From KG simulations, we have determined the values of these coefficients for nFDSOI devices: $\gamma_{PH} \simeq -1.7$, $\gamma_{SR} \simeq -0.95$, $\gamma_{RC} \simeq -0.41$ and $\gamma_{Tot} \simeq -1.1$. There is a strong difference in our TCAD models as the dependence of the SR and RC-limited mobility with temperature is neglected.

The calibrated RC-limited mobility model (Eq. (4)) is compared to KG results. Figure 12 shows the variation of the nMOS RC mobility with respect to the inversion charge for various high-k/IL interface charge densities (Fig. 12a) and for various IL EOT (Fig. 12b). The calibrated empirical model reproduces well the mobility determined with KG solvers. Similarly, RC-limited mobility has also been calibrated for pMOS in Fig. 13.

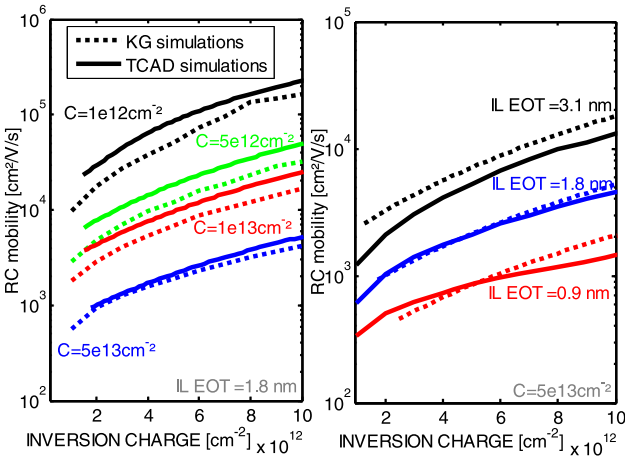

Fig. 12 nMOS effective remote Coulomb-limited electron mobility in FDSOI devices as a function of the inversion charge. KG and TCAD simulations are performed (**a**) for various high-k/IL interface charge density in a device with IL EOT = 1.8 nm and (**b**) for various IL EOT for a fixed interface charge density $C = 5\text{e}13\ \text{cm}^{-2}$. $T_{\text{Si}} = 7.5$ nm; $T = 300$ K. TCAD model parameters: $\mu_1 = 25\ \text{cm}^2/\text{V/s}$, $c_{\text{trans}} = 1\text{e}18\ \text{cm}^{-3}$, $\nu = 1.3$, $\eta_2 = 1$, $l_{\text{crit}} = 1.25\text{e-}7$ cm. Phonons parametersfrom [28]

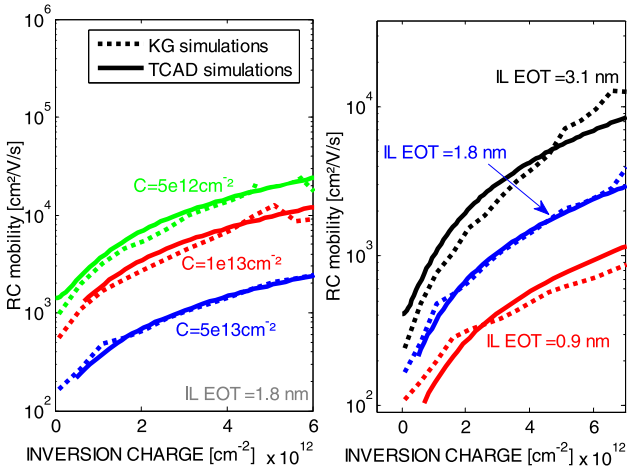

Fig. 13 Same as Fig. 12 but for holes. TCAD models parameters: $\mu_1 = 23\ \text{cm}^2/\text{V/s}$, $c_{\text{trans}} = 1\text{e}18\ \text{cm}^{-3}$, $\nu = 1.6$, $\eta_2 = 1$, $l_{\text{crit}} = 1.5\text{e}^{-7}$ cm

4.2 Comparison to experimental data

In order to investigate the accuracy of calibrated TCAD models, the total mobility for nMOS is then simulated using TCAD and KG solvers (parameters in Table 1) varying the IL EOT (Fig. 14) and the temperature of the device (Fig. 15). Concerning nMOS, a charge density of $3\text{e}13\ \text{cm}^{-2}$ at high-k/IL interface is used to fit experimental data and excellent agreements are found between solvers and experimental data. This charge density theoretically leads [10] to a variation of VTH of nearly 0.45 V.

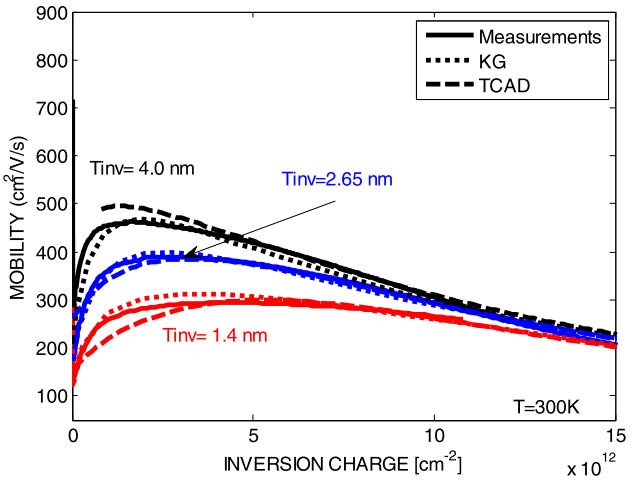

Fig. 14 n-MOS mobility as a function of the inversion charge for structures with various IL EOT. Comparison between TCAD, KG solvers and experiments. $R_{\text{access}} = 2 \times 60\ \Omega{\cdot}\mu\text{m}$

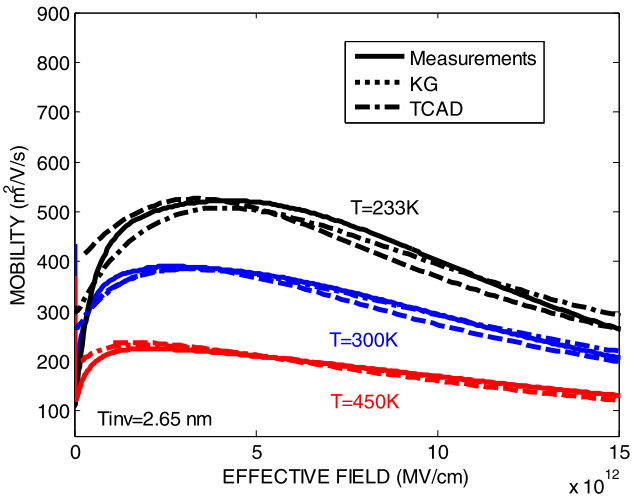

Fig. 15 n-MOS mobility as a function of the inversion charge for various temperatures. Comparison between TCAD, KG solvers and experiments. $R_{\text{access}} = 2 \times 60\ \Omega{\cdot}\mu\text{m}$

These simulations have been also performed for pMOS devices, see Figs. 16 and 17, using a charge density of $6\text{e}13\ \text{cm}^{-2}$ at high-k/IL interface. In TCAD, the slight underestimation of the mobility variation with temperature can be due to the fact that our RC and SR-limited mobility models neglect the variation with the temperature.

The total mobility is then extracted as a function of the IL EOT, at $N_{\text{inv}} = 2\text{e}13\ \text{cm}^{-2}$ (Fig. 18). Good agreement is found for IL EOT > 1 nm for both devices. The degradation of the mobility with the IL thickness is well captured by considering RC scattering only. This tends to suggest that RP and RSR has a negligible impact for IL EOT > 1 nm.

Figure 19 is the variation of the mobility with the temperature for various inversion charges and for n- and pMOS.

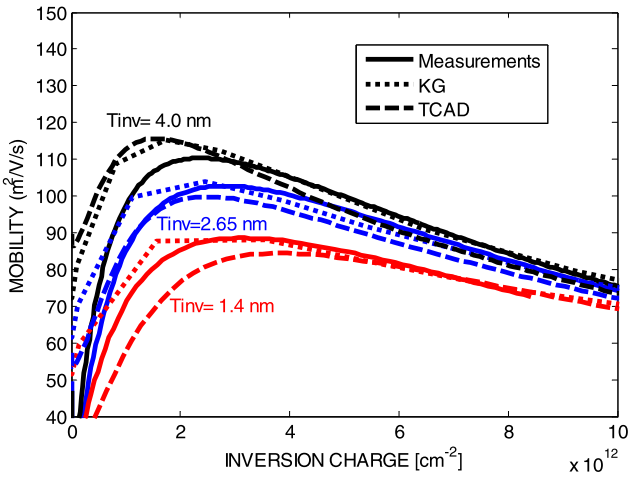

Fig. 16 pMOS mobility as a function of the inversion charge for structures with various IL EOT. Comparison between TCAD, KG solvers and experiments. $R_{\text{access}} = 2 \times 60\ \Omega{\cdot}\mu\text{m}$

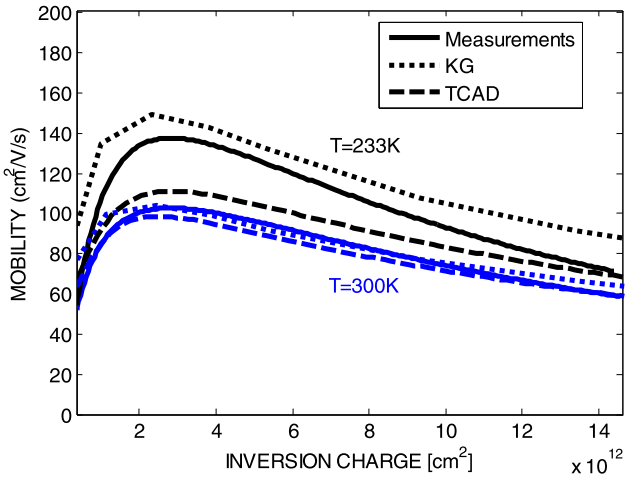

Fig. 17 pMOS mobility as a function of the inversion charge for various temperatures. Comparison between TCAD, KG solvers and experiments. $R_{\text{access}} = 2 \times 60\ \Omega{\cdot}\mu\text{m}$

The mobility degradation (due to the increase of phonon scattering) with increasing temperatures is well reproduced by simulations for both devices.

As a ultimate benchmark, the variation of the mobility with VB is accurately accounted for, as testified by Fig. 20. As can be seen, the experimental behavior (depicted in Fig. 5) is well captured by KG solvers but also by TCAD simulations.

5 Conclusions

In this paper, we presented a multi-scale simulation strategy for UTBB-FDSOI devices featuring high-k/metal-gate. In a first part, we demonstrated from split-CV measurements

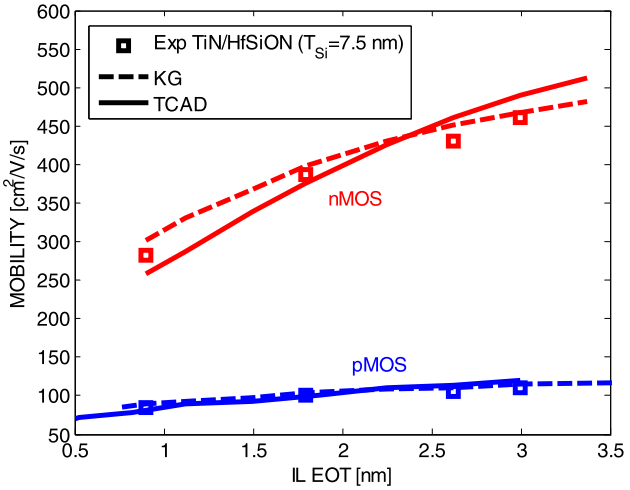

Fig. 18 n- and pMOS mobility extracted at fixed inversion density (2e12 cm^{-2}) as a function of the IL EOT for various temperatures: 233, 300 and 450 K. Comparison between TCAD, KG solvers and experiments. $R_{\text{access}} = 2 \times 60\ \Omega{\cdot}\mu\text{m}$

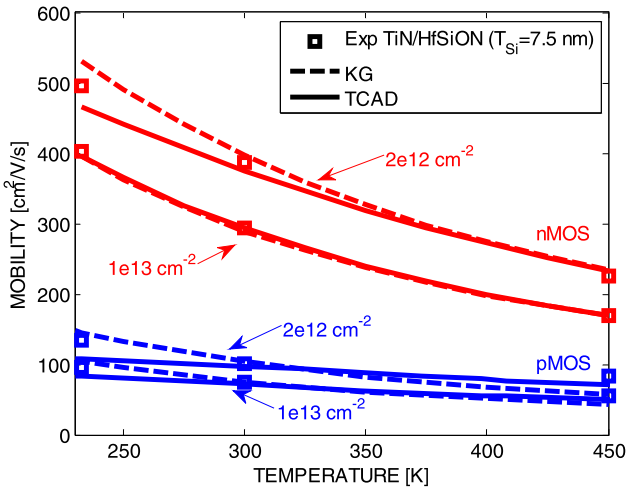

Fig. 19 n- and pMOS mobility as a function of the temperature at fixed inversion densities (2e12 cm^{-2} and 1e13 cm^{-2}). Comparison between TCAD, KG solvers and experiments. $T_{\text{inv}} = 2.65$ nm; $T_{\text{Si}} = 7.5$ nm. $R_{\text{access}} = 2 \times 60\ \Omega{\cdot}\mu\text{m}$

that the mobility can significantly be improved by applying positive and negative BB for n- and pMOS respectively. The high applied VB induces a back channel inversion and a displacement of the inversion charge centroid affecting surface roughness scattering mechanisms as well as the screening of the coulombic effect at high-k/IL interface.

In the second part of this paper, we presented a direct comparison between NEGF and KG solvers with a view of obtaining reference mobility curves for TCAD models calibration. Adjusting KG SR parameters (Δ_{SR}) and the charge density at high-k/IL interface, we demonstrated that KG solvers reproduce well NEGF results. These solvers are consequently accurate and more CPU efficient than NEGF to be

Table 1 Simulations parameters for KG solvers

	Band structure	Phonon	Surface roughness	Remote Coulomb
Electron	parabolic band structure	Parameters of [29]	Exponential Autocorrelation $\Delta_{SR} = 0.47$ nm and $\Lambda_{SR} = 1.3$ nm. Scalar Lindhard screening.	Tensorial Lindhard screening. Charge density at high-k/IL interface: 3e13 cm^{-2}.
Hole	six-bands $k.p$ model	Parameters of [29]	Exponential Autocorrelation $\Delta_{SR} = 0.40$ nm and $\Lambda_{SR} = 1.3$ nm. Scalar Lindhard screening.	Tensorial Lindhard screening. Charge density at high-k/IL interface: 6e13 cm^{-2}.

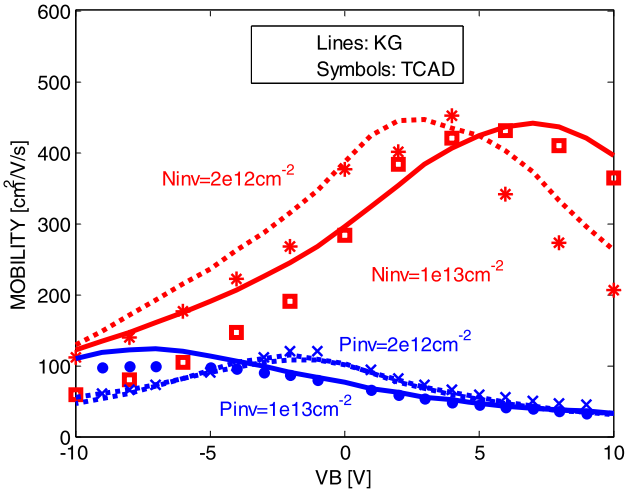

Fig. 20 Simulated effective mobility as a function of the back bias for various inversion densities: $N_{inv} = 1e13$ and $2e12$ cm^{-2}. $T_{inv} = 2.65$ nm; $T_{Si} = 7.5$ nm; $T = 300$ K. $R_{access} = 2 \times 60\ \Omega{\cdot}\mu$m

used as a reference to calibrate TCAD empirical mobility models.

In conclusion, we demonstrated that, after a calibration on KG solvers, TCAD mobility models can well reproduce the mobility behavior in high-k/metal-gate UTBB-FDSOI devices varying the back bias, the high-k/IL concentration charge and the temperature. Moreover, we successfully model mobility degradation in high-k/metal-gate device with the IL thickness considering RC only (in addition to PH and SR). This suggests that, for the considered devices with EOT IL > 1 nm, other high-k degradation mechanisms can be neglected.

Acknowledgements This work was supported by the French ANR project QUASANOVA. The NEGF calculations were run on the TGCC/Curie machine using allocations from PRACE and GENCI.

References

1. Fenouillet-Beranger, C., et al.: Fully-depleted SOI technology using high-k and single-metal gate for 32 nm node LSTP applications featuring 0.179 µm 2 6T-SRAM bitcell. In: IEEE International Electron Devices Meeting. IEDM 2007. IEEE Press, New York (2007)
2. Fenouillet-Beranger, C., et al.: FDSOI devices with thin BOX and ground plane integration for 32 nm node and below. Solid-State Electron. **53**(7), 730–734 (2009)
3. Planes, N., et al.: 28 nm FDSOI technology platform for high-speed low-voltage digital applications. In: 2012 Symposium on VLSI Technology (VLSIT), pp. 133–134. IEEE Press, New York (2012)
4. www.itrs.net: International Technology Roadmap for Semiconductors
5. Ragnarsson, L.-A., et al.: On the origin of the mobility reduction in bulk-Si, UTBOX-FDSOI and SiGe devices with ultrathin-EOT dielectrics. In: 2011 International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA), pp. 1–2. IEEE, New York (2011)
6. Cassé, M., et al.: Carrier transport in HfO_2/metal gate MOSFETs: physical insight into critical parameters. IEEE Trans. Electron Devices **53**(4), 759–768 (2006)
7. Esseni, D., Abramo, A.: Modeling of electron mobility degradation by remote Coulomb scattering in ultrathin oxide MOSFETs. IEEE Trans. Electron Devices **50**(7), 1665–1674 (2003)
8. Barraud, S., Bonno, O., Cassé, M.: The influence of Coulomb centers located in HfO/SiO gate stacks on the effective electron mobility. J. Appl. Phys. **104**, 073725 (2008)
9. Casterman, D., De Souza, M.M.: Evaluation of the Coulomb-limited mobility in high-κ dielectric metal oxide semiconductor field effect transistors. J. Appl. Phys. **107**(6), 063706 (2010)
10. Toniutti, P., et al.: On the origin of the mobility reduction in n-and p-metal–oxide–semiconductor field effect transistors with hafnium-based/metal gate stacks. J. Appl. Phys. **112**(3), 034502 (2012)
11. Gamiz, F., Roldan, J.B.: Scattering of electrons in silicon inversion layers by remote surface roughness. J. Appl. Phys. **94**(1), 392–399 (2003)
12. Rideau, D., et al.: Mobility in FDSOI devices: Monte Carlo and Kubo Greenwood approaches compared to NEGF simulations. In: Proc. SSDM, p. 60 (2012)
13. Rideau, D., et al.: Mobility in High-K Metal Gate UTBB-FDSOI Devices: from NEGF to TCAD perspectives. Accepted IEDM
14. Esseni, D., Sangiorgi, E.: Low field electron mobility in ultra-thin SOI MOSFETs: experimental characterization and theoretical investigation. Solid-State Electron. **48**(6), 927–936 (2004)
15. Ernst, T., et al.: Ultimately thin double-gate SOI MOSFETs. IEEE Trans. Electron Devices **50**(3), 830–838 (2003)
16. Niquet, Y.-M., et al.: Quantum calculations of the carrier mobility in thin film devices: Methodology, Matthiessen's rule and comparison with semi-classical approaches. Submitted J. Appl. Phys.
17. http://inac.cea.fr/L_Sim/TB_Sim/
18. Zhang, X.F., et al.: A physical model on scattering at high-k dielectrics/SiO_2 interface of SiGe p-MOSFETs. IEEE Trans. Electron Devices **54**, 3097–3102 (2007)

19. Ghosh, B., et al.: Monte Carlo study of remote Coulomb and remote surface roughness scattering in nanoscale Ge PMOSFETs with ultrathin high-k dielectrics. Solid-State Electron. **50**(2), 248–253 (2006)
20. UTOX regroups a series of k.p-Schrodinger-based tools including a KG solver. Garetto, D., et al. Modeling study of capacitance and gate current in strained High–K Metal gate technology: impact of Si/SiO_2/HK interfacial layer and band structure model (2010)
21. http://www.synopsys.com/Tools/TCAD/
22. Jin, S., Fischetti, M.V., Tang, T.-W.: Modeling of surface-roughness scattering in ultrathin-body SOI MOSFETs. IEEE Trans. Electron Devices **54**(9), 2191–2203 (2007)
23. Esseni, D., Driussi, F.: A quantitative error analysis of the mobility extraction according to the Matthiessen rule in advanced MOS transistors. IEEE Trans. Electron Devices **58**(8), 2415–2422 (2011)
24. Chen, M.-J., Lee, W.-H., Huang, Y.-H.: Error-Free Matthiessen's Rule in the MOSFET Universal Mobility Region. IEEE Trans. Electron Devices **60**(2), 1–6
25. Reggiani, S., et al.: Low-field electron mobility model for ultrathin-body SOI and double-gate MOSFETs with extremely small silicon thicknesses. IEEE Trans. Electron Devices **54**(9), 2204–2212 (2007)
26. Sentaurus Device User Guide. Version H-2013.03. SYNOPSYS
27. Fischetti, M.V., Neumayer, D.A., Cartier, E.A.: Effective electron mobility in Si inversion layers in metal–oxide–semiconductor systems with a high−κ insulator: the role of remote phonon scattering. J. Appl. Phys. **90**(9), 4587–4608 (2001)
28. Paussa, A., Esseni, D.: An exact solution of the linearized Boltzmann transport equation and its application to mobility calculations in graphene bilayers. J. Appl. Phys. **113**, 093702 (2013)
29. Esseni, D., et al.: Physically based modeling of low field electron mobility in ultrathin single-and double-gate SOI n-MOSFETs. IEEE Trans. Electron Devices **50**(12), 2445–2455 (2003)
30. Chao, C.Y.-P., Chuang, S.L.: Spin-orbit-coupling effects on the valence-band structure of strained semiconductor quantum wells. Phys. Rev. B **46**(7), 4110–4122 (1992)
31. Anantram, M.P., Lundstrom, M.S., Nikonov, D.E.: Proc. IEEE **96**, 1511 (2008)