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Analysis of trap distribution and NBTI degradation in Al_2O_3/SiO_2 dielectric stack

Yiyi Yan *, Valeriya Kilchytska, Denis Flandre, Jean-Pierre Raskin

ICTEAM Institute, Université catholique de Louvain, Louvain-la-Neuve, Belgium

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ABSTRACT

In this work, p-substrate MOS capacitors with plasma-enhanced atomic-layer-deposited Al_2O_3/ thermally-grown SiO_2 dielectric stack (with a target equivalent oxide thickness of 4.2 nm) are investigated by means of the conductance method in a temperature range from 25 °C to 150 °C. The trap state density and energy level distribution in the silicon bandgap are extracted over the bandgap. Furthermore, negative bias temperature instability is analyzed by two-point capacitance–voltage characterization to evaluate the electrical stability and dielectric reliability of the Al_2O_3/SiO_2 stack. The contributions from interface and oxide trap generations are detailed. Our results indicate that plasma-enhanced atomic layer deposited Al_2O_3 on thermal SiO_2 stack features low interface trap density, and comparable dielectric reliability to conventional SiO_2, SiO_xN_y, and high-*k* dielectric stacks.

1. Introduction

Recently, high negative fixed oxide charges (Q_f), sufficiently low interface trap density (D_{it}) and sustainable material usage have been investigated in atomic-layer-deposited (ALD) Al_2O_3 layers for surface passivation in photodetectors and photovoltaics [1]. In relation with its (i) higher dielectric constant (k ~ 10) for high field-effect gate control with the low electrical thickness, (ii) wide energy bandgap (~8.3 eV) for decreasing leakage currents, and (iii) good thermal stability close to silicon for reliable transistor fabrication, questions have been raised in the past concerning the use of Al_2O_3 in advanced CMOS nodes with EOT < 3 nm due to (relatively low dielectric constant, high D_{it} [2], inadequate reliability performance [3]) compared to HfO_2. In this work, we would like to revisit the use of Al_2O_3/SiO_2 stack for EOT ≈ 4.2 nm as used in analog, I/O (input/output) or resistive random access memory (RRAM)-based radio-frequency (RF) switches supporting higher operating voltages than the core (i.e. digital) MOSFETs. According to literature [4,5], Al_2O_3/SiO_2 stack with 6.5 nm EOT allows operating voltage ($V_{max} \geq 7$ V) twice exceeding the value of thermal SiO_2 of the same EOT (~3.6 V for 0.18 μm process HV gate oxide with EOT 6.2 nm).

Indeed, for n-MOS transistors, large number of negative fixed oxide charges (Q_f) in ALD Al_2O_3 layers would result in a shift of threshold voltage (V_{th}) towards positive values. This could be advantageous for decreasing the doping concentration in the channel for compensating (V_{th}) change, simultaneously increasing channel mobility [6] and decreasing variability. The quality of the silicon interface critically influences the performance of such devices: interface charge scattering decreasing the channel mobility in n-MOS; SiO_x formation at interface during negative bias causing the nonlinearity of resistive switching (RS) in RRAM-based RF switches. Thus, a thermally-grown high-quality interfacial SiO_2 layer is usually needed between metal oxide and silicon to achieve more stable electrical properties but limits the range of feasible EOT above a few nanometers.

For the successful integration of Al_2O_3/SiO_2 dielectric stacks into n-MOS devices, the electrical stability and dielectric reliability have to exceed or match those of the conventional SiO_2 dielectrics. So far only a few studies have investigated the reliability of Al_2O_3/SiO_2 dielectric stacks on p-doped substrate [7]. It is widely recognized that negative bias temperature instability (NBTI) is a critical reliability concern, particularly for p-MOSFET. NBTI in n-MOSFET has been ignored because of its insignificant effect on V_{th}. In the case of RRAM-based RF switches, endurance and retention time as important consideration, refer to the reliability of a switch and the amount of time a switch maintains ON/OFF states, respectively. The OFF states are determined by the rapture of conductive filaments composed of the oxygen vacancy related intrinsic defects, which can be affected by applied negative bias and elevated temperature [8]. To optimize the performance of RRAM-based RF switches, NBTI can be employed.

* Corresponding author.
E-mail address: yiyi.yan@uclouvain.be (Y. Yan).

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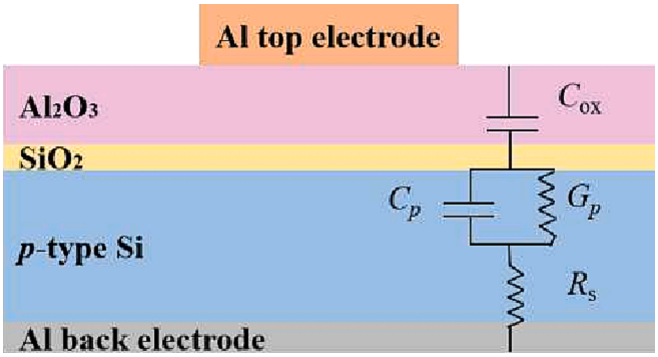

Fig. 1. Schematic cross-section of MOS capacitor with the Al_2O_3/SiO_2 stack. The inset shows the equivalent circuit of the MOS capacitor.

Table 1
Summary of electrical parameters in DUT.

Dielectric stack	Measured thickness (nm) *	EOT (nm)**	Theoretical C_{ox} (μF/cm^2)	Measured C_{ox} (μF/cm^2)
PE-ALD Al_2O_3/ thermal SiO_2	3.1 ± 0.1/2.5	4.2	0.80	0.82

* Measured thickness is the average value of 16 ellipsometry points on one sample.
** Equivalent Oxide Thickness (EOT) is calculated by: $t_{EOT} = \varepsilon_{SiO_2}\varepsilon_0 A/C_c$, where A is the gate area (0.1 cm × 0.1 cm) and C_c is the measured maximum capacitance in accumulation corrected for series resistance.

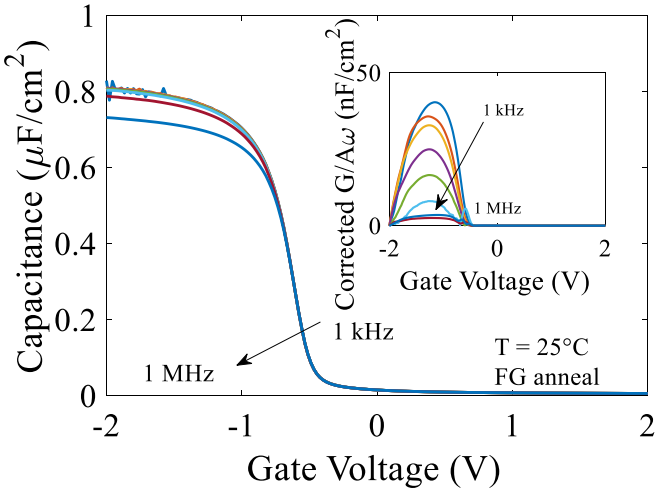

Fig. 2. Corrected capacitance versus gate voltage at room temperatures from 1 kHz to 1 MHz for DUT. The inset represents corrected conductance versus gate voltage at the same conditions.

In our previous work, the investigation of the interface between different thin dielectric Al_2O_3/SiO_2 stacks and silicon substrates was focused on the interface trap density (D_{it}) and energy level distribution in a narrow part of Si bandgap at room temperature [9]. In this work, measurements at higher temperatures are analyzed to deduce the energy level distribution of the interface states over a wider part of the bandgap, which is helpful to understand different conduction mechanisms related to shallow and deep traps in RRAM applications for further I-V characterizations. To get deeper insight on the robustness of the Al_2O_3/SiO_2 stack, we extend to p-substrate, a NBTI measurement method based on MOS capacitor *C-V* characterization named two-point capacitance–voltage (TPCV) [10].

This paper is organized as follows. Section II presents the experiment details, i.e. fabrication process, experimental setup and conditions. Results are presented and discussed in Section III. Finally, conclusions are summarized in Section IV.

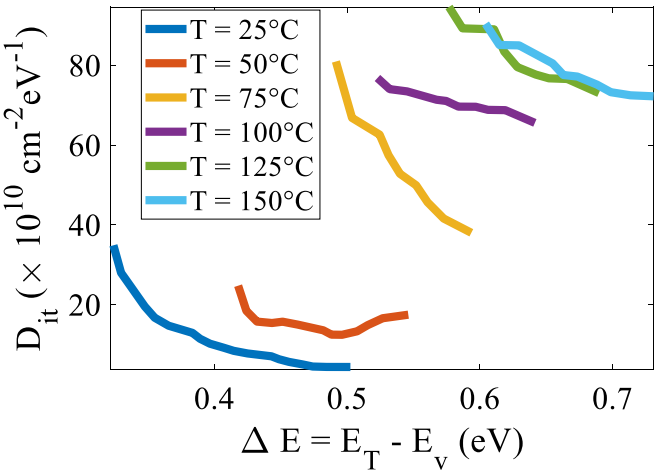

Fig. 3. D_{it} ($\Delta E = E_T - E_v$) profile under elevated temperature on DUT showing the temperature dependence of D_{it} energy distribution.

Table 2
Summary of thermal velocity and state of density with different temperatures.

Temperature (°C)	v_t(cm/s)	N_v (cm^{-3})
25	1.95×10^7	3.10×10^{19}
50	2.02×10^7	3.59×10^{19}
75	2.10×10^7	4.13×10^{19}
100	2.17×10^7	4.69×10^{19}
125	2.24×10^7	5.30×10^{19}
150	2.31×10^7	6.02×10^{19}

$v_t = \sqrt{3kT/m^*}$, where m (0.36 m_0) is the transport effective mass for holes.
** The density of state $N_v = 2(2\pi m_{dv}{}^* kT/h^2)^{3/2}$, where $m_{dv}{}^*$ is the density-of-states effective masses in the valence bands in silicon [17].

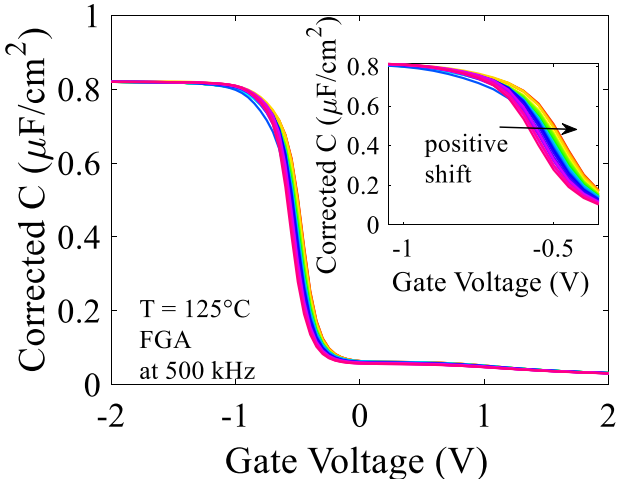

Fig. 4. C-V curve shift and stretch-out under NBTI stress at 500 kHz and 125 °C for DUT. The inset represents positive shifts of C-V curves in the depletion regime.

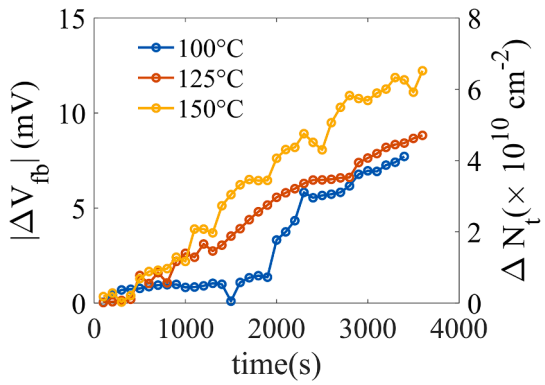

Fig. 5. Time evolution of ΔV_{fb} in absolute value and trap density ΔN_t for different temperatures from 100 to 150 °C at −2 V (E_{ox} = −4.9 MV/cm) on DUT.

2. Fabrication and characterization technique

2.1. Sample fabrication

It was reported in our previous work [9,11], that PE-ALD Al_2O_3/thermal SiO_2 stack is better suited to achieve low interface trap density (D_{it}), high negative fixed oxide charges (Q_f), and lower leakage current (J_{leak}). Thus, the present work investigates trap distribution and NBTI on this stack, as device under test (DUT) below.

Fig. 1 shows the corresponding MOS capacitor's schematic cross-section, consistent with the previous research [9]. Here, R_s is the series resistance of the Si substrate. C_{ox} is the capacitance of the dielectric stack, which simplifies the procedure of removing R_s and also the volume density of oxide traps in Al_2O_3/SiO_2 to be located at SiO_2/Si interface. G_p and C_p are the parallel equivalent conductance and capacitance, respectively, corresponding to the Si top interface.

The preparation of the MOS capacitors is as described hereafter. 3-inch Si wafers (⟨100⟩, *p*-type, 10 Ω·cm, single-side polished) were cleaned by Piranha solution (H_2SO_4/H_2O_2 3:1) at 110 °C for 20 min. After the Piranha cleaning, all the wafers were dipped in HF/deionized water (1:50) solution for removing the native oxide on the Si surfaces. Then the Si wafers were immediately put into Koyo thermal system for forming thermal SiO_2 and Fiji F200 ALD machine for Al_2O_3. The thermal SiO_2 was grown at 900 °C in an ultra-dry oxygen atmosphere. Al_2O_3 layer was deposited by plasma-enhanced atomic layer deposition (PE-ALD) at 200 °C. Trimethylaluminum precursor (TMA) from Sigma-Aldrich was used as aluminum source. TMA pulse duration and purge time were of, respectively, 0.06 and 10 s. An O_2 flow of 30 sccm and a plasma power of 300 W were used. The pulse duration and purge time of the O_2 plasma were 20 s and 5 s, respectively. The growth rate of Al_2O_3 was 1 Å per cycle. After deposition, ellipsometer measurements mapped the thicknesses of the various dielectric layers over the whole wafers. Using E-gun evaporation, 300-nm-thick Al top electrodes were deposited on the top of Al_2O_3 dielectric film by using square shadow masks, the same Al thickness fully covers the backside of the Si wafers as the back electrode of the MOS capacitor. Finally, DUT was subjected to forming gas anneal (FGA) with N_2/H_2 ratio around 9:1 at 432 °C for 30 min. Table 1 lists the parameters of DUT with top gate area and the related thicknesses of different dielectric layers.

2.2. Experimental procedure

The *C-V* measurements were conducted under dark condition using a PM8PS prober and B1500 semiconductor analyzer, with a hot-plate temperature control system allowing for precise measurements at elevated temperatures. The frequency ranges from 1 kHz to 1 MHz and temperature from 25 to 150 °C.

DUT was subjected to NBTI degradation using the measure/stress/measure (MSM) protocol. The protocol sequentially applies a constant negative voltage (−2 V) stress for a certain period of time at elevated temperatures ranging from 75 to 150 °C. The whole stress time was fixed to 3,600 s, and a *C-V* measurement was done at each 100 s step at 500 kHz frequency. To extract the flat-band voltage ΔV_{fb}, two capacitance values were extracted at V_{fb} and V_{fb} + 100 mV, respectively [12]. The extraction of V_{fb} and N_a is based on the slope of the linear part of measured capacitance *C* versus gate voltage [13].

3. Results analysis and discussion

3.1. Interface traps effect on Al_2O_3/SiO_2 stack

Using the five-element model proposed previously [11], the corrected capacitance and conductance of the stack, C_c and G_c, can be extracted after the withdrawal of series resistance (R_s in Fig. 1). Fig. 2 shows corrected *C-V* curves measured at room temperature from 1 kHz to 1 MHz. The inset of Fig. 2 shows that the amplitudes of peaks of G/ω (V) fall with increased frequencies, and it reveals the voltage range from −1.28 to −1.16 V at which the interface traps respond based on their energy levels.

To quantitatively extract the interface trap response on DUT, Fig. 3 shows the D_{it} extracted by conductance method [1] as a function of silicon bandgap energy with respect to the valence band edge at different temperatures. In practice, D_{it} can be approximated by [14]:

$$D_{it} \approx \frac{2.49}{q}\left(\frac{G_p}{\omega}\right)_{max} \quad (1)$$

where ω is angular frequency and q is electron charge. For a given gate voltage response close to accumulation regime, $(G_p/\omega)_{max}$ is the maximum value on G_p/ω versus ω curve, normalized by the electrode area and expressed in F cm^{-2}. The constant value of 2.49 is used as the correction factor for a continuous distribution of interface state traps [15]. Accessible traps energy can be calculated for any temperature and frequency according to Shockley-Read-Hall statistics of the capture and emission rate [16]:

$$\tau = \frac{1}{\omega} = \frac{exp(\Delta E/kT)}{\sigma v_t N_V} \quad (2)$$

where τ is the time constant of the interface trap, v_t is the average thermal velocity, σ is the capture cross section, N_v is the density of state in valence band, k is Boltzmann constant, and ΔE ($\Delta E = E_T - E_v$) is the energy difference between the trap energy level (E_T) and the top of the Si valence band (E_v) in p-type Si. ΔE can be calculated using Eq. (2) from the angular frequency ω corresponding to the peak of the G_p/ω vs ω

Table 3
Comparison of SiO_2, SiO_xN_y and high-*k* dielectric stacks.

Materials	T_{ox} (nm)	Dielectric constant *k*	ΔV_{th} (mV)@125 °C	D_{it} (cm^{-2} eV^{-1})	Q_f (cm^{-2})	J_{leak} (A/cm^2)	References
SiO_2	2.2	3.9	~100 (@ −2.5 V)	2.00×10^{10}	$+1.00 \times 10^{12}$	10^{-5} @ 1 V	[23,24]
SiO_xN_y/SiO_2	2.5	5.0	~100 (@ −2.5 V)	7.00×10^{11}	$+6.21 \times 10^{11}$	10^{-6} @ 1 V	[24,25]
HfO_2/SiO_2	2.4	20.0	~100 (@ −2.0 V)	5.21×10^{12}	-1.80×10^{12}	8.95×10^{-7} @ 1 V	[26,27]
Al_2O_3/SiO_2	4.0	9.0	~200 (@ −2.0 V)	1.00×10^{11}	-5.00×10^{12}	3.88×10^{-6} @ 1 V	[20,28,29]
Al_2O_3/SiO_2(DUT)	4.2	9.0	~10.0 (@ −2.0 V)	5.20×10^{10}	-4.57×10^{12}	5.06×10^{-9} @ 1 V	This work, [11]

response. Table 2 presents the average thermal velocity v_t and density of states N_v for the calculation of trap response time τ under different temperatures. By combining Eqs. (1) and (2), we obtain the D_{it} ($\Delta E = E_T - E_V$) profile for DUT as in Fig. 3. At room temperature, the trap energy states can only be measured in the narrow range of energy bandgap from 0.32 to 0.50 eV above the top of the Si valence band. To probe D_{it} across a larger energy range in the Si bandgap, temperatures from 25 to 150 °C were considered. The conductance method is used at each temperature to draw a D_{it}(E) profile. D_{it} ($\Delta E = E_T - E_V$) distributions of DUT extracted for 25, 50, 75, 100, 125, and 150 °C at 1 kHz cover the silicon bandgap from 0.32 to 0.73 eV shown in Fig. 3. The increasing trend of D_{it} with elevated temperatures shows that the higher temperature increases the capture/emission rate (=1/τ) of interface traps corresponding to ac frequency. There are more traps responding at high temperature, thus the total D_{it} appears increased. The latter effect drives hole capture and determines higher energy loss - the peak of G_p as a function of frequency $(G_p/\omega)_{max}$ related to D_{it} [15].

3.2. NBTI effect on Al_2O_3/SiO_2 stacks

Fig. 4 shows the *C-V* evolution with stress time obtained on DUT, under NBTI stress ($E_{ox} = -4.9$ MV/cm and T = 125 °C) at 500 kHz. The *C-V* curves under stress show limited positive shift of the flat-band voltage and stretch-out of the curve. This could be related to the combination of two phenomena: generation of new defects and activation of pre-existing defects [18]. Under stress, electrons injected from the gate electrode trapping in pre-existing defects of Al_2O_3 may create active defects, responsible for the time dependent drift of electrical characteristics and are then related to additional apparent oxide charges. The *C-V* curves are more stretched out with time evolution due to the generation of more interface traps. The voltage shift of a MOS capacitor curve can be expressed as the sum of two components induced by the creation of interface traps (Q_{it}) and oxide charges (Q_{ot}) [19]:

$$\Delta V_{fb} = \Delta V_{ot} + \Delta V_{it} \tag{3}$$

where ΔV_T and ΔV_{it}, relate to the apparent oxide charges and interface traps, respectively, and can be obtained from TPCV method. ΔV_{ot} is calculated as mid-gap voltage shift (ΔV_{mg}) when the Fermi level is at mid-gap and both acceptor and donor-like interface traps are neutral. The mid-gap voltage is determined from full capacitance–voltage curves corresponding to the mid-gap capacitance $C_{mg} = \frac{C_{dep}C_{ox}}{C_{ox}+C_{dep}}$, where C_{ox} and C_{dep} are the oxide capacitance and the measured capacitance in depletion, respectively.

Fig. 5 illustrates that the obtained ΔV_{fb} in absolute value and the trap density (ΔN_t) increase as a function of stress time at applied stress E_{ox} (−4.9 MV/cm) for elevated temperatures from 100 to 150 °C. The increased value of ΔV_{fb} with time indicates the generation of traps at the interface and in the oxide induced by NBTI degradation. To give insight into the generation and evolution of ΔN_t (cm^{-2}), two relations for p-substrate are used below:

$$\Delta V_{fb} = -q(\Delta N_{it} + \Delta N_{ot})/C_{ox} \tag{4}$$

$$\Delta N_t = \Delta N_{it} + \Delta N_{ot} \tag{5}$$

where C_{ox} (F/cm^2) is the gate capacitance per unit area, q (C) is the electron charge, ΔN_{it} (cm^{-2}) is the interface trap density, and ΔN_{ot} (cm^{-2}) is the oxide trap density. The increased ΔN_{it} is caused by the generation of interface traps at interface SiO_2/Si. Two possible reasons led to the generation of new oxide traps associated with an increased ΔN_{ot} during the stressing of dielectric stacks. Compared with single SiO_2, Al_2O_3 in the stack produced by plasma ALD exhibits efficient negative charge trapping resulting from pre-existed oxide traps [7]. Another potential reason could be the occurrence of Al vacancies in the Al_2O_3 film [20]. To enhance reliability, we need to optimize the thermal budget for ALD deposition [21] and the diffusion of metal gate electrode to decrease the charge trapping.

According to the literature survey, we summarize in Table 3, the published important parameters for the conventional SiO_2, SiO_xN_y/SiO_2, HfO_2/SiO_2 and Al_2O_3/SiO_2 stacks with an EOT close to 4.2 nm. The stress bias we found is close to −2 V at which RS behaviors of RRAM-based RF switches can be observed for further application purpose. Among the stacks compared in the table, our stack (PE-ALD Al_2O_3/thermal SiO_2) presents the lowest D_{it}, high Q_f, lowest leakage current density J_{leak} at 1 V, and comparable ΔV_{th} at 125 °C under stress with sustainable material usage. Low D_{it} prevents the degradation of channel mobility, subthreshold slope as well as reliability (low D_{it} initially) in MOSFETs. A high negative Q_f value allows a low channel doping concentration at constant V_{th} and a reduced oxide electrical field, leading to an improved reliability [22]. The low J_{leak} confirms a good insulator property. The ΔV_{th} at a comparable level to other dielectric stacks indicates a sufficient gate stack reliability. The generation of EOT (~4.2 nm) used in our work allows high operating voltage, maintains the reliability and lowers the leakage current. Although the dielectric constant of Al_2O_3 is lower than HfO_2 and similar to SiO_xN_y, the stack shows overall better dielectric properties than the other stacks.

4. Conclusion

In this paper, we systematically investigate PE-ALD Al_2O_3/thermal SiO_2 MOS capacitor (p-substrate) with an equivalent oxide thickness (EOT) of ~ 4.2 nm. Using the conductance and NBTI TPCV methods, we investigate the electrical properties of interface traps and dielectric reliability in detail on the Al_2O_3/SiO_2 stack. The thermally-grown high-quality SiO_2 layer plays an important role in the thin Al_2O_3/SiO_2 stack on Si substrates. Our results reveal that the optimized synthesis technology of the SiO_2 layer allows for the reduction of the interface trap density and the improvement of the dielectric stack reliability. The PE-ALD Al_2O_3/thermal SiO_2 stack could be a good candidate to replace the conventional SiO_2 in CMOS technology nodes 65 nm and beyond for analog, I/O, RRAM-based RF switches, or high-voltage transistors. Its effective negative charge trapping induced by Q_f, N_{it}, and N_{ot} would allow to keep fixed threshold voltage while lowering the channel doping and hence improving mobility, variability and NBTI. This could improve the final performance of n-MOSFETs and RRAM applications.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

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