Parametric Modeling for Improved Die Area Estimation in the Life Cycle Assessment of Electronic Systems

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Extended Abstract— Integrated Circuits (ICs) are crucial in our digital age, serving as the hardware backbone for the Internet and Communications Technology. An IC typically comprises a small piece of semiconducting material called the die, on which miniaturized transistors are fabricated to implement a functional circuit. The die is encapsulated in a package that supports the following functions: (i) protection against physical damage, (ii) heat dissipation, and (iii) electrical contact with a circuit board.

When conducting the Life-Cycle Assessment (LCA) of an electronic system, ICs are often identified as major contributors to cradle-to-gate impacts [1]. Indeed, the front-end processes involved in manufacturing silicon dies need a significant amount of material and energy resources to operate – especially fluorinated gases, ultra-pure water, and electricity – resulting in important environmental impacts per unit of semiconductor area. Consequently, it is essential for LCA practitioners to accurately estimate the die areas enclosed in the ICs of an electronic system to produce sound Life-Cycle Impact Assessment (LCIA) results.

In practice, estimating the die area of an IC is difficult as it is (a) covered by the package and (b) not disclosed in the IC datasheet. Accordingly, LCA practitioners must resort to specific approaches to assess it:

A. Chemical decapsulation of the package using acid that does not react with silicon.
B. Removal of the package through mechanical grinding.
C. Visualization of the die area using X-rays.

While these approaches provide precise estimates, they are time-intensive and require dedicated facilities that may not always be available to LCA practitioners. Moreover, these become inconvenient for complex electronic systems containing several hundred ICs. For this reason, in a time-stressed context, LCA practitioners instead rely on knowledge-based assumptions or default values provided in the scientific literature to estimate this critical parameter more quickly. Nevertheless, these default values may not be sufficiently accurate for their specific case.

Therefore, alternative approaches that require fewer resources while still offering accurate estimates of die area need to be explored. A limited number of studies have been conducted in this research field. For instance, in [2], packaged ICs are X-rayed to measure their die areas. The silicon die area is then modeled as a linear function of package area and package mass, but the model does not fit the data correctly. As a matter of fact, this linear model forms the basis of the dataset that allows LCA practitioners to model ICs in the Ecoinvent database. In [3], the die-area-to-package-area relationship does not again exhibit consistent trends. This latter paper outlines that estimation methods relying exclusively on package area to predict the die area introduce uncertainty in LCIA results. It also motivates the need for more accurate estimation approaches using easily measurable parameters.

In this work, we hypothesize that relying on a more extensive set of parameters in conjunction with non-linear models could improve the prediction of the die area. Our extended parameter set includes IC package characteristics and datasheet information. To construct this dataset, we disassembled various electronic systems with different functions (such as computers, customer premises equipment, and smartphones). For each product, we then followed the protocol described below:

1. Collect every IC present on the printed circuit boards.
2. Note external package characteristics: package area, mass, number of pins, and package type (SOP, SOT, BGA, WLP, QFN, QFP).
3. Record information from their datasheets, such as power consumption, function, and input-to-output pins ratio, when the reference is available.
4. Decapsulate the collected ICs employing the approach A described earlier.
5. Measure the area of the silicon die (or ‘dies’ in the case of stacked ICs) for each.
6. Integrate this information into a spreadsheet.

The final step – *which will be presented during the conference* – of this ongoing research will be to apply data visualization techniques and regression analysis algorithms to explore the potential for more accurately predicting the die area from our expanded parameter set using non-linear models. The envisioned model aims to serve LCA practitioners seeking to obtain a fair estimate of the silicon die area of an IC based on easily measurable parameters and quantitative data.

References

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