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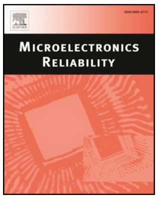

Experimental results on diodes and BIMOS ESD devices in 28 nm FD-SOI under TLP & TID radiation

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ABSTRACT

The electrostatic discharge (ESD) protection is a major concern for advanced CMOS technology manufacturing. Several solutions are available on market with efficient robustness and compliant with the ESD window especially in 28 nm FD-SOI technology. In the framework of harsh environment applications and to explore the performance under total ionizing dose (TID) radiation, it is important to investigate ESD protection devices such as gated and STI diodes in hybrid bulk or BIMOS solution in thin silicon film. This study is based on transmission line pulse (TLP) characterization before and after Co^{60} TID radiation in the range of [25 krad–200 krad]. This dose range is chosen for a first robustness exploration and in link with product applications. Following this analysis, we expect to gain better understanding of robustness and push the final performance of the device. The preliminary results will be useful to give a trend and to improve the device robustness against ESD and TID events and lead to more competitive solutions.

1. Introduction

Electro-static discharge (ESD) stress is a main challenge due to the scaling down of advanced CMOS technologies. The technology shrinkage leads to decrease the intrinsic robustness by the reduction of the ESD window. Nevertheless, several solutions with good performances and silicon integration are available for several platforms and markets [1]. Moreover, in the framework of ESD solutions in harsh environment, as ionizing radiation expected in space, medical or automotive applications, it is interesting to explore the features of ESD device protections under total ionizing dose (TID) [2]. The ESD/TID intrinsic robustness is obviously correlated to substrate, oxide and interface quality. Moreover, specific design techniques are useful to push the limit of the robustness in harsh environment. For the first time, this study delivers preliminary results and trends for gated and STI diodes and for a BIMOS transistor [3,4] under ESD and after radiation stresses (see Table 1), in 28 nm ultra-thin body and buried oxide (UTBB) fully depleted (FD) silicon on insulator (SOI) technology from STmicroelectronics.

On one hand, an open BOX area allows to reach the massive "bulk" substrate where power devices are integrated. Thus, ESD devices in this area, named hybrid bulk, have the full silicon volume to dissipate the surge. On another hand, the FD-SOI area consists of a thin silicon film with thickness $T_{si} = 7$ nm over a buried oxide with $T_{BOX} = 25$ nm. Fig. 1 depicts a cross section of substrate scanning electron microscopy (SEM) view with the FD-SOI and the hybrid bulk areas and with/without devices location.

High-k metal gate MOS transistors are built into the silicon film with thin ($T_{ox} = 1.5$ nm EOT) or thick ($T_{ox} = 3.4$ nm EOT) gate oxide to address low and high voltage biases for core and Input/Output (IO) designs. For this technology, the metal stack includes 8 copper layers (with extension to 10 layers possible). Therefore, in this study, the gated and the Shallow Trench Isolation (STI) diode(s) in hybrid bulk are selected to be designed and characterized, as well as a thin gate oxide ESD BIMOS transistor in thin silicon film. The characterization is carried out using DC measurements at room temperature in the range of [−1 V, 1 V] and I-V TLP curves with leakage monitoring and time response. The leakage current monitoring is chosen at $\pm V_D / 2 = \pm 0.3$ V where $V_D = 0.6$ V is the silicon diode standard threshold.

Electrical schematic and basic cross section of the twelve fingers N + gated diode isolated from substrate by a deep N_{WELL} doping are reported in Fig. 2, as well as the PAD test structure and the device layout in 28 nm FD-SOI. A zoom of this hybrid bulk gated diode is also given with the identification of the anode, the cathode and the front gate. The gate length is 160 nm. A front thick gate oxide is selected to allow both 1 V and 1.8 V bias voltages for core and IO design. One contact line is on the cathode and another on the anode to drive the current. The full stack metal is used to connect the device to the PAD with a minimum of ohmic path and to avoid electromigration. Moreover, the gate terminal is connected to the anode to be compliant with the IO's design

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Table 1
TLP + TID experimental plan for device families.

Device/part	#0	#1	#2	#3	#4
STI diode	Fresh	25 krad	50 krad	100 krad	200 krad
Gated diode	Fresh	25 krad	50 krad	100 krad	200 krad
BIMOS	Fresh	25 krad	50 krad	100 krad	200 krad

condition. The deep N_{WELL} doping isolation PAD is not used here.

For the STI diode, the difference is that the anode and cathode are separated by a shallow trench isolation with a SiO_2 oxide material (see next section and Fig. 5).

The ESD design for the thin gate oxide BIMOS transistor into the thin silicon film is reported in Fig. 3.

The front gate is connected to a lateral body contact. This terminal is connected to an external poly resistance to the source (equivalent to a ground). The back gate is connected to the ground.

The BIMOS transistor has 100 gate fingers (finger structure = 5 × 20) and with 1 μm width per finger. The total width of parallel transistors is 100 μm for 25 μm^2 common active surface. The gate length for this device is $L_G = 48$ nm.

For this device, one contact line is on the drain and the source connected to PAD with the full stack metal to minimize the access of the copper metal resistance.

The study is based on the designs for gated/STI diodes and for the BIMOS transistors in the standard 28 nm UTBB FD-SOI technology [3–6].

The main purpose is to have a behaviour trend of device response under ESD stress and after ionizing radiation stress. If the results are encouraging, a more systematic study could be possible in the future with statistical parameter extraction.

Fresh samples (diodes & BIMOS) are characterized through transmission line pulse (TLP) technique to determine at least the I_{t2} break point. The TLP uses 100 ns hold time and 10 ns rise time. The extraction of data points on temporal response is performed in the range [70 ns, 90 ns] and the average leads to the I-V points. Measurements are performed at wafer level using probe station and at room temperature.

Afterwards, 4 fresh samples (per device family) are characterized through TLP but till I_{t2} / 2 to avoid any ESD overstress and any self-heating during the TLP event. This is to avoid thermal annealing and I-V curve recovery. Next, these 4 sample groups are exposed to gamma-rays from Co^{60} up to 25 krad (part #1), 50 krad, 100 krad and 200 krad (part #4), respectively, at room temperature and without bias condition (all terminals are floating). A one-week room temperature parking is applied on samples to keep permanent damage(s). In this condition, all samples are once again characterized through TLP with the I_{t2} / 2 limit.

Experimental results are then comparatively assessed to determine the TID impact on devices according to the specific dose level. This will be an interesting input to have a trend of the device behaviour. And if needed, it will be used to improve the initial ESD solutions under TID radiation based on these preliminary results.

2. Diodes in hybrid bulk area

It is well known that the gated and STI diodes are useful devices for ESD protection and are designed in the bulk hybrid region to evacuate a high overvoltage (see Section 1, Fig. 2). Fig. 4 reports the TLP responses on a triggering diode before (Fig. 4a) and after exposure to 200 krad (Fig. 4b) and with the offset of the leakage current. Fig. 4c reports a comparison between fresh and 200 krad dose. It appears that the triggering diode is very robust under TLP and under TID. In addition, no degradation of temporal response and no overvoltage are observed during the extraction of the temporal response. To confirm these good TLP/TID results on hybrid bulk N+ gated diode, the same constraints and characterizations are performed on a hybrid bulk N + STI diode. Fig. 5 illustrates the same excellent trends on the robustness of the TLP with the same behaviour up to 200 krad TID. For these two diodes, the leakage is approximately 10^{-11} A before and after the TLP/TID constraints. This value lies within the dispersion range of the process. Thus, the quality of the silicon oxide and its interfaces leads to maintaining the TLP constraint up to 1.6 A and 200 krad Co^{60} TID.

According to these preliminary results, the two diode structures in the hybrid bulk could be used for primary ESD protection in the IO ring and also for secondary CDM protection in the core of IP and SOC. The sizing of the diode depends on the load to be protected and on the desired electronic function with its constraints.

The next section concerns the thin silicon film BIMOS (with thin gate oxide) evaluation under TLP & TID.

3. BIMOS in thin silicon film area

Fig. 6a gives the DC leakage and the TLP response on a fresh ESD BIMOS transistor in thin silicon film in 28 nm UTBB FD-SOI technology. The sweep current measurement is performed in [−1 V, 1 V] voltage range as previously and compliant for thin oxide standard voltage. Two current behaviours appear in DC mode: under direct bias, the BIMOS device is blocked with a few nano-amperes of current leakage and in reverse bias, the device is opened with milliamps of current control. In fact, the poly resistance biases the front gate and turns on the device. For TLP leakage monitoring, the voltage bias will be applied as previously at ± 0.3 V and reported during measurements. Basically, the parasitic capacitances C_{DG} and C_{DB} coupled with the external

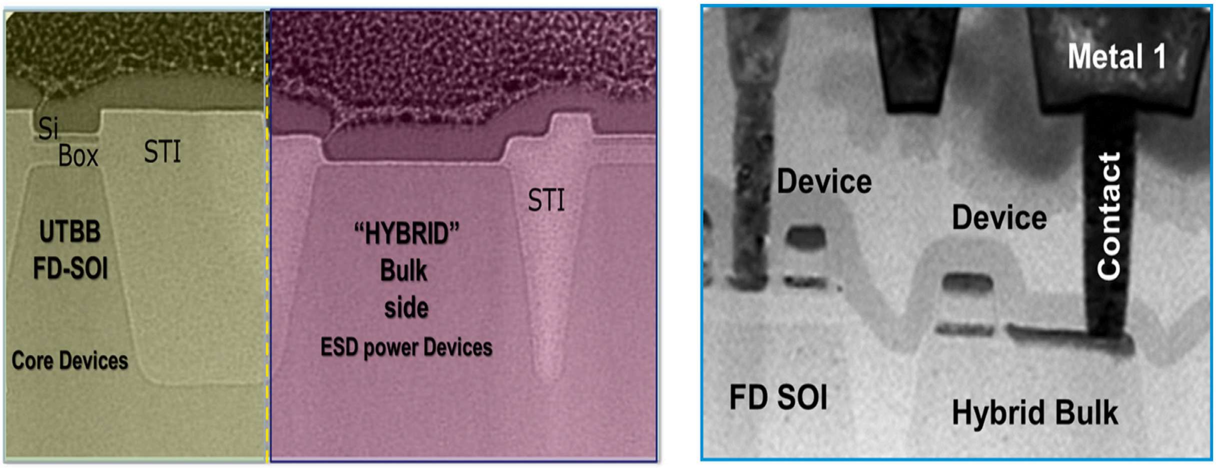

Fig. 1. FD-SOI and hybrid bulk areas w/wo devices.

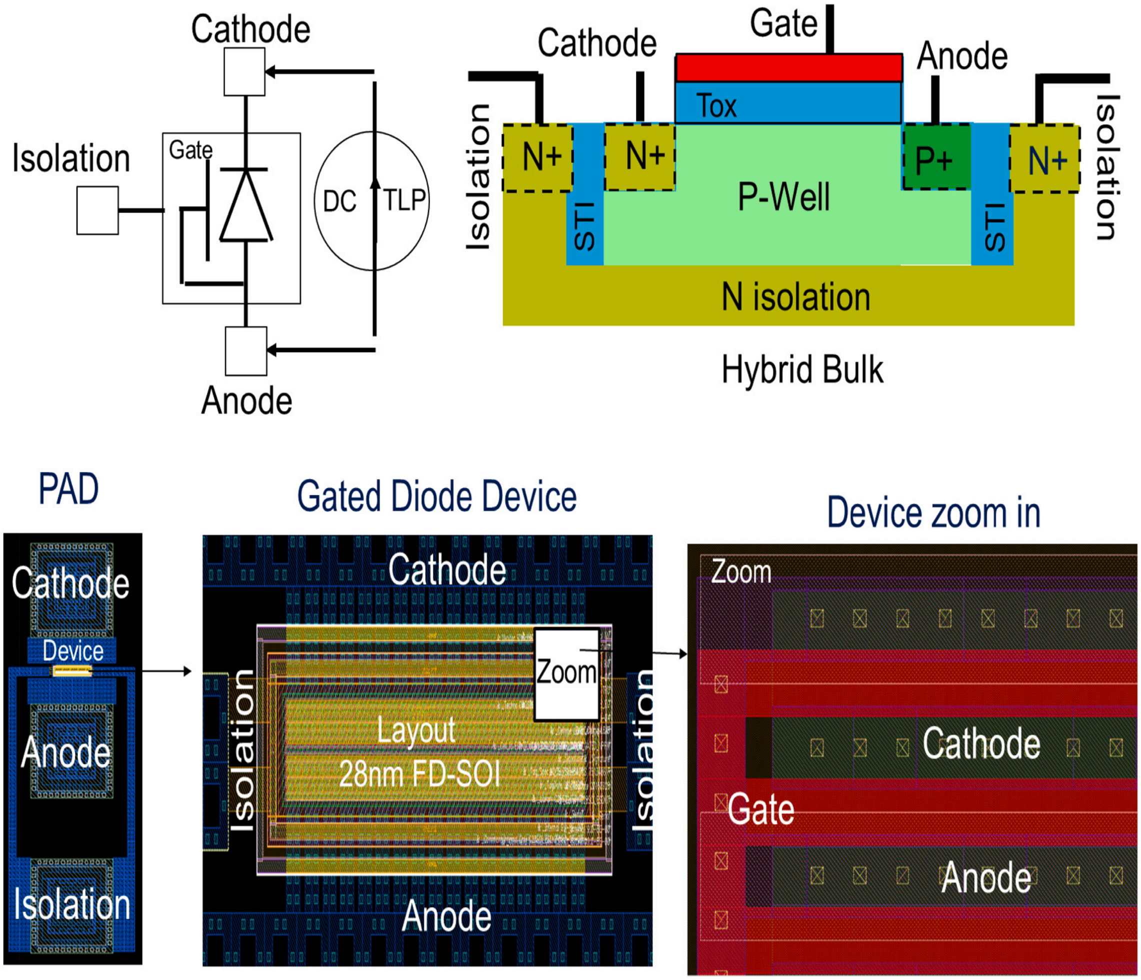

Fig. 2. Schematic and layout in hybrid bulk 28 nm FD-SOI technology of the isolated N+ gated diode.

polysilicon resistance perform a RC trigger circuit which detects the ESD event. In this condition, the initial ESD characterization leads to I_{t2} = 100 mA or after normalization: I_{t2} = 1 mA/µm. This current value is expected because the silicon film thickness is 7 nm, i.e. very small compared to the hybrid bulk (It_2 bulk > 10 mA/µm [4]). Thus, compared to previous study [3], the current ratio of BIMOS in FD-SOI and hybrid bulk is around 10. For the I_{t2} current value, the time response induces a self-heating of the device. After I_{t2} the device goes in short circuit as reported on I-V curve in Fig. 6b. Also time responses are reported.

These TLP measurements demonstrate that the BIMOS in thin silicon film is functional and does not show any overvoltage during switch-on. Thus, the holding voltage of this protection is V_{hold} = 2.4 V and the threshold voltage V_{t1} = 2.77 V (in 15 ns rise time) are fully compliant with the 28 nm FD-SOI technology window. Moreover, this threshold voltage could be adjusted thanks to the R_{poly} value. Based on these encouraging DC and TLP results for this solution, the measurements are extended to a very fast TLP (VFTLP 1 ns hold time and 100 ps rise time) stress at room temperature to evaluate the equivalent CDM robustness and the overvoltage during the 100 ps rise time event. Thus, Fig. 7 compares I-V curves for TLP, for VFTLP and the time response at the end of the VFTLP curve. It is measured that the breakpoint current is I_{t2} = 640 mA and without overvoltage as observed on time response.

Afterwards, four fresh parts are then characterized till $I_{TLP\ max}$ = 50 mA. Fig. 8 gives a time response which shows that no self-heating is activated during the pulse and TLP curves. We observe a good reproducibility of results and no major dispersion is reported on these samples.

The four parts (part #1–4) have been irradiated (unbiased device with floating terminals under Co^{60}) up to 25, 50, 100 and 200 krad, respectively and their TLP curves re-measured. The leakage current is also monitored to evaluate the impact of the radiation for the normal mode of operation.

For all characterizations, time response curves are reported at the end of TLP measurements to consolidate that the no self-heating condition is well respected (Fig. 9).

The TLP response is only slightly impacted at 100 krad and a 364 mV shift is next measured at 200 krad. This value needs to be consolidated and especially on other devices to evaluate it in a statistical way, the magnitude average of the shift. Also, the I_{t2} is not significantly impacted that means that it will be interesting to push the total TID dose to higher values to explore further the device and the final robustness of this solution. Time responses depict, for all samples, that no overvoltage occurs before/and after TID for the maximum current TLP stress (at 50 mA) (Fig. 10).

However, the leakage current shifts with the dose level increase

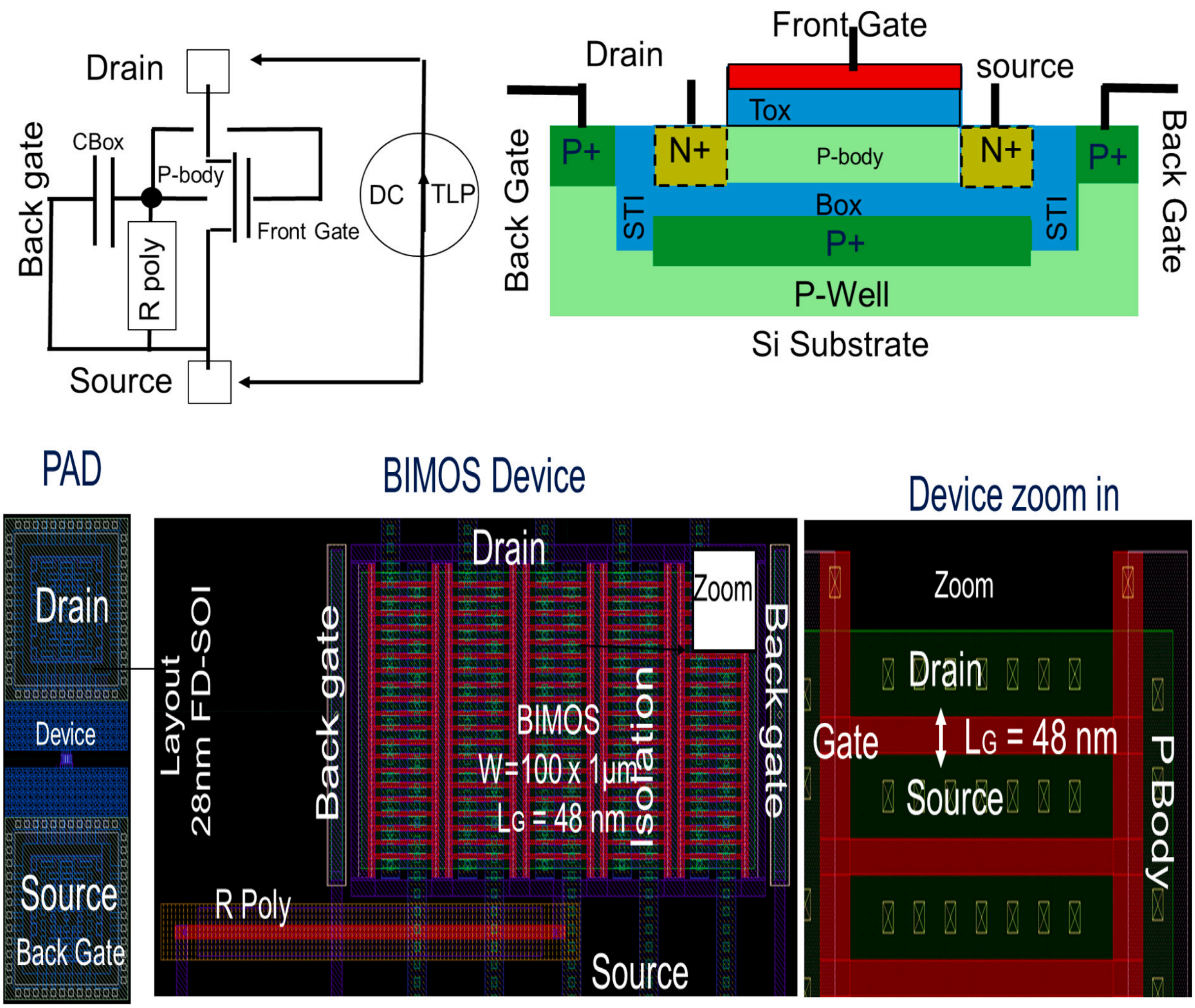

Fig. 3. 28 nm FD-SOI schematic and layout of the thin gate oxide BIMOS transistor into thin silicon film.

leading to values up to around 10 times greater than the initial one (on 1 sample, for 100 µm of width and for 10^{-8} A). Once again, this value needs to be consolidated by a statistical study. It is not a significant shift but could be not acceptable for some specific applications with ultra-lower power design. This issue could also become a problem if the dose is higher than 200 krad. Thus, the idea for a next investigation is to extend the total dose to 1 Mrad or with more aggressive radiation. And if a drastic current leakage is observed, the idea is to use a device with an in situ local heating to evaluate the impact of the local thermal annealing and recovering effect. This technique has already been evaluated by simulation and used on this technology on silicon samples for dispersion correction [7]. Moreover, furnace technique is always possible.

4. Conclusion

This paper introduces a methodology to investigate deeply scaled ESD solutions in hybrid bulk and in thin silicon film for 28 nm UTBB FD-SOI technology, under radiation conditions.

ESD gated/STI diodes and thin silicon film BIMOS transistor have been characterized under TLP before and after Co^{60} TID in the range of [25 krad–200 krad] at room temperature and with floating terminals.

It appears that both types of diodes are very robust under TLP and TID. The diodes in hybrid bulk demonstrate no significant degradation of ESD response and leakage till 200 krad.

For the BIMOS transistors with a thin oxide high-k metal gate, a very good performance is evaluated in the TLP and VFTLP constraints and no over-voltage is reported during measurements on both VFTLP and TLP. In thin silicon film, the current breakpoint is extracted at $I_{t2} = 1$ mA/µm and six times more for VFTLP. The ESD responses measured on devices before 200 krad do not show relevant impact and after 200 krad TID it has been slightly impacted with a 364 mV deviation and an increase of DC leakage.

The next step of this study could be to confirm these preliminary results by statistical investigation and to push the total dose to 1 Mrad. The current leakage recovery could be investigated by classical thermal annealing (furnace) or novel devices with in situ local heating technique. Moreover, the back-bias technique could also be used to counterbalance this leakage in case of major degradation.

To conclude, the FD-SOI technology is a very good candidate for harsh environments considering the ESD and the radiation issues (at room temperature).

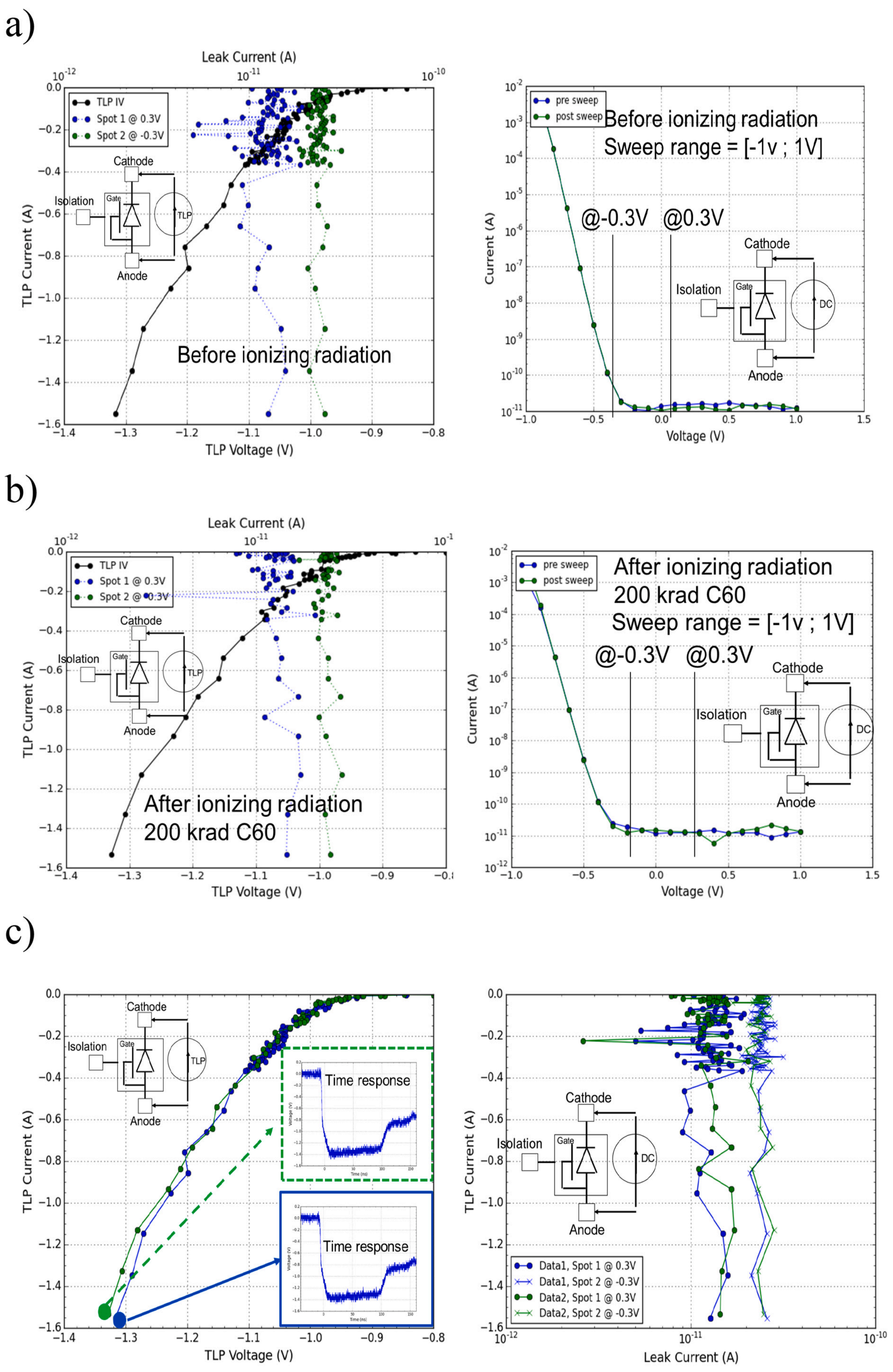

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Fig. 4. ESD gated diode (N+): TLP & time responses before (a)/after 200 krad (b) with current leakage monitoring. Comparison and time responses (c).

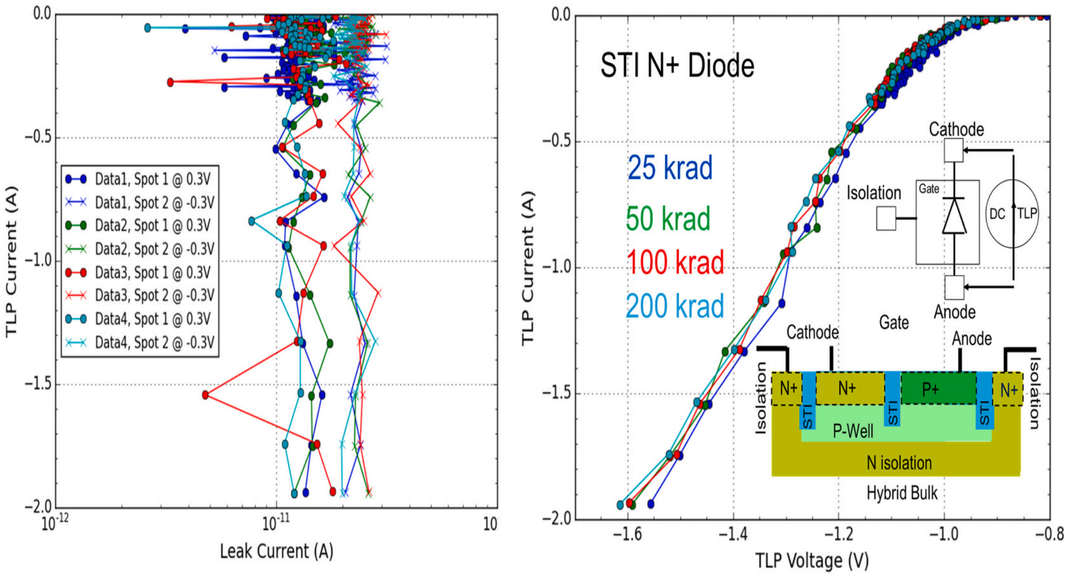

Fig. 5. ESD STI diode (N+): TLP & 25, 50, 100 and 200 krad TID with current leakage monitoring.

CRediT authorship contribution statement

Ph. Galy: Conceptualization, Methodology, Measurement, Writing - original draft preparation, editing
F. Soto: Methodology, Measurement, Reviewing
J. Bourgeat: Design, Layout, Reviewing
B. Jacquier: Methodology, Measurement
V. Kilchytska: Methodology, Measurement, Reviewing
D. Flandre: Methodology, Measurement, Reviewing.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Appendix A. Supplementary data

Supplementary data to this article can be found online at https://doi.org/10.1016/j.microrel.2020.113938.

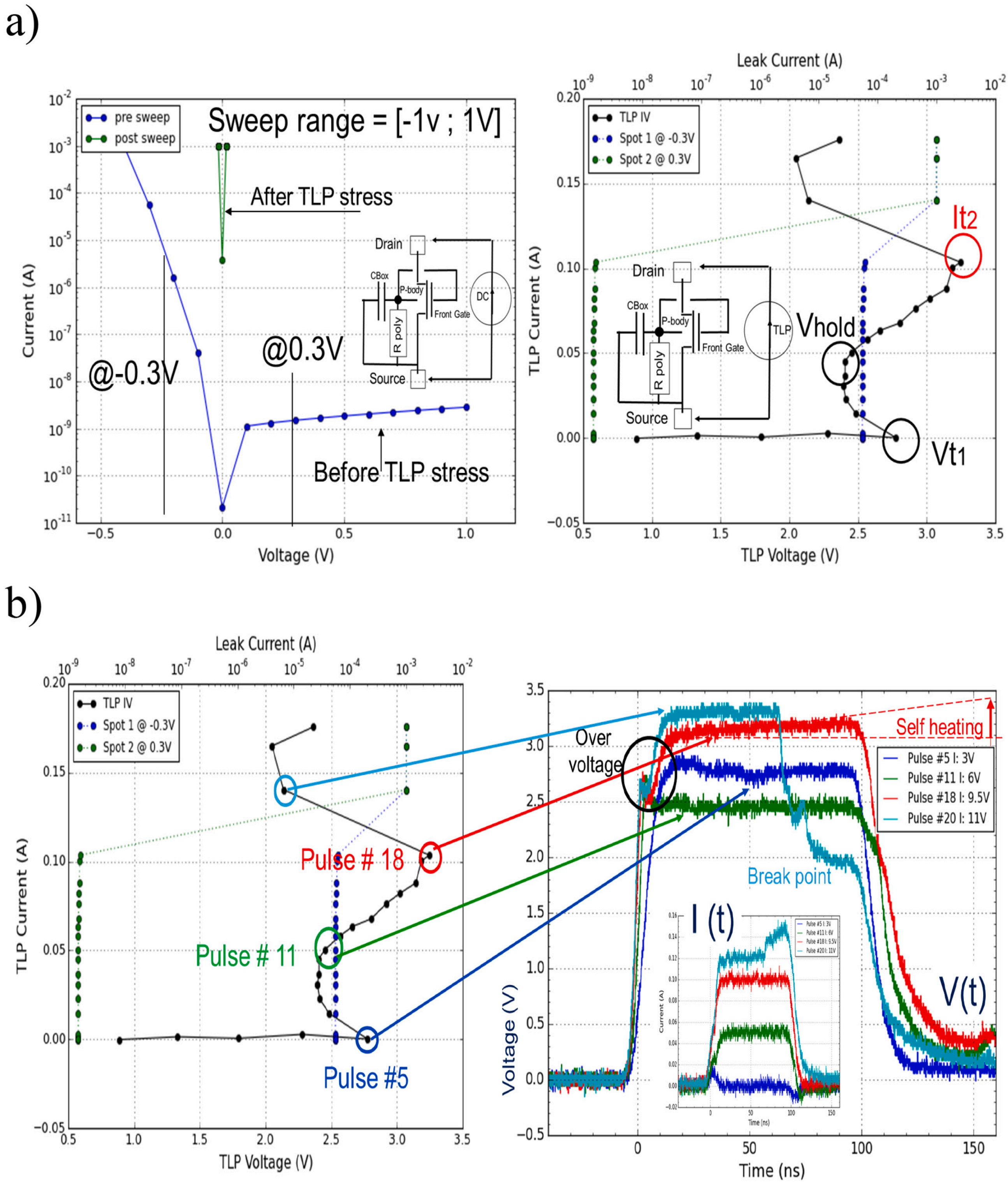

Fig. 6. ESD thin silicon film BIMOS transistor: a) leakage current and response under TLP (10 ns rise time & 100 ns hold time); b) TLP and time responses.

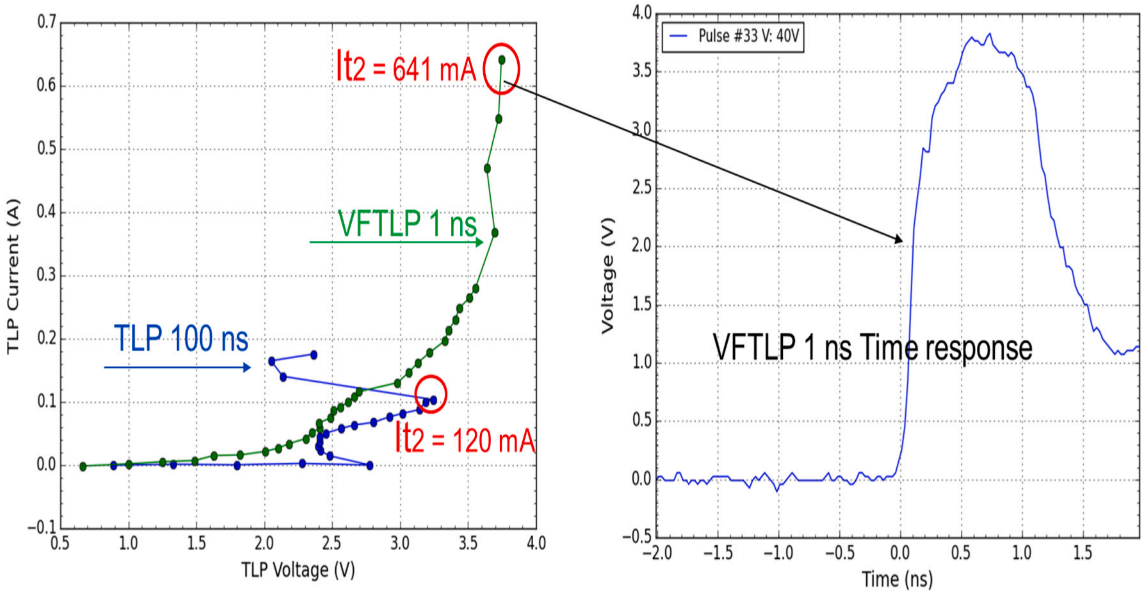

Fig. 7. Thin silicon film ESD BIMOS transistor response under TLP & VFTLP with time response.

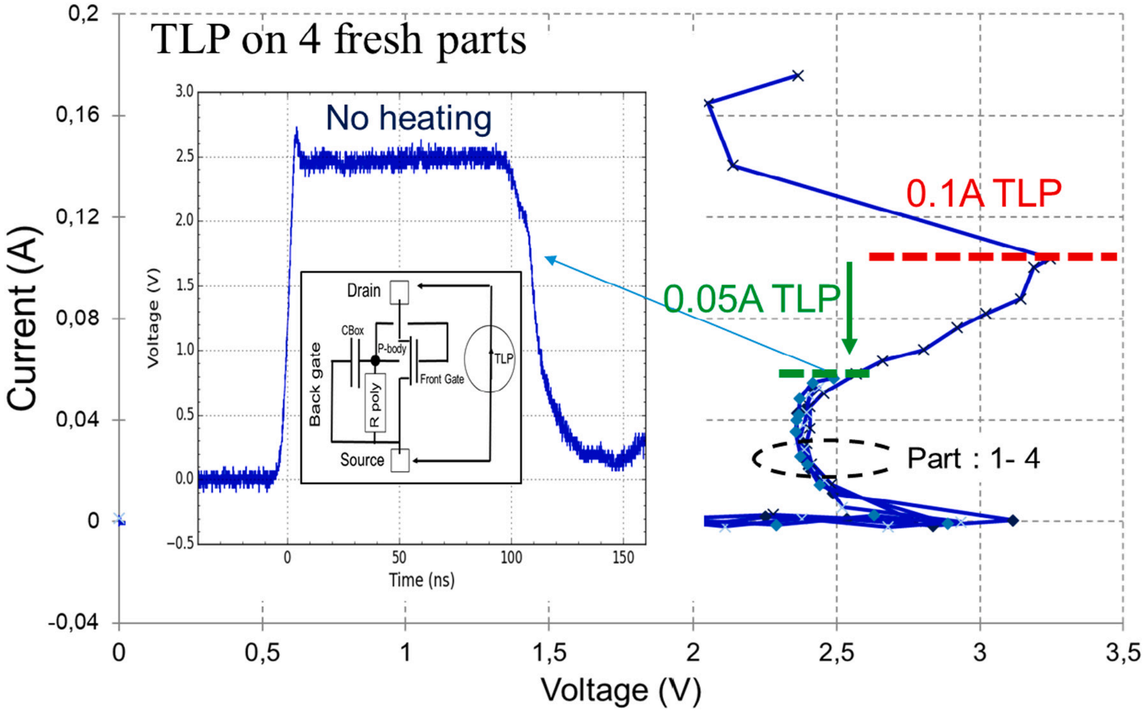

Fig. 8. ESD BIMOS transistor layout and four responses under TLP for parts #1–4 and comparison to the first measurement.

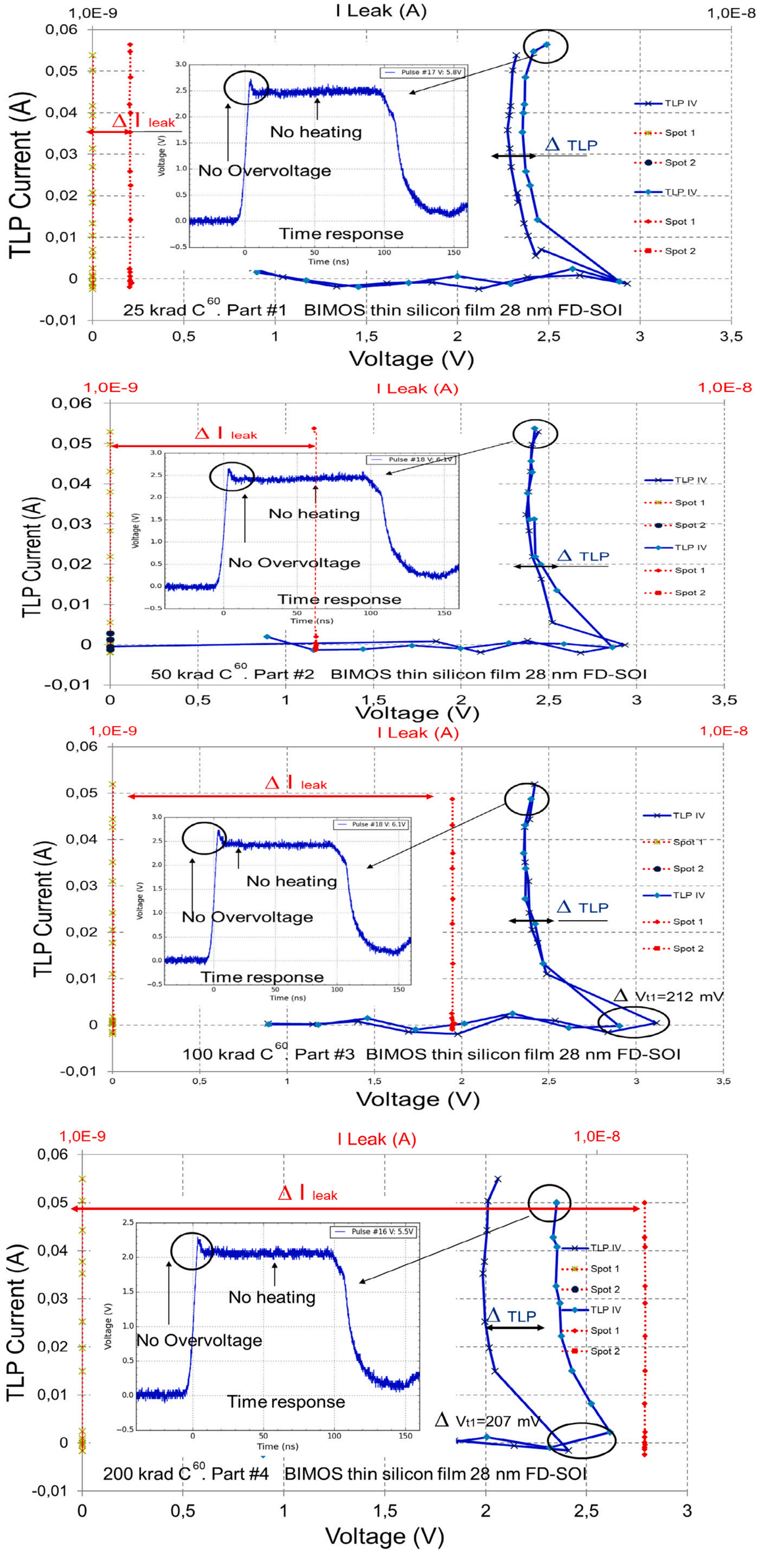

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Fig. 9. Comparison of TLP responses of thin silicon film thin oxide BIMOS devices for TID of 25, 50, 100 and 200 krad (part #1–4, respectively, from top to bottom).

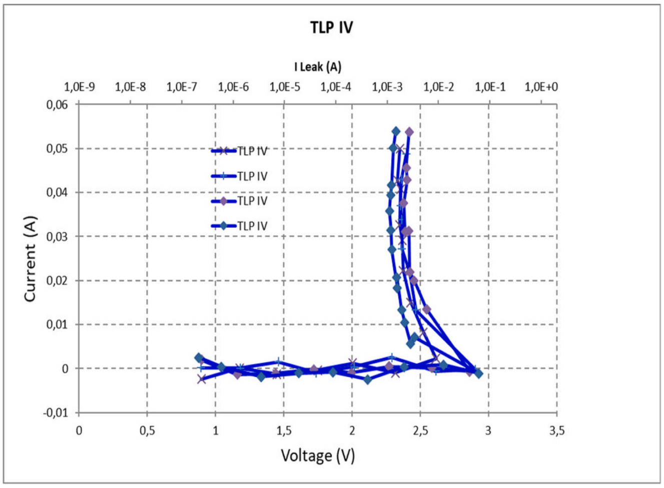

Fig. 10. Comparison on TLP responses of BIMOS devices for 25, 50, 100 and 200 krad TID (part #1–4, respectively).

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